PRELIMINARY
CUSTOMER PROCUREMENT SPECIFICATION

Z86E73/E74 32K OTP
Z86L73/L74 32K ROM

INFRARED REMOTE CONTROLLERS

FEATURES

Part	ROM (Kbyte)	RAM* (Kbyte)	One-Time Programmable	Speed (MHz)
Z86E73	32	1004	Yes	8
Z86L73	32	492	No	8
Z86E74	32	1004	Yes	8
Z86L74	32	1004	No	8

* General-Purpose

- 40-Pin DIP, 44-Pin PLCC/QFP Packages (E73/L73)
  64-Pin DIP, 68-Pin PLCC Packages (E74/L74)
- 2.0V to 3.9V Operating Range (L73/L74)
  4.5V to 5.5V Operating Range (E73/E74)
- Low-Power Consumption
  (Typical: 40 mw for L73/L74)
  (Typical: 60 mw for E73/E74)
- 0°C to +70°C Temperature Range
- Expanded Register Files (ERF)
- 31 Input/Output Lines (E73/L73)
  51 Input/Output Lines (E74/L74*)
  ***Note: With Auto Latch on Port 4, 5 and 6.**
- Five Prioritized Interrupts with Programmable Polarity
- Two Comparators
- 8-Bit Counter/Timer with Two Capture Registers and 16-Bit Counter/Timer with One Capture Register
- Watch-Dog Timer (WDT)/Power-On Reset (POR)
- On-Chip Oscillator that Accepts a Crystal, Ceramic Resonator, LC, RC, or External Clock Drive
- Low-Voltage Detection and Protection
- 32-KHz Mask Option to Disable Internal Feedback Resistor (L73/L74)

GENERAL DESCRIPTION

The Z86E73/L73/E74/L74 are ROM-based members of Zilog's Z8® single-chip microcontroller family of infrared (IR) consumer controller processors featuring fast and flexible code execution. The Z86E73/E74 devices offer a one-time programmable (OTP) option.

For applications demanding powerful I/O capabilities, the Z86E73/L73's dedicated input and output lines are grouped into four ports, and into seven ports for the Z86E74/L74. They are configurable under software control to provide timing, status signals, or parallel I/O.

Four address spaces, the Program Memory, Register File, Data Memory, and Expanded Register File (ERF) support a wide range of memory configurations. Through the ERF the designer has access to three additional control registers that provide extra peripheral devices, I/O ports, and register addresses.

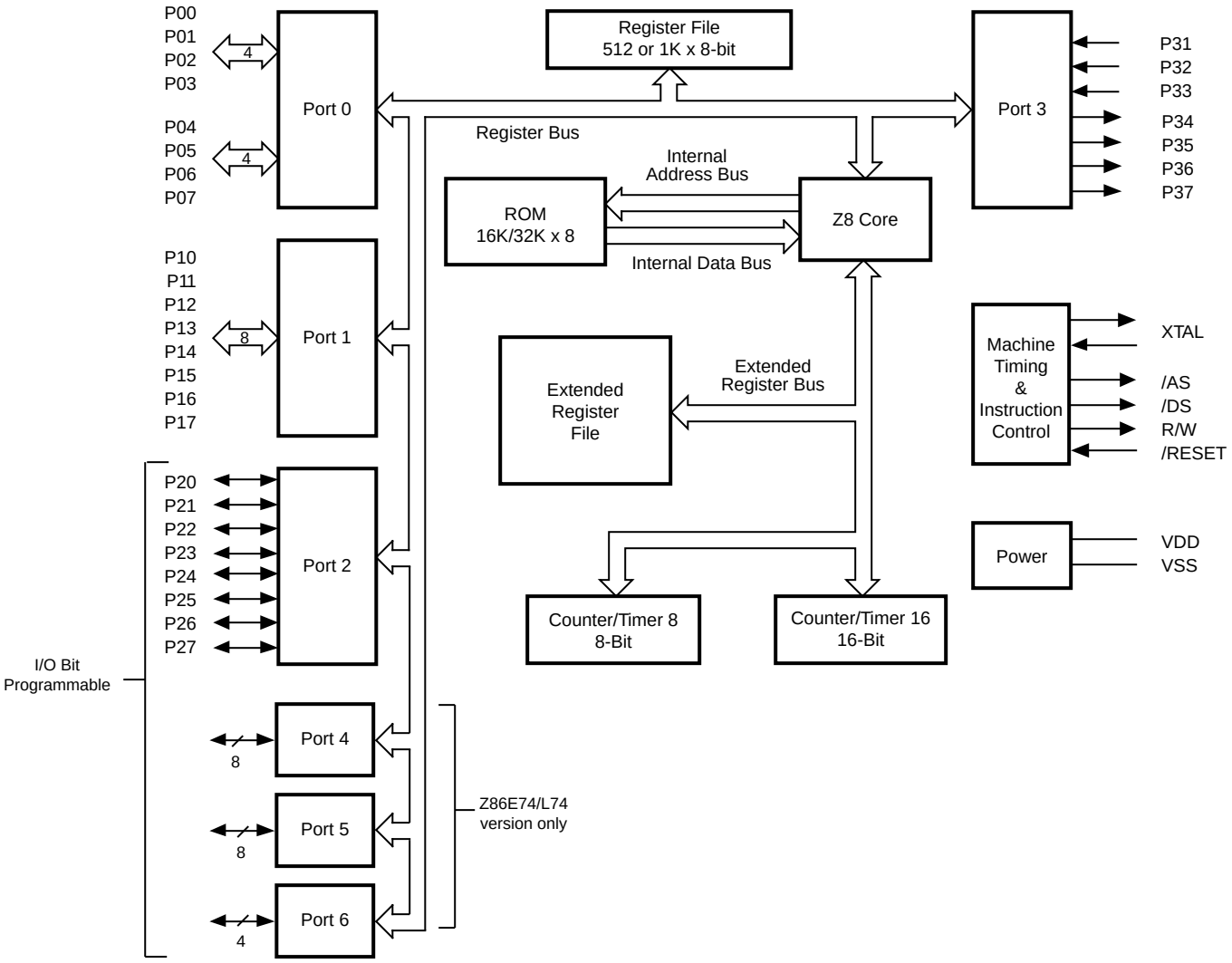
Two on-chip counter/timers, with a large number of selectable modes, offload the system of administering real-time tasks such as counting/timing and I/O datacommunications.

Notes:
All Signals with a preceding front slash, "/", are active Low, e.g., B//W (WORD is active Low); /B/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

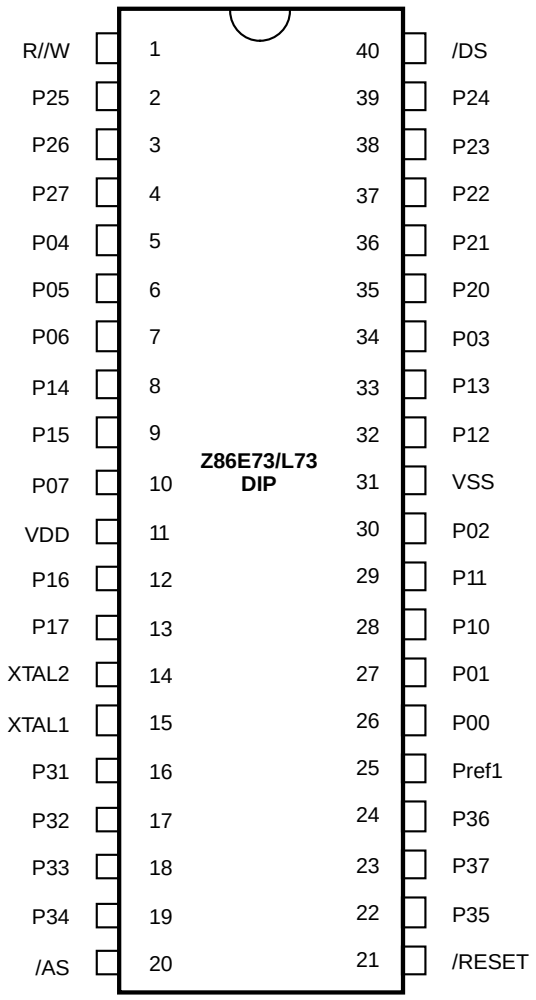
Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

GENERAL DESCRIPTION (Continued)

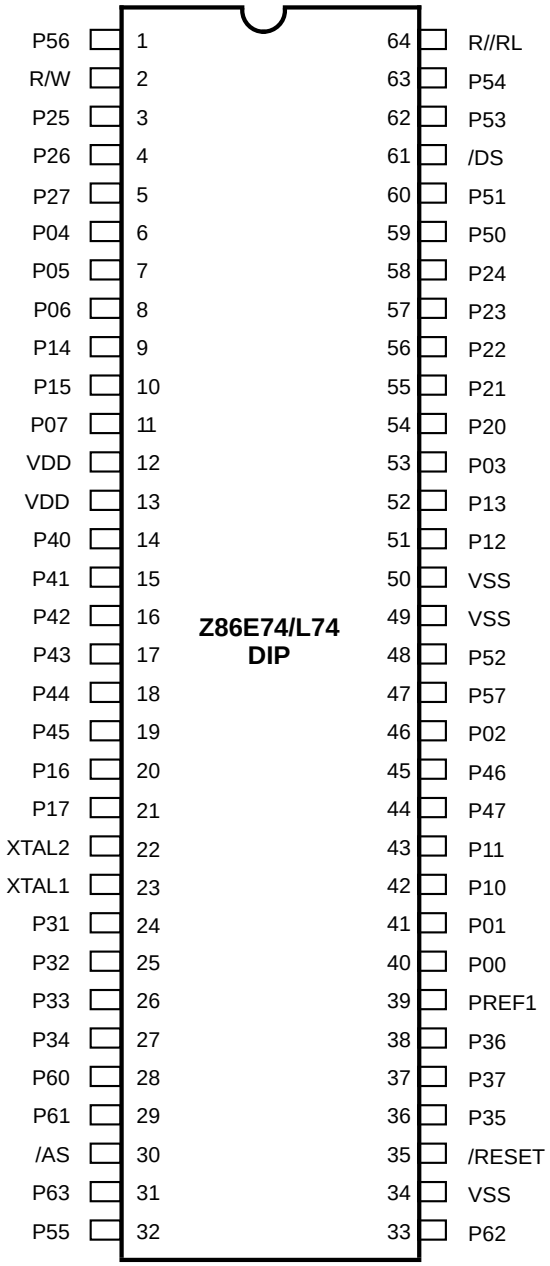


Functional Block Diagram

PIN DESCRIPTION

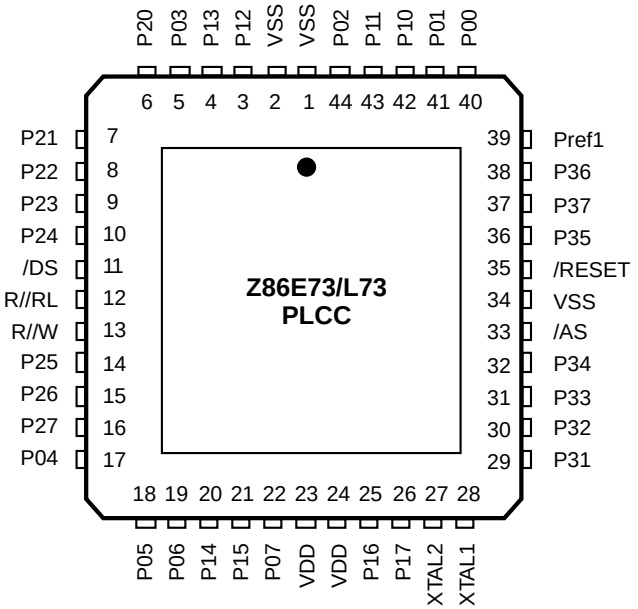


Z86E73 (Standard Mode)
Z86L73 40-Pin DIP
Pin Assignments

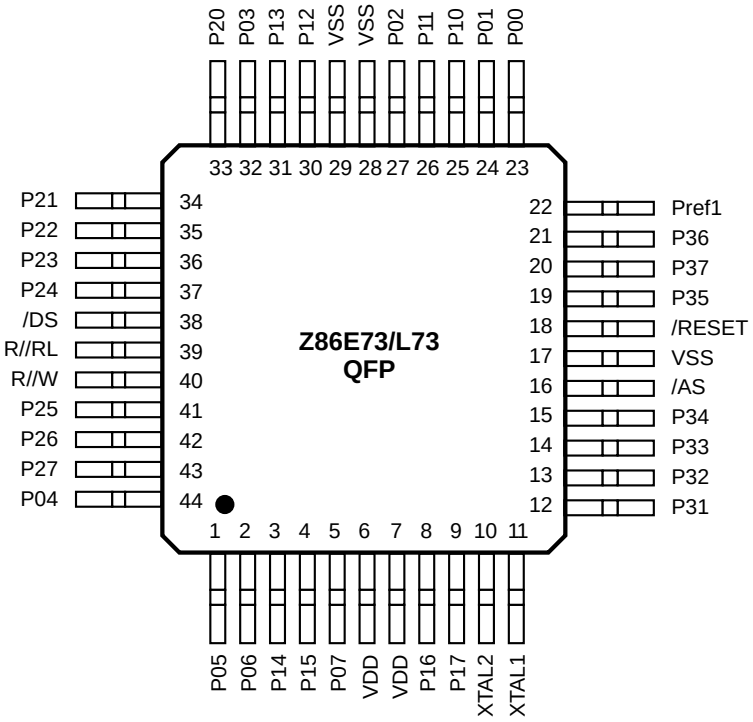


Z86E74 (Standard Mode)
Z86L74 64-Pin DIP
Pin Assignments

PIN DESCRIPTION

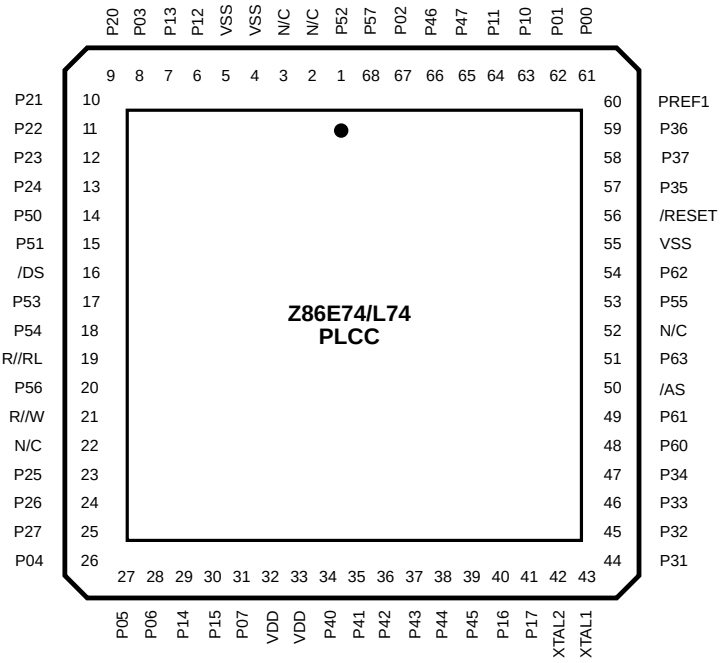


Z86E73 (Standard Mode)
Z86L73 44-Pin PLCC
Pin Assignments



Z86E73 (Standard Mode)
Z86L73 44-Pin QFP
Pin Assignments

PIN DESCRIPTION (Continued)



Z86E74 (Standard Mode)
Z86L74 68-Pin PLCC Pin Assignments

ABSOLUTE MAXIMUM RATINGS

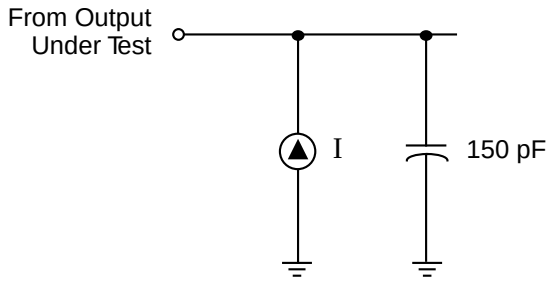
Symbol	Description	Min	Max	Units
V_{CC}	Supply Voltage (*)	–0.3	+7.0	V
T_{STG}	Storage Temp.	–65°	+150°	C
T_A	Oper. Ambient Temp.		†	C

Notes:
* Voltage on all pins with respect to GND.
† See Ordering Information.

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for an extended period may affect device reliability.

STANDARD TEST CONDITIONS

The characteristics listed below apply for standard test conditions as noted. All voltages are referenced to GND. Positive current flows into the referenced pin (Test Load).



Test Load Diagram

CAPACITANCE

T_A = 25°C, V_{CC} = GND = 0V, f = 1.0 MHz, unmeasured pins returned to GND.

Parameter	Max
Input capacitance	12 pF
Output capacitance	12 pF
I/O capacitance	12 pF

DC CHARACTERISTICS (Z86E73/E74)

Sym	Parameter	V_{CC}	T_A = 0°C to +70°C Min	Max	Typ @ 25°C	Units	Conditions	Notes [3]
	Max Input Voltage	4.0V		7		V	I_{IN} 250 µA	
		5.5V		7		V	I_{IN} 250 µA	
V_{CH}	Clock Input High Voltage	4.0V	0.9 V_{CC}	V_{CC} + 0.3		V	Driven by External Clock Generator	
		5.5V	0.9 V_{CC}	V_{CC} + 0.3		V	Driven by External Clock Generator	
V_{CL}	Clock Input Low Voltage	40V	V_{SS} – 0.3	0.2 V_{CC}		V	Driven by External Clock Generator	
		5.5V	V_{SS} – 0.3	0.2 V_{CC}		V	Driven by External Clock Generator	
V_{IH}	Input High Voltage	4.0V	0.7 V_{CC}	V_{CC} + 0.3	1.3	V		
		5.5V	0.7 V_{CC}	V_{CC} + 0.3	2.5	V		
V_{IL}	Input Low Voltage	4.0V	V_{SS} – 0.3	0.2 V_{CC}	0.5	V		
		5.5V	V_{SS} – 0.3	0.2 V_{CC}	0.9	V		
V_{OH1}	Output High Voltage	4.0V	V_{CC} – 0.4		1.7	V	I_{OH} = –0.5 mA	
		5.5V	V_{CC} – 0.4		3.7	V	I_{OH} = –0.5 mA	
V_{OH2}	Output High Voltage	4.0V	0.7			V	I_{OH} = –7 mA	[10]
	(P36, P37)	5.5V	0.7			V	I_{OH},= –7 mA	[10]
V_{OL1}	Output Low Voltage	4.0V		0.4	0.2	V	I_{OL} = 1.0 mA	
		5.5V		0.4	0.1	V	I_{OL} = 4.0 mA	
V_{OL2}	Output Low Voltage	4.0V		0.8	0.3	V	I_{OL} = 2.0 mA 3 Pin Max	
		5.5V		0.8	0.5	V	I_{OL} = 8.0 mA 3 Pin Max	
V_{OL2}	Output Low Voltage (P20-P22, P36,	4.0V		0.8	0.3	V	I_{OL} = 10 mA	[9]
	P00, P01, P07)	5.5V		0.8	0.5	V	I_{OL} = 10 mA 2 O/P only	[9]
V_{RH}	Reset Input	4.0V	0.8 V_{CC}	V_{CC}	1.5	V		
	High Voltage	5.5V	0.8 V_{CC}	V_{CC}	3.0	V		
V_{RI}	Reset Input	4.0V	V_{SS} – 0.3	0.2 V_{CC}	0.5			
	Low Voltage	5.5V	V_{SS} – 0.3	0.2 V_{CC}	0.9			
V_{OFFSET}	Comparator Input	4.0V		25	10	mV		
	Offset Voltage	5.5V		25	10	mV		
I_{IL}	Input Leakage	4.0V	–1	1	< 1	µA	V_{IN} = OV, V_{CC}	
		5.5V	–1	1	< 1	µA	V_{IN} = OV, V_{CC}	
I_{OL}	Output Leakage	4.0V	–1	1	< 1	µA	V_{IN} = OV, V_{CC}	
		5.5V	–1	1	< 1	µA	V_{IN} = OV, V_{CC}	
I_{IR}	Reset Input Current	4.0V		–45	–20	µA		
		5.5V		–55	–30	µA		
I_{CC}	Supply Current	4.0V		10	4	mA	@ 8.0 MHz	[4, 5]
		5.5V		15	10	mA	@ 8.0 MHz	[4, 5]
		4.0V		100	10	µA	@ 32 kHz	[4, 5,11]
		5.5V		300	10	µA	@ 32 kHz	[4, 5,11]

DC CHARACTERISTICS (Z86E73/E74) (Continued)

Sym	Parameter	V_{CC}	T_A = 0°C to +70°C Min	Max	Typ @ 25°C	Units	Conditions	Notes [3]
I_{CC1}	Standby Current	4.0V		3	1	mA	HALT Mode V_{IN} = OV, V_{CC} @ 8.0 MHz	[4,5]
		5.5V		5	4	mA	HALT Mode V_{IN} = OV, V_{CC} @ 8.0 MHz	[4,5]
		4.0V		2	0.8	mA	Clock Divide-by-16 @ 8.0 MHz	[4,5]
		5.5V		4	2.5	mA	Clock Divide-by-16 @ 8.0 MHz	[4,5]
I_{CC2}	Standby Current	4.0V		8	2	µA	STOP Mode V_{IN} = OV, V_{CC} WDT is not Running	[6,8]
		5.5V		10	3	µA	STOP Mode V_{IN} = OV, V_{CC} WDT is not Running	[6,8]
		4.0V		500	310	µA	STOP Mode V_{IN} = OV, V_{CC} WDT is Running	[6,8]
		5.5V		800	600	µA	STOP Mode V_{IN} = OV, V_{CC} WDT is Running	[6,8]
T_{POR}	Power-On Reset	4.0V	15	75	13	ms		
		5.5V	5	20	7	ms		
V_{LV}	V_{CC} Low Voltage Protection			3.3	2.75	V	8 MHz max Ext. CLK Freq.	[7]

Notes:

[1]

I_{CC1}	Typ	Max	Unit	Frequency
Crystal/Resonator	3.0 mA	5	mA	8.0 MHz
External Clock Drive	0.3 mA	5	mA	8.0 MHz

[2] GND = 0V.
[3] 4.0V to 5.5V.
[4] All outputs unloaded, I/O pins floating, inputs at rail.
[5] CL1 = CL2 = 100 pF.
[6] Same as note [4] except inputs at V_{CC}.
[7] The V_{LV} increases as the temperature decreases.
[8] Oscillator stopped.
[9] Two outputs at a time, independent to other outputs.
[10] One at a time.
[11] 32 kHz clock driver input.

DC CHARACTERISTICS (Z86L73/L74)

Sym	Parameter	V_{CC}	T_A = 0°C to +70°C Min	Max	Typ @ 25°C	Units	Conditions	Notes [3]
	Max Input Voltage	2.0V		7		V	I_{IN} 250 µA	
		3.9V		7		V	I_{IN} 250 µA	
V_{CH}	Clock Input High Voltage	2.0V	0.9 V_{CC}	V_{CC} + 0.3		V	Driven by External Clock Generator	
		3.9V	0.9 V_{CC}	V_{CC} + 0.3		V	Driven by External Clock Generator	
V_{CL}	Clock Input Low Voltage	2.0V	V_{SS} – 0.3	0.2 V_{CC}		V	Driven by External Clock Generator	
		3.9V	V_{SS} – 0.3	0.2 V_{CC}		V	Driven by External Clock Generator	
V_{IH}	Input High Voltage	2.0V	0.7 V_{CC}	V_{CC} + 0.3	1.3	V		
		3.9V	0.7 V_{CC}	V_{CC} + 0.3	2.5	V		
V_{IL}	Input Low Voltage	2.0V	V_{SS} – 0.3	0.2 V_{CC}	0.5	V		
		3.9V	V_{SS} – 0.3	0.2 V_{CC}	0.9	V		
V_{OH1}	Output High Voltage	2.0V	V_{CC} – 0.4		1.7	V	I_{OH} = –0.5 mA	
		3.9V	V_{CC} – 0.4		3.7	V	I_{OH} = –0.5 mA	
V_{OH2}	Output High Voltage (P36, P37)	2.0V	0.7			V	I_{OH} = –7 mA	[10]
		3.9V	0.7			V	I_{OH},= –7 mA	[10]
V_{OL1}	Output Low Voltage	2.0V		0.4	0.2	V	I_{OL} = 1.0 mA	
		3.9V		0.4	0.1	V	I_{OL} = 4.0 mA	
V_{OL2}	Output Low Voltage	2.0V		0.8	0.3	V	I_{OL} = 2.0 mA 3 Pin Max	
		3.9V		0.8	0.5	V	I_{OL} = 8.0 mA 3 Pin Max	
V_{OL2}	Output Low Voltage (P20-P22, P36, P00, P01, P07)	2.0V		0.8	0.3	V	I_{OL} = 10 mA	[9]
		3.9V		0.8	0.5	V	I_{OL} = 10 mA 2 O/P only	[9]
V_{RH}	Reset Input High Voltage	2.0V	0.8 V_{CC}	V_{CC}	1.5	V		
		3.9V	0.8 V_{CC}	V_{CC}	3.0	V		
V_{RI}	Reset Input Low Voltage	2.0V	V_{SS} – 0.3	0.2 V_{CC}	0.5			
		3.9V	V_{SS} – 0.3	0.2 V_{CC}	0.9			
V_{OFFSET}	Comparator Input Offset Voltage	2.0V		25	10	mV		
		3.9V		25	10	mV		
I_{IL}	Input Leakage	2.0V	–1	1	< 1	µA	V_{IN} = OV, V_{CC}	
	3.9V	–1	1	< 1	µA	V_{IN} = OV, V_{CC}		
I_{OL}	Output Leakage	2.0V	–1	1	< 1	µA	V_{IN} = OV, V_{CC}	
		3.9V	–1	1	< 1	µA	V_{IN} = OV, V_{CC}	
I_{IR}	Reset Input Current	2.0V		–45	–20	µA		
		3.9V		–55	–30	µA		
I_{CC}	Supply Current	2.0V		10	4	mA	@ 8.0 MHz	[4, 5]
		3.9V		15	10	mA	@ 8.0 MHz	[4, 5]
		2.0V		100	10	µA	@ 32 kHz	[4, 5,11]
		3.9V		300	10	µA	@ 32 kHz	[4, 5,11]

DC CHARACTERISTICS (Z86L73/L74) (Continued)

Sym	Parameter	V_{CC}	T_A = 0°C to +70°C Min	Max	Typ @ 25°C	Units	Conditions	Notes [3]
I_{CC1}	Standby Current	2.0V		3	1	mA	HALT Mode V_{IN} = OV, V_{CC} @ 8.0 MHz	[4,5]
		3.9V		5	4	mA	HALT Mode V_{IN} = OV, V_{CC} @ 8.0 MHz	[4,5]
		2.0V		2	0.8	mA	Clock Divide-by-16 @ 8.0 MHz	[4,5]
		3.9V		4	2.5	mA	Clock Divide-by-16 @ 8.0 MHz	[4,5]
I_{CC2}	Standby Current	2.0V		8	2	µA	STOP Mode V_{IN} = OV, V_{CC} WDT is not Running	[6,8]
		3.9V		10	3	µA	STOP Mode V_{IN} = OV, V_{CC} WDT is not Running	[6,8]
		2.0V		500	310	µA	STOP Mode V_{IN} = OV, V_{CC} WDT is Running	[6,8]
		3.9V		800	600	µA	STOP Mode V_{IN} = OV, V_{CC} WDT is Running	[6,8]
T_{POR}	Power-On Reset	2.0V	15	75	13	ms		
		3.9V	5	20	7	ms		
V_{LV}	V_{CC} Low Voltage Protection			2.15	1.7	V	8 MHz max Ext. CLK Freq.	[7]

Notes:

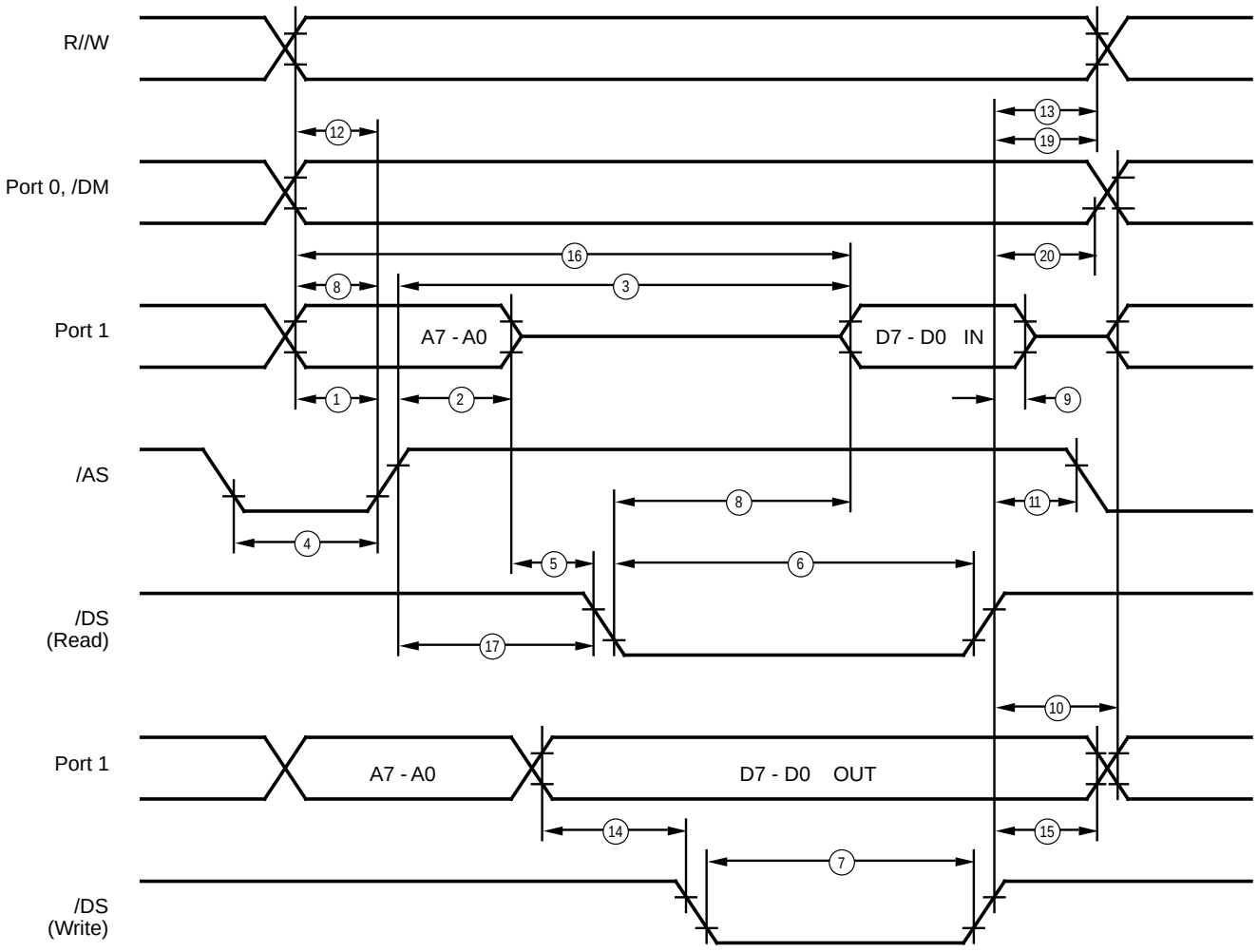
[1] I_{CC1}

	Typ	Max	Unit	Frequency
Crystal/Resonator	3.0 mA	5	mA	8.0 MHz
External Clock Drive	0.3 mA	5	mA	8.0 MHz

[2] GND = 0V.
[3] 2.0V to 3.9V.
[4] All outputs unloaded, I/O pins floating, inputs at rail.
[5] CL1 = CL2 = 100 pF.
[6] Same as note [4] except inputs at V_{CC}.
[7] The V_{LV} increases as the temperature decreases.
[8] Oscillator stopped.
[9] Two outputs at a time, independent to other outputs.
[10] One at a time.
[11] 32 kHz clock driver input.

AC CHARACTERISTICS

External I/O or Memory Read and Write Timing Diagram



External I/O or Memory Read/Write Timing

AC CHARACTERISTICS (Z86E73/E74)

External I/O or Memory Read and Write Timing Table

No.	Symbol	Parameter	V_{CC} Note [3]	T_A = 0°C to +70°C 8.0 MHz Min	Max	Units	Notes
1	TdA(AS)	Address Valid to	4.0V	55		ns	[2]
		/AS Rising Delay	5.5V	55		ns	
2	TdAS(A)	/AS Rising to Address	2.0V	70		ns	[2]
		Float Delay	5.5V	70		ns	
3	TdAS(DR)	/AS Rising to Read	4.0V		400	ns	[1, 2]
		Data Required Valid	5.5V		400	ns	
4	TwAS	/AS Low Width	4.0V	80		ns	[2]
			5.5V	80		ns	
5	Td	Address Float to	4.0V	0		ns	
		/DS Falling	5.5V	0		ns	
6	TwDSR	/DS (Read) Low Width	4.0V	300		ns	[1, 2]
			5.5V	300		ns	
7	TwDSW	/DS (Write) Low Width	4.0V	165		ns	[1, 2]
			5.5V	165		ns	
8	TdDSR(DR)	/DS Falling to Read	4.0V		260	ns	[1, 2]
		Data Required Valid	5.5V		260	ns	
9	ThDR(DS)	Read Data to	4.0V	0		ns	[2]
		/DS Rising Hold Time	5.5V	0		ns	
10	TdDS(A)	/DS Rising to Address	4.0V	85		ns	[2]
		Active Delay	5.5V	95		ns	
11	TdDS(AS)	/DS Rising to /AS	4.0V	60		ns	[2]
		Falling Delay	5.5V	70		ns	
12	TdR/W(AS)	R//W Valid to /AS	4.0V	70		ns	[2]
		Rising Delay	5.5V	70		ns	
13	TdDS(R/W)	/DS Rising to	4.0V	70		ns	[2]
		R//W Not Valid	5.5V	70		ns	
14	TdDW(DSW)	Write Data Valid to /DS	4.0V	80		ns	[2]
		Falling (Write) Delay	5.5V	80		ns	
15	TdDS(DW)	/DS Rising to Write	4.0V	70		ns	[2]
		Data Not Valid Delay	5.5V	80		ns	
16	TdA(DR)	Address Valid to Read	4.0V		475	ns	[1, 2]
		Data Required Valid	5.5V		475	ns	
17	TdAS(DS)	/AS Rising to	4.0V	100		ns	[2]
		/DS Falling Delay	5.5V	100		ns	
18	TdDM(AS)	/DM Valid to /AS	4.0V	55		ns	[2]
		Falling Delay	5.5V	55		ns	
19	TdDS(DM)	/DS Rise to	4.0V	70		ns	
		/DM Valid Delay	5.5V	70		ns	
20	ThDS(A)	/DS Rise to Address	4.0V	70		ns	
		Valid Hold Time	5.5V	70		ns	

Notes:

[1] When using extended memory timing add 2 TpC.

[2] Timing numbers given are for minimum TpC.

[3] 4.0V to 5.5V.

Standard Test Load.

All timing references use 0.9 V_{CC} for a logic 1 and 0.1 V_{CC} for a logic 0.

AC CHARACTERISTICS (Z86L73/L74)

External I/O or Memory Read and Write Timing Table

No.	Symbol	Parameter	V_{CC} Note [3]	T_A = 0°C to +70°C 8.0 MHz Min	Max	Units	Notes
1	TdA(AS)	Address Valid to	2.0V	55		ns	[2]
		/AS Rising Delay	3.9V	55		ns	
2	TdAS(A)	/AS Rising to Address	2.0V	70		ns	[2]
		Float Delay	3.9V	70		ns	
3	TdAS(DR)	/AS Rising to Read	2.0V		400	ns	[1, 2]
		Data Required Valid	3.9V		400	ns	
4	TwAS	/AS Low Width	2.0V	80		ns	[2]
			3.9V	80		ns	
5	Td	Address Float to	2.0V	0		ns	
		/DS Falling	3.9V	0		ns	
6	TwDSR	/DS (Read) Low Width	2.0V	300		ns	[1, 2]
			3.9V	300		ns	
7	TwDSW	/DS (Write) Low Width	2.0V	165		ns	[1, 2]
			3.9V	165		ns	
8	TdDSR(DR)	/DS Falling to Read	2.0V		260	ns	[1, 2]
		Data Required Valid	3.9V		260	ns	
9	ThDR(DS)	Read Data to	2.0V	0		ns	[2]
		/DS Rising Hold Time	3.9V	0		ns	
10	TdDS(A)	/DS Rising to Address	2.0V	85		ns	[2]
		Active Delay	3.9V	95		ns	
11	TdDS(AS)	/DS Rising to /AS	2.0V	60		ns	[2]
		Falling Delay	3.9V	70		ns	
12	TdR/W(AS)	R//W Valid to /AS	2.0V	70		ns	[2]
		Rising Delay	3.9V	70		ns	
13	TdDS(R/W)	/DS Rising to	2.0V	70		ns	[2]
		R//W Not Valid	3.9V	70		ns	
14	TdDW(DSW)	Write Data Valid to /DS	2.0V	80		ns	[2]
		Falling (Write) Delay	3.9V	80		ns	
15	TdDS(DW)	/DS Rising to Write	2.0V	70		ns	[2]
		Data Not Valid Delay	3.9V	80		ns	
16	TdA(DR)	Address Valid to Read	2.0V		475	ns	[1, 2]
		Data Required Valid	3.9V		475	ns	
17	TdAS(DS)	/AS Rising to	2.0V	100		ns	[2]
		/DS Falling Delay	3.9V	100		ns	
18	TdDM(AS)	/DM Valid to /AS	2.0V	55		ns	[2]
		Falling Delay	3.9V	55		ns	
19	TdDS(DM)	/DS Rise to	2.0V	70		ns	
		/DM Valid Delay	3.9V	70		ns	
20	ThDS(A)	/DS Rise to Address	2.0V	70		ns	
		Valid Hold Time	3.9V	70		ns	

Notes:

[1] When using extended memory timing add 2 TpC.

[2] Timing numbers given are for minimum TpC.

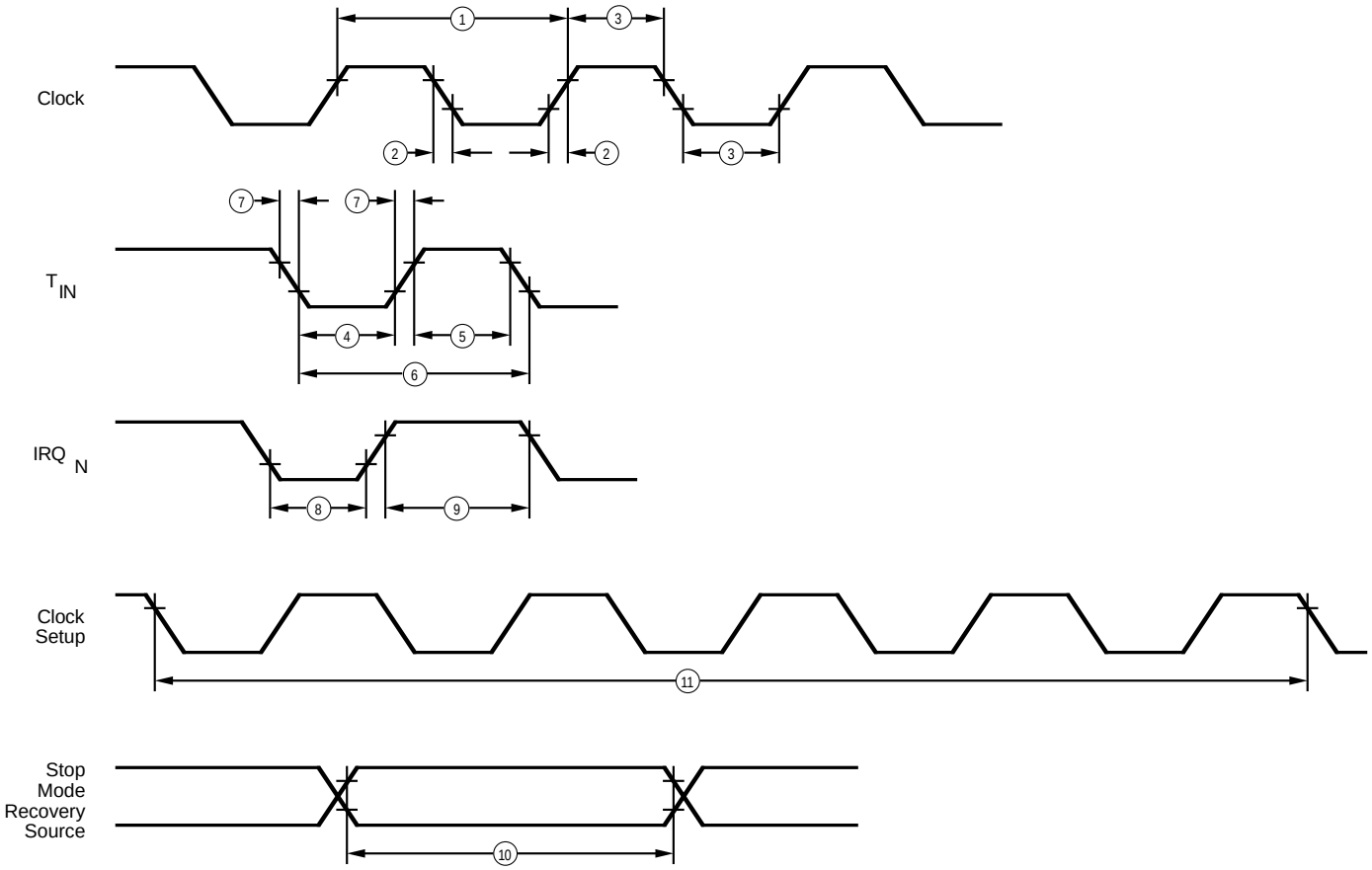
[3] 2.0V to 3.9V.

Standard Test Load.

All timing references use 0.9 V_{CC} for a logic 1 and 0.1 V_{CC} for a logic 0.

AC CHARACTERISTICS

Additional Timing Diagram



Additional Timing

AC CHARACTERISTICS (Z86E73/E74)

Additional Timing Table

No	Symbol	Parameter		V_{CC} Note [3]	T_A = 0°C to +70°C 8.0 MHz Min	Max	Units	Notes
1	TpC	Input Clock Period		4.0V	121	DC	ns	[1]
				5.5V	121	DC	ns	[1]
2	TrC,TfC	Clock Input Rise		4.0V		25	ns	[1]
		and Fall Times		5.5V		25	ns	[1]
3	TwC	Input Clock Width		4.0V	37		ns	[1]
				5.5V	37		ns	[1]
4	TwTinL	Timer Input		4.0V	100		ns	[1]
		Low Width		5.5V	70		ns	[1]
5	TwTinH	Timer Input		4.0V	3TpC			[1]
		High Width		5.5V	3TpC			[1]
6	TpTin	Timer Input Period		4.0V	8TpC			[1]
				5.5V	8TpC			[1]
7	TrTin,TfTin	Timer Input Rise		4.0V		100	ns	[1]
		and Fall Timers		5.5V		100	ns	[1]
8A	TwIL	Interrupt Request		4.0V	100		ns	[1, 2]
		Low Time		5.5V	70		ns	[1, 2]
8B	TwIL	Int. Request		4.0V	3TpC			[1, 3]
		Low Time		5.5V	3TpC			[1, 3]
9	TwIH	Interrupt Request		4.0V	3TpC			[1, 2]
		Input High Time		5.5V	3TpC			[1, 2]
10	Twsm	Stop-Mode Recovery		4.0V	12		ns	[8]
		Width Spec		5.5V	12		ns	[8]
				4.0V	5TpC			[7]
				5.5V	5TpC			[7]
11	Tost	Oscillator		4.0V		5TpC		[4]
		Start-up Time		5.5V		5TpC		[4]
12	Twdt	Watch-Dog Timer	(5 ms)	4.0V	12	75	ms	D0 = 0 [5]
		Delay Time		5.5V	5	20	ms	D1 = 0 [5]
			(10 ms)	4.0V	25	150	ms	D0 = 1 [5]
				5.5V	10	40	ms	D1 = 0 [5]
			(20 ms)	4.0V	50	300	ms	D0 = 0 [5]
				5.5V	20	80	ms	D1 = 1 [5]
			(80 ms)	4.0V	225	1200	ms	D0 = 1 [5]
				5.5V	80	320	ms	D1 = 1 [5]

Notes:

[1] Timing Reference uses 0.9 V_{CC} for a logic 1 and 0.1 V_{CC} for a logic 0.
[2] Interrupt request through Port 3 (P33-P31).
[3] Interrupt request through Port 3 (P30).
[4] SMR – D5 = 0.
[5] Reg. WDTMR.
[6] 4.0V to 5.5V.
[7] Reg. SMR – D5 = 0.
[8] Reg. SMR – D5 = 1.

AC CHARACTERISTICS (Z86L73/L74)

Additional Timing Table

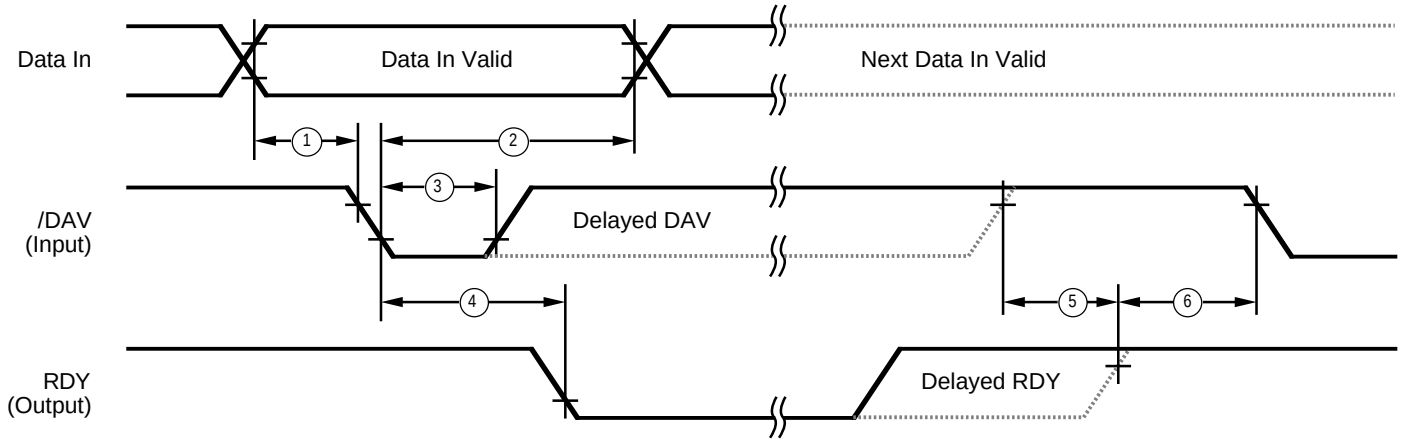
No	Symbol	Parameter		V_{CC} Note [3]	T_A = 0°C to +70°C 8.0 MHz Min	Max	Units	Notes
1	TpC	Input Clock Period		2.0V	121	DC	ns	[1]
				3.9V	121	DC	ns	[1]
2	TrC,TfC	Clock Input Rise		2.0V		25	ns	[1]
		and Fall Times		3.9V		25	ns	[1]
3	TwC	Input Clock Width		2.0V	37		ns	[1]
				3.9V	37		ns	[1]
4	TwTinL	Timer Input		2.0V	100		ns	[1]
		Low Width		3.9V	70		ns	[1]
5	TwTinH	Timer Input		2.0V	3TpC			[1]
		High Width		3.9V	3TpC			[1]
6	TpTin	Timer Input Period		2.0V	8TpC			[1]
				3.9V	8TpC			[1]
7	TrTin,TfTin	Timer Input Rise		2.0V		100	ns	[1]
		and Fall Timers		3.9V		100	ns	[1]
8A	TwIL	Interrupt Request		2.0V	100		ns	[1, 2]
		Low Time		3.9V	70		ns	[1, 2]
8B	TwIL	Int. Request		2.0V	3TpC			[1, 3]
		Low Time		3.9V	3TpC			[1, 3]
9	TwIH	Interrupt Request		2.0V	3TpC			[1, 2]
		Input High Time		3.9V	3TpC			[1, 2]
10	Twsm	Stop-Mode Recovery		2.0V	12		ns	[8]
		Width Spec		3.9V	12		ns	[8]
				2.0V	5TpC			[7]
				3.9V	5TpC			[7]
11	Tost	Oscillator		2.0V		5TpC		[4]
		Start-up Time		3.9V		5TpC		[4]
12	Twdt	Watch-Dog Timer	(5 ms)	2.0V	12	75	ms	D0 = 0 [5]
		Delay Time		3.9V	5	20	ms	D1 = 0 [5]
			(10 ms)	2.0V	25	150	ms	D0 = 1 [5]
				3.9V	10	40	ms	D1 = 0 [5]
			(20 ms)	2.0V	50	300	ms	D0 = 0 [5]
				3.9V	20	80	ms	D1 = 1 [5]
			(80 ms)	2.0V	225	1200	ms	D0 = 1 [5]
				3.9V	80	320	ms	D1 = 1 [5]

Notes:

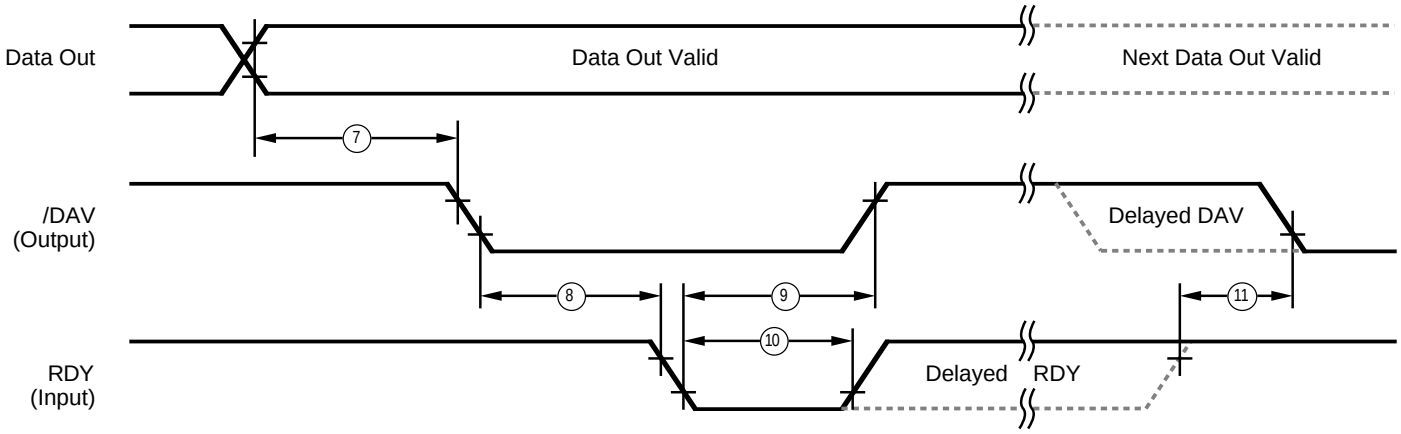
[1] Timing Reference uses 0.9 V_{CC} for a logic 1 and 0.1 V_{CC} for a logic 0.
[2] Interrupt request through Port 3 (P33-P31).
[3] Interrupt request through Port 3 (P30).
[4] SMR – D5 = 0.
[5] Reg. WDTMR.
[6] 2.0V to 3.9V.
[7] Reg. SMR – D5 = 0.
[8] Reg. SMR – D5 = 1.

AC CHARACTERISTICS

Handshake Timing Diagrams



Input Handshake Timing



Output Handshake Timing

AC CHARACTERISTICS (Z86E73/E74)

Handshake Timing Table

No	Symbol	Parameter	V_{CC} Note [3]	T_A = 0°C to +70°C 8.0 MHz Min	Max	Data Direction
1	TsDI(DAV)	Data In Setup Time	4.0V	0		IN
			5.5V	0		IN
2	ThDI(DAV)	Data In Hold Time	4.0V	160		IN
			5.5V	115		IN
3	TwDAV	Data Available Width	4.0V	155		IN
			5.5V	110		IN
4	TdDAVI(RDY)	DAV Falling to RDY	4.0V		160	IN
		Falling Delay	5.5V		115	IN
5	TdDAVId(RDY)	DAV Rising to RDY	4.0V		120	IN
		Falling Delay	5.5V		80	IN
6	TdRDYO(DAV)	RDY Rising to DAV	4.0V	0		IN
		Falling Delay	5.5V	0		IN
7	TdDO(DAV)	Data Out to DAV	4.0V	63		OUT
		Falling Delay	5.5V	63		OUT
8	TdDAV0(RDY)	DAV Falling to RDY	4.0V	0		OUT
		Falling Delay	5.5V	0		OUT
9	TdRDY0(DAV)	RDY Falling to DAV	4.0V		160	OUT
		Rising Delay	5.5V		115	OUT
10	TwRDY	RDY Width	4.0V	110		OUT
			5.5V	80		OUT
11	TdRDY0d(DAV)	RDY Rising to DAV	4.0V		110	OUT
		Falling Delay	5.5V		80	OUT

Note:
[3] 4.0V to 5.5V.

AC CHARACTERISTICS (Z86L73/L74)

Handshake Timing Table

No	Symbol	Parameter	V_{CC} Note [3]	T_A = 0°C to +70°C 8.0 MHz Min	Max	Data Direction
1	TsDI(DAV)	Data In Setup Time	2.0V	0		IN
			3.9V	0		IN
2	ThDI(DAV)	Data In Hold Time	2.0V	160		IN
			3.9V	115		IN
3	TwDAV	Data Available Width	2.0V	155		IN
			3.9V	110		IN
4	TdDAVI(RDY)	DAV Falling to RDY	2.0V		160	IN
		Falling Delay	3.9V		115	IN
5	TdDAVId(RDY)	DAV Rising to RDY	2.0V		120	IN
		Falling Delay	3.9V		80	IN
6	TdRDYO(DAV)	RDY Rising to DAV	2.0V	0		IN
		Falling Delay	3.9V	0		IN
7	TdDO(DAV)	Data Out to DAV	2.0V	63		OUT
		Falling Delay	3.9V	63		OUT
8	TdDAV0(RDY)	DAV Falling to RDY	2.0V	0		OUT
		Falling Delay	3.9V	0		OUT
9	TdRDY0(DAV)	RDY Falling to DAV	2.0V		160	OUT
		Rising Delay	3.9V		115	OUT
10	TwRDY	RDY Width	2.0V	110		OUT
			3.9V	80		OUT
11	TdRDY0d(DAV)	RDY Rising to DAV	2.0V		110	OUT
		Falling Delay	3.9V		80	OUT

Note:
[3] 2.0V to 3.9V.