YAMAHA LSI

YMF753

AC'97 Revision2.2 Audio CODEC with Digital Audio I/F

■ OVERVIEW

YMF753 is an AC'97 Audio CODEC LSI, which is fully compliant with the industry standard "Audio CODEC '97" component specification (Revision 2.2).

Different from former AC'97, YMF753 supports new features like SPDIF OUT and Zoomed Video Port. Without using a digital controller, these new features can be enhanced in the AC'97 sound system that has an ICH controller built-in chipset.

Low power consumption is supported not only in the normal mode but can be controlled in the power-down mode.

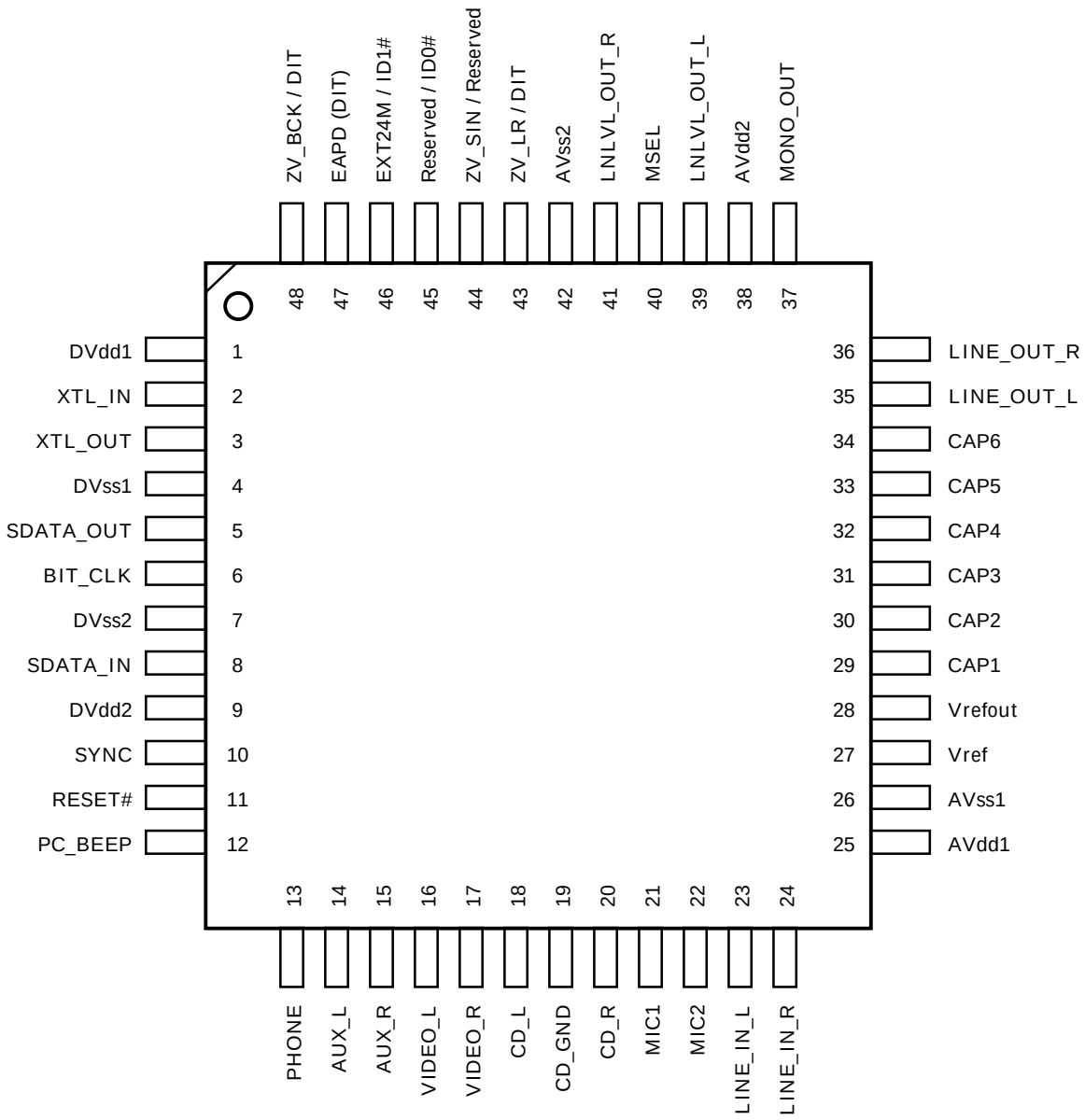
■ FEATURES

- AC'97 Revision 2.2 Compliant
- Exceeds PC99 / PC2001 Analog Performance Requirement
  (Mobile PC Audio Performance Compliant when analog low power supply is used.)
- Analog Inputs :
  - 4 Stereo Inputs: LINE, CD, VIDEO, AUX
  - 2 Monaural Inputs: Speakerphone and PC BEEP Inputs
  - 2 Independent Microphone Inputs
- PC BEEP can directly output to Line Out
- Internal +20dB amplifier circuitry for microphone
- Analog Outputs : Stereo LINE Output, True LINE Level and Monaural Output
- Supports Zoomed Video Port
- Supports Consumer IEC958 Output Port (SPDIF OUT)
- SPDIF Output for AC'97 Revision 1.0 Compliant
- Different audio data from AC-Link can be output to SPDIF and Line Out
- Supports 3D Enhancement (Wide Stereo), and Bass / Treble control
- Multiple CODEC Capability
- Programmable Power Down Mode
- Supports EAPD (External Amplifier Power Down)
- Power Supplies : Analog 4.3V to 5.0V, Digital 3.3V or 5.0V
- 48-Pin SQFP Package (YMF753-S)

YAMAHA CORPORATION

YMF753 CATALOG
CATALOG No.:LSI-4MF753A2
March 6, 2001

■ PIN CONFIGURATION



48-Pin SQFP Top View

■ PIN DESCRIPTION

No.	Name	I/O	Function
1	DVdd1	-	Digital power supply (Typ. +3.3V / +5.0V) Connect to the digital ground with 0.1μF and 47μF capacitors. Connect this pin to DVdd2.
2	XTL_IN	I	24.576MHz Clock Input
3	XTL_OUT	O	24.576MHz Clock Output
4	DVss1	-	Digital ground. Connect this pin to DVss2.
5	SDATA_OUT	I	AC'97 Serial Input Stream
6	BIT_CLK	I/O	AC'97 Bit Clock As an output pin at the primary codec where CODEC ID=00. As an input pin at the secondary codec where CODEC ID=01,10,11.
7	DVss2	-	Digital ground. Connect this pin to DVss1.
8	SDATA_IN	O	AC'97 Serial Output Stream
9	DVdd2	-	Digital power supply (Typ. +3.3V / +5.0V) Connect to the digital ground with 0.1μF and 47μF capacitors. Connect this pin to DVdd1.
10	SYNC	I	SYNC Input (Fixed at 48kHz)
11	RESET#	I	Hardware Reset
12	PC_BEEP	AI	PC Speaker Beep
13	PHONE	AI	Telephony Input
14	AUX_L	AI	AUX Input Left Channel
15	AUX_R	AI	AUX Input Right Channel
16	VIDEO_L	AI	Video Audio Input Left Channel
17	VIDEO_R	AI	Video Audio Input Right Channel
18	CD_L	AI	CD Audio Input Left Channel
19	CD_GND	AI	CD Audio Analog Ground Connect this pin to CD Ground or Analog Ground.
20	CD_R	AI	CD Audio Input Right Channel
21	MIC1	AI	Microphone Input 1
22	MIC2	AI	Microphone Input 2
23	LINE_IN_L	AI	Line Input Left Channel
24	LINE_IN_R	AI	Line Input Right Channel
25	AVdd1	-	Analog Power Supply (Typ. +4.3V to +5.0V) Connect to the analog ground with 0.1μF and 47μF capacitors. Connect this pin to AVdd2.
26	AVss1	-	Analog ground. Connect this pin to AVss2.
27	Vref	AO	Analog Reference Voltage Connect to the analog ground with 0.1μF and 22μF capacitors.
28	Vrefout	AO	Analog Reference Voltage Output Connect to the analog ground with 0.1μF and 22μF capacitors when it is used to the external circuit.

No.	Name	I/O	Function
29	CAP1	A	Connect to the analog ground with a 2200pF capacitor.
30	CAP2	A	Connect to the analog ground with a 0.015μF capacitor.
31	CAP3	A	Connect to the analog ground with a 0.01μF capacitor.
32	CAP4	A	Connect to the analog ground with a 2200pF capacitor.
33	CAP5	A	Connect to the analog ground with a 0.015μF capacitor.
34	CAP6	A	Connect to the analog ground with a 0.01μF capacitor.
35	LINE_OUT_L	AO	Line Output Left Channel
36	LINE_OUT_R	AO	Line Output Right Channel
37	MONO_OUT	AO	Monaural Output
38	AVdd2	-	Analog power supply (Typ. +4.3V to +5.0V) Connect to the analog ground with 0.1μF and 47μF capacitors. Connect this pin to AVdd1.
39	LNLVL_OUT_L	AO	True LINE Level Output Left Channel
40	MSEL	I	Mode Select, which changes the pin function of No.43 – 46, 48.
41	LNLVL_OUT_R	AO	True LINE Level Output Right Channel
42	AVss2	-	Analog ground. Connect to AVss1.
47	EAPD (DIT)	O	The function is selected at 62h TX-7 bit. TX-7=“0”, External Amplifier Power Down TX-7=“1”, Digital Audio Interface Output (48kHz)

1. MSEL= “High” (Connect to analog power supply.)

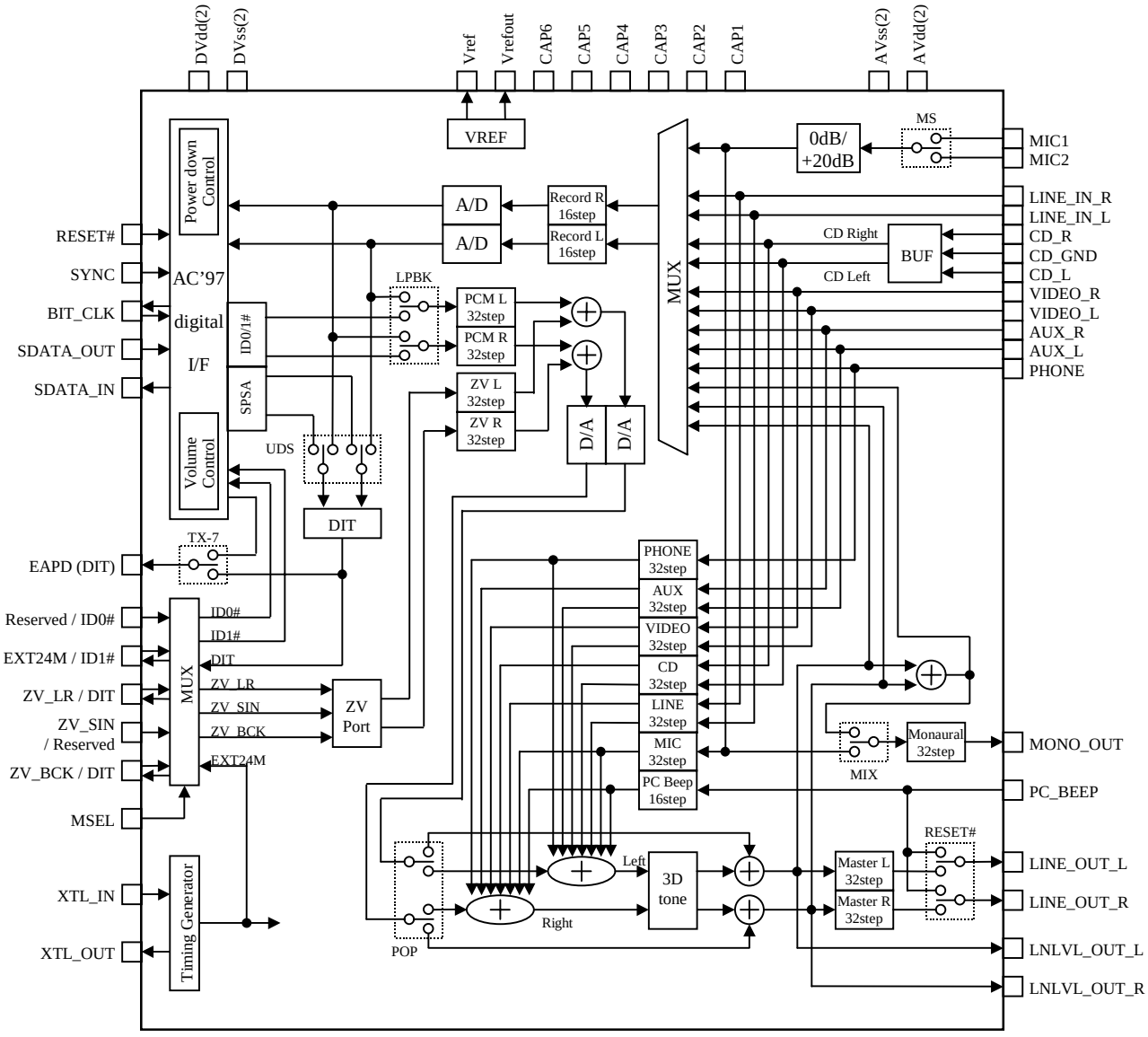
No.	Name	I/O	Function
43	ZV_LR	I-	Zoomed Video Port L/R clock
44	ZV_SIN	I-	Zoomed Video Port serial data
45	Reserved	-	Do not connect externally.
46	EXT24M	O	24.576MHz clock output
48	ZV_BCK	I-	Zoomed Video Port bit clock

2. MSEL= “Low” (Connect to analog ground.)

No.	Name	I/O	Function
43	DIT	O	Digital Audio Interface Output (48kHz)
44	Reserved	-	Do not connect externally.
45	CODEC ID0#	I+	CODEC ID
46	CODEC ID1#	I+	CODEC ID
48	DIT	O	Digital Audio Interface Output (48kHz)

Note) AI: Analog Input Pin, AO: Analog Output Pin, I+: Input Pin with a Pull-up resistor,
I-: Input Pin with a Pull-down resistor

■ BLOCK DIAGRAM



■ MIXER REGISTERS

	NAME	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
00h	Reset	"0"	"0"	"0"	"0"	"0"	"0"	"0"	"0"	"0"	"1"	"0"	"0"	"0"	"0"	"0"	"0"	0040h
02h	Master vol.	Mute	-	ML5-0						-	-	MR5-0						8000h
04h	LNLVL vol.	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0000h
06h	Master vol. Mono	Mute	-	-	-	-	-	-	-	-	-	MM5-0						8000h
08h	Master tone	-	-	-	-	-	BA2-0			-	-	-	-	-	TR2-0			0707h
0Ah	PC_BEEP vol.	Mute	-	-	-	-	-	-	-	-	-	-	PV3-0				-	0000h
0Ch	Phone vol.	Mute	-	-	-	-	-	-	-	-	-	-	GN4-0					8008h
0Eh	Mic vol.	Mute	-	-	-	-	-	-	-	-	20dB	-	GN4-0					8008h
10h	Line in vol.	Mute	-	-	GL4-0					-	-	-	GR4-0					8808h
12h	CD vol.	Mute	-	-	GL4-0					-	-	-	GR4-0					8808h
14h	Video vol.	Mute	-	-	GL4-0					-	-	-	GR4-0					8808h
16h	Aux vol.	Mute	-	-	GL4-0					-	-	-	GR4-0					8808h
18h	PCM out vol.	Mute	-	-	GL4-0					-	-	-	GR4-0					8808h
1Ah	Record Select	-	-	-	-	-	SL2-0			-	-	-	-	-	SR2-0			0000h
1Ch	Record Gain	Mute	-	-	-	GL3-0				-	-	-	-	GR3-0				8000h
20h	General Purpose	POP	-	3D	-	-	-	MIX	MS	LPBK	-	-	-	-	-	-	-	0000h
22h	3D Control	-	-	-	-	WD3-1			-	-	-	-	-	-	-	-	-	0000h
26h	Power Down	EAPD	-	PR5	PR4	PR3	PR2	PR1	PR0	-	-	-	-	REF	ANL	DAC	ADC	000xh
28h	Extended Audio ID	ID1	ID0	-	-	REV1-0		AMAP	LDAC	SDAC	CDAC	-	-	-	SPDIF	-	-	xxx4h
2Ah	Ext Audio Stat/Ctrl	-	-	-	-	-	SPCV	-	-	-	-	SPSA1-0		-	SPDIF	-	-	0400h
3Ah	DIT Control 1	V	-	SPSR1-0		GL	CC6	CC5	CC4	CC3	CC2	CC1	CC0	PRE	COPY	AUD#	PRO	2000h
62h	Vendor Function	*	*	*	*	*	*	*	*	*	*	*	*	TX-7	EXEN	*	*	0224h
64h	ZV vol.	Mute	MSEL	-	GL4-0					ZEN	ZAC	-	GR4-0					x808h
66h	DIT Control 2	-	-	-	-	-	-	-	*	*	*	TX-3	*	TX-8	DMU	UDS	3AWE	0040h
68h	3D Mode Select	-	-	-	-	WM1-0		-	-	-	-	-	-	-	-	-	-	0C00h
7Ch	Vendor ID 1	"0"	"1"	"0"	"1"	"1"	"0"	"0"	"1"	"0"	"1"	"0"	"0"	"1"	"1"	"0"	"1"	594Dh
7Eh	Vendor ID 2	"0"	"1"	"0"	"0"	"1"	"0"	"0"	"0"	"0"	"0"	"0"	"0"	"0"	"0"	"1"	"1"	4803h

Note) The * bits of 62h and 66h should not be changed from the default value.

Do not access to 5Ah and 60h because they are LSI test registers.

00h : Reset (Read/Write reset, Default: 0040h)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
"0"	"0"	"0"	"0"	"0"	"0"	"0"	"0"	"0"	"1"	"0"	"0"	"0"	"0"	"0"	"0"

When any value is written to this register, all registers except for the lower 4 bits of 26h:Power Down are reset to the default value.

02h : Master Volume (Read/Write, Default: 8000h)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Mute	-	ML5-0						-	-	MR5-0					

Mute.....Setting this bit to “1” mutes both left and right channels of the line output.

ML5-0.....These bits determine the volume level of the line output left channel by 1.5dB step. The volume range is from 0dB to -46.5dB. When all bits are set to “0”, volume is maximum (0dB) and when they are set to “011111b”, volume is minimum (-46.5dB). And when ML5 bit is set to “1”, the volume level is minimum (-46.5dB), then their status become “011111b”.

MR5-0.....These bits determine the volume level of the line output right channel by 1.5dB step. Setting to them is the same as the upper ML5-0 bits.

04h : LNLVL Volume (Read/Write, Default: 0000h)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

Though the register can be written any value, it does not function.

0000h is always read out.

06h : Master Volume Mono (Read/Write, Default: 8000h)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Mute	-	-	-	-	-	-	-	-	-	MM5-0					

Mute.....Setting this bit to “1” mutes the monaural output.

MM5-0.....These bits determine the volume level of the monaural output by 1.5dB step. The volume range is from 0dB to -46.5dB. When all bits are set to “0”, volume is maximum (0dB) and when they are set to “011111b”, volume is minimum (-46.5dB). And when MM5 bit is set to “1”, the volume level is minimum (-46.5dB), then their status become “011111b”

08h : Master Tone (Read/Write, Default: 0707h)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
-	-	-	-	-	BA2-0			-	-	-	-	-	TR2-0		

BA2-0 .....These bits determine the bass level by 1.5dB step. The tone range is from 0dB to +10.5dB. When all bits are set to “0”, tone is maximum (+10.5dB) and when all bits are set to “1”, tone is minimum (0dB)

TR2-0.....These bits determine the treble level by 1.5dB step. Setting to them is the same as the upper BA2-0.

0Ah : PC_BEEP Volume (Read/Write, Default: 0000h)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Mute	-	-	-	-	-	-	-	-	-	-	PV3-0				-

Mute.....Setting this bit to "1" mutes the PC_BEEP.

PV3-0.....These bits determine the volume level of the PC_BEEP by 3.0dB step. The volume range is from 0dB to -45dB. When all bits are set to "0", volume is maximum (0dB) and when all bits are set to "1", volume is minimum (-45dB).

0Ch : Phone Volume (Read/Write, Default: 8008h)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Mute	-	-	-	-	-	-	-	-	-	-	GN4-0				

Mute.....Setting this bit to "1" mutes the Phone.

GN4-0 .....These bits determine the volume level of the Phone by 1.5dB step. The volume range is from +12dB to -34.5dB. When all bits are set to "0", volume is maximum (+12dB) and when all bits are set to "1", volume is minimum (-34.5dB).

0Eh : Mic Volume (Read/Write, Default: 8008h)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Mute	-	-	-	-	-	-	-	-	20dB	-	GN4-0				

Mute.....Setting this bit to "1" mutes the Microphone.

20dB .....Setting this bit to "1" increases +20dB for the microphone volume, which is set to GN4-0 bits.

GN4-0 .....These bits determine the volume level of the microphone by 1.5dB step. The volume range is from +12dB to -34.5dB. When all bits are set to "0", volume is maximum (+12dB) and when all bits are set to "1", volume is minimum (-34.5dB).

10h : Line in Volume (Read/Write, Default: 8808h)
12h : CD Volume (Read/Write, Default: 8808h)
14h : Video Volume (Read/Write, Default: 8808h)
16h : Aux Volume (Read/Write, Default: 8808h)
18h : PCM out Volume (Read/Write, Default: 8808h)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Mute	-	-	GL4-0					-	-	-	GR4-0				

Mute.....Setting this bit to "1" mutes both left and right channels of the each source.

GL4-0 .....These bits determine the volume level of the left channel by 1.5dB step. The volume range is from +12dB to -34.5dB. When all bits are set to "0", volume is maximum (+12dB) and when all bits are set to "1", volume is minimum (-34.5dB).

GR4-0 .....These bits determine the volume level of the right channel by 1.5dB step.
Setting to them is the same as the upper GL4-0 bits.

1Ah : Record Select (Read/Write, Default: 0000h)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
-	-	-	-	-	SL2-0			-	-	-	-	-	SR2-0		

SL2-0 .....These bits select the left channel source for A/D converter.

SR2-0 .....These bits select the right channel source for A/D converter.

SL2	SL1	SL0	Left Source	SR2	SR1	SR0	Right Source
0	0	0	Mic	0	0	0	Mic
0	0	1	CD L-ch	0	0	1	CD R-ch
0	1	0	Video L-ch	0	1	0	Video R-ch
0	1	1	Aux L-ch	0	1	1	Aux R-ch
1	0	0	Line in L-ch	1	0	0	Line in R-ch
1	0	1	Stereo Mix L-ch	1	0	1	Stereo Mix R-ch
1	1	0	Mono Mix	1	1	0	Mono Mix
1	1	1	Phone	1	1	1	Phone

1Ch : Record Gain (Read/Write, Default: 8000h)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Mute	-	-	-	GL3-0				-	-	-	-	GR3-0			

Mute.....Setting this bit to “1” mutes the source which is selected at 1Ah:Record Select.

GL3-0 .....These bits determine the volume level, which is selected at 1Ah:Record Select SL2-0 bits, by 1.5dB step. The volume range is from 0dB to +22.5dB. When all bits are set to “0”, volume is minimum (0dB) and when all bits are set to “1”, volume is maximum (+22.5dB).

GR3-0 .....These bits determine the volume level, which is selected at 1Ah:Record Select SR2-0 bits, by 1.5dB step. Setting to them is the same as the upper GL3-0 bits.

20h : General Purpose (Read/Write, Default: 0000h)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
POP	-	3D	-	-	-	MIX	MS	LPBK	-	-	-	-	-	-	-

POP.....This bit selects whether PCM (DAC) output is gone through the 3D and Tone (Bass / Treble) or not.

"0" : PCM (DAC) output is gone through the 3D and Tone.

"1" : PCM (DAC) output is bypassed the 3D and Tone.

3D .....This bit selects whether 3D enhancement is used or not.

"0" : Off

"1" : On

MIX .....This bit selects the output to MONO_OUT(No.37).

"0" : All mixing sources are output to MONO_OUT.

"1" : The microphone input is output to MONO_OUT.

MS .....This bit selects either MIC1 or MIC2 for the microphone input.

"0" : MIC1 (No.21)

"1" : MIC2 (No.22)

LPBK.....This bit selects data to the D/A converter.

"0" : Data from the AC-Link

"1" : Loopback from A/D converted data

22h : 3D Control (Read/Write, Default: 0000h)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
-	-	-	-	WD3-1			-	-	-	-	-	-	-	-	-

WD3-1 .....These bits determine the wide level of 3D enhancement (wide stereo). The wide range is from 0% to 100%. When all bits are set to "0", wide level is 0% and when all bits are set to "1", wide level is 100%.

26h : Power Down (Read/Write, Default: 000xh)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
EAPD	-	PR5	PR4	PR3	PR2	PR1	PR0	-	-	-	-	REF	ANL	DAC	ADC

EAPD.....This bit controls the state of EAPD (No.47) pin.
"0" : Low
"1" : High

PR5 .....This bit controls the power state of the clock oscillation circuit.
"0" : Normal
"1" : Power down

PR4 .....This bit controls the power state of the AC-Link.
"0" : Normal
"1" : Power down

PR3 .....This bit controls the power state of the analog mixer.
"0" : Normal
"1" : Power down (Vref off)

PR2 .....This bit controls the power state of the analog mixer.
"0" : Normal
"1" : Power down (Vref still on)

PR1 .....This bit controls the power state of the D/A converter.
"0" : Normal
"1" : Power down

PR0 .....This bit controls the power state of the A/D converter.
"0" : Normal
"1" : Power down

REF.....This bit is Read Only, and indicates the state of Vref.
"0" : Ground level
"1" : Reference voltage

ANL.....This bit is Read Only, and indicates the state of the analog mixer.
"0" : The analog mixer does not work.
"1" : The analog mixer works normally.

DAC.....This bit is Read Only, and indicates the state of the D/A converter.
"0" : The D/A converter does not work.
"1" : The D/A converter works normally.

ADC.....This bit is Read Only, and indicates the state of the A/D converter.
"0" : The A/D converter does not work.
"1" : The A/D converter works normally.

Note) When YMF753 is the Secondary CODEC, and both PR5 and PR4 are set to "1", these bits are not cleared by Warm Reset.

28h : Extended Audio ID (Read Only, Default: xxx4h)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
ID1	ID0	-	-	REV1-0		AMAP	LDAC	SDAC	CDAC	-	-	-	SPDIF	-	-

ID1,ID0.....These bits indicate CODEC ID. The states are determined by setting both No.46 and 45 pins. When MSEL is high, they are fixed to "Primary ID00".

ID1# (No.46)		ID0# (No.45)		CODEC ID Configuration
Pin Status	Logic Value	Pin Status	Logic Value	
OPEN ("H")	"0"	OPEN ("H")	"0"	Primary ID00
OPEN ("H")	"0"	GND ("L")	"1"	Secondary ID01
GND ("L")	"1"	OPEN ("H")	"0"	Secondary ID10
GND ("L")	"1"	GND ("L")	"1"	Secondary ID11

REV1-0.....These bits are hardwired to "01b", which indicates AC'97 Revision 2.2 Compliant.

AMAP.....This bit is hardwired to "1". It indicates that the PCM DAC uses data of the standard slot into twelve slots, as the following table.

CODEC ID	Slot Number		
	PCM Left DAC	PCM Right DAC	
00	Slot 3	Slot 4	Original definition (master)
01	Slot 3	Slot 4	Original definition (docking)
10	Slot 7	Slot 8	Left / Right surround channels
11	Slot 6	Slot 9	Center / LFE channels

LDAC .....When PCM DAC uses the LFE channel, this bit is set to "1".

SDAC .....When PCM DAC uses the surround channels, this bit is set to "1".

CDAC .....When PCM DAC uses the center channel, this bit is set to "1".

SPDIF .....This bit is hardwired to "1", which indicates that SPDIF output is compliant with AC'97 Revision 2.2.

2Ah : Ext Audio Stat/Ctrl (Read/Write, Default: 0400h)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
-	-	-	-	-	SPCV	-	-	-	-	SPSA1-0		-	SPDIF	-	-

SPCV .....This bit is hardwired to "1", which indicates that SPDIF output configuration is valid.

SPSA1-0 .....These bits select DIT output slot.

SPSA1	SPSA0	L-ch Slot Number	R-ch Slot Number
0	0	Slot 3	Slot 4
0	1	Slot 7	Slot 8
1	0	Slot 6	Slot 9
1	1	Slot 10	Slot 11

SPDIF .....This bit selects whether the SPDIF signal is output from DIT or not.

"0" : DIT is power down state, and outputs low level.

"1" : SPDIF signal is output from DIT.

3Ah : DIT Control 1 (Read/Write, Default: 2000h)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
V	-	SPSR1-0		GL	CC6	CC5	CC4	CC3	CC2	CC1	CC0	PRE	COPY	AUD#	PRO

V .....This bit determines V-bit (Validity flag) output from DIT.
"0" : The Validity flag is "0" (Valid).
"1" : The Validity flag is "1" (Invalid).

SPSR1-0 .....These bits determine sampling frequency of channel status output from DIT. These bits are hardwired to "10b", because SPDIF output of YMF753 is fixed to 48kHz.

GL.....This bit determines bit15: L-bit (Generation status) of channel status output from DIT. The sense of Generation status is different by Category Code.

CC6-0 .....These bits determine bit14-8: Category Code of channel status output from DIT.

PRE.....This bit determines bit3: Pre-emphasis of channel status output from DIT.
"0" : without Pre-emphasis
"1" : with Pre-emphasis of 50/15µs

COPY .....This bit determines bit2: Copy protection of channel status output from DIT.
"0" : Copyright
"1" : No Copyright

AUD# .....This bit determines bit1 of channel status output from DIT. If AC-3 or DTS is output, set to "1".
"0" : PCM format
"1" : Non-PCM format

PRO .....This bit determines bit0 of channel status output from DIT. It should be set to "0" as Consumer use.

62h : Vendor Function (Read/Write, Default: 0224h)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
*	*	*	*	*	*	*	*	*	*	*	*	TX-7	EXEN	*	*

TX-7 .....This bit selects the pin function of No.47.
"0" : EAPD
"1" : DIT

EXEN .....This bit selects whether EXT24M pin outputs clock or not.
"0" : EXT24M is power down state, and outputs low level.
"1" : EXT24M outputs the clock.

The bits except TX-7 and EXEN should not be changed from the default value.

64h : ZV Port Volume (Read/Write, Default: 8808h or C808h)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Mute	MSEL	-	GL4-0					ZEN	ZAC	-	GR4-0				

Mute.....Setting this bit to “1” mutes both left and right channels of the ZV port.

MSEL .....This bit is read only, and indicates the status of No.40 MSEL pin.

“0” : Low

“1” : High

GL4-0 .....These bits determine the volume level of the ZV port left channel by 1.5dB step. The volume range is from +12dB to -34.5dB. When all bits are set to “0”, volume is maximum (+12dB) and when all bits are set to “1”, volume is minimum (-34.5dB).

ZEN .....This bit selects whether ZV port is used or not.

“0” : ZV port is power down state, and can not be used.

“1” : ZV port can be used.

ZAC .....This bit is read only, and indicates whether the bit clock (ZV_BCK) is input to ZV port or not.

“0” : The bit clock (ZV_BCK) is not input.

“1” : ZV port is active because the bit clock (ZV_BCK) is input.

GR4-0 .....These bits determine the volume level of the ZV port right channel by 1.5dB step. Setting to them is the same as the upper GL4-0 bits.

66h : DIT Control 2 (Read/Write, Default: 0040h)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
-	-	-	-	-	-	-	*	*	*	TX-3	*	TX-8	DMU	UDS	3AWE

TX-3 .....SPDIF signal is output from No.43 DIT, if this bit is set to “1” at MSEL= “Low”.

TX-8 .....SPDIF signal is output from No.48 DIT, if this bit is set to “1” at MSEL= “Low”.

DMU.....Setting this bit to “1” mutes audio data output from DIT.

UDS.....This bit selects the data output from DIT.

“0” : Data from the AC-Link

“1” : Data from A/D converter

3AWE.....This bit selects whether 3Ah register can be written or not.

“0” : 3Ah register is Read Only.

“1” : 3Ah register is Read / Write.

D8, D7, D6 and D4 should not be changed from the default value.

68h : 3D Mode Select (Read/Write, Default: 0C00h)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
-	-	-	-	WM1-0		-	-	-	-	-	-	-	-	-	-

WM1-0 .....These bits select the mode of 3D / Bass / Treble according to the frequency response of the speaker.

WM1	WM0	3D Mode	Target Speaker	Speaker Size
0	0	Do not select.	–	–
0	1	DeskTop	Standard Speaker	5 – 12 cm
1	0	Notebook PC 1	Small Speaker	3 cm
1	1	Notebook PC 2	Smaller Speaker	1.5 cm

7Ch : Vendor ID 1 (Read Only, Default: 594Dh)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
“0”	“1”	“0”	“1”	“1”	“0”	“0”	“1”	“0”	“1”	“0”	“0”	“1”	“1”	“0”	“1”

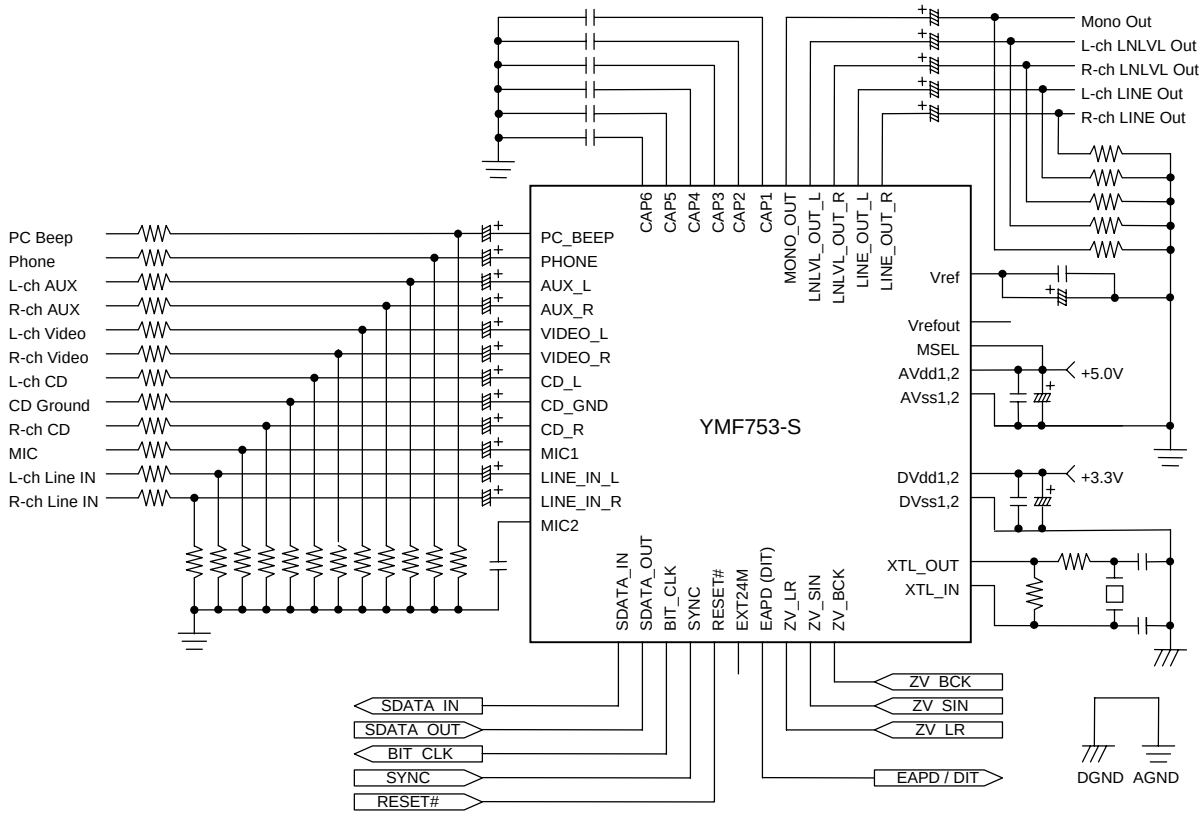
7Eh : Vendor ID 2 (Read Only, Default: 4803h)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
“0”	“1”	“0”	“0”	“1”	“0”	“0”	“0”	“0”	“0”	“0”	“0”	“0”	“0”	“1”	“1”

7Ch and upper 8 bits of 7Eh indicate Yamaha vendor ID, which is “YMH”. “Y” is 59h, “M” is 4Dh, and “H” is 48h with ASCII code.

Lower 8 bits of 7Eh is YMF753 revision ID (03h).

■ SYSTEM CONNECTION DIAGRAM



1) Power and Ground

To get the most out of analog performance, it is necessary to split the ground into analog and digital blocks. Analog ground and digital ground earth at one point closed to the initial ground supply of the board. The layout of the ground pattern should be designed as large as possible and the impudence should be reduced to prevent from receiving ambient noise. In addition, use 0.1µF and 47µF capacitors to connect between the analog voltage pin and the analog ground as well as between the digital supply pin and the digital ground.

2) Reference Voltage

As the reference voltage determines all analog signals' reference levels of YMF753, noise generated from the reference voltage could affect the YMF753's analog performance. To stabilize the YMF753's reference voltage, insert a 0.1µF ceramic capacitor in parallel with a 22µF capacitor between Vref pin and the ground. The 0.1µF ceramic capacitor should be designed as close to the Vref pin as possible

3) Master Clock

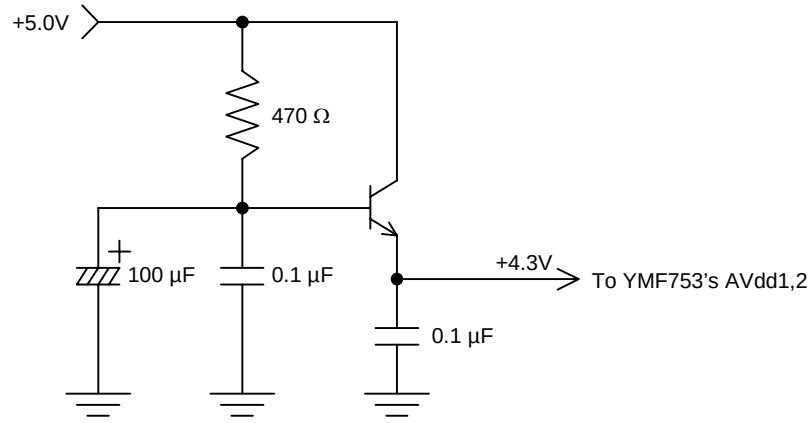
To suppress the master clock from affecting its surroundings, it is recommended to keep the master clock guarded on the ground so the noise can be reduced.

4) Unused Analog Input / Output pins

For the unused analog input pins, short them through a 0.1µF ceramic capacitor to the analog ground. For the unused analog output pins, they should be left opened.

5) Recommended Analog Voltage Circuit

YMF753 is presumed that it is made to work in the analog power supply formed from +5.0±0.25V power supply, because the range of analog operating voltage is being made +4.0V to +5.25V. The recommended circuit to form the analog power supply from +5V power supply is shown in below.



■ ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit
Analog Supply Voltage	AV_{DD}	-0.3	7.0	V
Digital Supply Voltage	DV_{DD}	-0.5	7.0	V
Analog Input Voltage	V_{INA}	-0.5	AV_{DD} + 0.5	V
Digital Input Voltage	V_{IND}	-0.5	DV_{DD} + 0.5	V
Ambient Temperature	T_{OP}	0	70	°C
Storage Temperature	T_{STG}	-50	125	°C

Note) $DV_{SS} = AV_{SS} = 0V$

2. Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit
Analog Operating Voltage	AV_{DD}	4.00	5.00	5.25	V
Digital Operating Voltage	DV_{DD}	4.75	5.00	5.25	V
		3.135	3.30	3.465	V
Operating Ambient Temperature	T_{OP}	0	25	70	°C

Note) $DV_{SS} = AV_{SS} = 0V$

When using a recommended analog voltage circuit, the output serves as AV_{DD} (typical 4.3V).

3. DC Characteristics

3-1. AC-Link

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Input Voltage	V_{IN}		-0.30	-	DV_{DD} + 0.30	V
Input Voltage High Level	V_{IH}		0.65 × DV_{DD}	-	-	V
Input Voltage Low Level	V_{IL}		-	-	0.35 × DV_{DD}	V
Output Voltage High Level	V_{OH}	I_{OH} = -5mA	0.9 × DV_{DD}	-	-	V
Output Voltage Low Level	V_{OL}	I_{OL} = 5mA	-	-	0.1 × DV_{DD}	V
Input Leakage Current	-		-10	-	10	µA
Output Leakage Current	-	Hi-Z	-10	-	10	µA

Note) Applicable to RESET#, SYNC, BIT_CLK, SDATA_IN and SDATA_OUT.

3-2. Miscellaneous

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Input Voltage High Level 1	V_{IH1}	*1	0.7 × DV_{DD}	-	-	V
Input Voltage Low Level 1	V_{IL1}	*1	-	-	0.3 × DV_{DD}	V
Input Voltage High Level 2	V_{IH2}	*2	0.8 × AV_{DD}	-	-	V
Input Voltage Low Level 2	V_{IL2}	*2	-	-	0.2 × AV_{DD}	V
Input Voltage High Level 3	V_{IH3}	*3, DV_{DD}=3.3V	2.0	-	-	V
		*3, DV_{DD}=5.0V	0.7 × DV_{DD}	-	-	V
Input Voltage Low Level 3	V_{IL3}	*3, DV_{DD}=3.3V	-	-	0.8	V
		*3, DV_{DD}=5.0V	-	-	0.3 × DV_{DD}	V
Output Voltage High Level 1	V_{OH1}	*4, I_{OH} = -4mA	0.65 × AV_{DD}	-	-	V
Output Voltage Low Level 1	V_{OL1}	*4, I_{OL} = 4mA	-	-	0.4	V
Output Voltage High Level 2	V_{OH2}	*5, I_{OH} = -2mA	0.65 × AV_{DD}	-	-	V
Output Voltage Low Level 2	V_{OL2}	*5, I_{OL} = 2mA	-	-	0.4	V
Output Voltage High Level 3	V_{OH3}	*6, I_{OH} = -2mA	DV_{DD} - 0.4	-	-	V
Output Voltage Low Level 3	V_{OL3}	*6, I_{OL} = 2mA	-	-	0.4	V
Pull-up Resistor	R_{ONUP}	ID0#, ID1#	-	100	-	kΩ
Pull-down Resistor	R_{ONDW}	*3	-	100	-	kΩ

Note) *1 : Applicable to XTL_IN, ID0# and ID1#.

*2 : Applicable to MSEL.

*3 : Applicable to ZV_LR, ZV_SIN and ZV_BCK.

*4 : Applicable to EAPD.

*5 : Applicable to DIT(No.43).

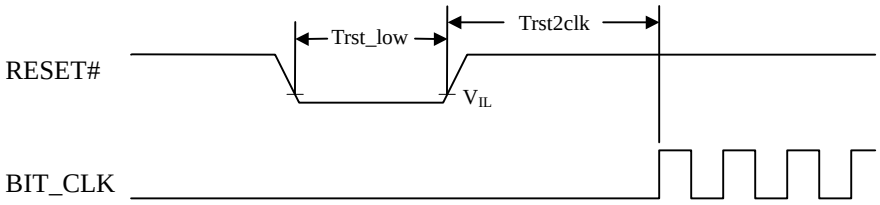
*6 : Applicable to EXT24M and DIT(No.48).

4. AC Characteristics (Under recommended operating conditions, Capacitor load=50pF)

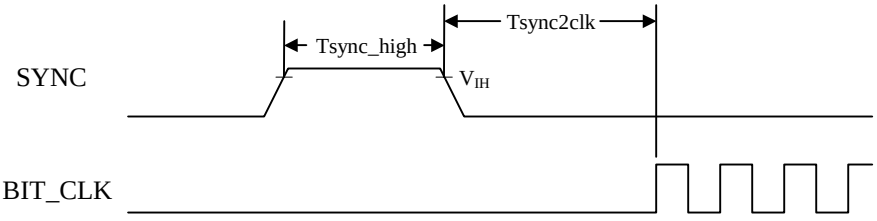
4-1. Reset

Parameter	Symbol	Min.	Typ.	Max.	Unit
Cold Reset (SDATA_OUT="L", SYNC="L")					
RESET# active low pulse width	Trst_low	1.0	-	-	µs
RESET# inactive to BIT_CLK start up delay	Trst2clk	162.8	-	-	ns
Warm Reset					
SYNC active high pulse width	Tsync_high	1.0	-	-	µs
SYNC inactive to BIT_CLK start up delay	Tsync2clk	162.8	-	-	ns

Cold Reset



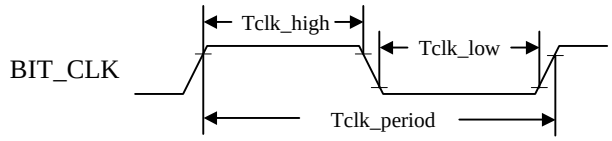
Warm Reset



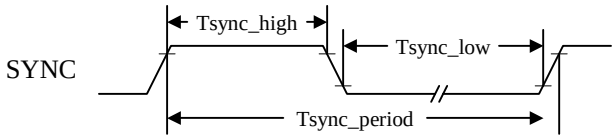
4-2. AC-link Interface

Parameter	Symbol	Min.	Typ.	Max.	Unit
BIT_CLK frequency		-	12.288	-	MHz
BIT_CLK clock period	Tclk_period	-	81.4	-	ns
BIT_CLK output jitter		-	-	750	ps
BIT_CLK low pulse width	Tclk_low	36.0	40.7	45.0	ns
BIT_CLK high pulse width	Tclk_high	36.0	40.7	45.0	ns
SYNC frequency			48.0		kHz
SYNC period	Tsync_period	-	20.8	-	µs
SYNC low pulse width	Tsync_low	-	19.5	-	µs
SYNC high pulse width	Tsync_high	-	1.3	-	µs
SDATA_OUT, SYNC setup time	Tsetup	10.0	-	-	ns
SDATA_OUT hold time	Thold	20.0	-	-	ns
SDATA_IN delay time	Tco	-	-	15.0	ns
AC-link Low Power Mode End of slot 2 to BIT_CLK, SDATA_IN low	Ts2_pdown	-	-	1.0	µs

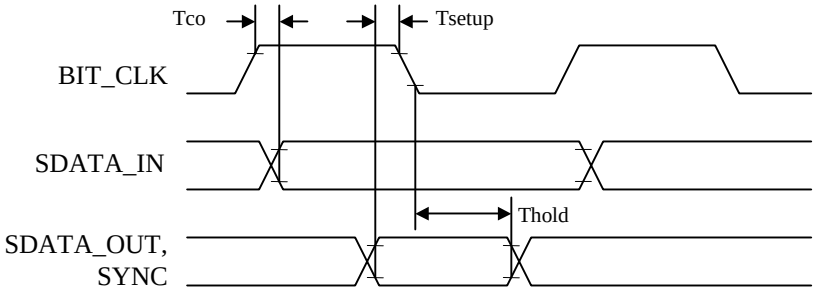
BIT_CLK



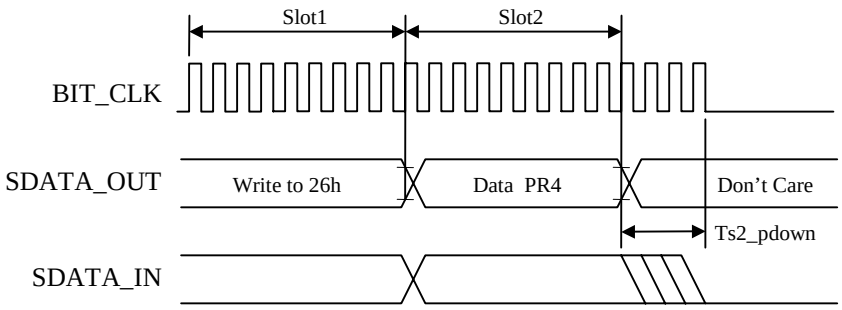
SYNC



Data Output and Input Timing



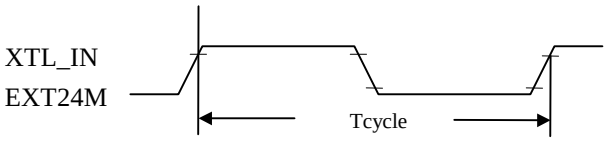
AC-link Low Power Mode



4-3. Master Clock & External Clock Out

Parameter	Symbol	Min.	Typ.	Max.	Unit
XTL_IN, EXT24M clock period	Tcycle	-	40.69	-	ns
XTL_IN clock duty	Duty-xtl	40	-	60	%
EXT24M clock duty	Duty-ext	40	-	60	%

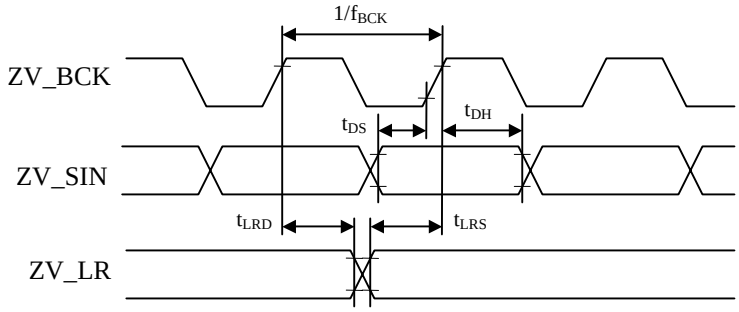
XTL_IN & EXT24M



4-4. Zoomed Video Port

Parameter	Symbol	Min.	Typ.	Max.	Unit
ZV_BCK frequency	f_{BCK}	32fs	48fs	64fs	kHz
ZV_BCK duty	D_{BCK}	40	50	60	%
ZV_LR delay time	t_{LRD}	120	-	-	ns
ZV_LR setup time	t_{LRS}	32	-	-	ns
ZV_SIN setup time	t_{DS}	32	-	-	ns
ZV_SIN hold time	t_{DH}	2	-	-	ns

Zoomed Video Port



5. Power Consumption

Parameter	Min.	Typ.	Max.	Unit
Normal Operating				
AV_{DD} = 4.3V / DV_{DD} = 3.3V			45	mA
AV_{DD} = 5.0V / DV_{DD} = 5.0V			55	mA
AV_{DD} = 4.3V		35		mA
AV_{DD} = 5.0V		43		mA
DV_{DD} = 3.3V		8		mA
DV_{DD} = 5.0V		12		mA
Power Down Mode (PR0-PR5=0)				
AV_{DD} = 4.3V / DV_{DD} = 3.3V			10	µA
AV_{DD} = 5.0V / DV_{DD} = 5.0V			20	µA
AV_{DD} = 4.3V		7		µA
AV_{DD} = 5.0V		12		µA
DV_{DD} = 3.3V		2		µA
DV_{DD} = 5.0V		4		µA

6. Analog Characteristics

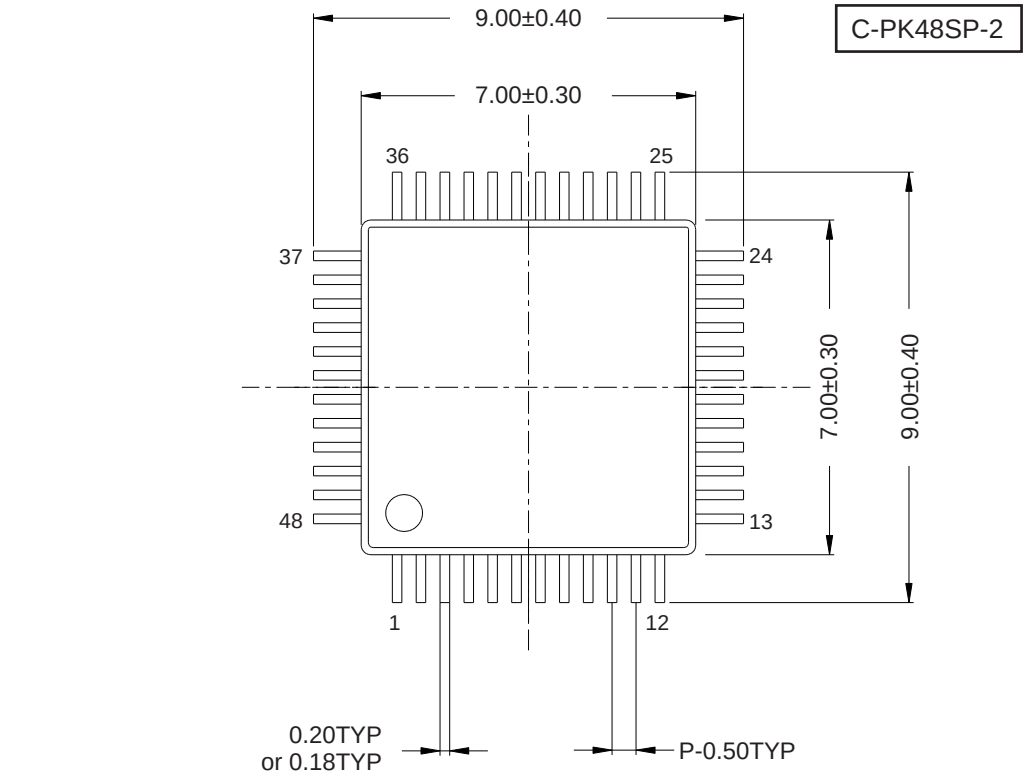
Parameter	Min.	Typ.	Max.	Unit
Full Scale Line Input		AV_{DD} / 5		Vrms
Full Scale Microphone Input (0dB)		AV_{DD} / 5		Vrms
Full Scale Microphone Input (+20dB)		AV_{DD} / 50		Vrms
Full Scale Line Output		AV_{DD} / 5		Vrms
Analog S/N				
CD to LINE_OUT		90		dB
Stereo input except CD to LINE_OUT	90	95		dB
Analog Frequency Response	20		20,000	Hz
S/N : D/A converter (fs=48kHz)	85	90		dB
S/N : A/D converter (fs=48kHz)	75	85		dB
THD+N : Line Output AV_{DD}=5.0V		-70	-65	dB
AV_{DD}=4.3V		-68	-62	dB
D/A & A/D Frequency Response	20		19,200	Hz
Transition Band	19,200		28,800	Hz
Stop Band	28,800			Hz
Stop Band Rejection	70			dB
Out-of-Band Rejection		40		dB
Group Delay			1	ms
Power Supply Rejection Rate (1kHz)		40		dB
Crosstalk between Inputs Channels			-70	dB
Attenuation & Gain Step				
PC_BEEP		3.0		dB
Other than PC_BEEP		1.5		dB
Input Impedance	10			kΩ
Input Capacitor		7.5		pF
Vrefout Voltage		AV_{DD} / 2		V

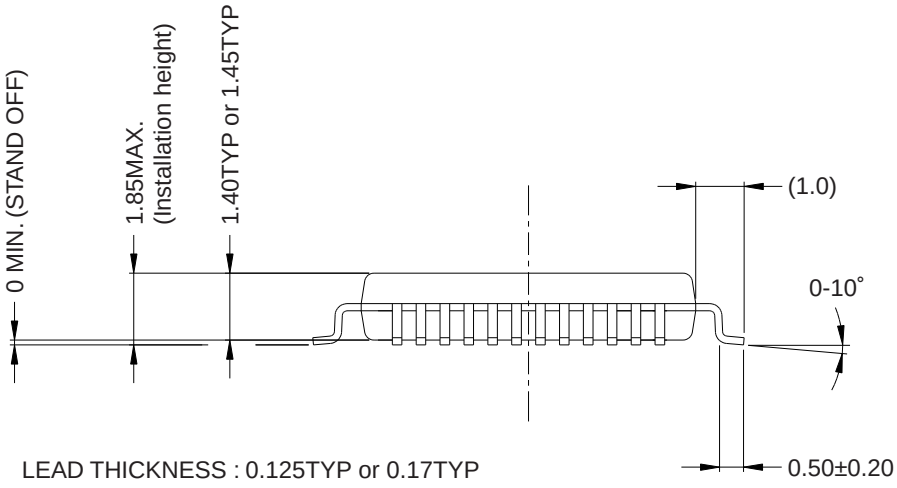
Note) Typical conditions : T_{OP}=25°C, DV_{DD}=3.3V, AV_{DD}=4.3V to 5.0V,

1kHz input sine wave, fs=48kHz, 0dB=AV_{DD}/5 Vrms, 10kΩ / 50pF

S/N (dynamic range) measurement: -60dB input, THD+N measurement: -3dB input

■ EXTERNAL DIMENSIONS





The shape of the molded corner may slightly different from the shape in this diagram.
The figures in the parenthesis ( ) should be used as a reference.
Plastic body dimension do not include burr of resin. UNIT : mm

Note : The LSIs for surface mounting need for special care on storage and soldering conditions.
For detailed information, please contact your nearest agent of Yamaha.

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