Preliminary

XR16C872

Dual UART with 1284 Parallel Port and Plug-and-Play Controller

June 1999-1

FEATURES

- Plug and Play ISA Bus Specification Compliant
  - Auto Configuration
  - Direct Connection, Needing no External Buffers
  - Resource Data in External 4K EEPROM
  - 10-Interrupts IRQ3-7, IRQ9-12, IRQ15
- Manual Configuration for Standard COM1-COM-4 and LPT1-LPT2
- IEEE 1284 Compliant
  - Bidirectional Host Port
  - Level-II Electrical Interface, Needing no External Transceivers
  - Standard Centronics/ECP/EPP Mode
  - 16-byte FIFO in ECP mode
- Dual UART Software Compatible with 16C550
- 128-Byte Transmit and Receiver FIFOs Reduce CPU Interrupt
- FIFO Counters in Transmitter and Receiver
- Automatic RTS/CTS Flow Control with Hysteresis to Increase Data Throughput
- IrDA Infrared Pulse Shaping Encoder/Decoder for up to 115.2Kbps Data Rate
- Up to 460.8 Kbps Standard Serial Data Rate
- +5V and +3.3V Operation
- 100-pin Quad Flat Package (14x20mm)
- Reference PC ISA Card Design Available
- Windows[2] 95, 98 and NT4.0 Device Drivers are Available

APPLICATIONS

- Multi-function PC/ISA Bus Card with RS-232/ RS-422/RS-485 Interface and Printer/parallel Port
- Embedded Systems
- Portable Infrared Wireless Systems
- High-speed Bidirectional Parallel Port
- High-speed Serial Ports

DESCRIPTION

The XR16C872[1] (872) is a dual universal asynchronous receiver and transmitter (UART) with a 1284 bi-directional parallel port and ISA Bus Plug-and-Play (PnP) interface. The PnP interface supports auto configuration for desktop and embedded PC computers. The host bus interface can also be configured to manually support standard PC addresses COM1-4 and LPT1-2. The parallel port is compatible to IEEE 1284 specification and supports Compatible Centronics, Extended Capability (ECP) and Enhanced Parallel Port (EPP) protocols. The UARTs are software compatible to industry standard 16C550 and include enhanced features of 128 bytes of transmit and receive FIFOs, programmable transmit and receive FIFO trigger levels, transmit and receive FIFO counters, IrDA (Infrared Data Association) encoder/decoder, automatic RTS/CTS hardware flow control with selectable hysteresis, and automatic software (Xon/Xoff) flow control. On board status registers provide interrupt priorities, receive data errors and modem status. Each channel has a programmable baud rate generator to provide data rates up to 460.8Kbps. The bi-directional parallel port can be configured as a general purpose input/output interface or connected to a printer or portable storage devices. The 872 operates on a single +5V and +3.3 power supply. It is available in a small 100-pin QFP package and offers commercial and industrial temperature ranges. The chip is fabricated in an advanced CMOS process to reduce power consumption.

ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR16C872CQ	100-Lead QFP	0° C to + 70° C
XR16C872IQ	100-Lead QFP	-40° C to + 85° C

Notes:

[1] Covered by U.S. patent number 5,649,122 and patent pending.

[2] Windows is a trademark of Microsoft Corp.

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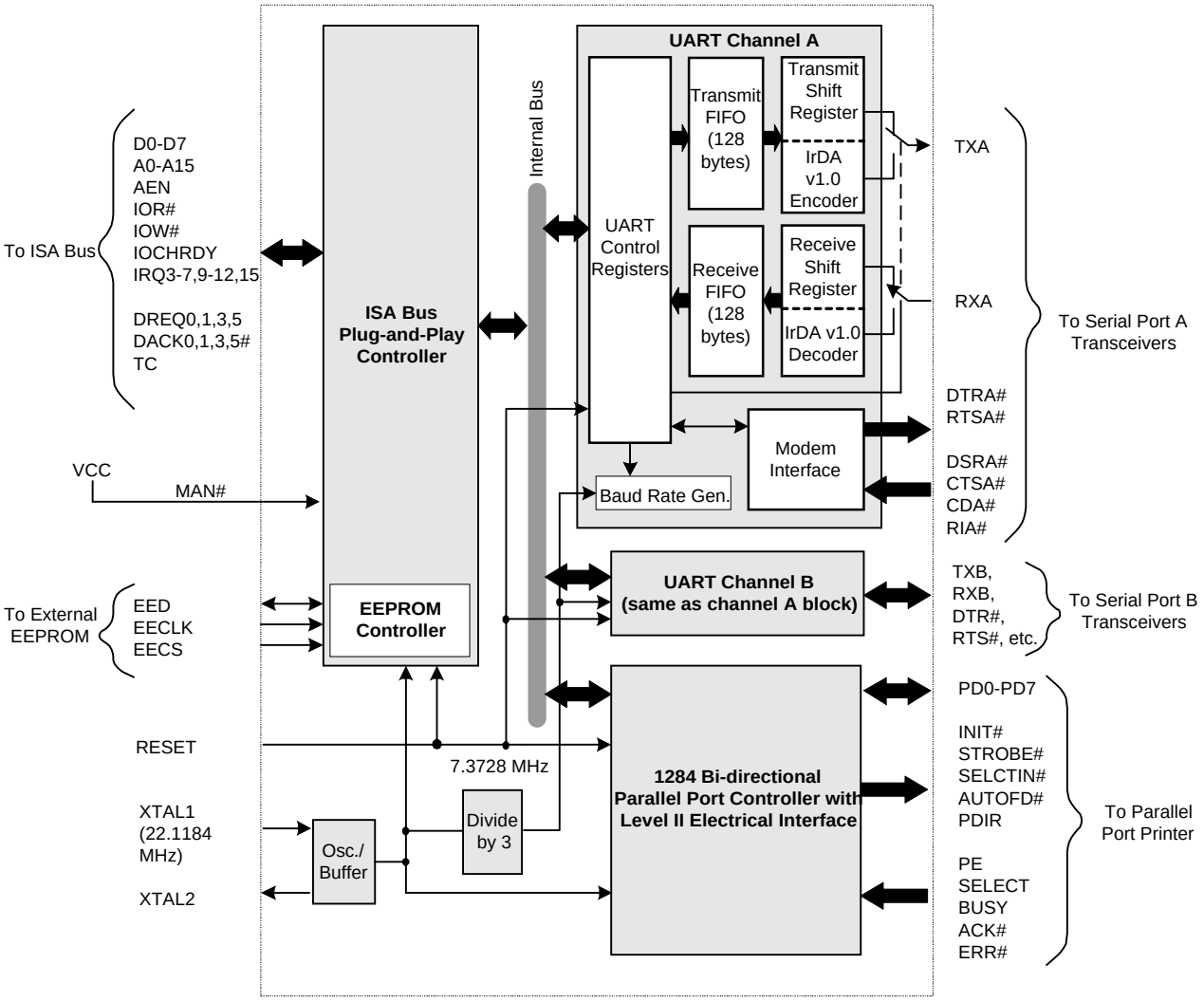


Figure 1. Functional Block Diagram with Plug-and-Play Interface

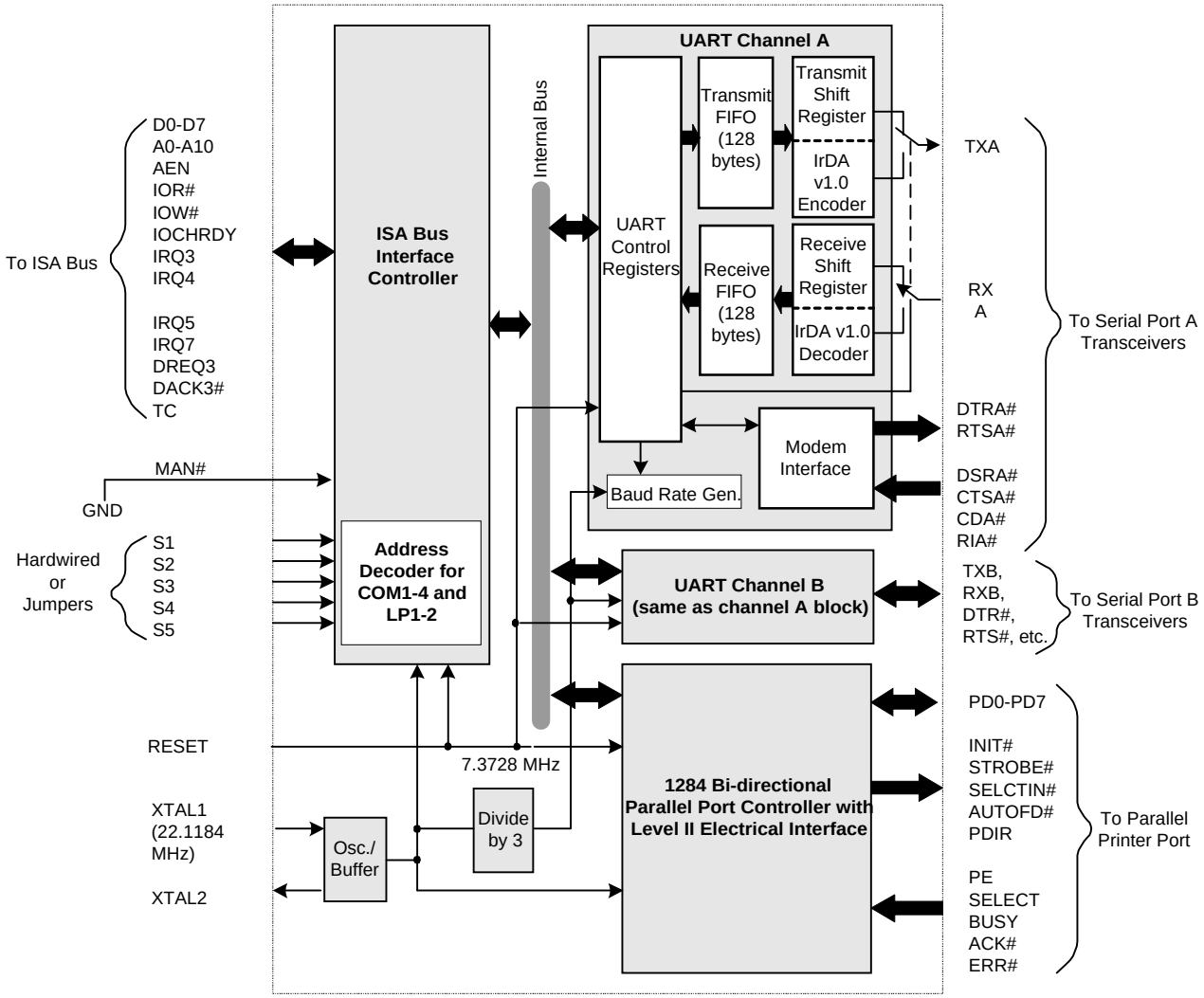
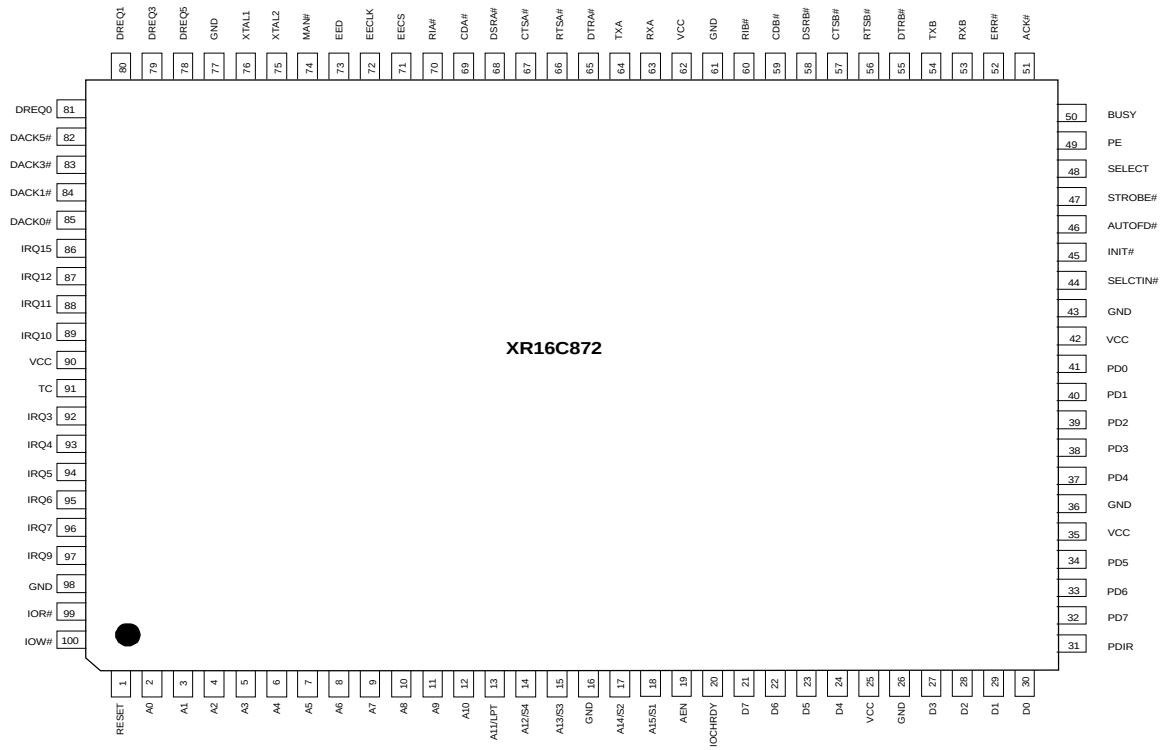


Figure 2. Functional Block Diagram with Manual Configuration Interface.



100-Pin QFP (14X20x3 mm, 1.95 mm form)
Package Description (Top View)

PIN DESCRIPTION

Signal Type Definition. The following signal type definitions are from the 872 device point of view.

I	Standard input
O	Standard active output
OT24	Tri-state output
IOP14	Tri-state bi-directional input/output
IO24	Tri-state bi-directional input/output

Symbol	Pin #	Type	Pin Description
HOST INTERFACE			
A0-A15	2-15 17, 18	I	ISA Bus Address. All 16-bits are used during PnP auto configuration sequence with external EEPROM providing the resource data. In the manual configuration mode A0-A10 are used for decoding COM1-4 and LPT1-2 addresses. After auto or manual configuration, bits A0-A2 select UART internal registers and A3-A10 are used to select UART A or B, or the 1284 printer port.
D0-D7	30-21	IO24	ISA Data Bus. These are the eight three state data lines for transferring data to or from the controlling CPU. D0 is the least significant bit and the first data bit in a transmit or receive serial data stream.
AEN	19	I	Address Enable. Active high to validate A0-A15 address lines during Direct Memory Access operation on the ISA bus. Connect to logic 0 when it is not used.
IOR#	99	I	Read Strobe. A logic 0 transition on this pin will request the contents of an Internal register defined by address bits A0-A2 for either UART channels A/B or A0-A1 for the printer port, be place onto D0-D7 data bus for a read cycle by the CPU.
IOW#	100	I	Write Strobe. A logic 1 transition on this pin will transfer the data on the data bus (D0-D7), as defined by either address bits A0-A2 for UART channels A/B or A0-A1 for the printer port, into an internal register during a write cycle from the CPU.
IRQ15 IRQ12-10 IRQ9 IRQ3-7	86 87-89 97 92-96	OT24	Interrupt Request Lines. These are three state active high interrupt lines to controlling CPU when an interrupt request is generated by the UART channel A/B or 1284 printer port.
DREQ5 DREQ3 DREQ1 DREQ0	78 79 80 81	OT24	DMA Request Channel 0,1,3 and 5. These are three state active high outputs with internal weak pull down resistor. DMA request is used by the 1284 parallel port during ECP and FIFO mode.
DACK5# DACK3# DACK1# DACK0#	82 83 84 85	I	DMA Acknowledge Channel 0,1,3 and 5. These are active low inputs and are used by the 1284 parallel port during ECP and FIFO mode.

PIN DESCRIPTION (CONT'D)

Symbol	Pin #	Type	Pin Description
IOCHRDY	20	OT24	Input/Output Channel Ready. IOCHRDY is a three-state active high output with an internal weak pull-up resistor. This pin goes low when 1284 parallel port requires additional clock during a read or write cycle.
TC	91	I	Terminal Count. TC is an active high input during DMA cycle and when DACK# is low to indicate data transfer is complete.
RESET	1	I	System Reset. Reset is an active high input. A 40ns minimum pulse will reset the internal registers and outputs to the default state. The TX output is at logic 1 and RX input is internally held at logic 1 during reset. See XR16C872 Reset Conditions for details.
XTAL1	76	I	Crystal Oscillator Input. A 22.1184 MHz crystal must be connected to this input and XTAL2 pin to form an internal oscillator circuit which provides the main clock to the the baud rate generators. An external clock of same frequency may be used instead.
XTAL2	75	O	Crystal Oscillator Output. The other side of the crystal is connected to this pin to form an internal crystal oscillator.
EED	73	Bidir	EED is a bi-directional serial data bus to the external 93C46 EEPROM.
EECLK	72	O	EECLK is a 500KHz clock output to the external EEPROM for serial data timing reference.
EECS	71	Bidir	EEPROM Chip Select. EECS is an active high output to the external EEPROM. During Manual configuration mode, a logic 1 input will bypass the internal divide-by-3 clock circuit to the two UARTs.
MAN#	74	I	Manual Configuration Select. MAN# is an active low input that enables S1-S5 for selection of COM1-4 and LPT1-2 or in embedded applications.
1284 CONTROLLER INTERFACE			
PD7-PD0	32-34 37-41	IOP14	Parallel Data Bus. PD0-PD7 are three-state bi-directional data lines to the parallel port. PD0 is the least significant bit with PD7 being the most significant bit. PD0-PD7 are high current drive outputs and can connect to the printer/parallel connector without external buffers.
ACK#	51	IP24	Acknowledge. ACK# is an active low input with with an internal weak pull-up. It can be a general purpose input or line printer acknowledge signal. A logic 0 from the parallel/printer indicates successful data transfer to the print buffer.
AUTOFD#	46	IOP14	AutoLineFeed. AUTOFD# is an active low tri-state with an internal weak pull-up. It can be a general purpose I/O or automatic line feed. When this signal is low the printer should automatically line feed after each printed line.

PIN DESCRIPTION (CONT'D)

Symbol	Pin #	Type	Pin Description
PDIR	31	O	Parallel Port Direction Indicator. PDIR indicates the operating direction of the parallel port. An output logic 0 indicates the parallel port is operating as an output port and a logic 1 indicates it is an input port.
BUSY	50	IP24	BUSY is an active high printer busy indicator or general purpose input. Generally, it is used as an input from the printer and a logic 1 indicates it is not ready. The input has an internal weak pull-up resistor.
ERR#	52	IP24	ERR# is printer error indicator or a general purpose input. Generally, it is used as an input from the printer and a logic 0 indicates it has an error condition. The input has a weak internal pull-up resistor.
INIT#	45	IOP14	INIT# is a printer initialization signal or a general purpose output. Generally, it is used with the printer (active low) for system initialization or reset. The pin is a tri-state output and has an internal weak pull-up resistor.
PE	49	IP24	PE is a signal from the printer indicating a paper empty condition or general purpose input. Generally, it is used with a printer and a logic 1 indicates the printer is out of paper. This input has an internal weak pull-up resistor.
SELECT	48	IP24	SELECT is the printer select status indicator to the host or general purpose input. Normally this pin is connected to a printer output and a logic 0 indicates the ready status of the printer, i.e., on-line and/or on-line and ready condiftion. This pin has an internal weak pull-up resistor.
SELCTIN#	44	IOP14	SELCTIN# is a select signal to the printer or general purpose I/O pin. This pin can be read via bit-3 in the printer command register, or written via bit-3 in the printer control register. Normally this signal is connected to a printer to select the printer with an active low signal. The pin is tri-state output and has an internal weak pull-up resistor.
STROBE#	47	IOP14	STROBE# is a data strobe output or general purpose I/O pin. Normally this output is connected to a printer and indicates that valid data is available on the data bus (PD0-PD7). The pin is a tri-state output with an intenal weak pull-up resistor.
MODEM OR SERIAL PORT INTERFACE			
RXA, RXB	63,53	I	Receive Data A/B. Serial receive data or IR pulses input to UART channel A and B. The RX signal to the UART should be a logic 1 state during reset, idle (no data) and sleep mode. During the local loop-back mode, the RX input pins are disabled and TX data is internally connected to the UART RX Inputs. In the IR mode, this input is normally at logic 0.
TXA, TXB	64,54	O	Transmit Data A/B. Serial transmit data or IR pulses output from channel A and B. The normal output is a logic 1 for serial data during reset, idle (no data), sleep mode, or when the transmitter is disabled. During the local loop-back mode, the TX output pin is held at logic 1and internally it connects to RX input. In IR mode, the output changes to a logic 0 after it is enabled (MCR bit 5=1).

PIN DESCRIPTION (CONT'D)

Symbol	Pin #	Type	Pin Description
DTRA#, DTRB#	65 55	O	Data Terminal Ready A/B or general purpose output. DTRA/B# are active low and associated with UARTchannel A and B. A logic 0 on indicates that UART A/B is ready. This pin is controlled via the MCR register for channel A/B. Setting MCR bit-0 to logic 1 puts the output pin to logic 0. This pin will be a logic 1 after writing a logic 0 to MCR bit-0. This pin has no effect on the UART transmitter or receiver.
RTSA#, RTSB#	66 56	O	Request to Send A/B or general purpose output. RTSA/B# are active low outputs and associated with UART channels A/B. Writing a logic 1 to MCR bit-1sets the pin to a logic 0 and requests remote unit to send data. After a reset this pin is set to a logic 1. When auto RTS flow control is enabled (EFR bit-6=1), a logic 0 asks remote modem to send data and a logic 1 requests to suspend. The user must assert RTS# after enabling auto RTS flow control.
CTSA#, CTSB#	67, 57	I	Clear to Send A/B or general purpose input. CTSA/B# are active low inputs and associated with UART channels A and B. A logic 0 indicates the remote modem is ready for data. A level change on this input pin will generate a status change interrupt (MSR bit-0). When auto CTS flow control is enabled, a logic 1 suspends local data transmission and a logic 0 restarts the local transmitter.
DSRA#, DSRB#	68, 58	I	Data Set Read A/B or general purpose input. DSRA/B# are active low inputs and associated with UARTchannel A and B. A logic 0 on indicates the modem is ready for data exchange with the UART. A logic level change on this input pin will generate a status change interrupt (MSR bit-1).This pin has no effect on the UART's transmit or receive operation.
CDA#, CDB#	69, 59	I	Carrier Detect A/B or general purpose input. CDA/B# are active low inputs and associated with UART channels A and B. A logic 0 on this pin indicates a carrier signal has been detected by the modem. A logic level change on this input pin will generate a status change interrupt (MSR bit-3). This pin has no effect on the UART's transmit or receive operation.
RIA#, RIB#	70, 60	I	Ring Indicator A/B or general purpose input. RIA/B# are active low inputs and associated with UART channels A and B. A logic 0 on indicates the modem has received a ringing signal from the telephone line. A logic 1 transition on this input pin will generate a status change interrupt (MSR bit-2). This pin has no effect on UART's transmit or receive operation.
VCC	25,35,42 62,90	PWR	+5 Volts power supply.
GND	16,26,36,43 61,77,98	PWR	Signal ground.

DC ELECTRICAL CHARACTERISTICS

T_A=0° - 70° C (-40° - +85°C for IQ package), Vcc=3.3 or 5.0 V ± 10% unless otherwise specified.

Symbol	Parameter	Limits 3.3		Limits 5.0		Units	Conditions
		Min	Max	Min	Max		
V_{ILCK}	Clock input low level		0.6		0.6	V	
V_{IHCK}	Clock input high level	2.4		3.0		V	Vcc
V_{IL}	Input low level	-0.5	0.8	-0.5	0.8	V	
V_{IH}	Input high level	2.0		2.2	Vcc	V	
V_{OL}	Output low level on type O outputs				0.4	V	I_{OL}= 6 mA
V_{OL}	Output low level on type OT24 outputs				0.4	V	I_{OL}= 24mA
V_{OL}	Output low level on type IO14 outputs				0.4	V	I_{OL}= 14 mA
V_{OL}	Output low level on type I024 outputs				0.4	V	I_{OL}= 24 mA
V_{OL}	Output low level on type O outputs		0.4			V	I_{OL}= tbd
V_{OL}	Output low level on type OT24 outputs		0.4			V	I_{OL}= tbd
V_{OL}	Output low level on type IO14 outputs		0.4			V	I_{OL}= tbd
V_{OL}	Output low level on type I024 outputs		0.4			V	I_{OL}= tbd
V_{OH}	Output high level on type O outputs			2.4		V	I_{OH}= -6 mA
V_{OH}	Output high level on type OT24 outputs			2.4		V	I_{OH}= -12 mA
V_{OH}	Output high level on type IO14 outputs			2.4		V	I_{OH}= -14 mA
V_{OH}	Output high level on type I024 outputs			2.4		V	I_{OH}= -12 mA
V_{OH}	Output high level on type O outputs	2.0				V	I_{OH}= tbd
V_{OH}	Output high level on type OT24 outputs	2.0				V	I_{OH}= tbd
V_{OH}	Output high level on type IO14 outputs	2.0				V	I_{OH}= tbd
V_{OH}	Output high level on type I024 outputs	2.0				V	I_{OH}= tbd
I_{IL}	Input leakage		±10		±10	uA	
I_{CL}	Clock leakage		±10		±10	uA	
ICAP	Input capacitance		5		5	pF	
RIN	Internal pull up/down resistance			20	50	K ohms	
I_{CC}	Supply current		8		10	mA	4-6 mA typ.

HOST INTERFACE AND UART AC ELECTRICAL CHARACTERISTICS

T_A= 0° - 70°C (-40° - +85°C for Industrial grade packages), Vcc=3.3 - 5.0 V ± 10% unless otherwise specified.

Symbol	Parameter	Limits 3.3		Limits 5.0		Units	Conditions
		Min	Max	Min	Max		
T_{1CW}	Clock pulse duration	20		20		ns	
T_{2FQ}	Oscillator/Clock frequency		tbd		24	MHz	
T_{3AS}	Address setup time	10		5		ns	
T_{4AH}	Address hold time	10		5		ns	
T_{5RD}	IOR# strobe width	50		25		ns	
T_{6DY}	Read/Write cycle delay	50		50		ns	
T_{7DA}	Delay from IOR# to data	35		25		ns	
T_{8DH}	Data disable time	25		15		ns	
T_{9WR}	IOW# strobe width	40		40		ns	
T_{10DS}	Data setup time	20		15		ns	
T_{11DH}	Data hold time	50		35		ns	
T_{12D}	Delay from IOW# to modem output		50		50	ns	100 pF load
T_{13D}	Delay from modem input to MSR interrupt		50		35	ns	100 pF load
T_{14D}	Delay from IOR# to reset MSR interrupt		50		35	ns	100 pF load
T_{15D}	Delay from stop bit to set RX interrupt		1		1	Rclk	
T_{16D}	Delay from IOR# to reset interrupt		200		200	ns	100 pF load
T_{17D}	Delay from stop bit to set TX interrupt		100		100	ns	
T_{18D}	Delay from INT reset to transmit start	8	24	8	24	Rclk	
T_{19D}	Delay from IOW# to reset interrupt		175		175	ns	
T_{RST}	Reset pulse width	40		40		ns	
N	Baud rate divisor	1	2^{16}-1	1	2^{16}-1	Rclk	

1284 CONTROLLER AC ELECTRICAL CHARACTERISTICS

T_A=0° - 70°C (-40° - +85°C for Industrial grade packages), Vcc=3.3 - 5.0 V ± 10% unless otherwise specified.

Symbol	Parameter	Limits 3.3		Limits 5.0		Units	Conditions
		Min	Max	Min	Max		
T20	PD7-PD0, STROBE#, AUTOFD#, INIT, SLCTIN# delay from IOW# inactive				100	ns	
T21	Interrupt delay from ACK#				60	ns	
T22	Interrupt pre-charge pulse at release				10	ns	
T23	TC pulse width			60		ns	
T24	TC active to DRQx inactive				100	ns	
T25	DRQx active to DACKx# active			0		ns	
T26	DRQx inactive delay from DACKx# active				100	ns	
T27	PD7-PD0 setup to STROBE# active			600		ns	
T28	STROBE# width			600		ns	
T29	PD7-PD0 hold from STROBE# inactive			450		ns	
T30	PD7-PD0 hold from BUSY inactive			80		ns	
T31	STROBE# active to BUSY active (handshake)				500	ns	
T32	BUSY inactive to STROBE# active (cycle delay)			680		ns	
T33	PD7-PD0, AUTOFD# setup to STROBE# active			0	60	ns	
T34	PD7-PD0, AUTOFD# hold from BUSY active			80	180	ns	
T35	STROBE# inactive to BUSY inactive			0		ns	
T36	BUSY inactive to #STROBE active			80	200	ns	
T37	#STROBE active to BUSY active			0		ns	
T38	BUSY active to #STROBE inactive			80	180	ns	
T39	PD7-PD0, BUSY setup to ACK# active			0		ns	
T40	PD7-PD0 data hold from AUTOFD# active			0		ns	
T41	ACK# inactive to AUTOFD# active			80	200	ns	
T42	AUTOFD# active to ACK# active			0		ns	
T43	ACK# active to AUTOFD# inactive			80	200	ns	
T44	AUTOFD# inactive to ACK# inactive			0		ns	
T45	Host address setup to IOW# active			40		ns	
T46	Host address hold from IOW# active			10		ns	
T47	Host data setup to IOW# active			0	20	ns	
T48	Host data hold from IOW# active			0		ns	
T49	IOW# active to IOCHRDY low			0	20	ns	
T50	IOCHRDY high to Host terminate (IOW# inactive)			10		ns	

1284 CONTROLLER AC ELECTRICAL CHARACTERISTICS (CONT'D)

Symbol	Parameter	Limits 3.3		Limits 5.0		Units	Conditions
		Min	Max	Min	Max		
T51	IOW# inactive to Host command active (IOW# or IOR#)			40		ns	
T52	IOCHRDY pre-charge width at release				10	ns	
T53	Host address setup to IOR# active			40		ns	
T54	Host address hold from IOR# active			10		ns	
T55	Host data setup to IOR# inactive			0	20	ns	
T56	Host data hold from IOR# inactive			0		ns	
T57	IOR# active to IOCHRDY low			0	20	ns	
T58	IOCHRDY high to Host terminate (IOR# inactive)			10		ns	
T59	IOR# inactive to Host command active (IOW# or IOR#)			40		ns	

ABSOLUTE MAXIMUM RATINGS

Supply range . . . . . -0.5 to 7V
Voltage at any pin . . . . . -0.5 V to VCC+0.5V
Operating temperature . . . . . -40°C to +85°C
Storage temperature . . . . . -65°C to +150°
Package dissipation (100-PQFP) . . . . . 500 mW
* thermal resistance: theta-ja . . . . . 45 °C/Watt
theta-jc . . . . . 12 °C/Watt

FUNCTION DESCRIPTION

The XR16C872 (872) is a highly integrated chip combining the functionality of two XR16C850 enhanced UART, an IEEE 1284 bi-directional printer interface, and the PC/ISA bus Plug-and-Play (PnP) interface. The PnP interface meets the Plug-and-Play ISA Specification Version 1.0a of May 5,1994. The PnP interface and the 1284 printer port are both clocked for maximum performance by an external crystal oscillator of 22.1184 MHz. This clock is then internally divided by three to obtain a 7.3728 MHz clock for the two UARTs.

CPU Bus Interface Options

The 872 has two data bus interface modes, PnP and manual. In PnP mode, the chip will interface to the PC/ISA bus directly and automatically configure each UART and the1284 parallel port address and IRQ interrupt. Figure 1, depicts the block diagram and interface.

Plug-and-Play Mode

The PnP interface supports industry standard jumperless auto configuration procedure in the PC/ISA bus system. With an external EEPROM chip providing the resource data for each of the logical devices, it automatically negotiates with Windows© 95 or 98 operating system and configures the operating setting for each device.

The PC host system identifies and configures each PnP device using a set of defined registers accessed on the ISA bus through three 8-bit I/O ports. All PnP interfaces in the host system respond to these same I/O ports, so after first sending an initiation key in order to enable all the interfaces, each interface is then isolated through the Isolation Protocol. Even though all interfaces initially respond to the Isolation Protocol, the protocol is accomplished in such a way that no bus contention will occur. After a given interface has been isolated it is then assigned a unique Card Select Number (CSN) so that there after the interface can be uniquely addressed.

All PnP interfaces support a defined readable resource data structure that completely describes the total resources required and the options supported by the interface. Resource requirements of each PnP interface are broken down into groupings called Logical Devices, each of which can be thought of as a separate device. The two 850 UART and the 1284 parallel data port are referred to as a logical device, for a total of three logical devices. When all resource requirements of the entire system are known, a process of resource arbitration is invoked on the host system under Windows operating system to determine the resources to allocate to each device. Finally, each device's resource usage is programmed through a set of configuration registers. Some of these configuration registers are common to all logical devices but the bulk of the registers are accessed separately for each logical device in the interface, with each particular logical device's configuration registers being mapped into the PnP register set one at a time.

After configuration is complete, each PnP interface is removed from configuration mode in order to prevent accidental erasure or modification of the interface's configuration. To re-enable configuration mode, the initiation key must be re-issued. The 872 uses all 16-bit address lines (A0-A15) for address decoding and supports 10 IRQ's (IRQ3-7, 9-12 and 15). Application note #xxxx describes the operation of the PnP interface in more detail.

Manual Configuration Mode Interface

The 872 provides an input pin (MAN#) to bypass the auto configuration procedure. It changes address lines A12-A15 to manual configuration inputs S1-S4 and LPT. These inputs can be designed with external jumpers to select COM1-COM4 for the serial ports, and LPT1 or LPT2 for the 1284 printer port.

Manual configuration mode supports the standard PC COM and LPT port addresses and associated IRQ. However, the address lines can be mapped to other memory space areas for embedded applications, more on this later. The 872 eliminates the external address decoding logic circuitry that is typically required.

The manual configuration is selected by making the MAN# pin logic 0 (GND). This changes five address lines to become configuration inputs. The manual configuration is accomplished by decoding the PC ISA bus address bits, A3 through A10 inside the 872 for chip select. These addresses select the UART for standard PC COM ports: COM-1, COM-2, COM-3, COM-4 and LPT-1 and LPT-2. Five inputs (S1-S5) are generally externally jumper or wired to logic 1 or logic 0 for the operating port. The configuration inputs are also associated with a given PC interrupt. The mapping for the COM port 1-4 and their associated interrupt selections are listed in Table 1. Besides the COM port addresses, the 872 also decodes two parallel or printer addresses.

The chip can be mapped into an embedded system memory space. Figure 4 shows an example of wiring S1-S5 for default port configuration with IRQA and IRQB for the two UARTs, and IRQC with DREQ, and DACK for the parallel port. Address lines A3-A10 are connected to the embedded system address lines A8-A15 instead, mapping it to address location 0x7F08-7F0F, 0x5F00-5F08, and 0x6F00-6F08 respectively. Application note #xxxx describes how to design with manual configuration mode in more detail.

MAN#	S1	S2	S3	S4	S5	A3-A9	COM Port	IRQ	Device Selected
0	0	0	x	x	x	3F8-3FF	COM-1	IRQ4	UART Channel A
0	1	0	x	x	x	2F8-2FF	COM-2	IRQ3	UART Channel A
0	0	1	x	x	x	3E8-3EF	COM-3	IRQ4	UART Channel A
0	1	1	x	x	x	2E8-2EF	COM-4	IRQ3	UART Channel A
0	x	x	0	0	x	3F8-3FF	COM-1	IRQ4	UART Channel B
0	x	x	1	0	x	2F8-2FF	COM-2	IRQ3	UART Channel B
0	x	x	0	1	x	3E8-3EF	COM-3	IRQ4	UART Channel B
0	x	x	1	1	x	2E8-2EF	COM-4	IRQ3	UART Channel B
0	x	x	x	x	1	378-37F	LPT-1	IRQ7	1284 Parallel Port
0	x	x	x	x	0	278-27F	LPT-2	IRQ5	1284 Parallel Port

x: don't care

Table 1. Manual Configuration Mode Internal Addess Decode

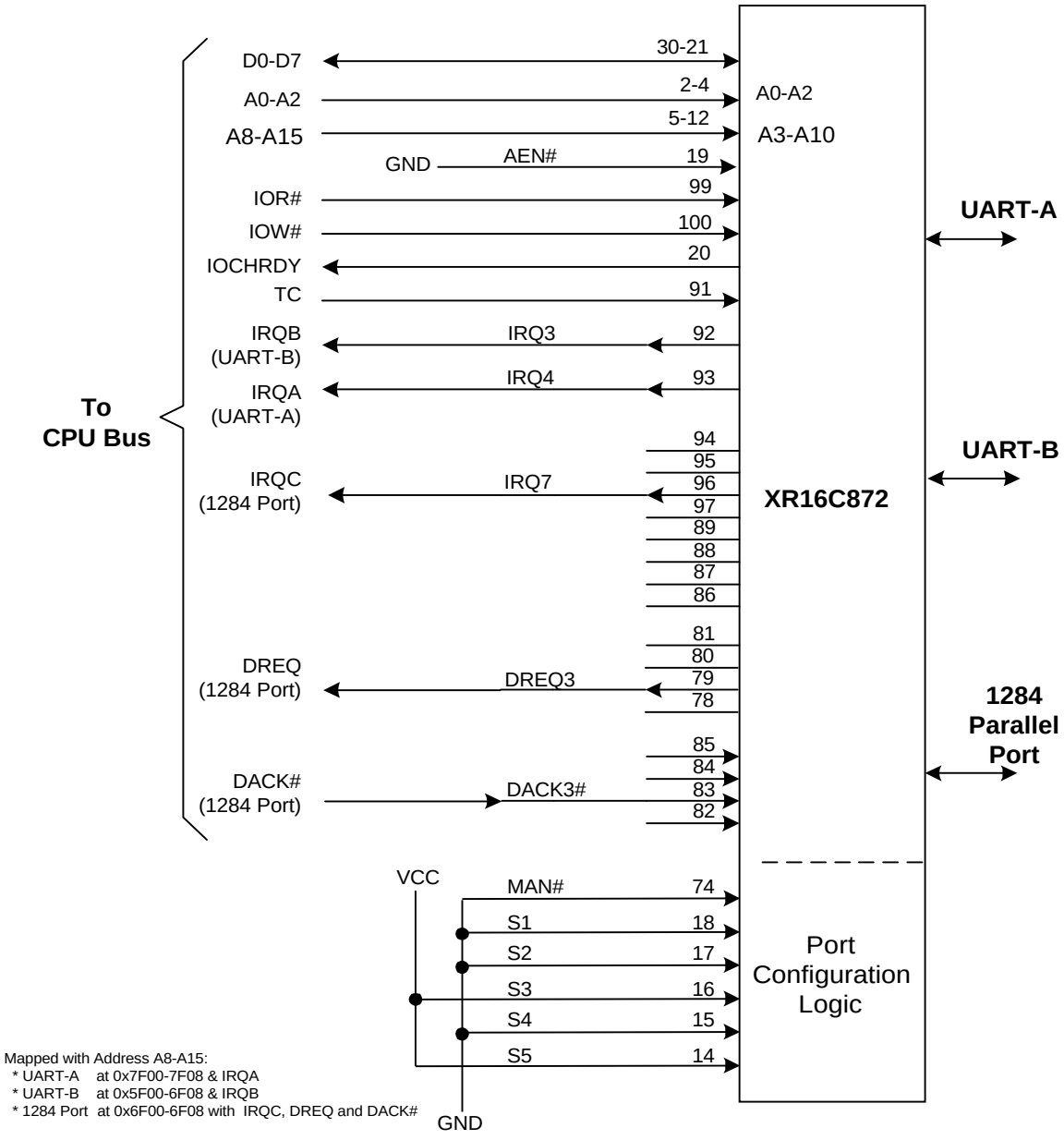


Figure 3. Manual Configuration Interface in Embedded Application

UART

The 872 UARTs are software compatible with the industry standard 16C550 on power up or reset. Each UART offers enhancements that are enabled through its Enhanced Features Registers. These features include transmit and receive FIFOs of 128 bytes, programmable transmit and receive FIFO trigger level from 0 to 128, baud rates with 1x or 4x clock pre-scaler, automatic RTS flow control level with trigger hysteresis, automatic CTS flow control, automatic software flow control, modem or general I/O interface control, infrared IrDA encoder/decoder select with a software option of inverting the decoder input logic level, sleep mode, device ID and revision. The baud rate generator input clock on both UARTs is supplied by a 7.3728 MHz clock. This clock comes from an internal divided by 3 circuit that is fed by the crystal oscillator or external clock input of 22.1184 MHz. Hence, the maximum operating data rate is 460.8 Kbps.

Each UART provides 128 bytes of transmit and receive FIFO memory instead of 16 in the 16C550. The larger FIFO greatly reduces the bandwidth requirement of the controlling CPU, increases system performance without increasing the speed of the CPU, and reduces overall power consumption. The 128 byte FIFOs also simplify software manipulation of flash memory data transfer where data page size is 128 bytes. Increased performance is realized by the larger transmit and receive FIFOs, FIFO counters, and programmable FIFO trigger level. This allows the processor to handle more networking tasks within a given time. For example, the 16C550 with 16 byte receive FIFO, will require 1.39 milliseconds to unload the FIFO (This example uses a character length of 10 bits, including start/stop bits at 115.2Kbps, [1/115200]x10x16). This means the external CPU will have to service the receive FIFO every 1.39 milliseconds. However with the 128 byte FIFO in the 872 UART, the data buffer will not require unloading/loading for 11.12 milliseconds. This increases the service interval giving the CPU additional time for other applications and reducing the overall UART interrupt servicing time. In addition, the FIFO counters and programmable FIFO trigger level interrupt is uniquely provided for maximum data throughput performance especially when operating in a multi-channel environment.

UART Internal Registers

Each 872 UART has 24 internal registers for monitoring and control. These resisters are summarized in Table 2 below. Twelve registers are compatible to those already in the standard 16C550. These registers function as data holding registers (THR/RHR), interrupt status and control registers (IER/ISR), a FIFO control register (FCR), line control register and line status register, (LCR/LSR), modem control and status registers (MCR/MSR), programmable baud rate control registers (DLL/DLM), and an user defined scratch pad register (SPR). Beyond the basic 16C550 features and capabilities, the 872 UART offers enhanced feature register set called TRG, FCTR, EFR, Xon1/2, Xoff1/2, EMSR, TXCNT,RXCNT, REV and DID, Register functions are fully described in the following paragraphs.

A2	A1	A0	Read Mode	Write Mode
Basic Registers (THR/RHR, FCR, IER/ISR, MCR/MSR, LCR/LSR, SPR/FCNT), accessible only when LCR bit-7 is set to logic 0.				
0	0	0	Receive Holding Register	Transmit Holding Register
0	0	1	Interrupt Enable Register	Interrupt Enable Register
0	1	0	Interrupt Status Register	FIFO Control Register
0	1	1	Line Control Register	Line Control Register
1	0	0	Modem Control Register	Modem Control Register
1	0	1	Line Status Register	Line Status Register
1	1	0	Modem Status Register	Modem Status Register
1	1	1	Scratch Pad Register	Scratch Pad Register
1	1	1	FIFO Counter (with FCTR bit-6=1)	
Baud Rate Registers (DLL, DLM), accessible only when LCR bit-7 is set to a logic 1.				
0	0	0	LSB of Divisor Latch	LSB of Divisor Latch
0	0	0	Device Revision (see text)	
0	0	1	MSB of Divisor Latch	MSB of Divisor Latch
0	0	1	Device Identification (see text)	
Enhanced Registers (TRG, FCTR, EFR, Xon/Xoff 1-2), accessible only when LCR is set to 0xBF.				
0	0	0	FIFO Trigger Register	FIFO trigger counter
0	0	1	Feature Control Register	Feature Control Register
0	1	0	Enhanced Feature Register	Enhanced Feature Register
1	0	0	Xon-1 Word	Xon-1 Word
1	0	1	Xon-2 Word	Xon-2 Word
1	1	0	Xoff-1 Word	Xoff-1 Word
1	1	1	Xoff-2 Word	Xoff-2 Word
Enhanced Mode Select Register (EMSR), accessible only when the FCTR bit-6 is set to logic 1.				
1	1	1	---	Enhanced Mode Select Register

Table 2. Internal Registers

FIFO Operation

128 byte transmit and receive data FIFOs are enabled by the FIFO Control Register (FCR) bit-0. The standard 16C550 provides only receive FIFO of 16 bytes with 4 selectable trigger levels and there is no transmit trigger level selection. The 872 UART provides independent programmable trigger levels from 0 to 128 for both receiver and transmitter. When receive or transmit data has reached the preset trigger level the UART generates an interrupt to call for service. The receive FIFO section includes a time-out function to ensure data is delivered to the CPU. A receive data time-out interrupt is generated when there is no receive data for a period of about 4-characters but the Receive Holding Register (RHR) is full or data did not reach the receive trigger level. See in the timing diagram area for TX and RX FIFO operation.

Hardware (RTS/CTS) Flow Control Operation

Automatic hardware or RTS and CTS flow control is used to prevent data overrun to the local receiver FIFO and remote receiver FIFO. The RTS# output pin is used to request remote unit to suspend/restart data transmission while the CTS# input pin is monitored to suspend/restart local transmitter. The auto RTS and auto CTS flow control features are individually selected to fit specific application requirements and enabled through EFR bit-6 and 7. The auto RTS function must be started by asserting RTS# pin (MCR bit-1=1) after it is enabled.

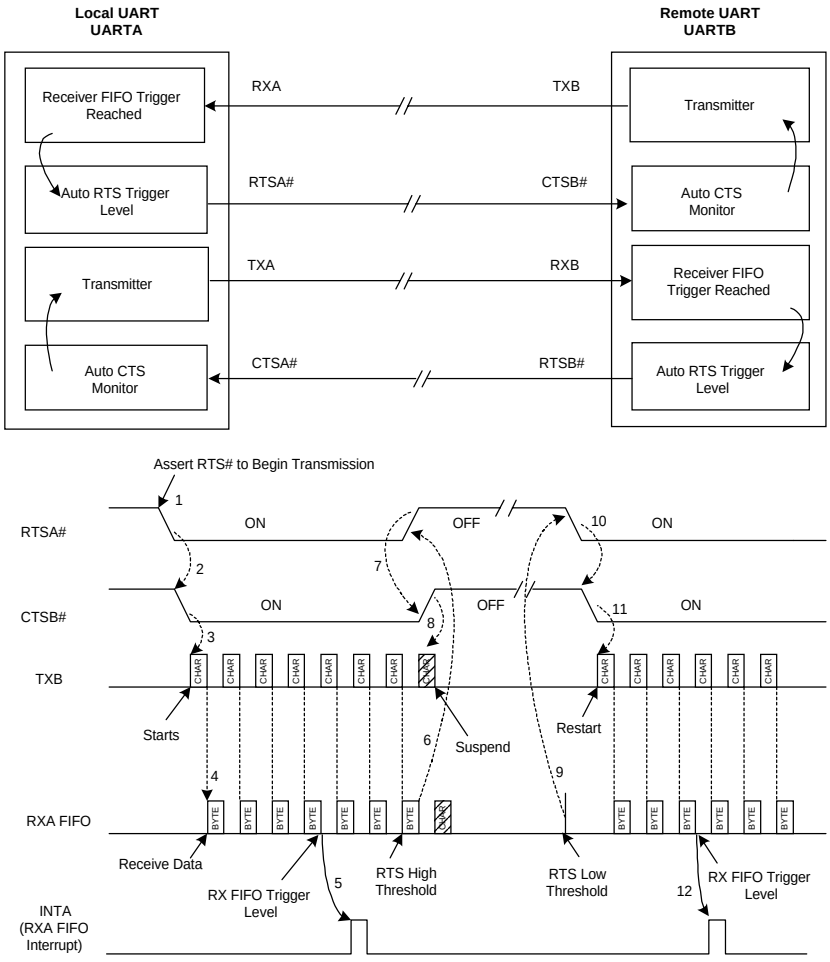


Figure 4.

Referring to Figure 4, the local UART (UARTA) starts data transfer by asserting RTSA# (1). RTSA# is normally connected to CTSB# (2) of remote UART (UARTB). CTSB# allows its transmitter to send data (3). TXB data arrives and fills UART-A receive FIFO (4). When RXA data fills up to its receive FIFO trigger level, UARTA activates its RXA data ready interrupt (5) and continues to receive and put data into its FIFO. If interrupt service latency is long and data is not being unloaded, UARTA monitors its receive data fill level to match the upper threshold of RTS delay and de-assert RTSA# (6). CTSB# follows (7) and request UARTB transmitter to suspend data transfer. UART-B stops or finishes sending the data bits in its transmit shift register (8). When receive FIFO data in UARTA is unloaded to match the lower threshold of RTS delay (9), UARTA re-assert RTSA# (10) CTSB# recognizes the change (11) and restarts its transmitter and data flow again until next RX trigger (12). This same event applies to the reverse direction when UARTA sends data to UARTB with RTSB# and CTSA# controlling the data flow.

Two interrupts associated with RTS and CTS flow control have been added to give indication when RTS# pin or CTS# pin is de-asserted during operation. The RTS and CTS interrupts must be first enabled by EFR bit-4, and then enabled individually by IER bit-6 and 7.

Automatic hardware flow control is selected by setting bits 6 (RTS) and 7 (CTS) of the EFR register to logic 1. If CTS# pin transitions from logic 0 to logic 1 indicating a flow control request, ISR bit-5 will be set to logic 1 (if enabled via IER bit 6-7), and the 872 UART will suspend TX transmissions as soon as the stop bit of the character in process is shifted out. Transmission is resumed after the CTS# input returns to logic 0, indicating more data may be sent.

The 872 UART offers a programmable flow control trigger hysteresis while maintains compatibility to 16C650A. With the Auto RTS function enabled, an interrupt is generated when receive FIFO reaches the programmed RX trigger level. The RTS# pin will not be forced to logic 1 (RTS Off) until it has reached the upper limit of the hysteresis level. This delay action of suspending remote transmitter increases data throughput. The RTS# pin will return to a logic 0 (RTS on) after RX data buffer (FIFO) is unloaded to the lower limit of the hysteresis level. Under these described conditions the UART will continue to accept data until receive FIFO gets full. The Auto RTS function must be started by asserting RTS# pin to logic 0 (RTS On). For a full description of the hysteresis selection, see EMSR bit 4 and 5 descriptions.

Software Flow Control

When software flow control is enabled, the 872 UART compares one or two sequential receive data characters with the programmed Xon or Xoff-1,2 character value(s). If receive character(s) match the programmed values, the transmitter will halt transmission as soon as the current character has completed sent out. When a match occurs, the Xoff-det interrupt (if enabled via IER bit-5) flag will be set and the interrupt output pin will be activated. Following a suspension due to a match of the Xoff characters values, the UART will monitor the receive data stream for a match to the Xon-1,2 character value(s). If a match is found, the UART will resume operation and clear the Xoff-det flag (ISR bit-4).

Reset initially sets the contents of the Xon/Xoff 8-bit flow control registers to logic 0. Following reset the user can writes any Xon/Xoff value desired for software flow control. Different conditions can be set to detect Xon/Xoff characters and suspend/resume transmissions. When double 8-bit Xon/Xoff characters are selected, the 872 UART compares two consecutive receive characters with two software flow control 8-bit values (Xon1, Xon2, Xoff1, Xoff2) and controls TX transmissions accordingly. Under the above described flow control mechanisms, flow control characters are not placed (stacked) in the user accessible RX data FIFO.

If the receive FIFO is overfilling and flow control needs to be executed, the 872 UART automatically sends a Xoff message via the serial TX output to the remote modem. The 872 UART sends the Xoff-1,2 characters as soon as received data passes the programmed RX FIFO trigger level. To clear this condition, the 872 UART will transmit the programmed Xon-1,2 characters as soon as receive data in the FIFO drops below the programmed RX FIFO trigger level.

Special Feature Software Flow Control

A special feature is provided to detect a 8-bit character when bit-5 is set in the Enhanced Feature Register (EFR). When this character is detected, it will be placed on the user accessible data stack along with normal incoming RX data. This condition is selected in conjunction with EFR bits 0-3. Note that the regular software flow control should be turned off when using this special mode by setting EFR bit 0-3 to logic 0.

The UART compares each incoming receive character with Xoff-2 data. If a match exists, the received data will be transferred to FIFO and ISR bit-4 will be set to indicate detection of special character. Although the Internal Register Table shows each register with eight bits of character information, the actual number of bits is dependent on the programmed word length. Line Control Register (LCR) bits 0-1 defines the number of character bits, i.e., either 5 bits, 6 bits, 7 bits, or 8 bits. The word length selected by LCR bits 0-1 also determines the number of bits that will be used for the special character comparison. Bit-0 in the X-registers corresponds to the LSB bit for the receive character.

Interrupts

Interrupt conditions and priorities are indicated in the interrupt status register (ISR), see Table 4. When the transmitter interrupt is enabled the UART will issue an interrupt to indicate that transmit holding register (THR) is empty. This interrupt must be serviced before continuing operations. The LSR register provides the current singular highest priority interrupt only. It could be noted that CTS and RTS interrupts have lowest interrupt priority. A condition can exist where a higher priority interrupt may mask the lower priority CTS/RTS interrupt(s). Only after servicing the higher pending interrupt will the lower priority CTS/ RTS interrupt(s) be reflected in the status register. Servicing the interrupt without investigating further interrupt conditions can result in data errors.

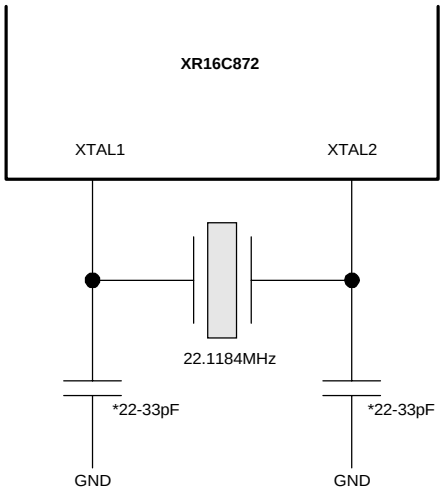
When two interrupt conditions have the same priority, it is important to service these interrupts correctly. Receive Data Ready and Receive Time Out have the same interrupt priority (when enabled by IER bit-0). The receiver issues an interrupt after the number of characters have reached the programmed trigger level. In this case the receive FIFO may hold more characters than the programmed trigger level. Following the removal of a data byte, the user should recheck LSR bit-0 for additional characters. A Receive Time Out will not occur if the receive FIFO is empty. The time out counter is reset at the center of each stop bit received or each time the receive holding register (RHR) is read. The actual time out value is T (**T**ime out length in bits) = 4 X P (**P**rogrammed word length) + 12. To convert the time out value to a character value, the user has to consider the complete word length, including data information length, start bit, parity bit, and the size of stop bit, i.e., 1X, 1.5X, or 2X bit times.

Example -B: If the user programs the word length = 7, with parity and one stop bit, the time out will be:
T = 4 X 7(programmed word length) + 12 = 40 bit times.
Character time = 40 / 10 [(programmed word length = 7) + (parity = 1) + (stop bit = 1) + (start bit = 1) = 4 characters.

Programmable Baud Rate Generator

The 872 UART supports high speed modem technologies that have increased input data rate by employing data compression schemes. For example a 33.6 Kbps modem that employs data compression may require a 115.2 Kbps input data rate. A 128.0 Kbps ISDN modem that supports data compression may need an input data rate of 460.8 Kbps. The 872 UART supports standard data rate from 50 to 460.8 Kbps with a main clock of 7.3728 MHz which is internally derived from the external crystal or clock of 22.1184 MHz. A single baud rate generator provides for each UART transmitter and receiver.

The 872 UART can be configured for internal or external clock operation. For internal clock oscillator operation, an industry standard microprocessor crystal (parallel resonant, 20-33pF loading capacitance) is connected externally between the XTAL1 and XTAL2 pin, see Figure 5. Alternatively, an external clock can be connected to the XTAL1 pin to clock the internal baud rate generator for standard or custom rates.



**Consult with crystal manufacturer for the proper loading capacitance*

Figure 5. Crystal Osc. Ext. Components

Output Baud Rate MCR BIT-7=1	Output Baud Rate MCR Bit-7=0	User 16 x Clock Divisor (Decimal)	User 16 x Clock Divisor (HEX)	DLM Program Value (HEX)	DLL Program Value (HEX)
50	200	2304	900	09	00
75	300	1536	600	06	00
150	600	768	300	03	00
300	1200	384	180	01	80
600	2400	192	C0	00	C0
1200	4800	96	60	00	60
2400	9600	48	30	00	30
4800	19.2K	24	18	00	18
7200	28.8K	16	10	00	10
9600	38.4k	12	0C	00	0C
19.2k	76.8k	6	06	00	06
38.4k	153.6k	3	03	00	03
57.6k	230.4k	2	02	00	02
115.2k	460.8k	1	01	00	01

Table 3. Baud Rate Generator Standard Programming Table with 7.3728 MHz Clock

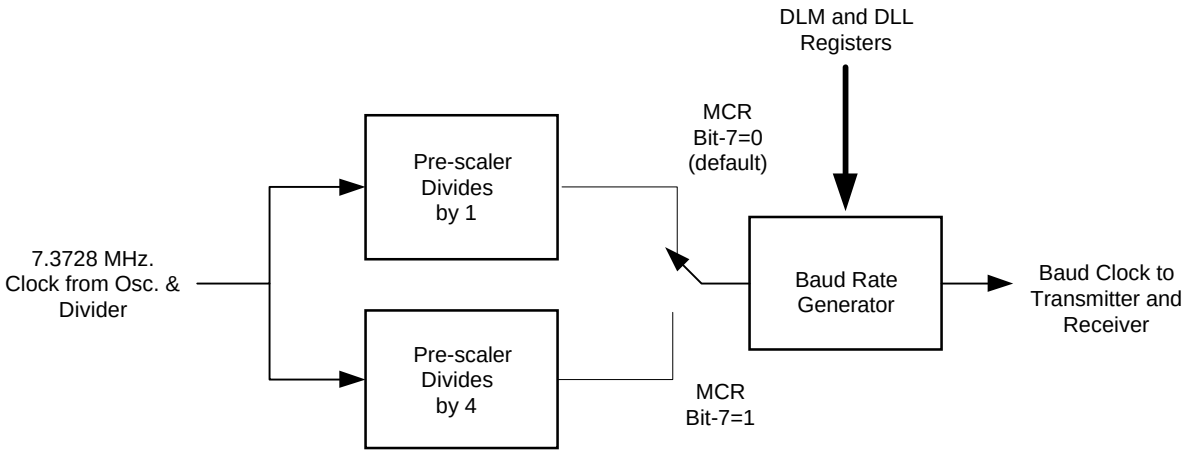


Figure 6. Clock Pre-scaler and Baud Rate Generator Circuitry

The generator divides the input 16X clock by any divisor from 1 to 2^{16} -1. The UART divides the input clock by 16. Further division of this 16X clock provides two table rates to support low and high data rate applications using the same system design. The two rate tables are selectable through the internal register, MCR bit-7. Setting MCR bit-7 to logic 1 provides an additional divide by 4 whereas, setting MCR bit-7 to logic 0 only divides by 1. (See Table 3 and Figure 6). The frequency of the internal sampling rate is exactly 16X (16 times) of the selected baud rate. Customized Baud Rates can be achieved by selecting the proper divisor values for the MSB and LSB sections of baud rate generator.

Programming the Baud Rate Generator Registers DLM (MSB) and DLL (LSB) provides the user capability for selecting the desired serial baud rate. Table 3 shows the two selectable baud rate tables available with the 7.3728 MHz clock. The output data rate tolerance is determined by the frequency accuracy of the 22.1184MHz crystal or external clock.

DMA Operation

The FIFO trigger level provides additional flexibility to the user for data block transfer operation. LSR bits 5-6 provide an indication when the transmitter is empty or has an empty location(s). The user can optionally operate the transmit and receive FIFOs in the DMA mode (FCR bit-3). When transmit and receive FIFOs are enabled and the DMA mode is deactivated (DMA Mode "0"), the UART activates the interrupt output pin for each data transmit or receive operation. When DMA mode is activated (DMA Mode "1"), the user takes the advantage of block mode operation by loading or unloading the FIFO in a block sequence determined by the preset trigger level. In this mode, the UART asserts the interrupt output pin when characters in the transmit FIFOs are below the transmit trigger level, or the number of characters in the receive FIFOs are above the receive trigger level. Transmit or receive DMA operation is selected by EMSR register bit 2.

Sleep Mode

The UARTs are designed to operate with low power consumption. A sleep mode is included to further reduce power consumption when the chip is not being used. The operating parameters are maintained while in sleep. With EFR bit-4 and IER bit-4 enabled (set to logic 1), the UART enters the sleep mode when no interrupt is pending and no activities on the modem port. If an external clock is supplied to the UART, you

may want to stop it. The UART resumes normal operation when a RX character's start bit is detected, a change of state on any of the modem input pins RX, RI#, CTS#, DSR#, CD#, or transmit data is loaded into the FIFO by the user. It typically takes 30us for the crystal oscillator to restart from sleep mode depending on the crystal properties. This delay must be taken into consideration during design as receive character(s) may be lost. The number of characters lost depends on the operating data rate, more at higher data rate. If the sleep mode is enabled and the UART is awakened by one of the conditions described above, it will return to the sleep mode automatically after the last character is transmitted or read by the user and no interrupt pending. The chip will not enter sleep mode while an interrupt(s) is still pending and the oscillator would still be running. The UART stays in the sleep mode of operation until it is disabled by setting IER bit-4 to logic 0.

Example of Sleep mode enable during initialization:

```
Write LCR with 0xBF          ; access to EFR registers
Set EFR bit-4 to logic 1     ; enable non-550 functions
                             ; in IER, EFR and MCR registers
Write LCR with Op.value      ; point to basic registers
Set IER bit-4 to logic 1     ; set sleep mode
                             ; service all pending interrupts
                             ; no modem port activity
                             ; enters sleep mode and stop
                             ; the oscillator
```

For lowest sleep current the following pins should idle at logic 1 state: RX A/B should be at logic 1 and data bus should be pull-down with ~47K resistors if the controller puts the data bus in tri-state condition. No input pins should be left floating.

Loopback Mode

The internal loopback capability allows on board diagnostics. In this mode, the normal modem interface pins are disconnected and re-configured for loopback internally. MSR bits 4-7 are also disconnected. However, MCR register bits 0-3 can be used for controlling loopback diagnostic testing. In this mode, OP1 and OP2 in the MCR register (bits 0-1) control the modem RI# and CD# inputs respectively. MCR signals DTR# and RTS# (bits 0-1) are used to control the modem CTS# and DSR# inputs respectively. The transmitter output (TX) and the receiver input (RX) are disconnected from their associated interface pins, and instead are connected together internally (See Figure 7). The CTS#, DSR#, CD#, and RI# are disconnected from their normal modem control inputs pins, and instead are connected internally to DTR#, RTS#, OP1# and OP2#. Loopback test data enters transmit holding register via the user data bus interface, D0-D7. The transmitter serializes the data and passes the serial data to the receive UART via the internal loopback connection. The receive UART converts the serial data back into parallel data that is then made available at the user data interface, D0-D7. The user optionally compares the received data to the initial transmitted data for verifying error free operation of the UART TX/RX circuits. In this mode, the receiver, transmitter and modem control interrupts are fully operational. However, the interrupts can only be read using lower four bits of the Modem Control Register (MCR bits 0-3) instead of the four Modem Status Register bits 4-7. The interrupts are still controlled by the IER. Please note that OP1# and OP2# pins are not brought out and not available.

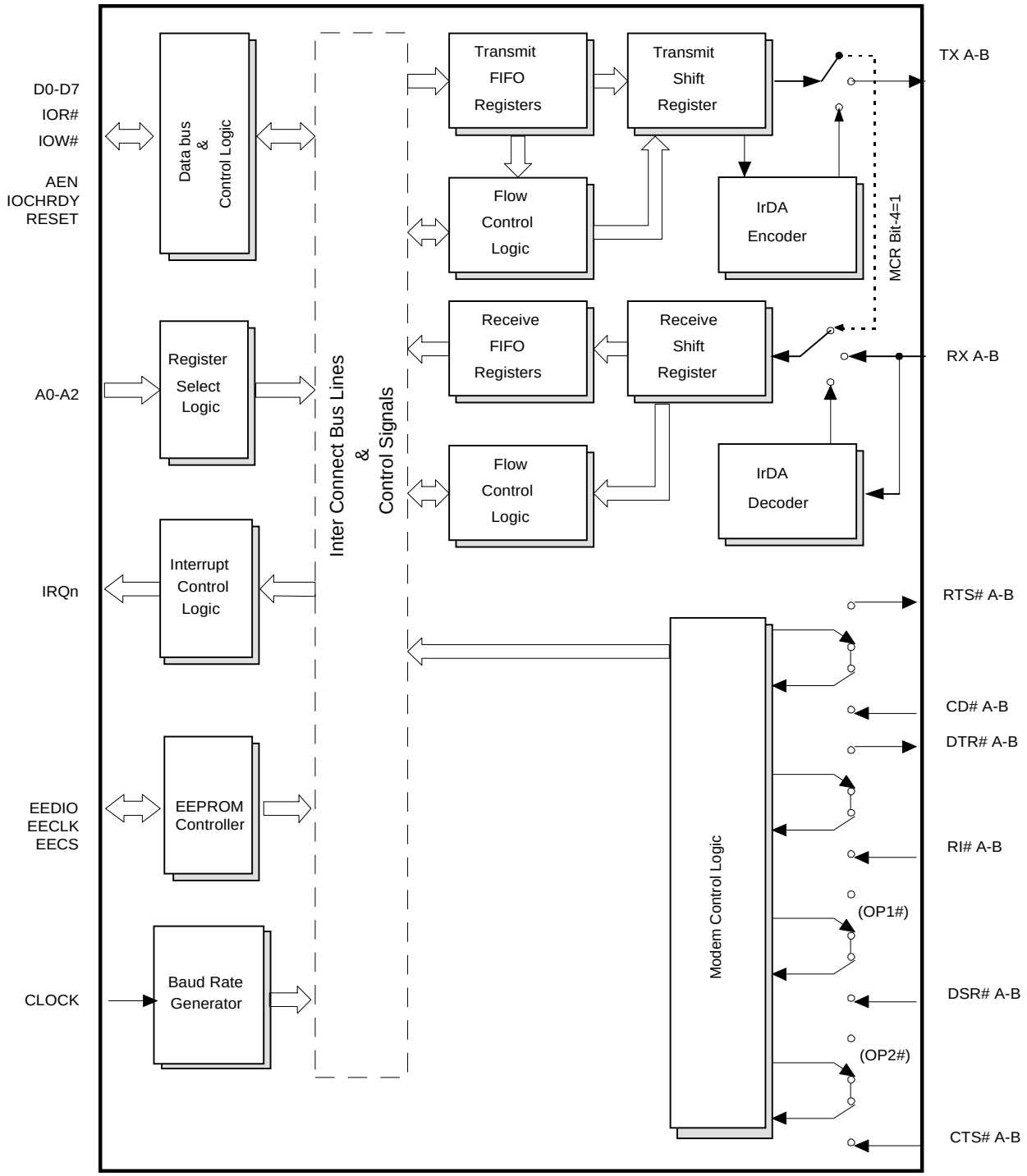


Figure 7. Internal Loop-Back Mode Diagram

REGISTER FUNCTIONAL DESCRIPTIONS

The following table delineates the assigned bit functions for the internal registers. UART A and B has same register set independently control. The assigned bit functions are defined in the following paragraphs.

UART INTERNAL REGISTERS

A2 A1 A0	Register [Default] Note *3	BIT-7	BIT-6	BIT-5	BIT-4	BIT-3	BIT-2	BIT-1	BIT-0
Basic Registers are accessible when LCR bit-7 is set to logic 0. *(Shaded bits are enabled by EFR bit-4)*									
0 0 0	RHR [XX]	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 0	THR [XX]	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 1	IER [00]	0/ CTS# interrupt	0/ RTS# interrupt	0/ Xoff interrupt	0/ Sleep mode	modem status interrupt	receive line status interrupt	transmit holding register	receive holding register
0 1 0	FCR [00]	RCVR trigger (MSB)	RCVR trigger (LSB)	0/TX trigger (MSB)	0/TX trigger (LSB)	DMA mode select	XMIT FIFO reset	RCVR FIFO reset	FIFO enable
0 1 0	ISR [01]	0/ FIFO's enabled	0/ FIFO's enabled	0/ RTS#, CTS#	0/ Xoff Det.	int priority bit-2	int priority bit-1	int priority bit-0	int status
0 1 1	LCR [00]	divisor latch enable	set break	set parity	even parity	parity enable	stop bits	word length bit-1	word length bit-0
1 0 0	MCR [00]	Clock select	0/ IRRT enable	0/ Xon-Any	loop back	(OP2#)	(OP1#)	RTS#	DTR#
1 0 1	LSR [60]	0/ FIFO error	trans. shift reg. empty	trans. holding reg. empty	break interrupt	framing error	parity error	overrun error	receive data ready
1 1 0	MSR [00]	CD#	RI#	DSR#	CTS#	delta CD#	delta RI#	delta DSR#	delta CTS#
1 1 1	SPR [FF] or FIFO Count	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
Baud Rate Generator Registers are accessible only when LCR bit-7 is set to a logic 1.									
0 0 0	DLL [XX]	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 1	DLM [XX]	bit-15	bit-14	bit-13	bit-12	bit-11	bit-10	bit-9	bit-8

UART INTERNAL REGISTERS (CONT'D)

A2 A1 A0	Register [Default] Note *3	BIT-7	BIT-6	BIT-5	BIT-4	BIT-3	BIT-2	BIT-1	BIT-0
Enhanced Registers are accessible only when LCR is set to 0xBF.									
0 0 0	TRG [00]	Trig/ FC	Trig/ FC	Trig/ FC	Trig/ FC	Trig FC	Trig/ FC	Trig/ FC	Trig/ FC
0 0 1	FCTR [00]	Rx/Tx Mode	SPR/EMSR Select	Trig bit-1	Trig bit-0	RS485 Auto control	IrRx Inv.	RTS Hysteresis bit-1	RTS Hysteresis bit-0
0 1 0	EFR [00]	Auto CTS	Auto RTS	Special Char. select		Cont-3 Tx,Rx Control	Cont-2 Tx,Rx Control	Cont-1 Tx,Rx Control	Cont-0 Tx,Rx Control
1 0 0	Xon-1[00]	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
1 0 1	Xon-2[00]	bit-15	bit-14	bit-13	bit-12	bit-11	bit-10	bit-9	bit-8
1 1 0	Xoff-1[00]	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
1 1 1	Xoff-2[00]	bit-15	bit-14	bit-13	bit-12	bit-11	bit-10	bit-9	bit-8
EMSR Register is accessible only when FCTR bit 6 is set to logic 1.									
1 1 1	EMSR [00]	Not Used	Not Used	RTS Hysteresis bit-3	RTS Hysteresis bit-2	Reserved	Reserved	ALT. Rx/Tx FIFO Count	Rx/Tx FIFO Count

Note:

*[*3] - The value represents the register's initialized HEX value. An "X" signifies a 4-bit un-initialized nibble.*

The UARTs have Device Identification and Device Revision code to distinguish the part with others. It is suggested to the user to read the identification and revision information from the part only during the power on initialization routine to avoid disturbing the baud rate generator during normal operation.

To read the identification number from the device, it is required to set the baud rate generator divisor latch to Logic 1 (LCR bit-7 = logic 1) and set the content of the baud rate generator DLL and DLM registers to 0x00. Then read the content of DLM=0x10 for XR16C850 type and the content of DLL for the device revision with 0x01 represents revision-A and 0x02 for revision-B, and so forth.

At the beginning of UART Initiation routine:
Write LCR bit-7=1
Write DLM = 0x00
Write DLL = 0x00
Read DLM for the UART type number (0x10)
Read DLL for the UART revision number (0x02)

Transmit and Receive Data Register

The serial transmitter section consists of a 8-bit Transmit Hold Register (THR) which is part of the transmit FIFO and Transmit Shift Register (TSR). The status of the THR and TSR are provided in the Line Status Register (LSR). Writing to THR address location transfers the contents of the data bus (D7-D0) to the THR, providing that the THR or TSR flag is set. The THR empty flag is set to logic 1 when the transmit FIFO has room for more data. The flag indicates either that the transmit holding register becomes empty in the non-FIFO mode or at the preset transmit trigger level when the transmit FIFO is enabled. The TSR flag always indicates the transmitter is empty and it has nothing to shift out. This flag can be use for directional control in half duplex operations.

The serial receive section also contains a 11-bit Receive Holding Register (RHR) which is part of the receive FIFO. Receive data is unloaded by reading the RHR register address location. The receive section provides a mechanism to detect false starts. On the falling edge of a start or false start bit on RX input, an internal sampling counter starts counting clocks at 16x of the operating data rate. After 7 1/2 clocks the incoming start bit time should be at the center of the bit time. At this time the start bit is sampled and if it is still a logic 0 it is validated. If false, the detection sequence starts all over again. Evaluating the start bit in this manner and validating data bits and stop bit also in the middle of the bit time helps to ensure the integrity of the receiving character. Receive errors such as Framing, Parity, and Overrun are saved in the receive FIFO and posted in the LSR as each data byte becomes available to the CPU. The receive FIFO is actually a 11-bit wide FIFO including the 3 receive error bits. The receiver FIFO pointer is bumped upon a data byte read operation. Therefore, it is necessary for the user to read the error bits prior to reading the data byte.

Interrupt Enable Register (IER)

The Interrupt Enable Register (IER) masks the interrupts for receiver ready, transmitter empty, line status, and modem status. It also optionally includes CTS#, RTS# and Xoff interrupts when enabled by EFR register bit-4. These interrupts are wired Or'ed to the INT output pin. See IER register description for more detail.

Receive FIFO Interrupt Mode Operation

When the receive FIFO (FCR bit-0 = logic 1) and receive interrupt (IER bit-0 = logic 1) are enabled, the receive interrupt and register status will reflect the following:

A) The receive data interrupt is issued when the receive FIFO has reached the programmed trigger level. The interrupt clears when 1) upon reading LSR register or 2) FIFO content drops below the programmed trigger level.

B) Receive FIFO status is also reflected in the ISR register when the FIFO trigger level has reached the programmed level. The ISR register status bit will clear only when the FIFO content drops below the programmed trigger level.

C) The receive data ready bit (LSR bit-0) is set as soon as a character is transferred from the receive shift register to the receive FIFO. This bit is reset when the FIFO becomes empty.

Receive/Transmit FIFO Polled Mode Operation

When FCR BIT-0 equals a logic 1; resetting IER bits 0-3 enables the 850 in the FIFO polled mode of operation. Since the receiver and transmitter have separate bits in the LSR either or both can be used in the polled mode by selecting respective transmit or receive control bit(s).

A) LSR BIT-0 will be a logic 1 as long as there is one byte in the receive FIFO.

B) LSR BIT 1-4 will indicate if an overrun error occurred in the receiver.

C) LSR BIT-5 will indicate when the transmit FIFO is empty.

D) LSR BIT-6 will indicate when both the transmit FIFO and transmit shift register are empty.

E) LSR BIT-7 will indicate any data errors within the receive FIFO. This bit will clear when the error byte is unloaded.

IER BIT-0:

Logic 0 = Disable the receiver ready interrupt. (normal default condition)

Logic 1 = Enable the receiver ready interrupt. The receiver ready interrupt is cleared when LSR is read.

IER BIT-1:

Logic 0 = Disable the transmitter empty interrupt. (normal default condition)

Logic 1 = Enable the transmitter empty interrupt. The transmitter empty interrupt is cleared when ISR is read.

IER BIT-2:

Logic 0 = Disable the receiver line status interrupt. (normal default condition)

Logic 1 = Enable the receiver line status interrupt. The receiver line interrupt is cleared when LSR is read.

IER BIT-3:

Logic 0 = Disable the modem status register interrupt. (normal default condition)

Logic 1 = Enable the modem status register interrupt. The modem status interrupt is cleared when MSR is read.

IER BIT -4:

Logic 0 = Disable sleep mode. (normal default condition)

Logic 1 = Enable sleep mode. See Sleep Mode section for details.

IER BIT-5:

Logic 0 = Disable the software flow control, receive Xoff-det interrupt. (normal default condition)

Logic 1 = Enable the software flow control, receive Xoff-det interrupt. The Xoff-det interrupt is cleared by reading the ISR register or upon receiving a Xon character. Also, when Special Character mode is enabled (EFR-bit 5 =1) reading the ISR register or a following received character will clear the interrupt.

IER BIT-6:

Logic 0 = Disable the RTS interrupt. (normal default condition)

Logic 1 = Enable the RTS interrupt. The UART issues an interrupt when the RTS# pin transitions from a logic 0 to a logic 1 as reported in MSR bit-register. The interrupt is cleared by reading the MSR register.

IER BIT-7:

Logic 0 = Disable the CTS interrupt. (normal default condition)

Logic 1 = Enable the CTS interrupt. The UART issues an interrupt when CTS# pin transitions from a logic 0 to a logic 1 as reported in MSR register. The interrupt is cleared by reading the MSR register.

FIFO Control Register (FCR)

This register is used to enable the FIFOs, clear the FIFOs, set the transmit/receive FIFO trigger levels, and select the DMA mode. The DMA, and FIFO modes are defined as follows:

DMA MODE

Mode 0 - Set and enable the interrupt for each single character transmit or receive operation. Transmit empty interrupt will be generated whenever the Transmit Holding Register (THR) is empty and receive ready interrupt will be generated whenever the Receive Holding Register (RHR) is loaded with a character. However, the RX FIFO continues to receive data up to its limit.

Mode 1 - Enable the interrupt in a block transfer mode operation. The transmit empty interrupt is set when the transmit FIFO trigger level is reached. The receive interrupt is set when the receive FIFO fills up to the programmed trigger level. However the FIFO continues to fill regardless of the programmed level until the FIFO is completely full.

FCR BIT-0:
Logic 0 = Disable the transmit and receive FIFO. (normal default condition)
Logic 1 = Enable the transmit and receive FIFO.
This bit must be a "1" when other FCR bits are written to or they will not be programmed.

FCR BIT-1:
Logic 0 = No FIFO receive reset. (normal default condition)
Logic 1 = Clears the FIFO counter and resets the pointers logic (the receive shift register is not cleared or altered). This bit will return to a logic 0 after clearing the FIFO.

FCR BIT-2:
Logic 0 = No FIFO transmit reset. (normal default condition)
Logic 1 = Clears the FIFO counter and resets the pointers logic (the transmit shift register is not cleared or altered). This bit will return to a logic 0 after clearing the FIFO.

FCR BIT-3:
Logic 0 = Set DMA mode "0". (normal default condition)
Logic 1 = Set DMA mode "1."

Transmit operation in mode "0":
This selects single character interrupt operation. The transmit empty interrupt will be set when the UART is set in this 16C450 or single character simulation mode (FIFOs disabled, FCR bit-0 = logic 0) or in the FIFO mode (FIFOs enabled, FCR bit-0 = logic 1, FCR bit-3 = logic 0) and when there are no characters in the transmit FIFO or transmit holding register.

Receive operation in mode "0":
When the UART is in mode "0" (FCR bit-0 = logic 0) or in the FIFO mode (FCR bit-0 = logic 1, FCR bit-3 = logic 0) and there is a character in RHR, the receive ready interrupt is generated.

Receive operation in mode "1":
When the UART is in FIFO mode (FCR bit-0 = logic 1, FCR bit-3 = logic 1) and the receive trigger level has been reached, or a Receive Time Out has occurred, the receive ready interrupt is generated.

FCR BIT 4-5: (logic 0 or cleared is the default condition, TX trigger level = none)

The XR16C850 provide 4 user selectable trigger levels, The FCTR Bits 4-5 selects one of the following table. These bits are used to set the trigger level for the transmit FIFO interrupt. The UART will issue a transmit empty interrupt when number of characters in FIFO drops below the selected trigger level.

Trigger Table-A (Transmit)
"Default setting after reset, ST16C550 mode"

BIT-5	BIT-4	FIFO Trigger Level
X	X	None

Trigger Table-B (Transmit)

BIT-5	BIT-4	FIFO Trigger Level
0	0	16
0	1	8
1	0	24
1	1	30

Trigger Table--C (Transmit)

BIT-5	BIT-4	FIFO Trigger Level
0	0	8
0	1	16
1	0	32
1	1	56

Trigger Table-D (Transmit)

BIT-5	BIT-4	FIFO trigger level
X	X	User programmable trigger levels

FCR BIT 6-7: (logic 0 or cleared is the default condition, RX trigger level =8)

These bits are used to set the trigger level for the receiver FIFO interrupt. The interrupt will trigger again when RX data is unloaded below the threshold and incoming data fills it back up to the trigger level. The FCTR Bits 4-5 selects one of the following table.

Trigger Table-A (Receive)
"Default setting after reset, ST16C550 mode"

BIT-7	BIT-6	FIFO trigger level
0	0	1
0	1	4
1	0	8
1	1	14

Trigger Table-B (Receive)

BIT-7	BIT-6	FIFO trigger level
0	0	8
0	1	16
1	0	24
1	1	28

Trigger Table-C (Receive)

BIT-7	BIT-6	FIFO trigger level
0	0	8
0	1	16
1	0	56
1	1	60

Trigger Table-D (Receive)

BIT-7	BIT-6	FIFO trigger level
X	X	User programmable trigger levels

An example to program the FIFO trigger level:

```
write LCR with 0xBF          ; point to enhanced registers
set FCTR bit4-5 to logic 1   ; select trigger Table-D
set FCTR bit-7 to logic 0    ; program RX FIFO trigger level
write TRG with 0x60          ; set your RX trigger level to 96
set FCTR bit-7 to logic 1    ; program TX FIFO trigger level
write TRG with 0x08          ; set your TX trigger level to 8
write LCR with 0x03          ; set operating parameters
```

Receive data ready interrupt will activates when RX FIFO fills up to 96 data bytes while the transmit empty interrupt gets set when data is empty to 8 bytes.

Interrupt Status Register (ISR)

The UART provides six levels of prioritized interrupts to minimize external software interaction. The Interrupt Status Register (ISR) provides the user with six interrupt status bits. Performing a read cycle on the ISR will provide the user with the highest pending interrupt level to be serviced. No other interrupts are acknowledged until the pending interrupt is serviced. Whenever the interrupt status register is read, the interrupt status is cleared. However it should be noted that only the current pending interrupt is cleared by the read. A lower level interrupt may be seen after re-reading the interrupt status bits. The Interrupt Source Table 6 (below) shows the data values (bit 0-5) for the six prioritized interrupt levels, the interrupt sources associated with each of these interrupt levels, and how to clear each interrupt (INT).

Priority Level	[ISR BITS] Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	Source of the Interrupt	INT Clears After A
1	0	0	0	1	1	0	LSR (Receiver Line Status Register)	LSR read
2	0	0	0	1	0	0	RXRDY (Received Data Ready)	LSR read
2	0	0	1	1	0	0	RXRDY (Receive Data time out)	LSR read
3	0	0	0	0	1	0	TXRDY (Transmitter Holding Register Empty)	ISR read
4	0	0	0	0	0	0	MSR (Modem Status Register)	MSR read
5	0	1	0	0	0	0	RXRDY (Rcv. Xoff signal / Special character)	ISR read
6	1	0	0	0	0	0	CTS, RTS change of state	MSR read

Table 4. Interrupt Priority and Source

ISR BIT-0:

Logic 0 = An interrupt is pending and the ISR contents may be used as a pointer to the appropriate interrupt service routine.

Logic 1 = No interrupt pending. (normal default condition)

ISR BIT 1-3: (logic 0 or cleared is the default condition)

These bits indicate the source for a pending interrupt at interrupt priority levels 1, 2, and 3 (See Interrupt Source Table).

ISR BIT 4-5: (logic 0 or cleared is the default condition)

These bits are enabled when EFR bit-4 is set to a logic 1. ISR bit-4 indicates that matching Xoff character(s) have been received. ISR bit-5 indicates that CTS# or RTS# condition have changed. Note that once set to a logic 1, the ISR bit-4 will stay a logic 1 until Xon character(s) is received or upon a read to register ISR.

ISR BIT 6-7: (logic 0 or cleared is the default condition)

These bits are set to a logic 0 when the FIFO is not being used. They are set to a logic 1 when the FIFOs are enabled.

Line Control Register (LCR)

The Line Control Register is used to specify the asynchronous data communication format. The word length, the number of stop bits, and the parity are selected by writing the appropriate bits in this register. This register also has a secondary function to select two other register sets. The first is by setting bit-7 = 1 to select the baud rate divisor (DLL and DLM) registers, and the second set of registers is selected when a "BF" hex is written to LCR to select the enhanced register set.

LCR BIT 0-1: (logic 0 or cleared is the default condition).

These two bits specify the word length to be transmitted or received. The upper unused bit(s) in the received data byte is set to zero.

BIT-1	BIT-0	Word Length
0	0	5
0	1	6
1	0	7
1	1	8

LCR BIT-2: (logic 0 or cleared is the default condition)

The length of stop bit is specified by this bit in conjunction with the programmed word length.

BIT-2	Word	Stop Bit Length (Bit Time(s))
0	5,6,7,8	1
1	5	1-1/2
1	6,7,8	2

LCR BIT-3:

Parity or no parity can be selected via this bit.

Logic 0 = No parity (normal default condition)

Logic 1 = A parity bit is generated during the transmission, the receiver checks and reports parity error in the LSR register. The parity is not presented in the received data byte.

LCR BIT-4:

If the parity bit is enabled with LCR bit-3 set to a logic 1, LCR BIT-4 selects the even or odd parity format.

Logic 0 = ODD Parity is generated by forcing an odd number of logic 1's in the transmitted data. The receiver must be programmed to check the same format. (normal default condition)

Logic 1 = EVEN Parity is generated by forcing an even number of logic 1's in the transmitted data. The receiver must be programmed to check the same format.

LCR BIT-5:

If the parity bit is enabled, LCR BIT-5 selects the forced parity format.

LCR BIT-5 = logic 0, parity is not forced (normal default condition)

LCR BIT-5 = logic 1 and LCR BIT-4 = logic 0, parity bit is forced to a logical 1 for the transmit and receive data.

LCR BIT-5 = logic 1 and LCR BIT-4 = logic 1, parity bit is forced to a logical 0 for the transmit and receive data.

LCR Bit-3	LCR Bit-4	LCR Bit-5	Parity Selection
0	X	X	No parity
1	0	0	Odd parity
1	1	0	Even parity
1	0	1	Forced parity="1"
1	1	1	Forced parity= 0"

LCR BIT-6:

When enabled the Break control bit causes a break condition to be transmitted (the TX output is forced to a logic 0 state). This condition exists until disabled by setting LCR bit-6 to a logic 0.

Logic 0 = No TX break condition. (normal default condition)

Logic 1 = Forces the transmitter output (TX) to a logic 0 for alerting the remote receiver to a line break condition.

LCR BIT-7:

The internal baud rate counter latch and Enhance Feature mode enable.

Logic 0 = Divisor latch disabled. (normal default condition)

Logic 1 = Select baud rate divisors (DLL and DLM) and enhanced feature register set enabled

Modem Control Register (MCR)

This register controls the interface with the modem or a peripheral device.

MCR BIT-0:

Logic 0 = Force -DTR output to a logic 1. (normal default condition)

Logic 1 = Force -DTR output to a logic 0.

MCR BIT-1:

Logic 0 = Force RTS# output to a logic 1. (normal default condition)

Logic 1 = Force RTS# output to a logic 0.

Automatic RTS may be used for hardware flow control by enabling EFR bit-6 (See EFR bit-6).

MCR BIT-2:

*OP1# output is not available in the 872.

Logic 0 = Set OP1# output to a logic 1. (normal default condition)

Logic 1 = Set OP1# output to a logic 0.

MCR BIT-3:

*OP2# output is not available in the 872

Logic 0 = Set OP2# output to a logic 1. (normal default condition)

Logic 1 = Set OP2# output to a logic 0.

MCR BIT-4:

Logic 0 = Disable loop-back mode. (normal default condition)

Logic 1 = Enable local loop-back mode (diagnostics).

MCR BIT-5:

Logic 0 = Disable Xon-Any function (normal default condition)

Logic 1 = Enable Xon-Any function. In this mode any RX character received will enable Xon.

MCR BIT-6:

Logic 0 = Enable Modem receive and transmit input/output interface. (normal default condition)

Logic 1 = Enable infrared IrDA receive and transmit inputs/outputs. While in this mode, the TX/RX output/inputs are routed to the infrared encoder/decoder. The data input and output levels will conform to the IrDA infrared interface requirement. As such, while in this mode the infrared TX output will be a logic 0 during idle data conditions. Care must be taken into consideration in the design not to over heat the IR LED during power up initialization state while TX output is still at logic 1.

Example to enable IR encoder and decoder:

```
Write LCR with 0xBF       ; access to EFR "shadow" register
Set EFR bit-4 to logic 1  ; enable non-550 bits in IER, EFR & MCR
Write LCR with op. value  ; set up LCR and point to base register set
Set MCR bit-6 to logic 1  ; enable IR mode, TX output pin goes logic 0
```

MCR BIT-7:
Logic 0 = Divide by one. The input clock (crystal or external) is divided by sixteen and then presented to the Programmable Baud Rate Generator (BGR) without further modification, i.e., divide by one. (normal, default condition)
Logic 1 = Divide by four. The divide by one clock described in MCR bit-7 equals a logic 0, is further divided by four (also see Programmable Baud Rate Generator section).

Line Status Register (LSR)

This register provides the status of data transfers between the UART and the CPU.

LSR BIT-0:
Logic 0 = No data in receive holding register or FIFO. (normal default condition)
Logic 1 = Data has been received and is saved in the receive holding register or FIFO.

LSR BIT-1:
Logic 0 = No overrun error. (normal default condition)
Logic 1 = Overrun error. A data overrun error occurred in the receive shift register. This happens when additional data arrives while the FIFO is full. In this case the previous data in the shift register is overwritten. Note that under this condition the data byte in the receive shift register is not transfer into the FIFO, therefore the data in the FIFO is not corrupted by the error.

LSR BIT-2:
Logic 0 = No parity error (normal default condition)
Logic 1 = Parity error. The receive character does not have correct parity information and is suspect. In the FIFO mode, this error is associated with the character at the top of the FIFO.

LSR BIT-3:
Logic 0 = No framing error (normal default condition).
Logic 1 = Framing error. The receive character did not have a valid stop bit(s). In the FIFO mode this error is associated with the character at the top of the FIFO.

LSR BIT-4:
Logic 0 = No break condition (normal default condition)
Logic 1 = The receiver received a break signal (RX was a logic 0 for one character frame time). In the FIFO mode, only one break character is loaded into the FIFO.

LSR BIT-5:
This bit is the Transmit Holding Register Empty indicator. This bit indicates that the UART is ready to accept a new character for transmission. In addition, this bit causes the UART to issue an interrupt to CPU when the THR interrupt enable is set. The THR bit is set to a logic 1 when a character is transferred from the transmit holding register into the transmitter shift register. The bit is reset to logic 0 concurrently with the loading of the transmitter holding register by the CPU. In the FIFO mode this bit is set when the transmit FIFO is empty; it is cleared when at least 1 byte is written to the transmit FIFO.

LSR BIT-6:
This bit is the Transmit Empty indicator. This bit is set to a logic 1 whenever the transmit holding register and the transmit shift register are both empty. It is reset to logic 0 whenever either the THR or TSR contains a data character. In the FIFO mode this bit is set to one whenever the transmit FIFO and transmit shift register are both empty.

LSR BIT-7:
Logic 0 = No Error (normal default condition)
Logic 1 = There is at least one parity error, framing error or break indication in the current FIFO data. This bit is cleared when LSR register is read.

When the LSR is read, bit 2,3 and 4 reflects the error bits of the character on top of the RX FIFO, next character to be read in RHR. Therefore, errors in a character are identified by reading the LSR and then reading the data character in RHR.

Modem Status Register (MSR)

This register provides the current state of the control interface signals from the modem, or other peripheral device that the UART A or B is connected. Four bits of this register are used to indicate the changed information. These bits are set to a logic 1 whenever a control input from the modem changes state. These bits are set to a logic 0 whenever the CPU reads this register.

MSR BIT-0:
Logic 0 = No CTS# Change (normal default condition)
Logic 1 = The CTS# input to the UART has changed state since the last time it was read. A modem Status Interrupt will be generated.

MSR BIT-1:
Logic 0 = No DSR# Change (normal default condition)
Logic 1 = The DSR# input to the UART has changed state since the last time it was read. A modem Status Interrupt will be generated.

MSR BIT-2:
Logic 0 = No RI# Change (normal default condition)
Logic 1 = The RI# input to the UART has changed from a logic 0 to a logic 1. A modem Status Interrupt will be generated.

MSR BIT-3:
Logic 0 = No CD# Change (normal default condition)
Logic 1 = Indicates that the CD# input to the UART has changed state since the last time it was read. A modem Status Interrupt will be generated.

MSR BIT-4:
CTS# functions as hardware flow control signal input if it is enabled via EFR bit-7. The transmit holding register flow control is enabled/disabled by MSR bit-4. Flow control (when enabled) allows suspending and resuming data transmissions based on the external modem CTS# signal. A logic 1 at the CTS# pin will suspend transmissions as soon as current character has finished transmission.

Normally MSR bit-4 bit is the complement of the CTS# input. However in the loop-back mode, this bit is equivalent to the RTS bit in the MCR register.

MSR BIT-5:
DSR (active high, logical 1). Normally this bit is the complement of the DSR# input pin. In the loop-back mode, this bit is the complement to the DTR bit in the MCR register.

MSR BIT-6:
RI (active high, logical 1). Normally this bit is the complement of the RI# input. In the loop-back mode this bit is equivalent to the OP1# bit in the MCR register.

MSR BIT-7:
CD (active high, logical 1). Normally this bit is the complement of the CD# input. In the loop-back mode this bit is equivalent to the OP2# bit in the MCR register.

Scratch Pad Register (SPR)

The UART A or B has a temporary data register to store 8 bits of user information. The register content is set to 0xFF upon power up or a hardware reset. This register is alternately used as TX or RX FIFO counter register, when FCTR bit-6=1 with EMSR bit-0 defining for TXCNT or RXCNT.

Enhanced Feature Register (EFR)

This register is only accessible when LCR is set to 0xBF. Enhanced feature functions in the 16C550 base register set area are enabled using this register bit-4. These are IER bits 4-7, ISR & FCR bits 4-5, and MCR bits 5-7.

Bits-0 through 3 provide single or dual character software flow control selection. When the Xon1 and Xon2 and/or Xoff1 and Xoff2 modes are selected (see Table 5), the double 8-bit words are concatenated into two sequential characters.

EFR BIT 0-3: (logic 0 or cleared is the default condition)
Combinations of software flow control can be selected by programming these bits.

Cont-3	Cont-2	Cont-1	Cont-0	TX, RX software flow controls
0	0	X	X	No transmit flow control
1	0	X	X	Transmit Xon1/Xoff1
0	1	X	X	Transmit Xon2/Xoff2
1	1	X	X	Transmit Xon1 and Xon2/Xoff1 and Xoff2
X	X	0	0	No receive flow control
X	X	1	0	Receiver compares Xon1/Xoff1
X	X	0	1	Receiver compares Xon2/Xoff2
1	0	1	1	Transmit Xon1/ Xoff1. Receiver compares Xon1 and Xon2, Xoff1 and Xoff2
0	1	1	1	Transmit Xon2/Xoff2 Receiver compares Xon1 and Xon2/Xoff1 and Xoff2
1	1	1	1	Transmit Xon1 and Xon2/Xoff1 and Xoff2 Receiver compares Xon1 and Xon2/Xoff1 and Xoff2
0	0	1	1	No transmit flow control Receiver compares Xon1 and Xon2/Xoff1 and Xoff2

Table 5. Software Flow Control Registers

EFR BIT-4:

Enhanced function control bit. The content of the IER bits 4-7, ISR bits 4-5, FCR bits 4-5, and MCR bits 5-7 can be modified and latched. After modifying any bits in the enhanced registers, EFR bit-4 can be set to a logic 0 to latch the new values. This feature prevents existing software from altering or overwriting the UART enhanced functions.

Logic 0 = disable/latch enhanced features. IER bits 4-7, ISR bits 4-5, FCR bits 4-5, and MCR bits 5-7 are saved to retain the user settings, then IER bits 4-7, ISR bits 4-5, FCR bits 4-5, and MCR bits 5-7 are initialized to the default values shown in the Internal Resister Table. After a reset, the IER bits 4-7, ISR bits 4-5, FCR bits 4-5, and MCR bits 5-7 are set to a logic 0 to be compatible with ST16C550 mode. (normal default condition).

Logic 1 = Enables the enhanced functions. When this bit is set to a logic 1 all enhanced features of the UART are enabled and user settings stored during a reset will be restored.

EFR BIT-5:

Logic 0 = Special Character Detect Disabled (normal default condition)

Logic 1 = Special Character Detect Enabled. The UART compares each incoming receive character with Xoff-2 data. If a match exists, the received data will be transferred to FIFO and ISR bit-4 will be set to indicate detection of special character. Bit-0 in the X-registers corresponds with the LSB bit for the receive character. When this feature is enabled, the normal software flow control must be disabled (EFR bits 0-3 must be set to a logic 0).

EFR BIT-6:

Automatic RTS is used for hardware flow control by enabling EFR bit-6. The user must assert RTS# to initiate this function. When AUTO RTS is selected, an interrupt will be generated when the receive FIFO is filled to the programmed RX trigger level and RTS# will go to a logic 1 when it reaches the upper limit of the hysteresis level. RTS# will return to a logic 0 when data

is unloaded to the lower limit of the hysteresis. The state of this register bit changes with the status of the hardware flow control. RTS# functions normally when hardware flow control is disabled.

0 = Automatic RTS flow control is disabled. (normal default condition)

1 = Enable Automatic RTS flow control.

EFR bit-7:

Automatic CTS Flow Control.

Logic 0 = Automatic CTS flow control is disabled. (normal default condition)

Logic 1 = Enable Automatic CTS flow control. Transmission stops when CTS# goes to a logical 1. Transmission resumes when the CTS# pin returns to a logical 0.

FEATURE CONTROL REGISTER (FCR)

This register is only accessible when LCR is set to 0xBF.

FCTR BIT 0-1:

User selectable RTS# delay or hysteresis for hardware flow control application. After reset, these bits are set to logic 0 to select the next trigger level on the RX FIFO trigger level (FCR bit 6-7,Table-A). These bits are also associated with EMSR bit-4 and 5 for the hysteresis control. See EMSR register for more details.

FCTR BIT-2:

0 = Select RX input as encoded IrDa data.

1 = Select RX input as active high encoded IrDa data.

FCTR BIT-3:

Auto RS485 Half Duplex Direction control.

*OP1# output is not available in the 872, however, it does change the behavior of the transmit empty interrupt.

0 = Transmitter generates an interrupt when transmit holding register becomes empty while transmit shift register is still shifting data out.

1 = Enable Auto RS485 Half Duplex Direction Control. The transmit empty interrupt generation is delayed until the Transmitter Shift Register (TSR) becomes empty.

FCTR BIT 4-5:

Transmit / receive trigger table select.

FCTR Bit-5	FCTR Bit-4	Trigger Table
0	0	Table-A (TX/RX)
0	1	Table-B (TX/RX)
1	0	Table-C (TX/RX)
1	1	Table-D (TX/RX)

FCTR BIT-6:

Scratch Pad Register (SPR) or EMSR select.

0 = Scratch Pad Register (SPR) is selected as general read and write register. 16C550 compatible mode.

1 = FIFO count register, Enhanced Mode Select Register (EMSR). Number of characters in transmit or receive holding register can be read via Scratch Pad Register when this bit is set. Enhanced Mode is selected when it is written into it.

FCTR BIT-7:

Programmable trigger register select.

0 = Receiver programmable trigger level register (TRG) is selected.

1 = Transmitter programmable trigger level register (TRG) is selected.

TRIGGER LEVEL/FIFO COUNT REGISTER (TRG)

This register is only accessible when LCR is set to 0xBF.

This register provides the user programmable transmit or receive trigger level from byte 0 to 128 (0xFF), and reading the number of data bytes in the transmit or receive FIFO.

TRG BIT 0-7: Write only.
This register sets the user programmable transmit or receive FIFO trigger levels. FCTR bit-7 must be set and point to the transmitter or receiver prior to programming the trigger level.

TRG BIT 0-7: Read only.
Transmit / receive FIFO count. Number of characters in transmit or receive FIFO can be read via this register. FCTR bit-7 must be set and point to the transmitter or receiver prior to reading the FIFO count.

ENHANCED MODE SELECT REGISTER (EMSR)

This register is only accessible when LCR is set to 0xBF and FCTR Bit-6 is set to logic 1.

EMSR BIT-0: Write only
0 = Receive FIFO count register. The Scratch Pad Register (SPR) is used to provide the receive FIFO count when it is read.
1 = Transmit FIFO count register. The Scratch Pad Register (SPR) is used to provide the transmit FIFO count when it is read.
Example to read the number of character count in TX or RX FIFO.

```
In the Initialization routine:
set LCR to 0xBF                 ; point to enhanced registers
set FCTR bit-6 to logic 1       ; swap  SPR to be FIFO counters and
                                ; point to EMSR register
set LCR to operating parameters
- in RX routine -
set EMSR bit-0 to logic 0       ; set to read RX FIFO count
read SPR                        ; obtain RX FIFO count
      or
- in TX routine -
set EMSR bit-0 to logic 1       ; read TX FIFO count
read SPR                        ; obtain TX FIFO Count
```

EMSR BIT-1: Write only
0 = Normal.
1 = Alternate receive - transmit FIFO count. When EMSR Bit-0=1 and EMSR Bit-1=1, Scratch Pad Register is used to provide the receive - transmit FIFO count when it is read every alternate read cycle. The TRG Bit-7 will provide FIFO count mode information, TRG Bit-7=0 receive mode, TRG Bit-7=1 transmit mode.

EMSR BIT-2: Write only
This bit is not available in the 872.

EMSR BIT4 and 5 - Write only
These bits select the RTS flow control hysteresis and are associated with FCTR bit 0 and 1. The RTS hysteresis is reference to the RX FIFO trigger level. Below table shows the 16 selectable hysteresis.

EMSR Bit-5	**EMSR Bit-4**	**FCTR Bit-1**	**FCTR Bit-0**	**RTS Hysteresis** (characters)
0	0	0	0	Next level
0	0	0	1	+/- 4
0	0	1	0	+/- 6
0	0	1	1	+/- 8
0	1	0	0	+/- 8
0	1	0	1	+/- 16
0	1	1	0	+/- 24
0	1	1	1	+/- 32
1	0	0	0	+/- 12
1	0	0	1	+/- 20
1	0	1	0	+/- 28
1	0	1	1	+/- 36
1	1	0	0	+/- 40
1	1	0	1	+/- 44
1	1	1	0	+/- 48
1	1	1	1	+/- 52

EMSR BIT 6-7:
Reserved for future use.

1284 Controller

The bi-directional parallel data port controller is compatible to IEEE Standard 1284 interface. The 1284 interface can be programmed as a standard printer port or bi-directional parallel port for high speed data transfer systems. The 1284 interface provides 1284 Level II electrical interface, needing no external transceivers to interface to the parallel port cable. Hence, it can connect directly to a printer or a high speed bi-directional parallel device. The 1284 controller supports the following modes of operation.

- Standard Centronics interface, forward only.
- Bi-directional Centronics.
- Parallel port with data FIFO.
- ECP, Extended Capabilities Port, and with 16 byte data FIFO in Forward and Reverse modes, supports Run Length Encoded (RLE) de-compression in the reverse mode, however, no compression is supported in the forward mode, and Direct Memory Access transfer capability.
- EPP, Enhanced Parallel Port.

On a reset, the device defaults to compatible mode which is the standard PC Centronics printer mode in PC computers. The EPP, and ECP modes can only be activated by programming the Extended Control Register (ECR), this requires address bit A10=1, which is outside the normal parallel port address in the ISA I/O space. The internal timing is designed to operate from a 22.1184 MHz clock which is supplied from an external source on pin XTAL1 or by the built-in oscillator circuit with an appropriate crystal.

Optional capabilities of the ECP specification are set as follows:

- ECP defined interrupts are pulsed, low true (Centronics ACK# is non-pulsed, low true).
- PWord size is forced to 1 byte.
- There is 1 byte in the transmitter that does not affect the FIFO full bit (ECP modes).
- RLE compression is not supported in hardware.
- IRQ channel is selectable as 5, 7, or 9.
- DMA channel is selectable as 3.
- FIFO THRESHOLD is set at 8 (used only for non-DMA access to the FIFO).

Port	Address	Read/Write	Mode	Function
DATA	000	R/W	000	Data port
ECP-AFIFO	000	W	011	ECP FIFO (Address)
DSR	001	R	All	Status Register
DCR	002	R/W	All	Control Register
EPP-APort	003	R/W	100	EPP Port (Address)
EPP-DPort	004-007	R/W	100	EPP Port (Data)
C-FIFO	400	W	010	Parallel Port Data FIFO
ECP-DFIFO	400	R/W	011	ECP FIFO (Data)
T-FIFO	400	R/W	110	Test FIFO
Cnfg-A	400	R	111	Configuration Register A
Cnfg-B	401	R-R/W	111	Configuration Register B
ECR	402	R/W	All	Extended Control Register

Table 6. Parallel Data Port Internal Register

STANDARD DEFINITIONS

- Forward direction only.
  Compatible Mode, "Centronics" or standard mode (SPP).

- Reverse direction only.
  Nibble mode:
  4 bits at a time using status lines for data "Hewlett Packard Bi-tronics".

- Bi-directional.
  EPP:
  Enhanced Parallel Port, used primarily by non-printer peripherals.

  ECP:
  Extended Capability Port, used primarily by latest generation of printers, scanners and external storage and CD drives for higher data transfer rate.

DATA REGISTER (DATA)

DATA Bit 0-7:
For host output cycles in SPP mode (ECR mode 000) or PS/2 mode (ECR mode 001), data from the host is registered at the trailing edge of IOW#. On host input cycles, data at the peripheral port is passed through to the host data bus.

ECP FIFO ADDRESS (ECP-AFIFO)

ECP-AFIFO Bit 0-7:
This port is only available for programmed I/O (non-DMA), and only has significance for host write. Data written to this port is stored in the FIFO if FIFO-F = 0 and will be lost if FIFO-F = 1. A 9th FIFO bit (tag) is set low on write. A read from this port is the same as a read at 400.

DATA STATUS REGISTER (DSR)

This status register is read-only except for bit-0, and all bits are latched for the duration of IOR#.

DSR Bit-0:
If EPP mode is not selected, this bit returns logic one. During EPP mode, bit-0 will return a high if the EPP 10 msecond TimeOut elapsed during the last EPP read or write cycle (this TimeOut also aborts the EPP cycle). This status bit is cleared by exiting EPP mode or by the host writing a high to bit-0 of this register.

DSR Bit 1-2:
Reserved, logic one.

DSR Bit-3:
The true state of the ERR# pin.

DSR Bit-4:
The true state of the SELECT pin.

DSR Bit-5:
The true state of the PE pin.

DSR Bit-6:
The true state of the ACK# pin.

DSR Bit-7:
The complement of the BUSY pad.

DATA CONTROL REGISTER (DCR)

DCR Bit-0:
The complement of this bit drives STROBE#, and the complement of the pad state is returned for read.

DCR Bit-1:
The complement of this bit drives AUTOFD#, and the complement of the pad state is returned for read.

DCR Bit-2:
This bit drives INIT#, and the pad state is returned for read.

DCR Bit-3:
The complement of this bit drives SELCTIN#, and the complement of the pad state is returned for read.

DCR Bit-4:
Ack Interrupt Enable set to a high will generate an interrupt when ACK# is low. When either returns to a high state, this interrupt source will go in-active. This interrupt is not pulsed.

DCR Bit-5:
Peripheral port direction, OUT = 0 and IN = 1.
This bit is forced to logic zero by ECR modes 000 or 010. It can be written only in ECR mode 001, and will maintain that state if the ECR mode is changed to 011, 100, or 110. This bit must be set low for EPP mode, which allows the host to control direction with IOR# and IOW#. The final port direction also drives PDIR.

DCR Bits 6-7:
Reserved, logic zero.

EPP ADDRESS PORT (EPP-APort)

When EPP mode is enabled, a host read or write with this port will result in a data transfer directly to/from the peripheral with SLCTIN# active. Direction is set by host read/write and will drive STROBE# low during a write if DCR bit 5 (DIR) is not set high.

EPP DATA PORT (EPP-DPort)

When EPP mode is enabled, a host read or write with this port will result in a data transfer directly to/from the peripheral with AUTOFD# active. Direction is set by host read/write and will drive STROBE# low during a write if DCR bit 5 (DIR) is not set high.

PARALLEL PORT DATA (C-FIFO)

This port is available for programmed I/O and DMA access. Data written to this port is stored in the FIFO if FIFO-F = 0 and will be lost if FIFO-F = 1.

Data written to this port will be automatically transferred to the peripheral with STROBE# handshaking with BUSY. This port is only defined for write, host reads will interfere with FIFO read sequencing.

ECP DATA FIFO (ECP-DFIFO)

This port is available for programmed I/O and DMA access. Data written to this port is stored in the FIFO if FIFO-F = 0 and will be lost if FIFO-F = 1. A 9th FIFO bit (tag) is set high on write.

Data read from this port will undergo de-compression if the FIFO tag bit and data bit-7 are both low. The byte containing the RLE count is loaded into the RLE counter and the succeeding byte in the FIFO will be returned to the host RLE count + 1 times before the FIFO read address is incremented. If a FIFO under-run is incurred during host read, the last data byte is returned and FIFO-E remains coherent.

TEST FIFO (T-FIFO)

This port is available for programmed I/O and DMA access. Data written to this port is stored in the FIFO if FIFO-F = 0 and will be lost if FIFO-F = 1. During a read cycle from this port a FIFO under-run will return last data read and FIFO-E remains coherent.

CONFIGURATION REGISTER A (Cnfg-A)

This read-only register is available in ECR mode 111 only.

Cnfg-A Bit 0-1:
Forced to logic zero, this field is don't care for PWord = 1 byte.

Cnfg-A Bit-2:
When transmitting, there is 1 byte waiting to be transmitted that does not affect FIFO-F.

Cnfg-A Bit-3:
Reserved, logic zero.

Cnfg-A Bit 4-6:
Indicates PWord = 1 byte (8-bit implementation).

Cnfg-A Bit-7:
Indicates ECP interrupts are pulsed.

CONFIGURATION REGISTER B (Cnfg-B)

This register is available in ECR mode 111 only, and returns bits 0-5 as logic zero.

Cnfg-B Bit 0-2:
In the PnP mode the DMA channel is assigned through auto configuration. It defaults to DMA 3 in the manual mode.

OW#	IOR#	DMA
X00	000	3
X01	001	3
X10	010	3
X11	011	3 (default)

Cnfg-B Bit 3-5:
In the PnP mode IRQ assignment is made through auto configuration. Manual mode defaults to IRQ 7.

IOW#	IOR#	IRQ
000	001	7
001	001	7 (default)
010	010	7
011	001	7
100	001	7
101	001	7
110	001	7
111	111	7

Cnfg-B Bit-6:
Returns the true value of the selected IRQ pad.

Cnfg-B Bit-7:
Indicates RLE compression is not supported.

EXTENDED CONTROL REGISTER (ECR)

The Extended Control Register has a system RESET state of 10010101. The significance of the bits is defined by the ECP specification as:

ECR Bit-0:
This read-only bit returns FIFO empty status (FIFO-E) and is forced high unless PPF, ECP, or TST mode is selected.

0 = At least one byte of data contains in the FIFO.
1 = FIFO is empty.

ECR Bit-1:
This read-only bit returns FIFO full status (FIFO-F) and is forced low unless PPF, ECP, or TST mode is selected.

0 = At least one empty location is available in the FIFO.
1 = FIFO is full.

ECR Bit-2:
When low, this bit (ServiceIntr) enables a pulsed interrupt and enables DMA requests (if bit-3 is set). If the enabled interrupt occurs, this bit is automatically returned to a high. The interrupt conditions are:

ECR Bit-3 = DMA

DCR Bit-5 = DIRection

DMA	DIR	CONDITION
0	0	8 empty bytes in the FIFO
0	1	8 filled bytes in the FIFO
1	X	DMA Terminal Count (TC)

ECR BIT-3:
This bit disables DMA when set low. When set high, a low on ServiceIntr will enable DMA requests.

0 = DMA disabled, DRQx pin is three-stated.
1 = DMA enabled

ECR Bit-4:
When low, this bit (ErrIntrEn#) enables a pulsed interrupt if ERR# (Fault#) is low. The interrupt is only enabled in ECP mode.

ECR Bit 5-7:
This field can be set to any value if the current value is 000 or 001. If the current value is not 000 or 001, then the field can only be written to 000 or 001. The modes are defined as:

Mode	Name	Description
000	SPP	Standard, output only. DCR bit-5 is forced to "0".
001	PS2	Bi-directional PS/2 parallel port. FIFO is disabled
010	PPF	FIFOed, output only. DCR bit-5 is forced to "0".
011	ECP	ECP FIFOed port with RLE decompression. FIFO direction is controlled by DCR Bit-5.
100	EPP	EPP mode.
101	-	reserved
110	TST	FIFO test mode. FIFO is accessible via TFIFO register.
111	CFG	Configuration A/B register enable.

OPERATION

SPP MODE

This is ECR mode 000 (system RESET mode).
In this output-only mode the host data is registered to PD[7:0] at the trailing edge of IOW#; PDIR is driven low; STROBE#, AUTOFD#, INIT#, and SELCTIN# are open-drain; and all timing is managed by the host through DSR and DCR registers.

PS2 MODE

This is ECR mode 001.
In this bi-directional mode the host output data is registered to PD[7:0] at the trailing edge of IOW#, PDIR is driven by DIR to allow peripheral data input, AUTOFD#, INIT#, and SELCTIN# are totem-pole, and all timing is managed by the host through DSR and DCR registers.

PPF MODE

This is ECR mode 010.
In this output-only mode the host data is written to the FIFO with I/O writes to address 400 or by DMA writes; PDIR is driven low. FIFO data is automatically registered to PD[7:0] whenever the FIFO-E bit is low (data available), and timing is generated by controller logic that handshakes STROBE# (controller) with BUSY (peripheral).

ECP MODE

This is ECR mode 011.
In this bi-directional mode the host data is written to the FIFO with I/O writes to address 000, 400 or DMA; PDIR is driven by DIR (can only be set in ECR mode 001); AUTOFD#, INIT, and SELCTIN# are totem-pole. I/O writes to address 000 will write a low into the FIFO tag bit, while I/O writes to address 400 or DMA will insert a high.

ECP FORWARD MODE (PDIR = 0)

FIFO data is automatically registered to PD[7:0] whenever the FIFO-E bit is low (data available), and timing is generated by controller logic that handshakes STROBE# (controller) with BUSY (peripheral). Data from the FIFO tag bit is output on AUTOFD# after being registered simultaneous with FIFO data.

ECP REVERSE MODE (PDIR = 1)

PD[7:0] data and BUSY are latched into the FIFO and tag bit respectively at the trailing edge of AUTOFD# if FIFO-F = 0. Timing is generated by controller logic that handshakes ACK# (peripheral) with AUTOFD# (controller).

EPP MODE

This is ECR mode 100.
In this bi-directional mode, I/O writes will latch host output data at the trailing edge of IOW#, and peripheral input data will be latched at the trailing edge of SELCTIN# or AUTOFD#. PDIR, and STROBE# are driven by the state of IOW# (DCR bits 5 and 0 must be set low).

EPP mode allows buffered access between the PC bus and the peripheral with timing provided by the peripheral via BUSY handshake into IOCHRDY. I/O cycles with address 003 - 007 will immediately drive IOCHRDY low. STROBE# will go low and PD[7:0] is allowed to change (write cycles) after BUSY has been low for at least 60n second. (This delay may have elapsed prior to cycle initiation). It is immediately followed by a low driven on SELCTIN# for address 003 or AUTOLF# (DATASTB*) for address 004 - 007 (read and write cycles). When BUSY returns high for a minimum of 60n second, IOCHRDY and the active strobe will be driven high -allowing the host to complete the I/O transaction.

To prevent a system stall, a 10 msecond TimeOut aborts the cycle if it expires before BUSY returns high. This TimeOut also sets bit 0 of DCR, which is cleared by disabling EPP mode or writing a high to DCR bit 0.

TST MODE

This is ECR mode 110.
This mode allows data to be transferred (read or write in any direction) between the FIFO and host at address 400 or DMA without activating the control interface (no data is transferred to/from the peripheral). PDIR is driven by DIR (can only be set in ECR mode 001).

Performing I/O cycles in this mode allows software to test for the value of FIFOThreshold (FT) for both output and input directions.

CFG MODE

This is ECR mode 111.
This mode enables I/O access to the configuration registers CONF-A and CONF-B and disables I/O access to the FIFO.

IRQ

The module has four sources of interrupt which may be directed to IRQ5, IRQ7, IRQ9 (see CONF-B). In PnP mode IRQ assignment is made through auto configuration.

1) When DCR bit 4 (AIE) is high and ACK# is low the interrupt is active.

2) When ECP mode is active, if ECR bit 4 is low when ERROR transitions low or ECR bit 4 transitions low when Fault# is low an interrupt pulse of at least 200n seconds will be generated.

3) In FIFO modes (PPF, ECP, or TST) with ECR bit 3 (DMA) low, an interrupt pulse of at least 200n seconds will be generated when ECR bit 2 (SI) is set low if there are at least 8 empty bytes in the FIFO and PDIR = 0 or there are at least 8 filled bytes in the FIFO and PDIR = 1. This interrupt will automatically disable itself by setting ECR bit 2 high.

4) In FIFO modes (PPF, ECP, or TST) with (DMA request enabled), an interrupt pulse of at least 200n seconds will be generated when TC is received if PD-ACK is low. This interrupt will automatically disable itself and the DMA request by setting ECR bit 2 high.

DMA

DMA cycles occur only between the host and the FIFO data port (address 400) for PPF, ECP, or TST modes. DRQ(1, 2, or 3) is selected through auto configuration in PnP mode and they will be driven high if ECR bit 3 (DMA) is high and ECR bit 2 (SI) is low when {PDIR = 0 and FIFO-F = 0} or {PDIR = 1 and FIFO-E = 0} or TST mode is active. Manual mode defaults to DRQ3.

When the selected DACKn#(1, 2, or 3) is low, IOW# will transfer host data to the FIFO and IOR# will transfer FIFO data to the host. The selected DREQn will be driven low to terminate the DMA channel when {PDIR = 0 and FIFO-F = 1} or {PDIR = 1 and FIFO-E = 1} or ECR bit 2 (SI) goes high (interrupt condition 4 above) or more than 32 consecutive DMA data cycles (read or write) have occurred.

FIFO-F and FIFO-E terminated cycles will automatically restart when their state returns low. Consecutive cycle termination will automatically restart because the counter is reset when the selected DACKn# goes high. TC terminated cycles can only be restarted by the host setting ECR bit 2 (SI) low again.

RLE

The module does not support Run Length Encoding (RLE) compression (indicated by the "0" in CONF-B bit 7) but does support RLE de-compression on the receiving side.

The host may send compressed data to the peripheral by writing the RLE length byte (bit 7 = 0) to address 000 (NOTE: DMA cannot be used for this byte) which will place a zero into the FIFO tag bit. This must be followed immediately by the data byte being written to the FIFO at address 400. These bytes will be transferred to the peripheral in the normal manner.

De-compression takes place if PDIR = 1 when data is read from the FIFO at address 000, 400 or DMA. When a byte is read from the FIFO, bits 0-6 (length) are placed in a counter if data bit-7 and the FIFO tag bit are both low. The subsequent byte in the FIFO (data) is presented to the host count + 1 times before the FIFO read pointer is advanced.

A10	A2 A1 A0	Register	D7	D6	D5	D4	D3	D2	D1	D0
0	0 0 0	Data ECP-AFIFO	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
0	0 0 1	DSR	Busy	ACKE	PE	Select	ERR#	1	1	1
0	0 1 0	DCR	0	0	DIR	INT enable	SelectIN#	INIT#	AutoFD#	Strobe#
0	0 1 1	EPP-APort	AP-7	AP-6	AP-5	AP-4	AP-3	AP-2	AP-1	AP-0
0	1 0 0	EPP-DPort	PDA-7	PDA-6	PDA-5	PDA-4	PDA-3	PDA-2	PDA-1	PDA-0
0	1 0 1	EPP-DPort	PDB-7	PDB-6	PDB-5	PDB-4	PDB-3	PDB-2	PDB-1	PDB-0
0	1 1 0	EPP-DPort	PDC-7	PDC-6	PDC-5	PDC-4	PDC-3	PDC-2	PDC-1	PDC-0
0	1 1 1	EPP-DPort	PDD-7	PDD-6	PDD-5	PDD-4	PDD-3	PDD-2	PDD-1	PDD-0
1	X 0 0	CONF-A	ECP INT type	0	0	1	0	FIFO-F	0	0
1	X 0 1	CONF-B	RLE	IRQ input	IRQ Sel-2	IRQ Sel-1	IRQ Sel-0	DMA Sel-2	DMA Sel-1	DMA Sel-0
1	X 1 0	ECR	Mode Sel-2	Mode Sel-1	Mode Sel-0	Fault enable	DMA En/Dis	Service INT	FIFO full	FIFO empty

Table 7. 1284 Control Register Description

Signal Name	Signal Type	Description
STROBE#	O	Active low. Indicates valid data is on the data lines.
AUTOFD#	O	Active low. Instructs the printer to automatically insert a line feed for each carriage return.
SELCTIN#	O	Active low. Used to indicate to the printer that it is selected.
INIT#	O	Active low. Used to reset the printer.
ACK#	I	A low asserted pulse used to indicate that the last character was received.
BUSY	I	A high signal asserted by the printer to indicate that it is busy and cannot take data.
PE	I	A high signal indicates that printer paper is empty.
SELECT	I	A high signal indicates that printer is online.
ERR#	I	Asserted low to indicate that some error condition exists.
PD0-PD7	O	Data.

Table 8. Centronics, SPP Signal Description

Signal Name	Signal Type	Nibble mode Name	Description
STROBE#	O	STROBE#	Not used for reverse data transfer.
AUTOFD#	O	HostBusy	Host nibble mode handshake signal. Set low to indicate host is ready for nibble. Set high to indicate nibble has been received.
SELCTIN#	O	1284Active	Set high when host is in a 1284 transfer mode.
INIT#	O	INIT#	Not used for reverse data transfer.
ACK#	I	PtrClk	Set low to indicate valid nibble data, set high in response to “HostBusy” going high.
BUSY	I	PtrBusy	Used for Data Bit-3, then Bit-7.
PE	I	AckDataReq	Used for Data Bit-2, then Bit-6.
SELECT	I	Xflag	Used for Data Bit-1, then Bit-5.
ERR#	I	DataAvail#	Used for Data Bit-0, then Bit-4.
PD0-PD7	O		Not used.

Table 9. Nibble Mode Signal Description

Nibble Mode Data Transfer Cycle

1. Host signals ability to take data by asserting HostBusy low.
2. Peripheral responds by placing first nibble on status lines.
3. Peripheral signals valid nibble by asserting PtrClk low.
4. Host sets HostBusy high to indicate that it has received the nibble and is not ready for another nibble.
5. Peripheral sets PtrClk high to acknowledge host.

Signal Name	Signal Type	EPP mode Name	Description
STROBE#	O	Write#	Active low. Indicates a write operation, high for a read cycle.
AUTOFD#	O	DataStb#	Active low. Indicates a Data-Read or Data-Write operation is in process.
SELCTIN#	O	AddrStb#	Active low. Indicates an Address-Read or Address-Write operation is in process.
INIT#	O	Reset#	Active low. Peripheral reset.
ACK#	I	Intr#	Peripheral interrupt. Used to generate an interrupt to the host.
BUSY	I	Wait#	Handshake signal. When low it indicates that is okay to start a cycle, when high it indicates that it is okay to end the cycle.
PE	I	User defined	Not used.
SELECT	I	User defined	Not used.
ERR#	I	User defined	Not used.
PD0-PD7	O	AD0-AD7	Bi-directional address / data lines.

Table 10. EPP Mode Signal Description

EPP Mode Data Transfer Cycle

1. Program executes an I/O write cycle to EPP Data Port-4.
2. The Write# line is asserted and the data is output to the parallel port.
3. The DataStb# is asserted, since Write# is asserted low.
4. The port waits for the acknowledge from the peripheral, Write# deasserted.
5. The DataStr# is deasserted and EPP cycle ends.
6. Write# is asserted low to indicate that the next cycle may begin.

Signal Name	Signal Type	ECP mode Name	Description
STROBE#	O	HostClk	Used with PeriphAck to transfer data or address information in the forward direction.
AUTOFD#	O	HostAck	Provides Command / Data status in the forward direction. Used with PeriphClk to transfer data in the reverse direction.
SELCTIN#	O	1284Active	Set high when host is in a 1284 transfer mode.
INIT#	O	ReverseReq#	Driven low to put the channel in reverse direction.
ACK#	I	PeriphClk	Used with HostAck to transfer data in the reverse direction.
BUSY	I	PeriphAck	Used with HostClk to transfer data or address information in the forward direction. Provides Command / Data status in the reverse direction.
PE	I	AckReverse#	Driven low to acknowledge ReverseRequest.
SELECT	I	Xflag	Extensibility flag.
ERR#	I	PeriphReq#	Set low by peripheral to indicate that reverse dat is available.
PD0-PD7	I/O	D0-D7	Bi-directional data lines.

Table 11. ECP Mode Signal Description

ECP Mode Forward Data and Command Transfer Cycle

1. Host places data on the data lines and indicates a data cycle by setting HostAck high.
2. Host asserts HostClk low to indicate valid data.
3. Peripheral acknowledge host by setting PeriphAck high.
4. Host sets HostClk high. This is the edge that should be used to clock the data in to the peripheral.
5. Peripheral sets PeriphAck low to indicate that it is ready for the next byte.
6. The cycle repeats, but this time it is command cycle because HostAck is low.

ECP Mode Reverse Data and Command Transfer Cycle

1. The Host requests a reverse channel transfer by setting ReverseReq# low.
2. The peripheral signals that it is okay to proceed by setting AckReverse# low.
3. The peripheral places data on the data lines and indicates a data cycle by setting PeriphAck high.
4. Peripheral asserts PeriphClk low to indicate valid data.
5. Host acknowledges by setting HostAck high.
6. Peripheral sets PeriphClk high. This is the edge that should be used to clock the data in to the host.
7. Host sets HostAck low to indicate that it is ready for the next byte.
8. The cycle repeats, but this time it is a Command cycle because PeriphAck is low.

UART Registers Reset Conditions

Register	Reset State
RHR	0xXX, X=random
THR	0xXX, X=random
IER	0x00
FCR	0x00
ISR	0x01
LCR	0x00
MCR	0x00
LSR	0x60
MSR	0xX0, X=state of input pins
SPR	0xFF
DLL	0xXX, X=random
DLM	0xXX, X=random
TRG	0x00
FCTR	0x00
EFR	0x00
Xon-1	0x00
Xon-2	0x00
Xoff-1	0x00
Xoff-2	0x00
EMSR	0x00

Output Signals	Reset State
TX A-B	logic 1
RTS# A-B	logic 1
DTR# A-B	logic 1

1284 Controller Register Reset Conditions

Register	Reset State
ECP-AFIFO	
DSR	0xXX, X=state of input pins
DCR	Bit 0-4=0
EPP-APort	
EPP-DPortA	
EPP-DPortB	
EPP-DPortC	
EPP-DPortD	
CONF-A	Bit 0-7=0
CONF-B	Bit 0-5=0
ECR	0x95

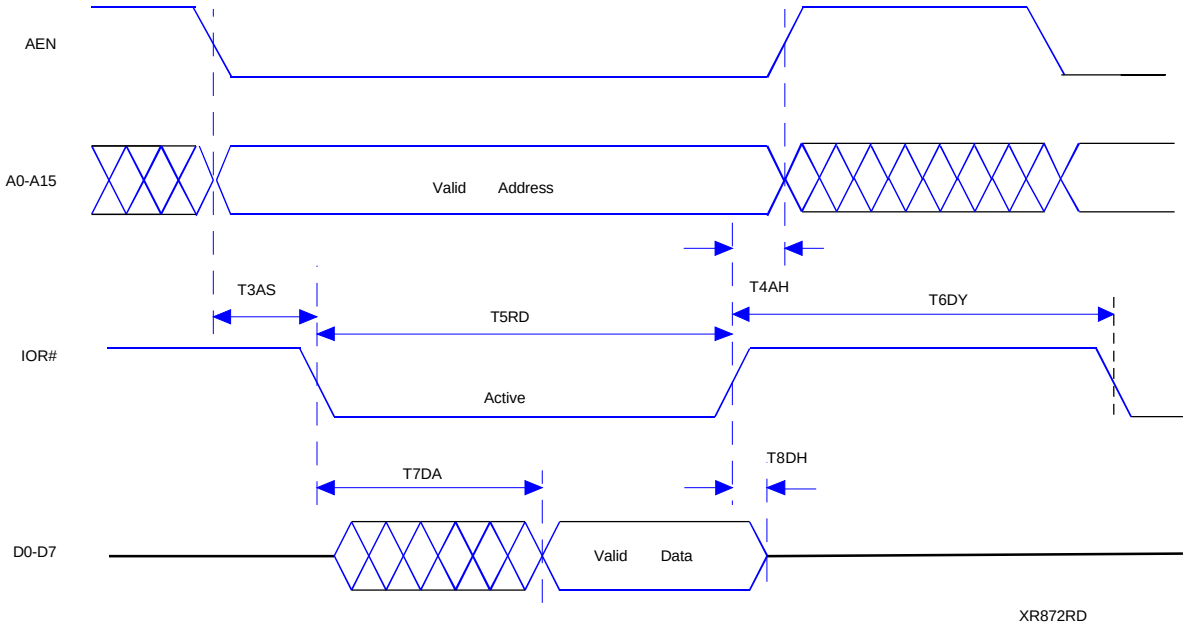


Figure 8. ISA Bus Read Timing

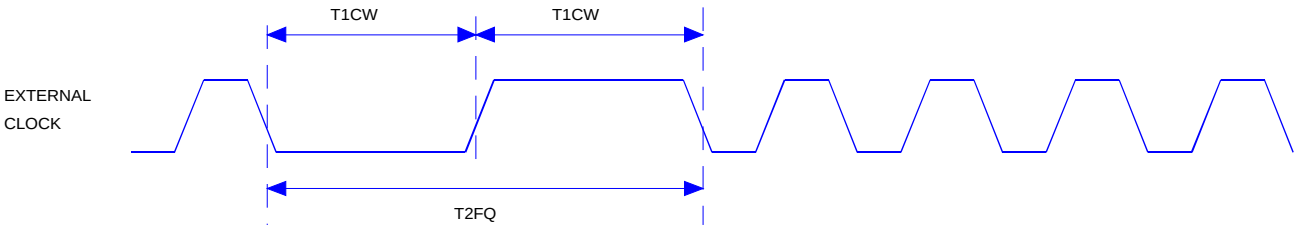


Figure 9. External Clock Timing

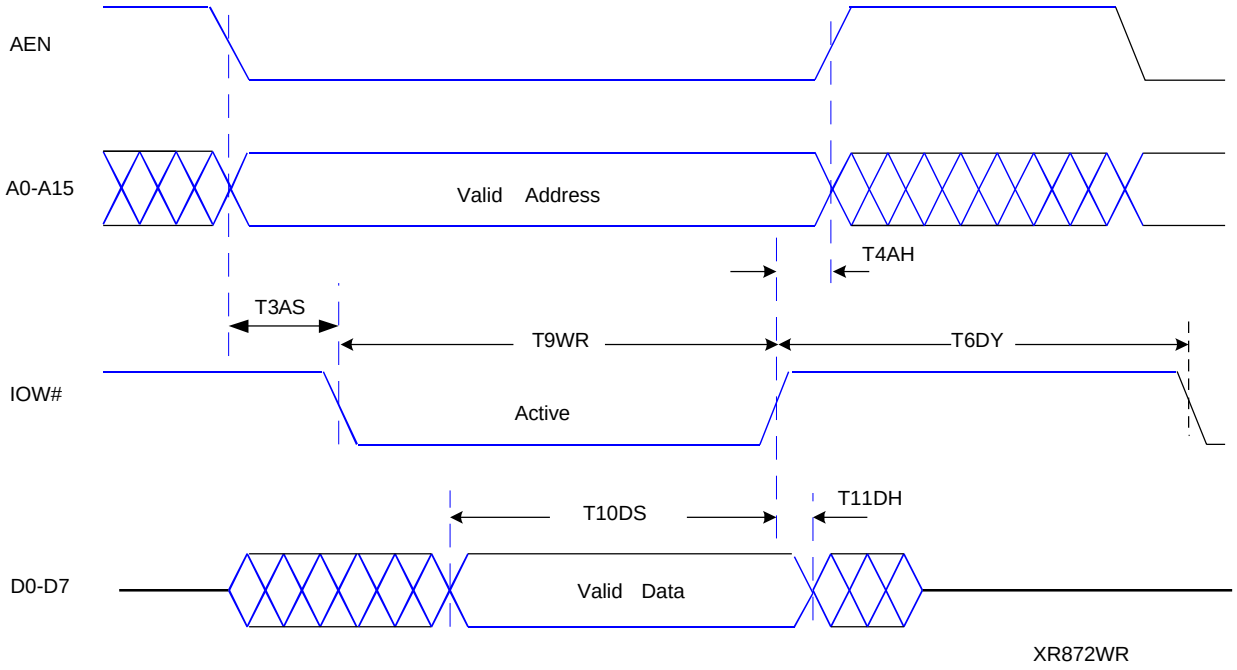


Figure 10. ISA Bus Write Timing

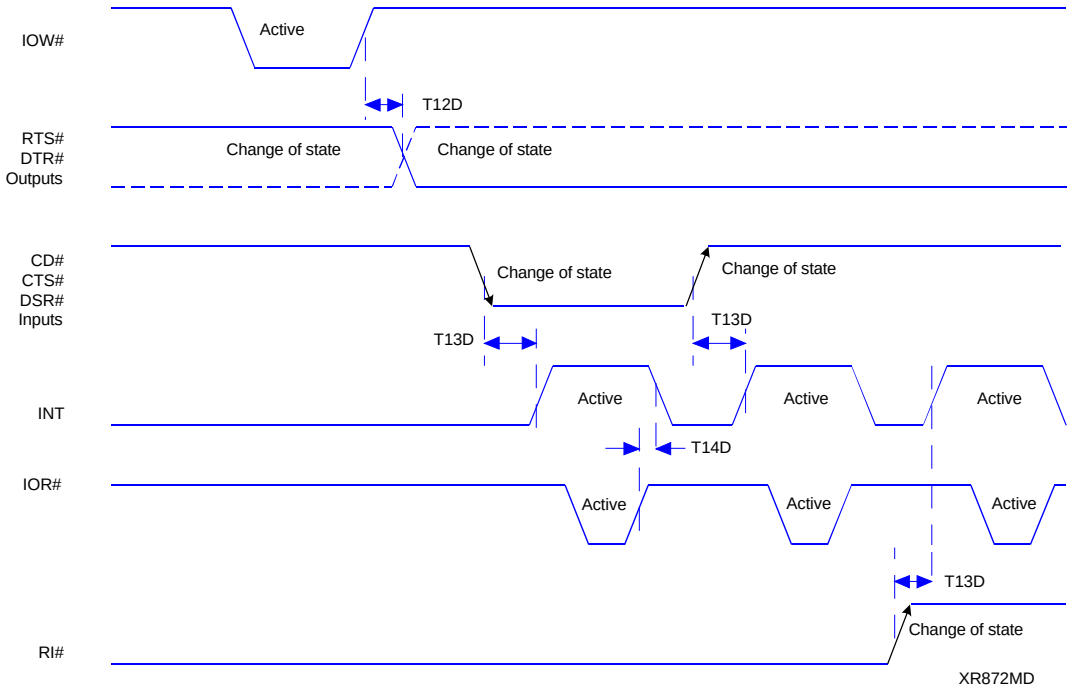


Figure 11. Modem Input/Output Timing

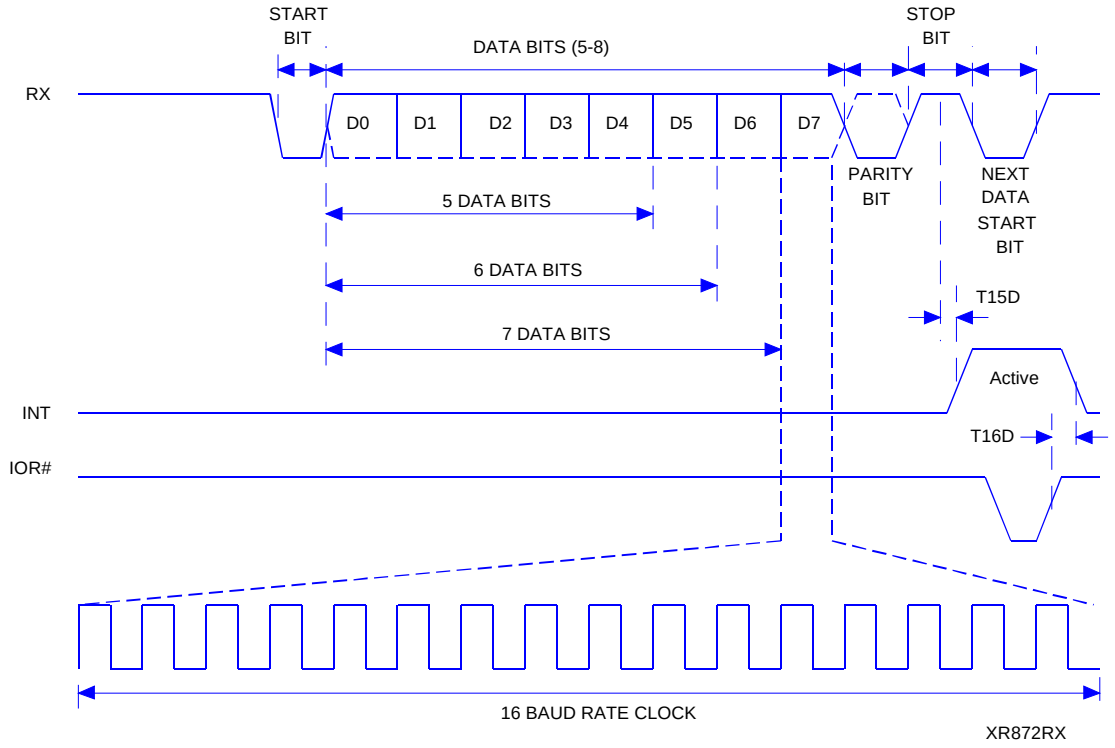


Figure 12. Receive Data Timing in DMA Mode 0

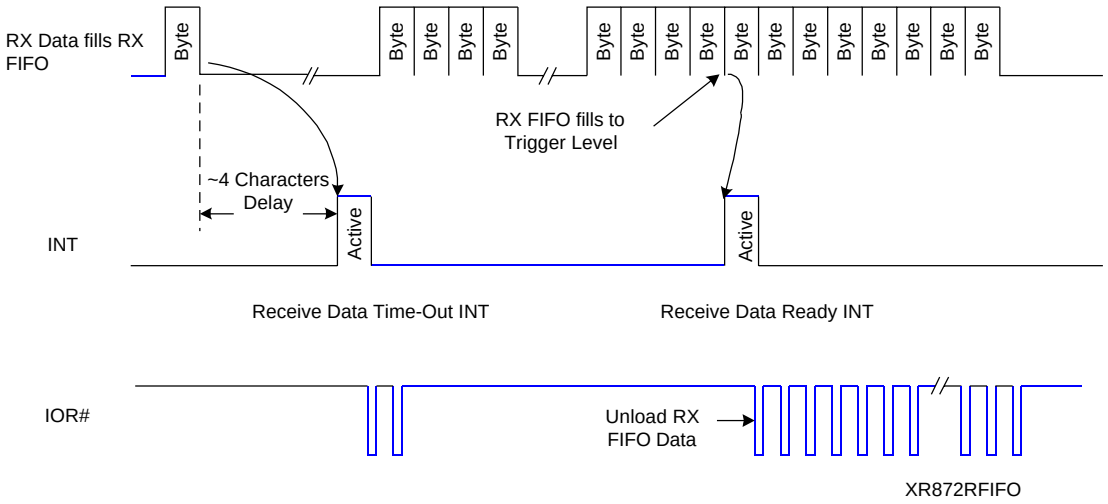


Figure 13. Receive Data Timing in FIFO and DMA Mode 1

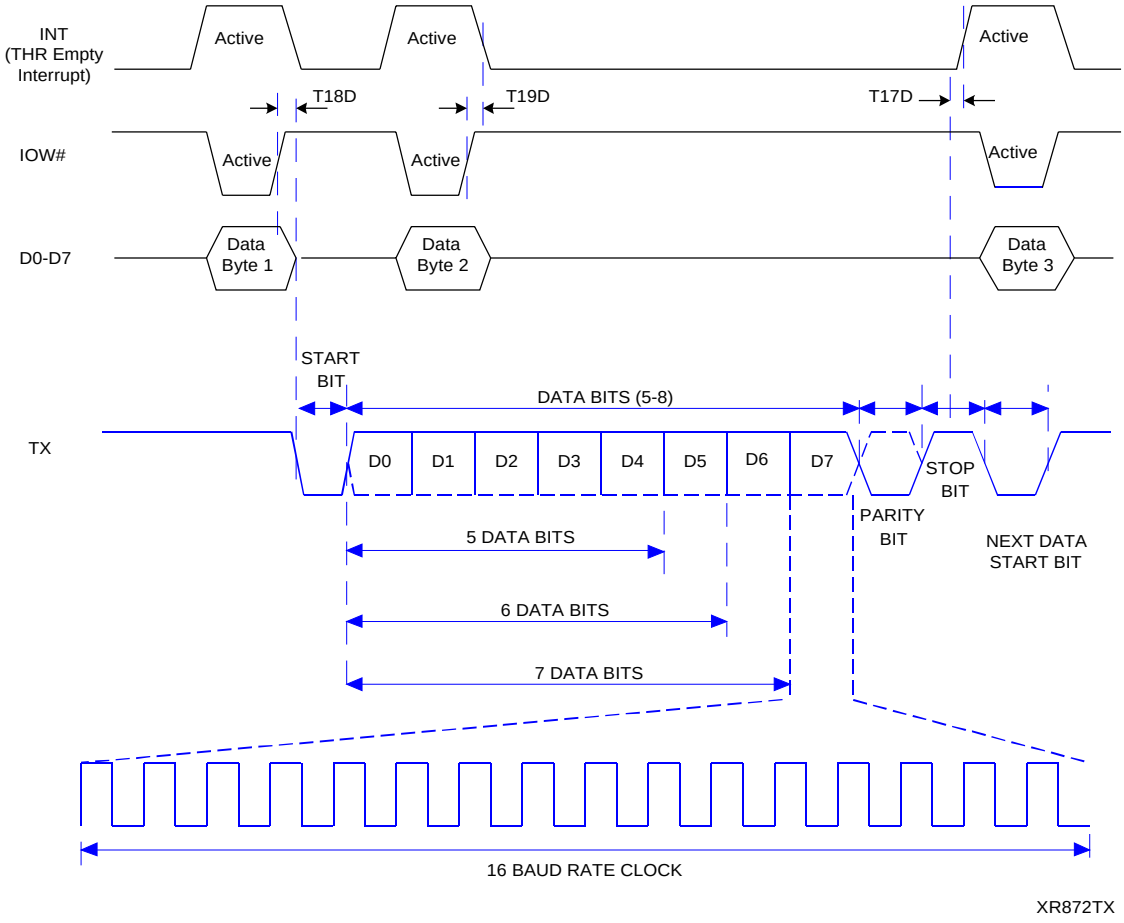


Figure 14. Transmit Data Timing

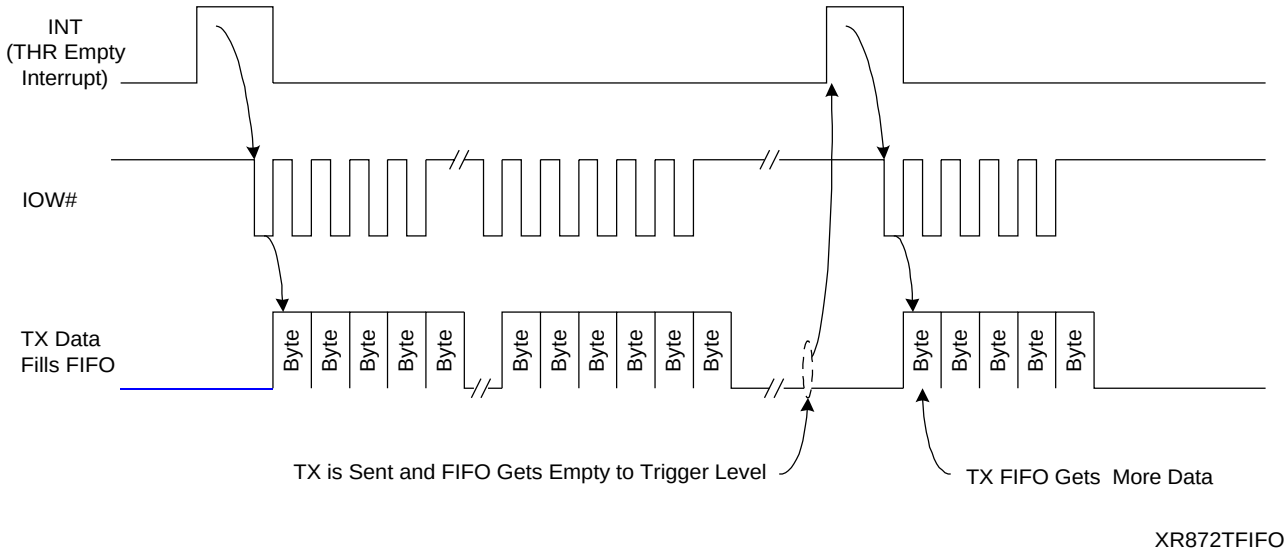


Figure 15. Transmit FIFO Operation

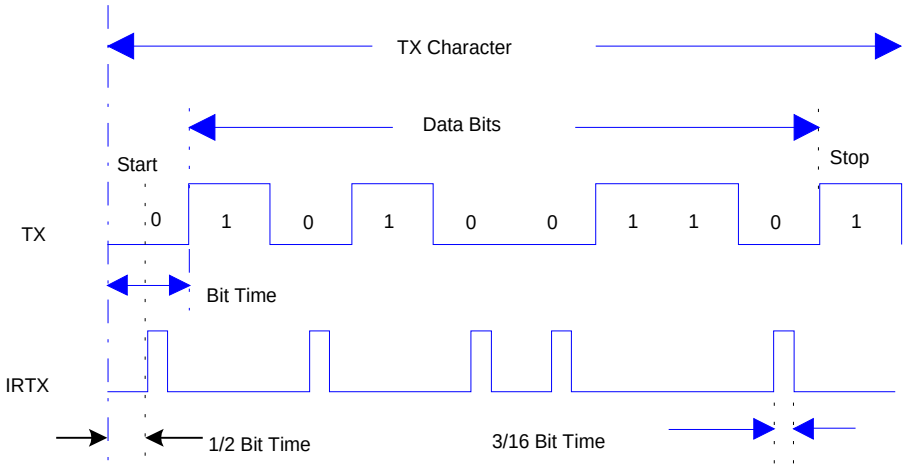


Figure 16. Infrared Transmit Timing

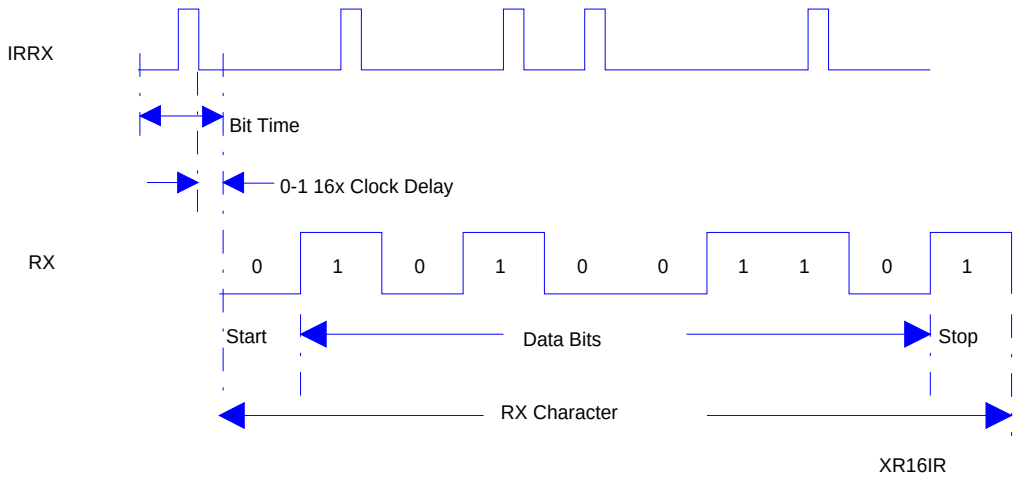


Figure 17. Infrared Receive Timing

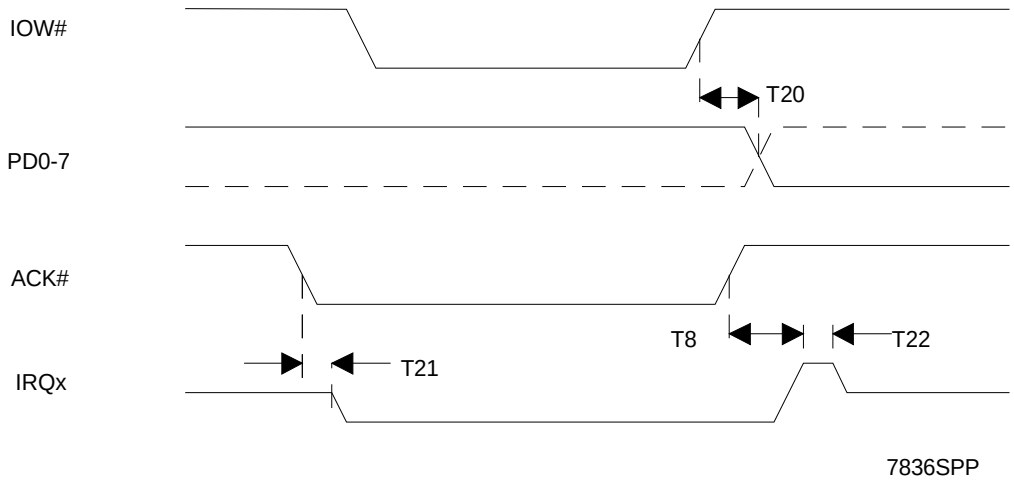


Figure 18. Parallel Port Timing in SPP, PS/2 Mode

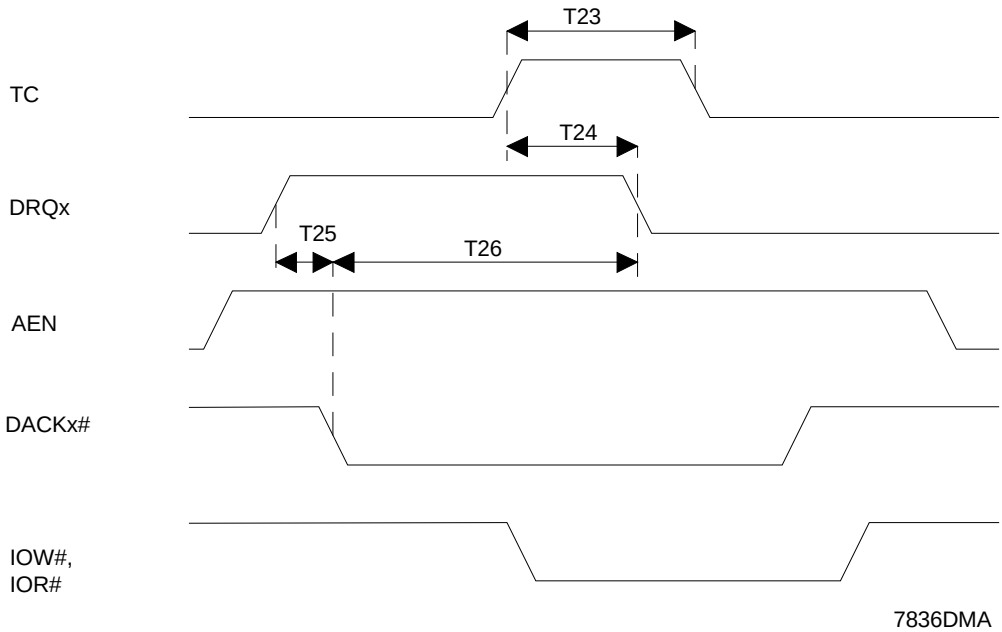


Figure 19. Host DMA Timing in ECP Mode

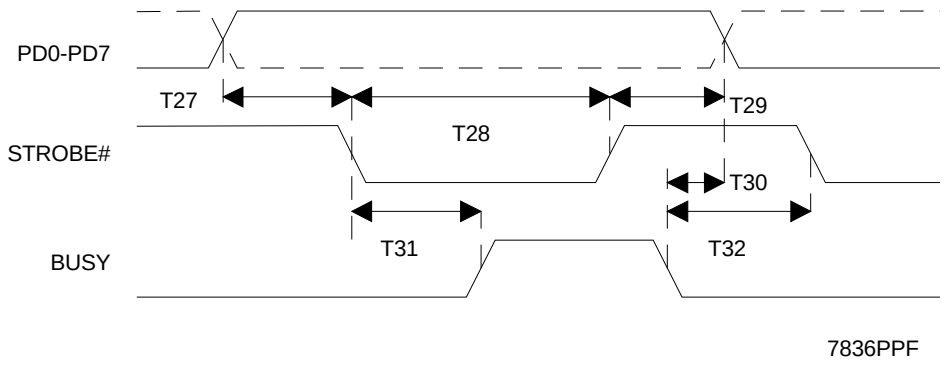


Figure 20. Parallel Port FIFO Timing

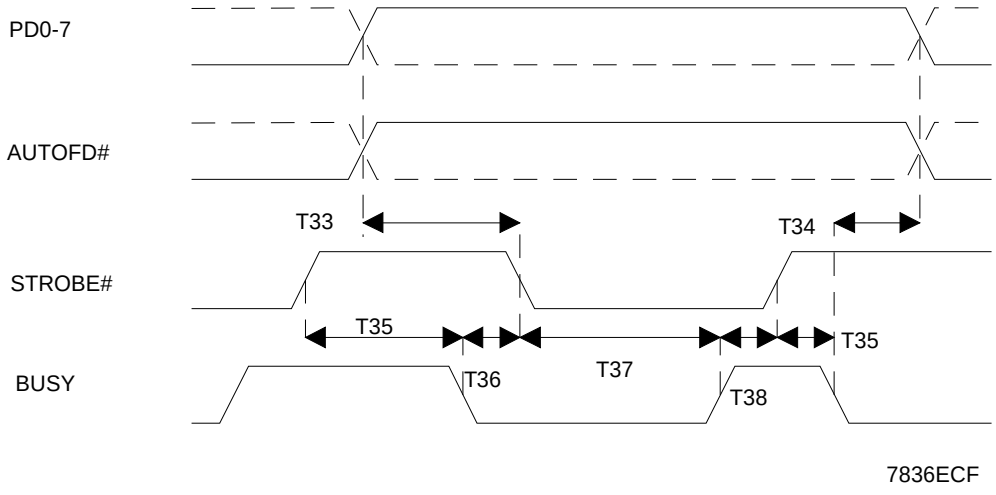


Figure 21. Parallel Port Forward Timing in ECP Mode

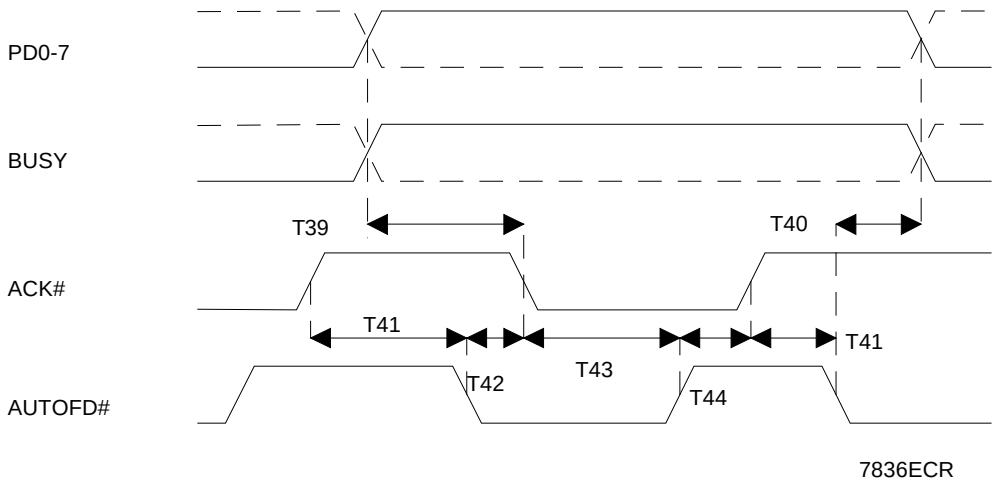


Figure 22. Parallel Port Reverse Timing in ECP Mode

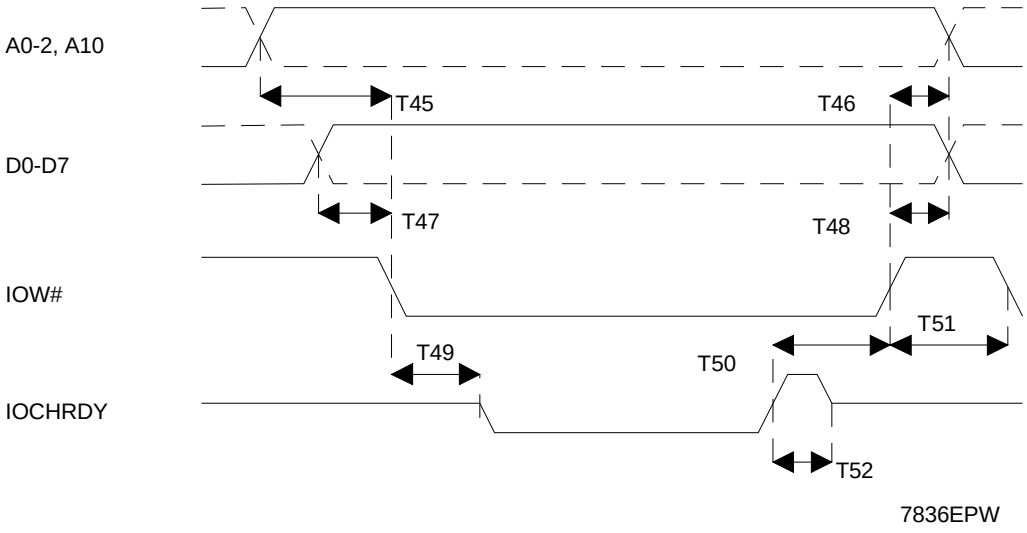


Figure 23. Address or Data Write Timing in EPP Mode

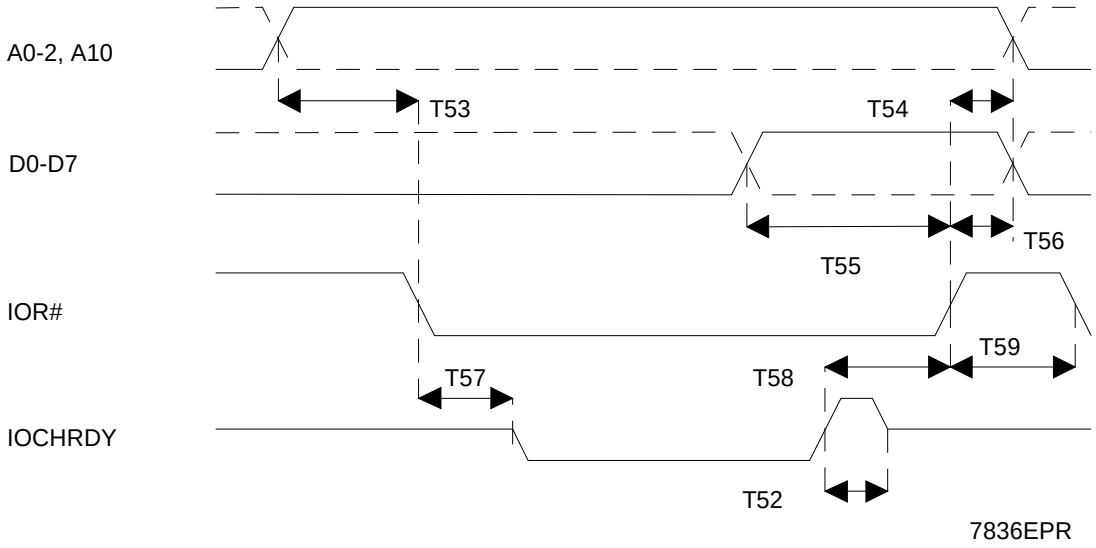
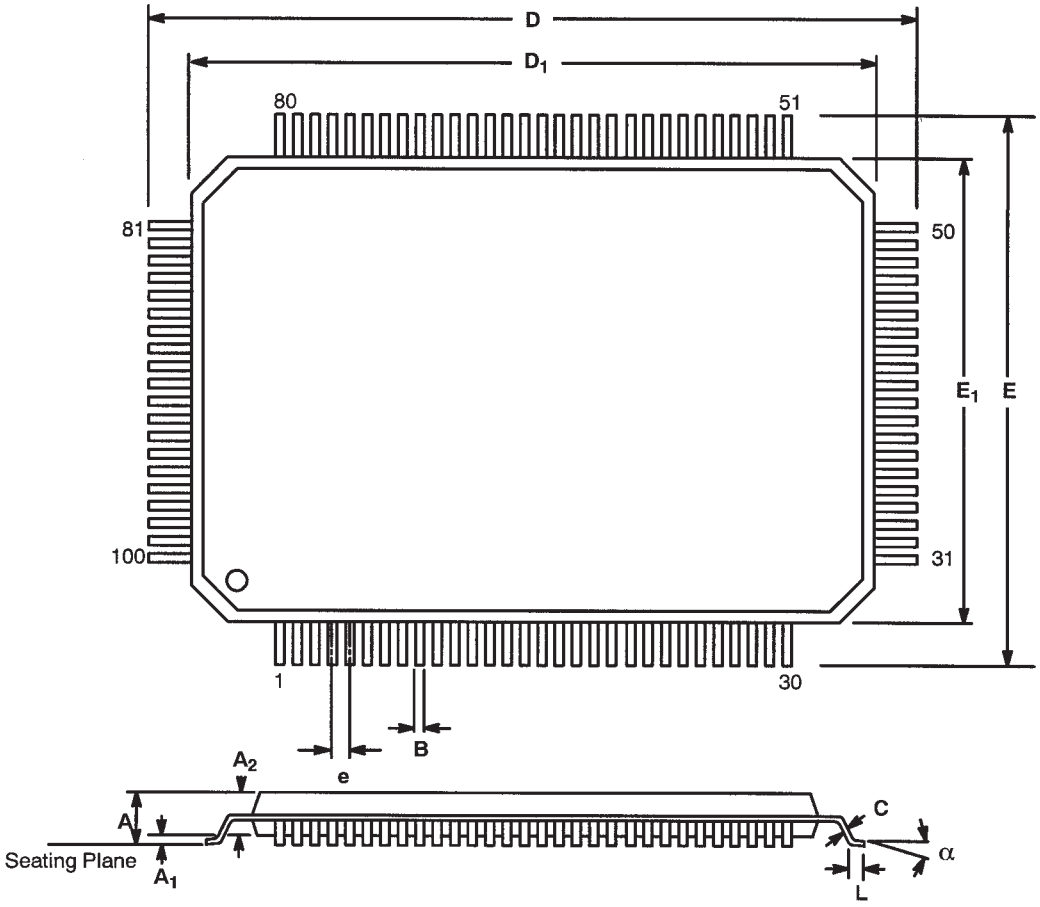


Figure 24. Address or Data Read Timing in EPP Mode

100 LEAD PLASTIC QUAD FLAT PACK (14 mm x 20 mm, QFP)

Rev. 2.00



1.95 mm Form

SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.102	0.134	2.60	3.40
A_1	0.002	0.014	0.05	0.35
A_2	0.100	0.120	2.55	3.05
B	0.009	0.015	0.22	0.38
C	0.005	0.009	0.13	0.23
D	0.931	0.951	23.65	24.15
D_1	0.783	0.791	19.90	20.10
E	0.695	0.715	17.65	18.15
E_1	0.547	0.555	13.90	14.10
e	0.0256 BSC		0.65 BSC	
L	0.026	0.037	0.65	0.95
α	0°	7°	0°	7°

Note: The control dimension is the millimeter column

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