



512Kx16 SRAM/FLASH MODULE, SMD 5962-96901

FEATURES

- Access Times of 35ns (SRAM) and 90ns (FLASH)
- Access Times of 70ns (SRAM) and 120ns (FLASH)
- Packaging
 - 66 pin, PGA Type, 1.385" square HIP, Hermetic Ceramic HIP (Package 402)
 - 68 lead, Hermetic CQFP (G2), 22mm (0.880") square (Package 500). Designed to fit JEDEC 68 lead 0.990" CQFJ footprint (Fig. 2)
- 512Kx16 SRAM
- 512Kx16 5V FLASH
- Organized as 512Kx16 of SRAM and 512Kx16 of Flash Memory with separate Data Busses
- Both blocks of memory are User Configurable as 1Mx8
- Low Power CMOS
- Commercial, Industrial and Military Temperature Ranges
- TTL Compatible Inputs and Outputs
- Built-in Decoupling Caps and Multiple Ground Pins for Low Noise Operation
- Weight - 13 grams typical

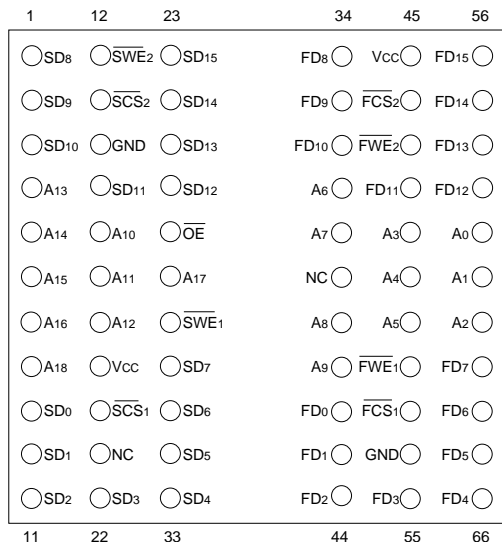
FLASH MEMORY FEATURES

- 100,000 Erase/Program Cycles
- Sector Architecture
 - 8 equal size sectors of 64K bytes each
 - Any combination of sectors can be concurrently erased. Also supports full chip erase
- 5 Volt Programming; 5V ± 10% Supply
- Embedded Erase and Program Algorithms
- Hardware Write Protection
- Page Program Operation and Internal Program Control Time.

Note: Programming information available upon request.

FIG. 1 PIN CONFIGURATION FOR WSF512K16-XH2X

TOP VIEW



PIN DESCRIPTION

FD0-15	Flash Data Inputs/Outputs
SD0-15	SRAM Data Inputs/Outputs
A0-18	Address Inputs
SWE1-2	SRAM Write Enable
SCS1-2	SRAM Chip Selects
OE	Output Enable
Vcc	Power Supply
GND	Ground
NC	Not Connected
FWE1-2	Flash Write Enable
FCS1-2	Flash Chip Select

BLOCK DIAGRAM

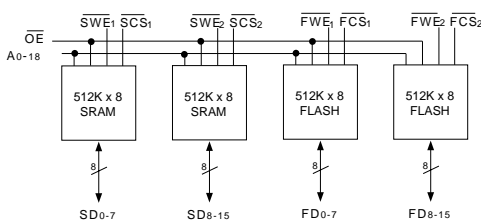
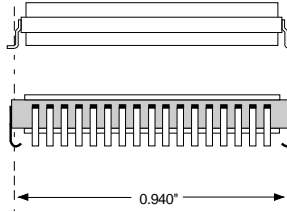
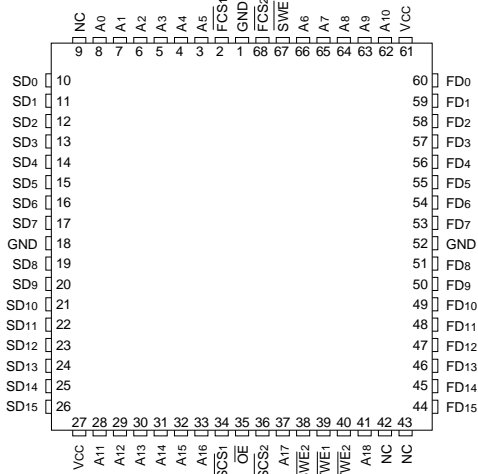




FIG. 2 PIN CONFIGURATION FOR WSF512K16-XG2X

TOP VIEW

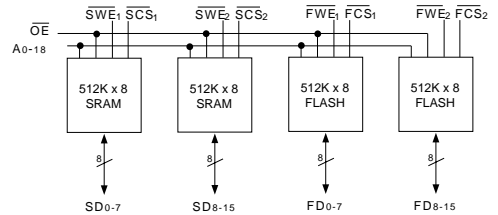


The WEDC 68 lead G2 CQFP fills the same fit and function as the JEDEC 68 lead CQFJ or 68 PLCC. But the G2 has the TCE and lead inspection advantage of the CQFP form.

PIN DESCRIPTION

FD0-15	Flash Data Inputs/Outputs
SD0-15	SRAM Data Inputs/Outputs
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SWE1-2	SRAM Write Enable
SCS1-2	SRAM Chip Selects
OE	Output Enable
VCC	Power Supply
GND	Ground
NC	Not Connected
FWE1-2	Flash Write Enable
FCS1-2	Flash Chip Select

BLOCK DIAGRAM





ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Unit
Operating Temperature	T _A	-55	+125	°C
Storage Temperature	T _{STG}	-65	+150	°C
Signal Voltage Relative to GND	V _G	-0.5	7.0	V
Junction Temperature	T _J		150	°C
Supply Voltage	V _{CC}	-0.5	7.0	V

Parameter	
Flash Data Retention	20 years
Flash Endurance (write/erase cycles)	100,000

NOTES:

- Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V _{CC}	4.5	5.5	V
Input High Voltage	V _{IH}	2.2	V _{CC} + 0.3	V
Input Low Voltage	V _{IL}	-0.5	+0.8	V

SRAM TRUTH TABLE

\overline{SCS}	\overline{OE}	\overline{SWE}	Mode	Data I/O	Power
H	X	X	Standby	High Z	Standby
L	L	H	Read	Data Out	Active
L	H	H	Read	High Z	Active
L	X	L	Write	Data In	Active

CAPACITANCE

(T_A = +25°C)

Test	Symbol	Condition	Max	Unit
\overline{OE} Capacitance	C _{OE}	V _{IN} = 0V, f = 1.0MHz	50	pF
F/S \overline{WE} 1-2 Capacitance	C _{WE}	V _{IN} = 0V, f = 1.0MHz	20	pF
F/S \overline{CS} 1-2 Capacitance	C _{CS}	V _{IN} = 0V, f = 1.0MHz	20	pF
Data I/O Capacitance	C _{I/O}	V _{IN} = 0V, f = 1.0MHz	20	pF
Address Input Capacitance	C _{AD}	V _{IN} = 0V, f = 1.0MHz	50	pF

This parameter is guaranteed by design but not tested.

DC CHARACTERISTICS

(V_{CC} = 5.0V, V_{SS} = 0V, T_A = -55°C to +125°C)

Parameter	Symbol	Conditions	Min	Max	Unit
Input Leakage Current	I _{LI}	V _{CC} = 5.5, V _{IN} = GND to V _{CC}		10	μA
Output Leakage Current	I _{LO}	$\overline{FCS} = \overline{SCS} = V_{IH}$, $\overline{OE} = V_{IH}$, V _{OUT} = GND to V _{CC}		10	μA
SRAM Operating Supply Current x 16 Mode	I _{CCx16}	$\overline{SCS} = V_{IL}$, $\overline{OE} = V_{IH}$, f = 5mHz, V _{CC} = 5.5, $\overline{FCS} = V_{IH}$		330	mA
Standby Current	I _{SB}	$\overline{FCS} = \overline{SCS} = V_{IH}$, $\overline{OE} = V_{IH}$, f = 5mHz, V _{CC} = 5.5		45	mA
SRAM Output Low Voltage	V _{OL}	I _{OL} = 8mA, V _{CC} = 4.5, $\overline{FCS} = V_{IH}$		0.4	V
SRAM Output High Voltage	V _{OH}	I _{OL} = -4.0mA, V _{CC} = 4.5, $\overline{FCS} = V_{IH}$	2.4		V
Flash V _{CC} Active Current for Read (1)	I _{CC1}	$\overline{FCS} = V_{IL}$, $\overline{OE} = V_{IH}$, $\overline{SCS} = V_{IH}$		130	mA
Flash V _{CC} Active Current for Program or Erase (2)	I _{CC2}	$\overline{FCS} = V_{IL}$, $\overline{OE} = V_{IH}$, $\overline{SCS} = V_{IH}$		150	mA
Flash Output Low Voltage	V _{OL}	I _{OL} = 8.0mA, V _{CC} = 4.5, $\overline{SCS} = V_{IH}$		0.45	V
Flash Output High Voltage	V _{OH1}	I _{OH} = -2.5 mA, V _{CC} = 4.5, $\overline{SCS} = V_{IH}$	0.85 x V _{CC}		V
Flash Low V _{CC} Lock Out Voltage	V _{LKO}		3.2	4.2	V

NOTES:

- The I_{CC} current listed includes both the DC operating current and the frequency dependent component (@ 5 MHz). The frequency component typically is less than 2 mA/MHz, with \overline{OE} at V_{IH}.
- I_{CC} active while Embedded Algorithm (program or erase) is in progress.
- DC test conditions: V_{IL} = 0.3V, V_{IH} = V_{CC} - 0.3V



SRAM AC CHARACTERISTICS

(VCC = 5.0V, TA = -55°C to +125°C)

Parameter	Symbol	-35		-70		Unit
		Min	Max	Min	Max	
Read Cycle Time	t _{RC}	35		70		ns
Address Access Time	t _{AA}		35		70	ns
Output Hold from Address Change	t _{OH}	0		5		ns
Chip Select Access Time	t _{ACS}		35		70	ns
Output Enable to Output Valid	t _{OE}		25		35	ns
Chip Select to Output in Low Z	t _{CLZ} ¹	4		10		ns
Output Enable to Output in Low Z	t _{OLZ} ¹	0		5		ns
Chip Disable to Output in High Z	t _{CHZ} ¹		15		25	ns
Output Disable to Output in High Z	t _{OHZ} ¹		15		25	ns

1. This parameter is guaranteed by design but not tested.

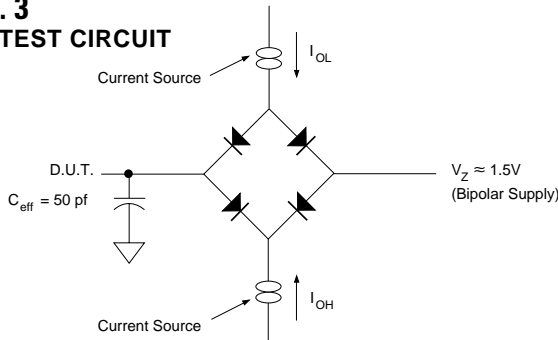
SRAM AC CHARACTERISTICS

(VCC = 5.0V, TA = -55°C to +125°C)

Parameter	Symbol	-35		-70		Unit
		Min	Max	Min	Max	
Write Cycle Time	t _{WC}	35		70		ns
Chip Select to End of Write	t _{CW}	25		60		ns
Address Valid to End of Write	t _{AW}	25		60		ns
Data Valid to End of Write	t _{DW}	20		30		ns
Write Pulse Width	t _{WP}	25		50		ns
Address Setup Time	t _{AS}	0		0		ns
Address Hold Time	t _{AH}	0		5		ns
Output Active from End of Write	t _{OW} ¹	0		5		ns
Write Enable to Output in High Z	t _{WHZ} ¹		15		25	ns
Data Hold from Write Time	t _{DH}	0		0		ns

1. This parameter is guaranteed by design but not tested.

FIG. 3
AC TEST CIRCUIT



AC TEST CONDITIONS

Parameter	Typ	Unit
Input Pulse Levels	$V_{IL} = 0, V_{IH} = 3.0$	V
Input Rise and Fall	5	ns
Input and Output Reference Level	1.5	V
Output Timing Reference Level	1.5	V

Notes:

V_Z is programmable from -2V to +7V.
 I_{OL} & I_{OH} programmable from 0 to 16mA.
 Tester Impedance $Z_0 = 75 \Omega$.
 V_Z is typically the midpoint of V_{OH} and V_{OL} .
 I_{OL} & I_{OH} are adjusted to simulate a typical resistive load circuit.
 ATE tester includes jig capacitance.



FIG. 4 SRAM
TIMING WAVEFORM - READ CYCLE

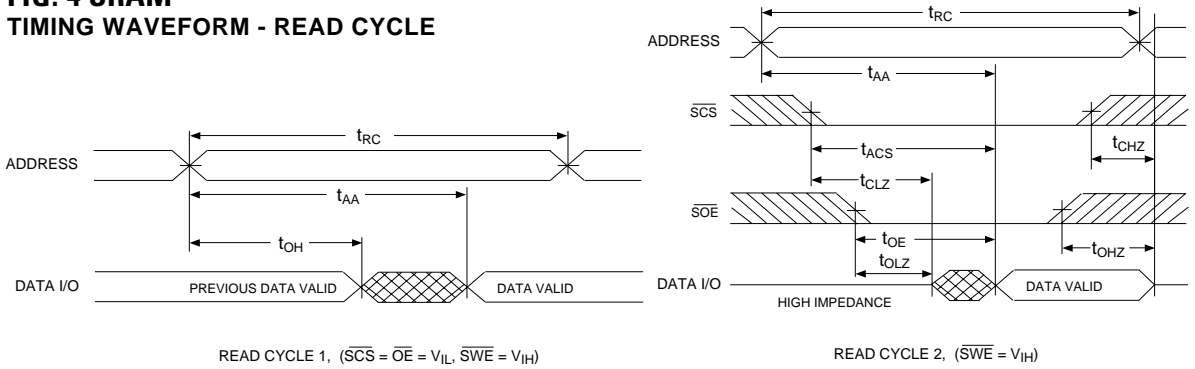


FIG. 5 SRAM
WRITE CYCLE - \overline{SWE} CONTROLLED

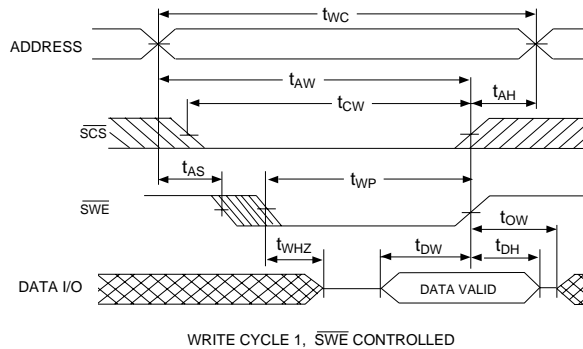
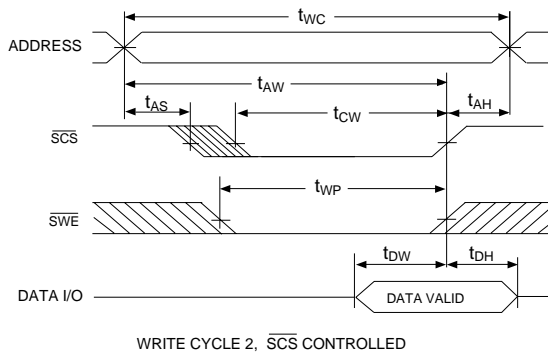


FIG. 6 SRAM
WRITE CYCLE - \overline{SCS} CONTROLLED





FLASH AC CHARACTERISTICS – WRITE/ERASE/PROGRAM OPERATIONS, \overline{FWE} CONTROLLED

(V_{CC} = 5.0V, T_A = -55°C to +125°C)

Parameter	Symbol		-90		-120		Unit
			Min	Max	Min	Max	
Write Cycle Time	tAVAV	tWC	90		120		ns
Chip Select Setup Time	tELWL	tCS	0		0		ns
Write Enable Pulse Width	tWLWH	tWP	45		50		ns
Address Setup Time	tAVWL	tAS	0		0		ns
Data Setup Time	tdVWH	tdS	45		50		ns
Data Hold Time	tWHDX	tdH	0		0		ns
Address Hold Time	tWLAX	tAH	45		50		ns
Write Enable Pulse Width High	tWHWL	tWPH	20		20		ns
Duration of Byte Programming Operation (1)	tWHWH1			300		300	μs
Sector Erase Time (2)	tWHWH2			15		15	sec
Read Recovery Time Before Write	tGHWL		0		0		μs
V _{CC} Set-up Time		tvCS	50		50		μs
Chip Programming Time				11		11	sec
Chip Select Hold Time		toEH	10		10		ns
Chip Erase Time (3)				64		64	sec

1. Typical value for tWHWH1 is 7ns.

2. Typical value for tWHWH2 is 1sec.

3. Typical value for Chip Erase Time is 8sec.

FLASH AC CHARACTERISTICS – READ ONLY OPERATIONS

(V_{CC} = 5.0V, T_A = -55°C to +125°C)

Parameter	Symbol		-90		-120		Unit
			Min	Max	Min	Max	
Read Cycle Time	tAVAV	tRC	90		120		ns
Address Access Time	tAVQV	tACC		90		120	ns
Chip Select Access Time	tELQV	tCE		90		120	ns
\overline{OE} to Output Valid	tGLQV	toE		35		50	ns
Chip Select to Output High Z (1)	tEHQZ	tdF		20		30	ns
\overline{OE} High to Output High Z (1)	tGHQZ	tdF		20		30	ns
Output Hold from Address, \overline{CS} or \overline{OE} Change, whichever is first	tAXQX	toH	0		0		ns

1. Guaranteed by design, not tested.



FLASH AC CHARACTERISTICS – WRITE/ERASE/PROGRAM OPERATIONS, FCS CONTROLLED

(VCC = 5.0V, TA = -55°C to +125°C)

Parameter	Symbol		-90		-120		Unit
			Min	Max			
Write Cycle Time	tAVAV	tWC	90		120		ns
FWE Setup Time	tWLEL	tWS	0		0		ns
FCS Pulse Width	tELEH	tCP	45		50		ns
Address Setup Time	tAVEL	tAS	0		0		ns
Data Setup Time	tDVEH	tDS	45		50		ns
Data Hold Time	tEHDX	tDH	0		0		ns
Address Hold Time	tELAX	tAH	45		50		ns
FCS Pulse Width High	tEHEL	tCPH	20		20		ns
Duration of Programming Operation (1)	tWHWH1			300		300	µs
Sector Erase Time (2)	tWHWH2			15		15	sec
Read Recovery Time	tGHEL		0		0		ns
Chip Programming Time				11		11	sec
Chip Erase Time (3)				64		64	sec

1. Typical value for tWHWH1 is 7ns.
2. Typical value for tWHWH2 is 1sec.
3. Typical value for Chip Erase Time is 8sec.



FIG. 7
AC WAVEFORMS FOR FLASH MEMORY READ OPERATIONS

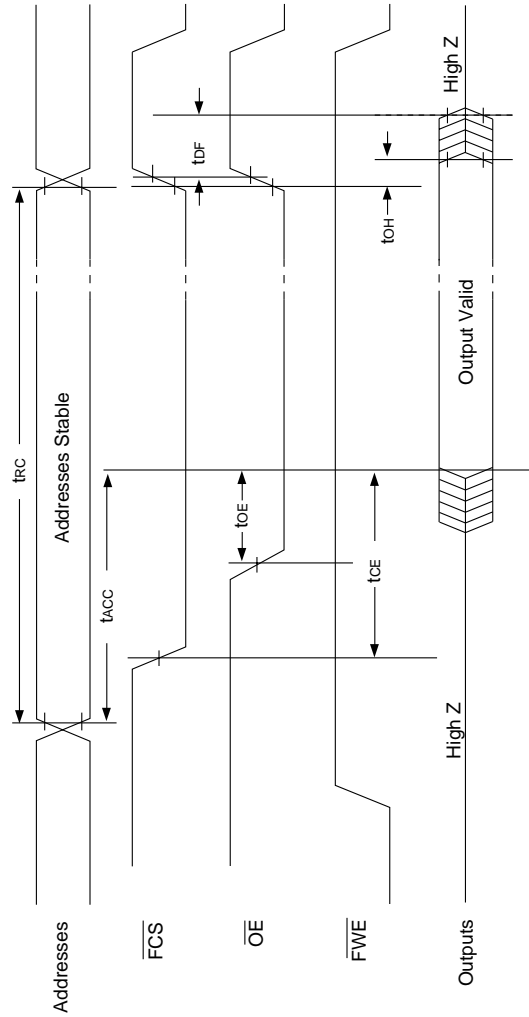
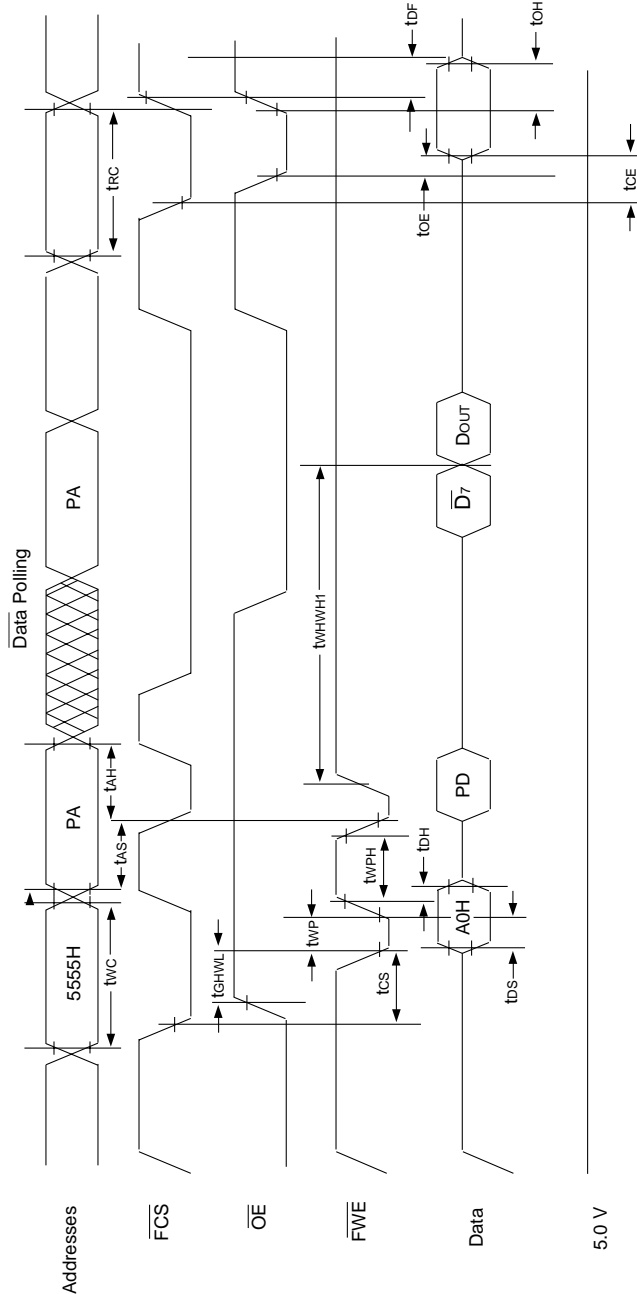




FIG. 8
WRITE/ERASE/PROGRAM OPERATION, FLASH MEMORY FW \bar{E} CONTROLLED

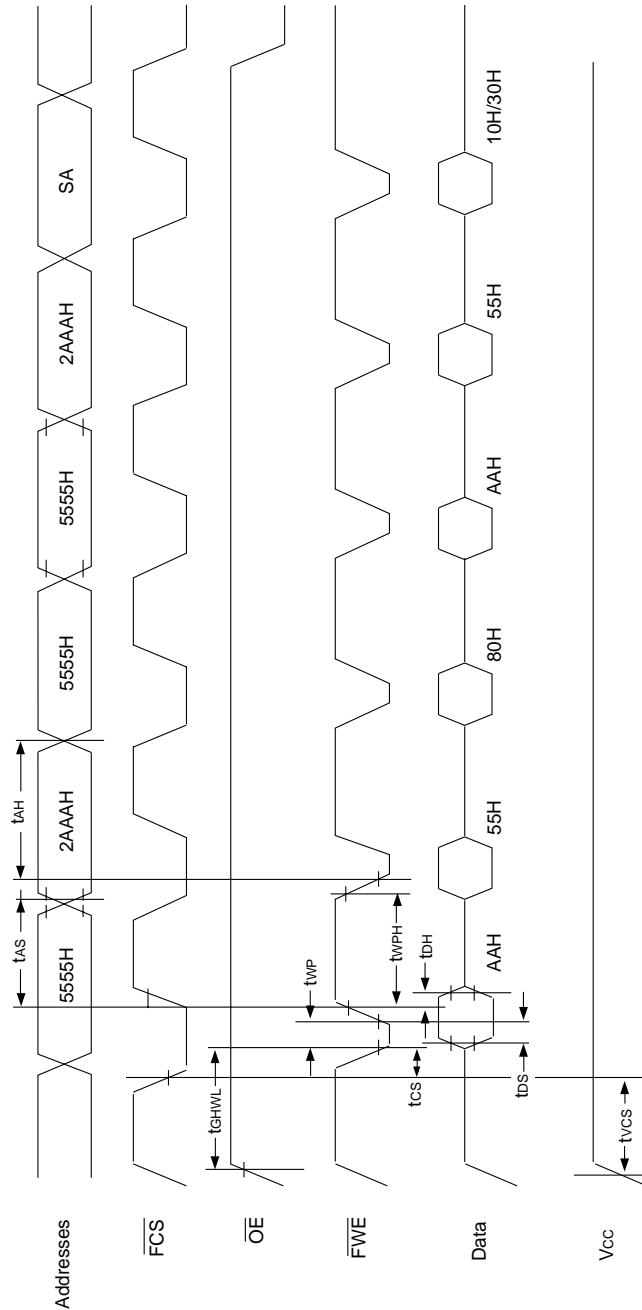


NOTES:

1. PA is the address of the memory location to be programmed.
2. PD is the data to be programmed at byte address.
3. D7 is the output of the complement of the data written to the device.
4. DOUT is the output of the data written to the device.
5. Figure indicates last two bus cycles of four bus cycle sequence.



FIG. 9
AC WAVEFORMS CHIP/SECTOR ERASE OPERATIONS FOR FLASH MEMORY



NOTES:

1. SA is the sector address for Sector Erase.



FIG. 10
AC WAVEFORMS FOR DATA POLLING DURING
EMBEDDED ALGORITHM OPERATIONS FOR
FLASH MEMORY

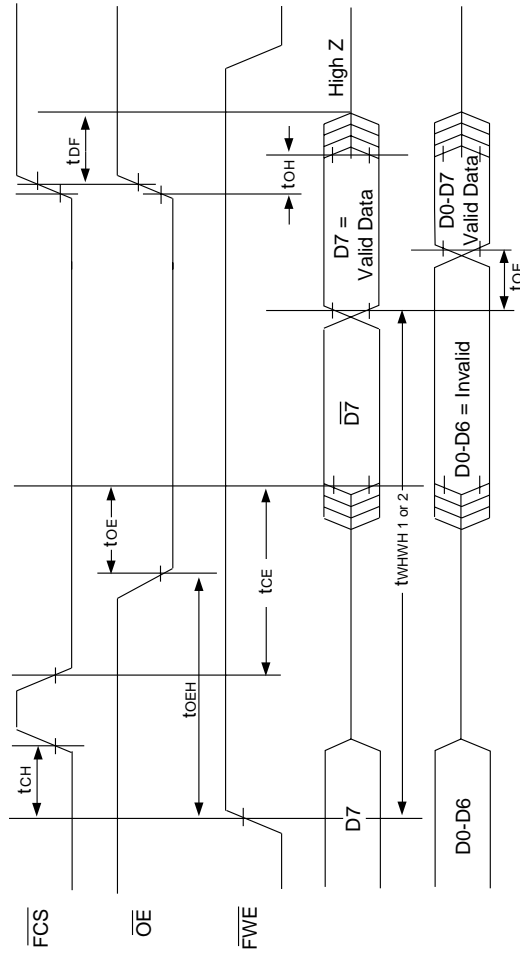
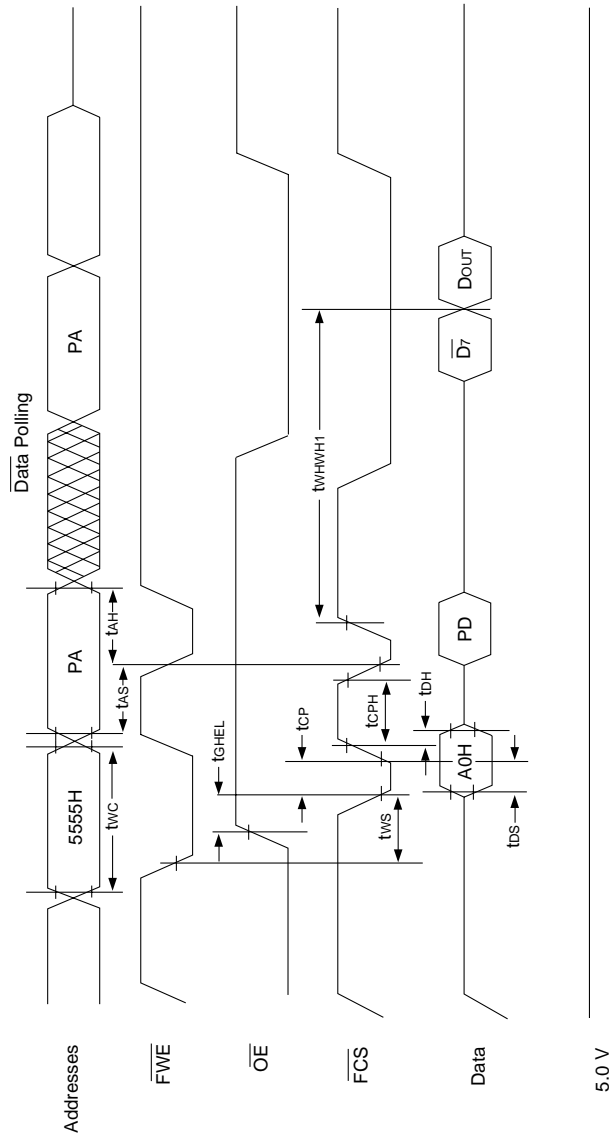




FIG. 11
WRITE/ERASE/PROGRAM OPERATION FOR FLASH MEMORY, CS CONTROLLED

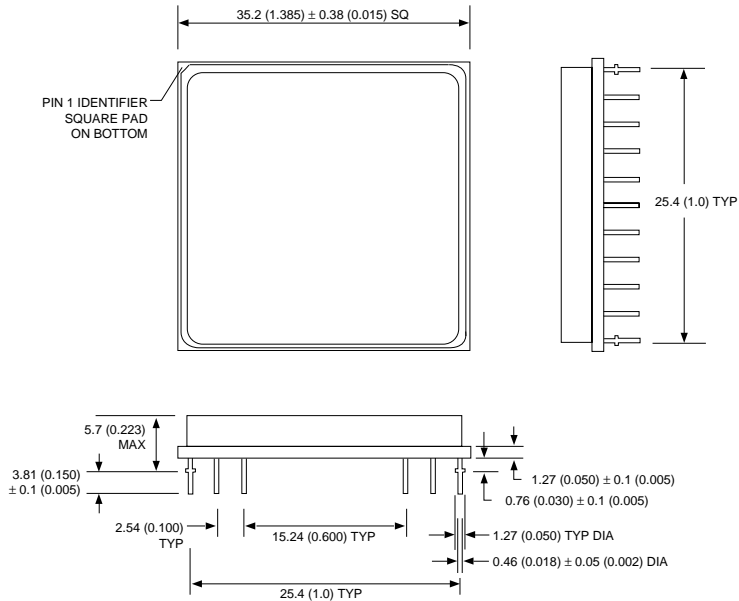


NOTES:

1. PA represents the address of the memory location to be programmed.
2. PD represents the data to be programmed at byte address.
3. $\overline{D7}$ is the output of the complement of the data written to the device.
4. D_{out} is the output of the data written to the device.
5. Figure indicates the last two bus cycles of a four bus cycle sequence.



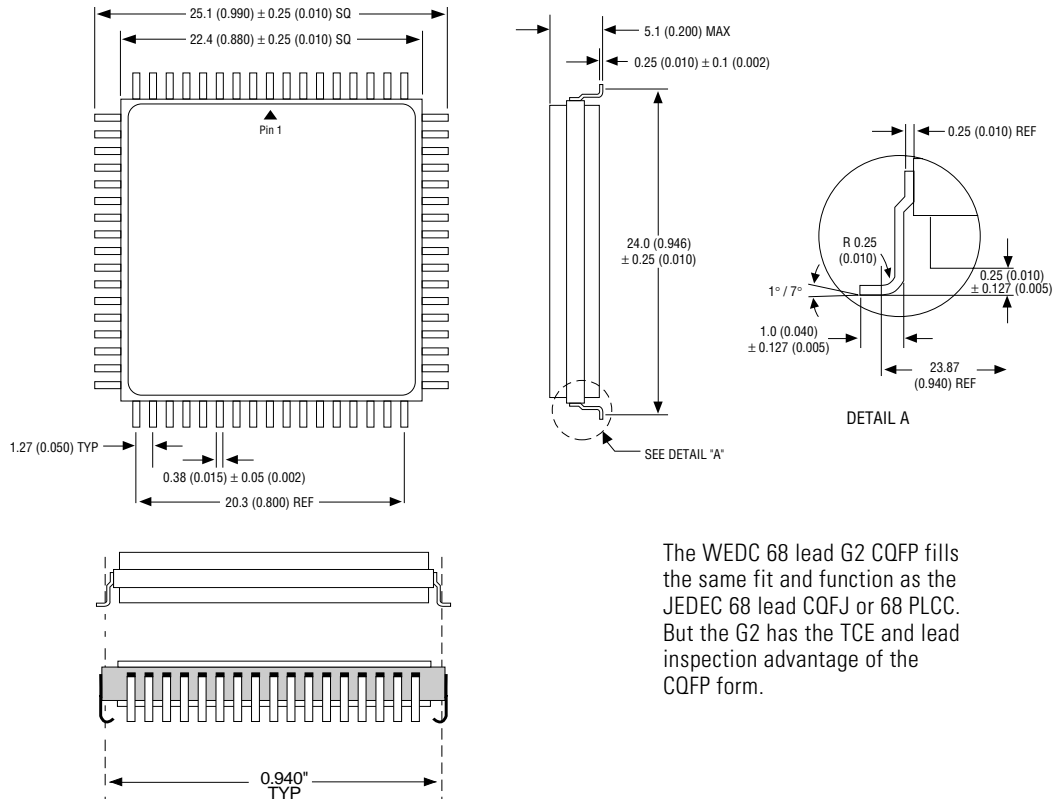
PACKAGE 402: 66 PIN, PGA TYPE, CERAMIC HEX-IN-LINE PACKAGE, HIP (H2)



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES



PACKAGE 500: 68 LEAD, CERAMIC QUAD FLAT PACK, CQFP (G2)



The WEDC 68 lead G2 CQFP fills the same fit and function as the JEDEC 68 lead CQFJ or 68 PLCC. But the G2 has the TCE and lead inspection advantage of the CQFP form.

ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES



ORDERING INFORMATION

W S F 512K16 - XXX X X X

LEAD FINISH:

- Blank = Gold plated leads
- A = Solder dip leads

DEVICE GRADE:

- M = Military Screened -55°C to +125°C
- I = Industrial -40°C to +85°C
- C = Commercial 0°C to +70°C

PACKAGE TYPE:

- H2 = Ceramic Hex In-line Package, HIP (Package 402)
- G2 = 22 mm Ceramic Quad Flat Pack, CQFP (Package 500)

ACCESS TIME (ns)

- 39 = 35ns SRAM and 90ns FLASH
- 72 = 70ns SRAM and 120ns FLASH also available

ORGANIZATION, 512K x 16

Flash

SRAM

WHITE ELECTRONIC DESIGNS CORP.

DEVICE TYPE	SRAM SPEED	FLASH SPEED	PACKAGE	SMD NO.
512K x 16 Mixed Module	70ns	120ns	66 pin HIP (H2)	5962-96901 01HXX
512K x 16 Mixed Module	35ns	90ns	66 pin HIP (H2)	5962-96901 02HXX
512K x 16 Mixed Module	70ns	120ns	68 lead CQFP/J (G2)	5962-96901 01HMX
512K x 16 Mixed Module	35ns	90ns	68 lead CQFP/J (G2)	5962-96901 02HMX