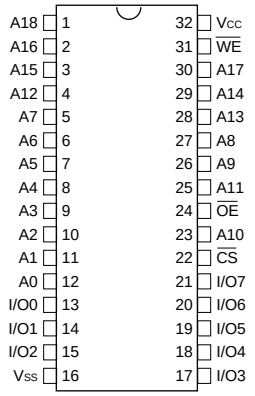
256Kx8 SRAM/ FLASH MODULE *ADVANCED**

FIG. 1

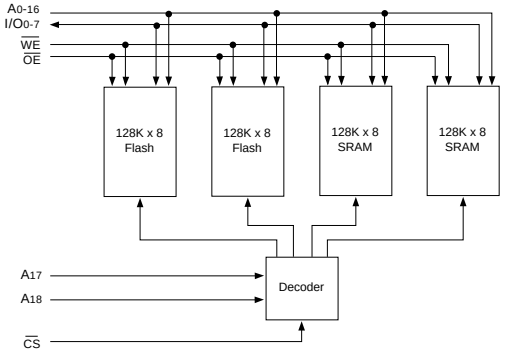
PIN CONFIGURATION TOP VIEW



PIN DESCRIPTION

A_{0-18}	Address Inputs
I/O_{0-7}	Data Input/Output
$\overline{CS}$	Chip Select
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
V_{CC}	+5.0V Power
V_{SS}	Ground

BLOCK DIAGRAM



FEATURES

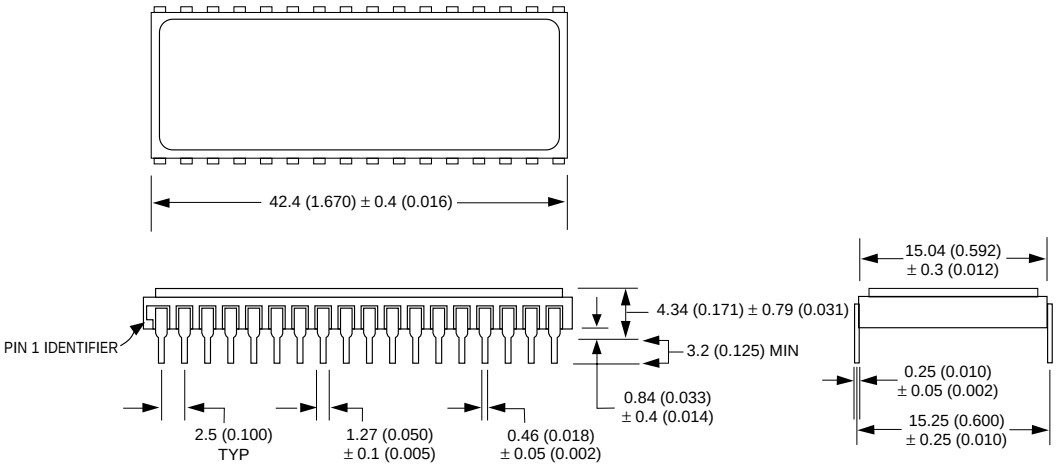
- Access Times of 35ns (SRAM) and 70ns (FLASH)
- JEDEC Standard, Hermetic Ceramic Package, 32 pin DIP (Package 300)
- 256Kx8 SRAM
- 256Kx8 5V FLASH
- Memory Map
  - Flash Memory: 0H-3FFFFH
  - SRAM: 40000H-7FFFFH
- Low Power CMOS
- Commercial, Industrial and Military Temperature Ranges
- TTL Compatible Inputs and Outputs
- Built-in Decoupling Caps and Multiple Ground Pins for Low Noise Operation

FLASH MEMORY FEATURES

- 10,000 Erase/Program Cycles
- Sector Architecture
  - 8 equal size sectors of 16KBytes each
  - Any combination of sectors can be concurrently erased. Also supports full chip erase
- Data Retention, 10 Years at 125°C
- 5 Volt Programming; 5V ±10% Supply
- Embedded Erase and Program Algorithms
- Hardware and Software Write Protection
- Page Program Operation and Internal Program Control Time

* *This data sheet describes a product that may or may not be under development and is subject to change or cancellation without notice.*

PACKAGE 300: 32 PIN, CERAMIC DIP, SINGLE CAVITY SIDE BRAZED



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

ORDERING INFORMATION

W S F 256K8 - XXX C X X

LEAD FINISH:
- Blank = Gold plated leads
- A = Solder dip leads

DEVICE GRADE:

M =	Military Screened	-55°C to +125°C
I =	Industrial	-40°C to +85°C
C =	Commercial	0°C to +70°C

PACKAGE TYPE:
- C = 32 DIP (Package 300)

ACCESS TIME (ns)
- 37 = 35ns SRAM and 70ns FLASH
- 72 = 70ns SRAM and 120ns FLASH also available

ORGANIZATION, 256K x 8

Flash PROM

SRAM

WHITE MICROELECTRONICS