



128Kx16 SRAM/FLASH MODULE, SMD 5962-96900

FEATURES

- Access Times of 35ns (SRAM) and 70ns (FLASH)
- Access Times of 70ns (SRAM) and 120ns (FLASH)
- Packaging
 - 66-pin, PGA Type, 1.075 inch square HIP, Hermetic Ceramic HIP (Package 400)
 - 66-pin, PGA Type, 1.185 inch square HIP, Hermetic Ceramic HIP (Package 401)
 - 68 lead, Hermetic CQFP (G1U)¹, 22.4mm (0.880 inch) square (Package 519). Designed to fit JEDEC 68 lead 0.990" CQFJ footprint (FIGURE 2)
 - 68 lead, Hermetic CQFP (G1T), 22.4mm (0.880 inch) square (Package 524)
- 128Kx16 SRAM
- 128Kx16 5V FLASH
- Organized as 128Kx16 of SRAM and 128Kx16 of Flash Memory with separate Data Buses
- Both blocks of memory are User Configurable as 256Kx8
- Low Power CMOS
- Commercial, Industrial and Military Temperature Ranges

- TTL Compatible Inputs and Outputs
- Built-in Decoupling Caps and Multiple Ground Pins for Low Noise Operation
- Weight
 - WSF128K16-XHX — 13 grams typical
 - WSF128K16-H1X — 13 grams typical
 - WSF128K16-XG1UX¹ — 5 grams typical
 - WSF128K16-XG1TX — 5 grams typical

FLASH MEMORY FEATURES

- 10,000 Erase/Program Cycles
- Sector Architecture
 - 8 equal size sectors of 16K bytes each
 - Any combination of sectors can be concurrently erased. Also supports full chip erase
- 5 Volt Programming; 5V ± 10% Supply
- Embedded Erase and Program Algorithms
- Hardware Write Protection
- Page Program Operation and Internal Program Control Time.

Note: For programming information refer to Flash Programming 1M5 Application Note.
 Note 1: Package not recommended for new designs

FIGURE1 PIN CONFIGURATION FOR WSF128K16-XHX AND WSF128K16-XH1X

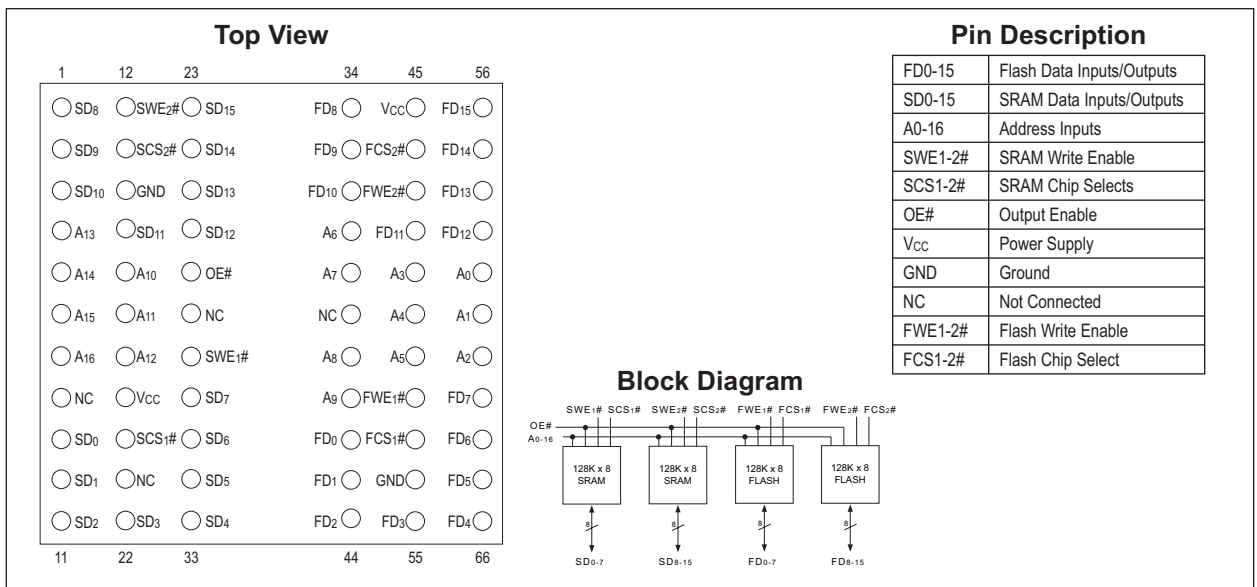
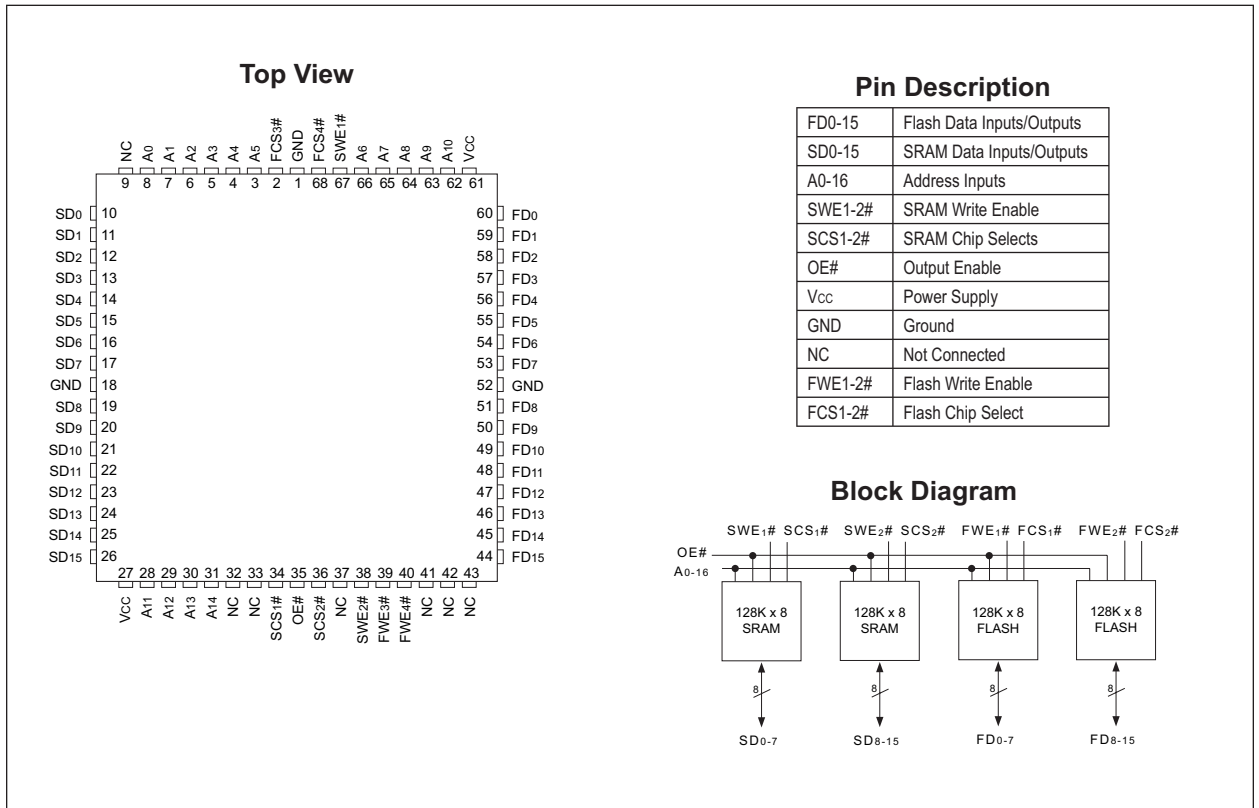




FIGURE 2 – PIN CONFIGURATION FOR WSF128K16-XG1UX¹, WSF128K16-XG1TX



NOTE 1: Package not recommended for new designs



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Unit
Operating Temperature	T _A	-55	+125	°C
Storage Temperature	T _{STG}	-65	+150	°C
Signal Voltage Relative to GND	V _G	-0.5	7.0	V
Junction Temperature	T _J		150	°C
Supply Voltage	V _{CC}	-0.5	7.0	V

Parameter	Symbol	Min	Max	Unit
Flash Data Retention			10 years	
Flash Endurance (write/erase cycles)			10,000	

NOTES: 1. Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

SRAM TRUTH TABLE

SCS#	OE#	SWE#	Mode	Data I/O	Power
H	X	X	Standby	High Z	Standby
L	L	H	Read	Data Out	Active
L	H	H	Read	High Z	Active
L	X	L	Write	Data In	Active

CAPACITANCE

T_A = +25°C

Test	Symbol	Condition	Max	Unit
OE# Capacitance	C _{OE}	V _{IN} = 0V, f = 1.0MHz	50	pF
F/S WE1-2# Capacitance	C _{WE}	V _{IN} = 0V, f = 1.0MHz	20	pF
F/S CS1-2# Capacitance	C _{CS}	V _{IN} = 0V, f = 1.0MHz	20	pF
SD0-15/FD0-15 Capacitance	C _{I/O}	V _{IN} = 0V, f = 1.0MHz	20	pF
A0 - A16 Capacitance	C _{AD}	V _{IN} = 0V, f = 1.0MHz	50	pF

This parameter is guaranteed by design but not tested.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V _{CC}	4.5	5.5	V
Input High Voltage	V _{IH}	2.2	V _{CC} + 0.3	V
Input Low Voltage	V _{IL}	-0.5	+0.8	V

DC CHARACTERISTICS

V_{CC} = 5.0V, V_{SS} = 0V, -55°C ≤ T_A ≤ +125°C

Parameter	Symbol	Conditions	Min	Max	Unit
Input Leakage Current	I _{LI}	V _{CC} = 5.5, V _{IN} = GND to V _{CC}		10	μA
Output Leakage Current	I _{LO}	SCS# = V _{IH} , OE# = V _{IH} , V _{OUT} = GND to V _{CC}		10	μA
SRAM Operating Supply Current x 16 Mode	I _{CCx16}	SCS# = V _{IL} , OE# = FCS# = V _{IH} , f = 5MHz, V _{CC} = 5.5		360	mA
Standby Current	I _{SB}	FCS# = SCS# = V _{IH} , OE# = V _{IH} , f = 5MHz, V _{CC} = 5.5		40	mA
SRAM Output Low Voltage	V _{OL}	I _{OL} = 2.1mA, V _{CC} = 4.5		0.4	V
SRAM Output High Voltage	V _{OH}	I _{OH} = -1.0mA, V _{CC} = 4.5	2.4		V
Flash V _{CC} Active Current for Read (1)	I _{CC1}	FCS# = V _{IL} , OE# = SCS# = V _{IH}		100	mA
Flash V _{CC} Active Current for Program or Erase (2)	I _{CC2}	FCS# = V _{IL} , OE# = SCS# = V _{IH}		130	mA
Flash Output Low Voltage	V _{OL}	I _{OL} = 8.0mA, V _{CC} = 4.5		0.45	V
Flash Output High Voltage	V _{OH1}	I _{OH} = -2.5 mA, V _{CC} = 4.5	0.85 x V _{CC}		V
Flash Output High Voltage	V _{OH2}	I _{OH} = -100 μA, V _{CC} = 4.5	V _{CC} - 0.4		V
Flash Low V _{CC} Lock Out Voltage	V _{LKO}		3.2		V

NOTES:

- The ICC current listed includes both the DC operating current and the frequency dependent component (@ 5 MHz). The frequency component typically is less than 2 mA/MHz, with OE# at V_{IH}.
- ICC active while Embedded Algorithm (program or erase) is in progress.
- DC test conditions: V_{IL} = 0.3V, V_{IH} = V_{CC} - 0.3V



SRAM AC CHARACTERISTICS

$V_{CC} = 5.0V, -55^{\circ}C \leq T_A \leq +125^{\circ}C$

Parameter Read Cycle	Symbol	-35		-70		Unit
		Min	Max	Min	Max	
Read Cycle Time	t_{RC}	35		70		ns
Address Access Time	t_{AA}		35		70	ns
Output Hold from Address Change	t_{OH}	0		3		ns
Chip Select Access Time	t_{ACS}		35		70	ns
Output Enable to Output Valid	t_{OE}		20		35	ns
Chip Select to Output in Low Z	t_{CLZ}^1	3		3		ns
Output Enable to Output in Low Z	t_{OLZ}^1	0		0		ns
Chip Disable to Output in High Z	t_{CHZ}^1		20		25	ns
Output Disable to Output in High Z	t_{OHZ}^1		20		25	ns

1. This parameter is guaranteed by design but not tested.

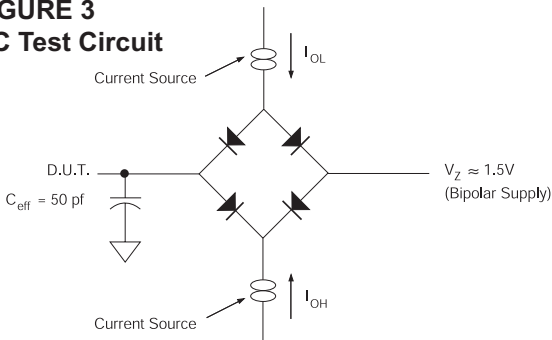
SRAM AC CHARACTERISTICS

$V_{CC} = 5.0V, -55^{\circ}C \leq T_A \leq +125^{\circ}C$

Parameter Write Cycle	Symbol	-35		-70		Unit
		Min	Max	Min	Max	
Write Cycle Time	t_{WC}	35		70		ns
Chip Select to End of Write	t_{CW}	25		60		ns
Address Valid to End of Write	t_{AW}	25		60		ns
Data Valid to End of Write	t_{DW}	20		30		ns
Write Pulse Width	t_{WP}	25		50		ns
Address Setup Time	t_{AS}	0		5		ns
Address Hold Time	t_{AH}	0		5		ns
Output Active from End of Write	t_{OW1}	4		5		ns
Write Enable to Output in High Z	t_{WHZ1}		20		25	ns
Data Hold from Write Time	t_{DH}	0		0		ns

1. This parameter is guaranteed by design but not tested.

**FIGURE 3
AC Test Circuit**



AC TEST CONDITIONS

Parameter	Typ	Unit
Input Pulse Levels	$V_{IL} = 0, V_{IH} = 3.0$	V
Input Rise and Fall	5	ns
Input and Output Reference Level	1.5	V
Output Timing Reference Level	1.5	V

Notes: V_Z is programmable from -2V to +7V.
 I_{OL} & I_{OH} programmable from 0 to 16mA.
 Tester Impedance $Z_0 = 75\Omega$.
 V_Z is typically the midpoint of V_{OH} and V_{OL} .
 I_{OL} & I_{OH} are adjusted to simulate a typical resistive load circuit.
 ATE tester includes jig capacitance.



FIGURE 4 – SRAM TIMING WAVEFORM — READ CYCLE

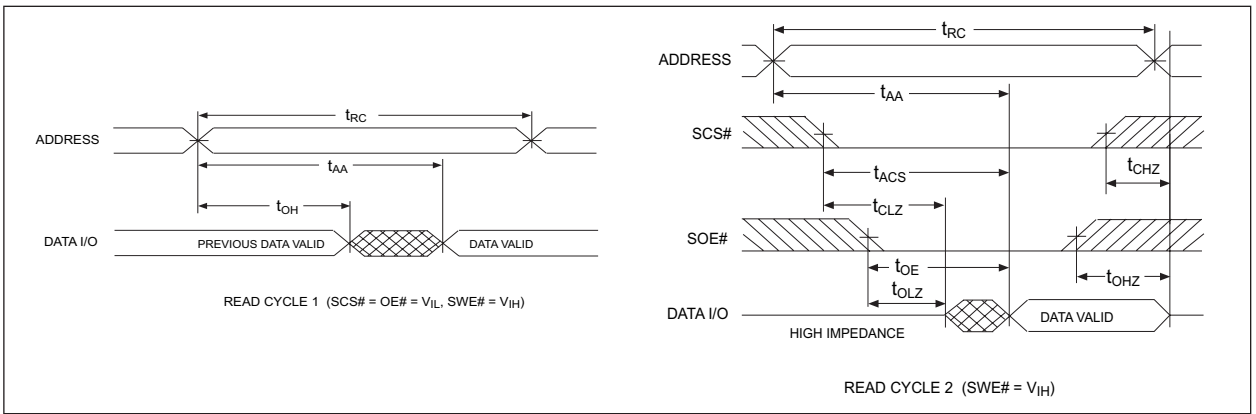


FIGURE 5 – SRAM WRITE CYCLE — SWE# CONTROLLED

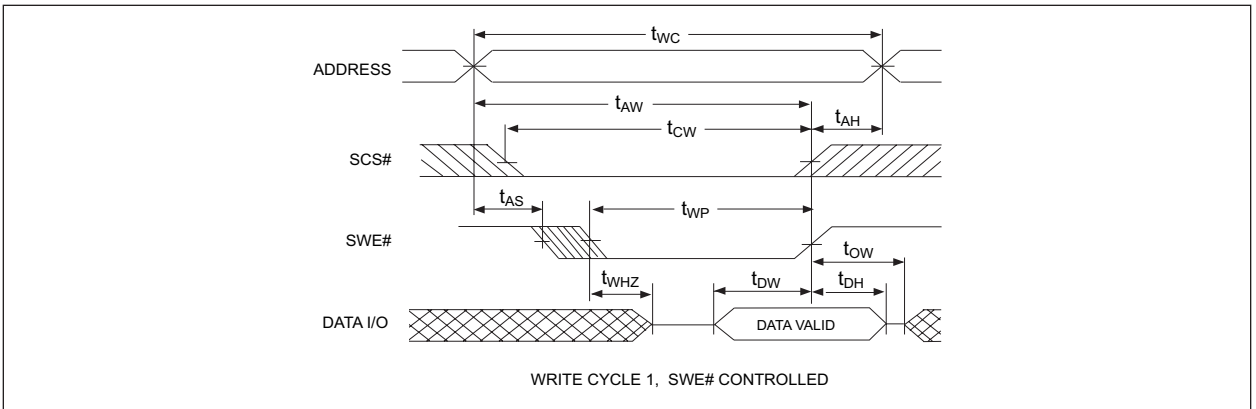
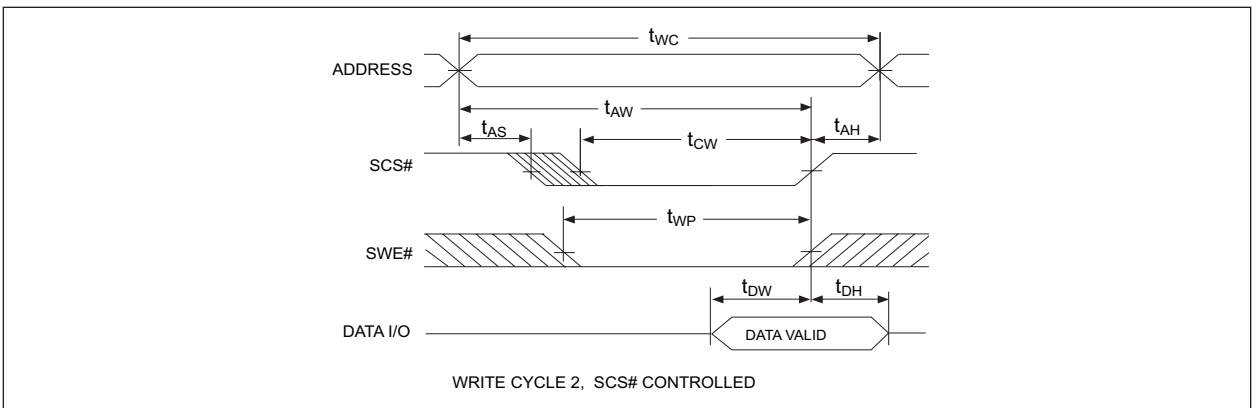


FIGURE 6 – SRAM WRITE CYCLE — SCS# CONTROLLED





FLASH AC CHARACTERISTICS – WRITE/ERASE/PROGRAM OPERATIONS, FWE# CONTROLLED

$V_{CC} = 5.0V, -55^{\circ}C \leq T_A \leq +125^{\circ}C$

Parameter	Symbol		-70		-120		Unit
			Min	Max	Min	Max	
Write Cycle Time	t _{AVAV}	t _{WC}	70		120		ns
Chip Select Setup Time	t _{ELWL}	t _{CS}	0		0		ns
Write Enable Pulse Width	t _{WLWH}	t _{WP}	35		50		ns
Address Setup Time	t _{AVWL}	t _{AS}	0		0		ns
Data Setup Time	t _{DVWH}	t _{DS}	30		50		ns
Data Hold Time	t _{WHDX}	t _{DH}	0		0		ns
Address Hold Time	t _{WLAX}	t _{AH}	45		50		ns
Chip Select Hold Time	t _{WHEH}	t _{CH}	0		0		ns
Write Enable Pulse Width High	t _{WHWL}	t _{WPH}	20		20		ns
Duration of Byte Programming Operation (min)	t _{WHWH1}		14		14		μs
Chip and Sector Erase Time	t _{WHWH2}		2.2	60	2.2	60	sec
Read Recovery Time Before Write	t _{GHWL}		0		0		μs
V _{CC} Set-up Time		t _{VCS}	50		50		μs
Chip Programming Time				12.5		12.5	sec
Output Enable Setup Time		t _{OES}	0		0		ns
Output Enable Hold Time (1)		t _{OEH}	10		10		ns

1. For Toggle and Data# Polling.

FLASH AC CHARACTERISTICS – READ ONLY OPERATIONS

$V_{CC} = 5.0V, -55^{\circ}C \leq T_A \leq +125^{\circ}C$

Parameter	Symbol		-70		-120		Unit
			Min	Max	Min	Max	
Read Cycle Time	t _{AVAV}	t _{RC}	70		120		ns
Address Access Time	t _{AVQV}	t _{ACC}		70		120	ns
Chip Select Access Time	t _{ELQV}	t _{CE}		70		120	ns
OE# to Output Valid	t _{GLQV}	t _{OE}		35		50	ns
Chip Select to Output High Z (1)	t _{EHQZ}	t _{DF}		20		30	ns
OE# High to Output High Z (1)	t _{GHQZ}	t _{DF}		20		30	ns
Output Hold from Address, CS# or OE# Change, whichever is first	t _{AXQX}	t _{OH}	0		0		ns

1. Guaranteed by design, not tested.



FLASH AC CHARACTERISTICS – WRITE/ERASE/PROGRAM OPERATIONS, FCS# CONTROLLED

V_{CC} = 5.0V, -55°C ≤ T_A ≤ +125°C

Parameter	Symbol		-70		-120		Unit
			Min	Max	Min	Max	
Write Cycle Time	t _{AVAV}	t _{WC}	70		120		ns
Fwe# Setup Time	t _{WLLEL}	t _{WS}	0		0		ns
Fcs# Pulse Width	t _{ELEH}	t _{CP}	35		50		ns
Address Setup Time	t _{AVEL}	t _{AS}	0		0		ns
Data Setup Time	t _{DVEH}	t _{DS}	30		50		ns
Data Hold Time	t _{EHDH}	t _{DH}	0		0		ns
Address Hold Time	t _{ELAX}	t _{AH}	45		50		ns
Fwe# Hold From Fwe# High	t _{EHWH}	t _{WH}	0		0		ns
Fcs# Pulse Width High	t _{EHEL}	t _{CPH}	20		20		ns
Duration Of Programming Operation	t _{WHWH1}		14		14		μs
Duration Of Erase Operation	t _{WHWH2}		2.2	60	2.2	60	sec
Read Recovery Before Write	t _{GHLEL}		0		0		ns
Chip Programming Time				12.5		12.5	sec



FIGURE 7 – AC WAVEFORMS FOR FLASH MEMORY READ OPERATIONS

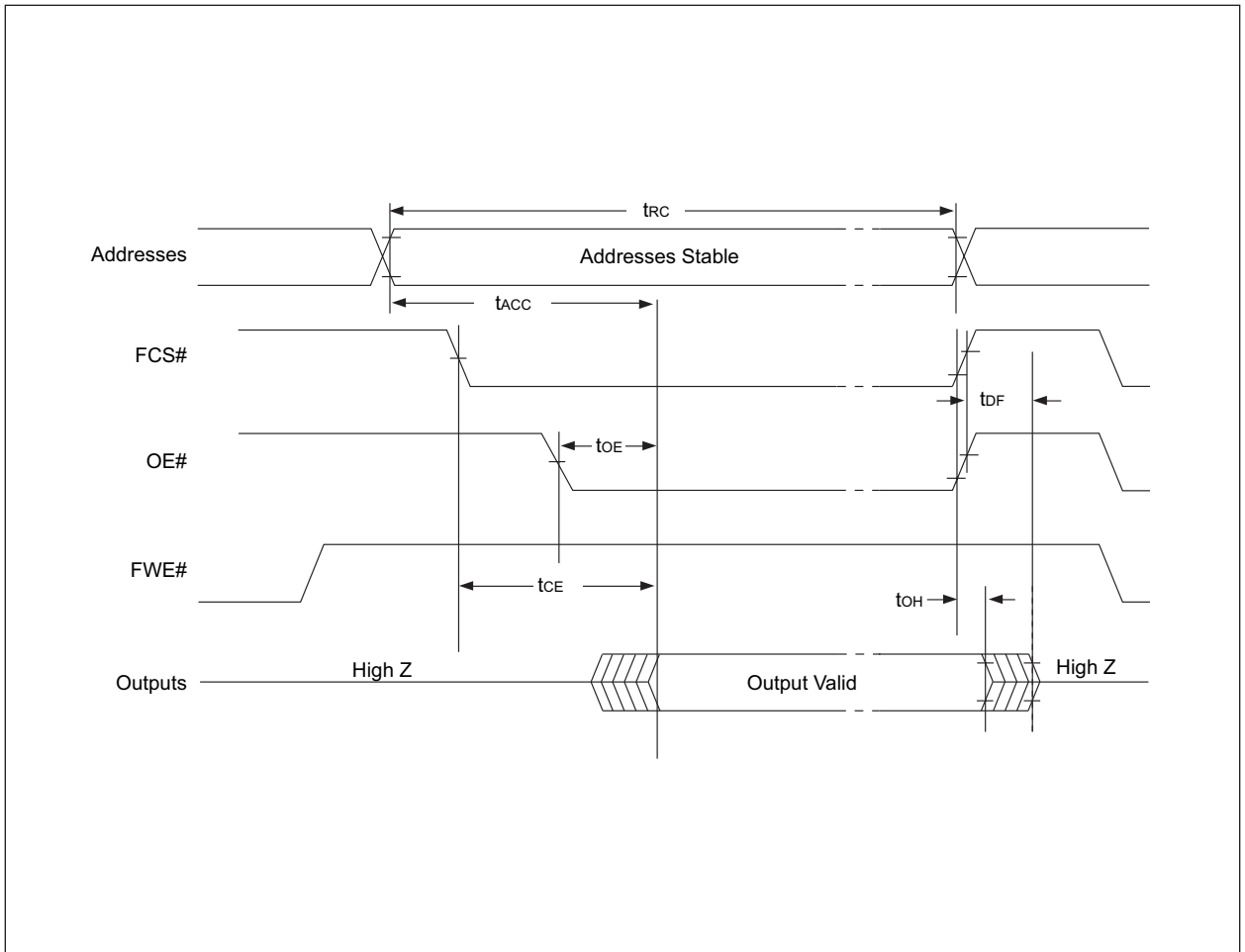




FIGURE 8 – WRITE/ERASE/PROGRAM OPERATION, FLASH MEMORY FWE# CONTROLLED

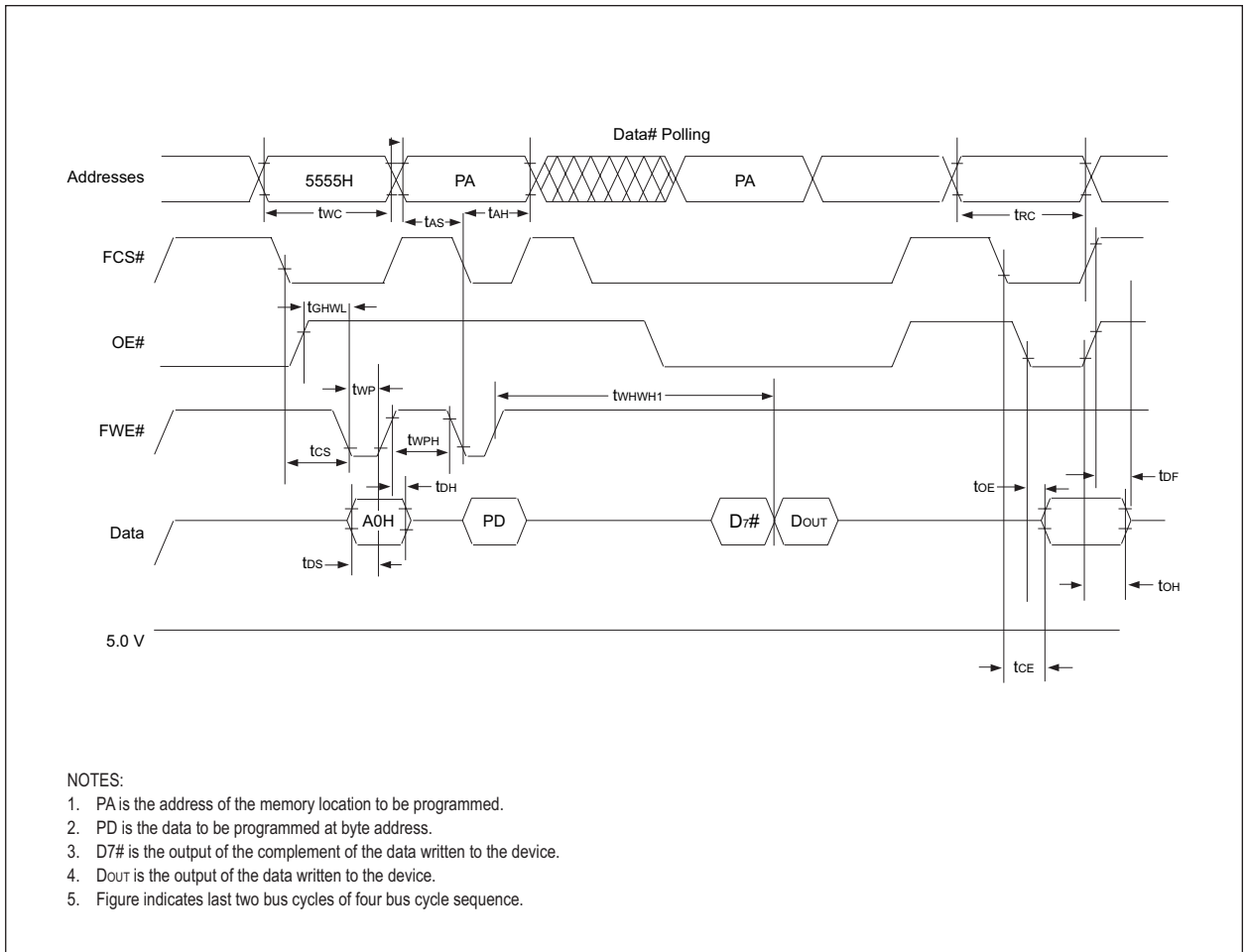




FIGURE 9 – AC WAVEFORMS CHIP/SECTOR ERASE OPERATIONS FOR FLASH MEMORY

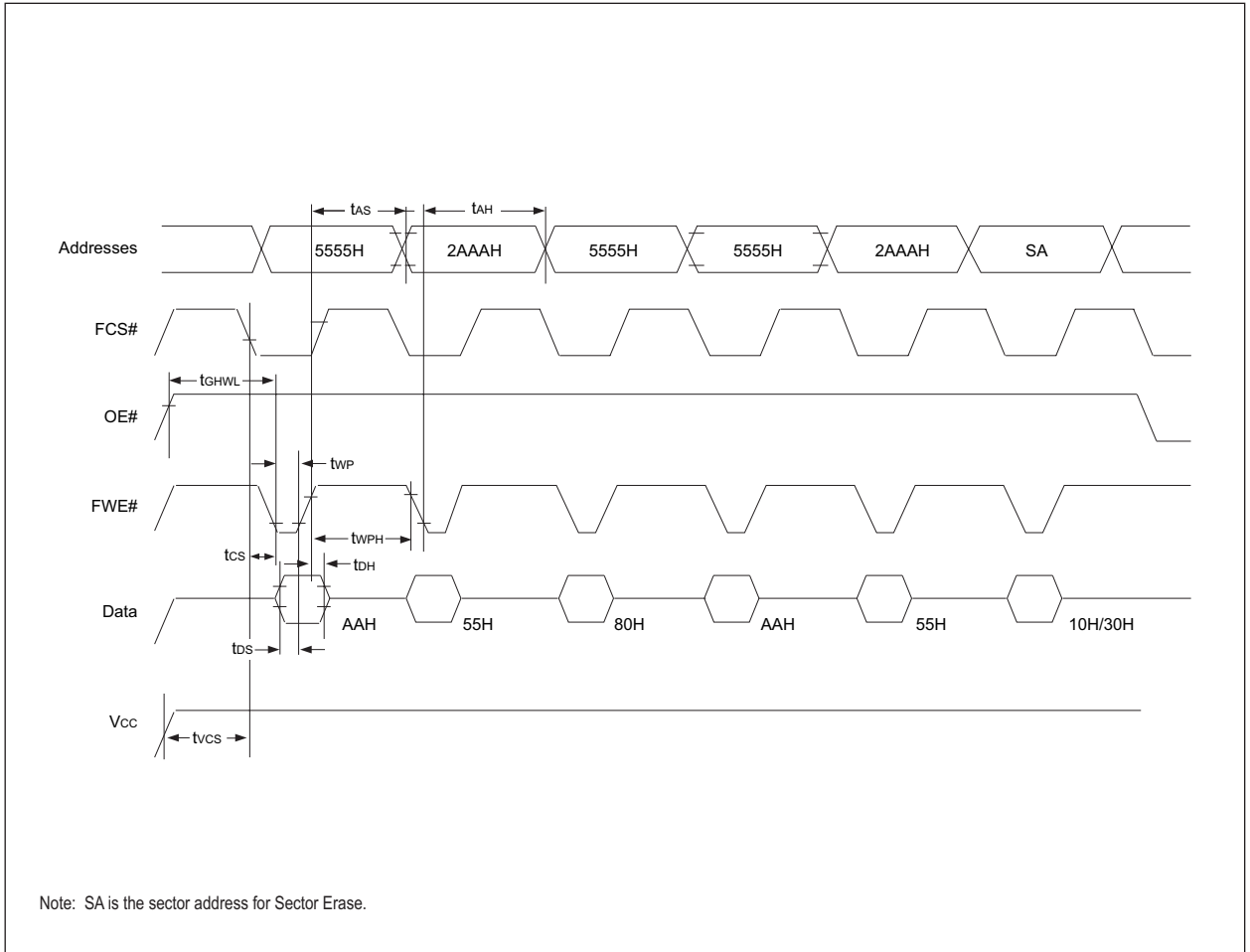




FIGURE 10 – AC WAVEFORMS FOR DATA# POLLING DURING EMBEDDED ALGORITHM OPERATIONS FOR FLASH MEMORY

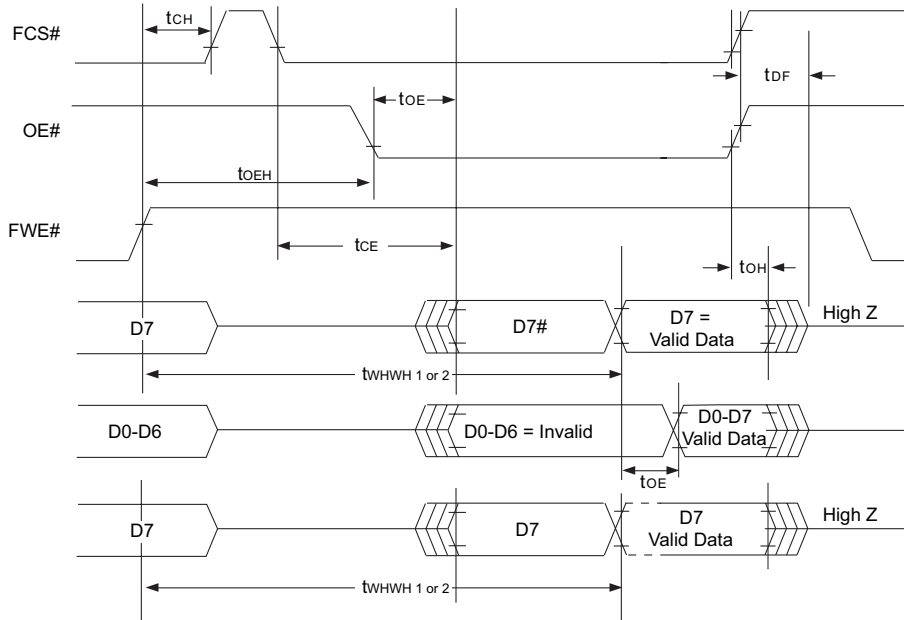
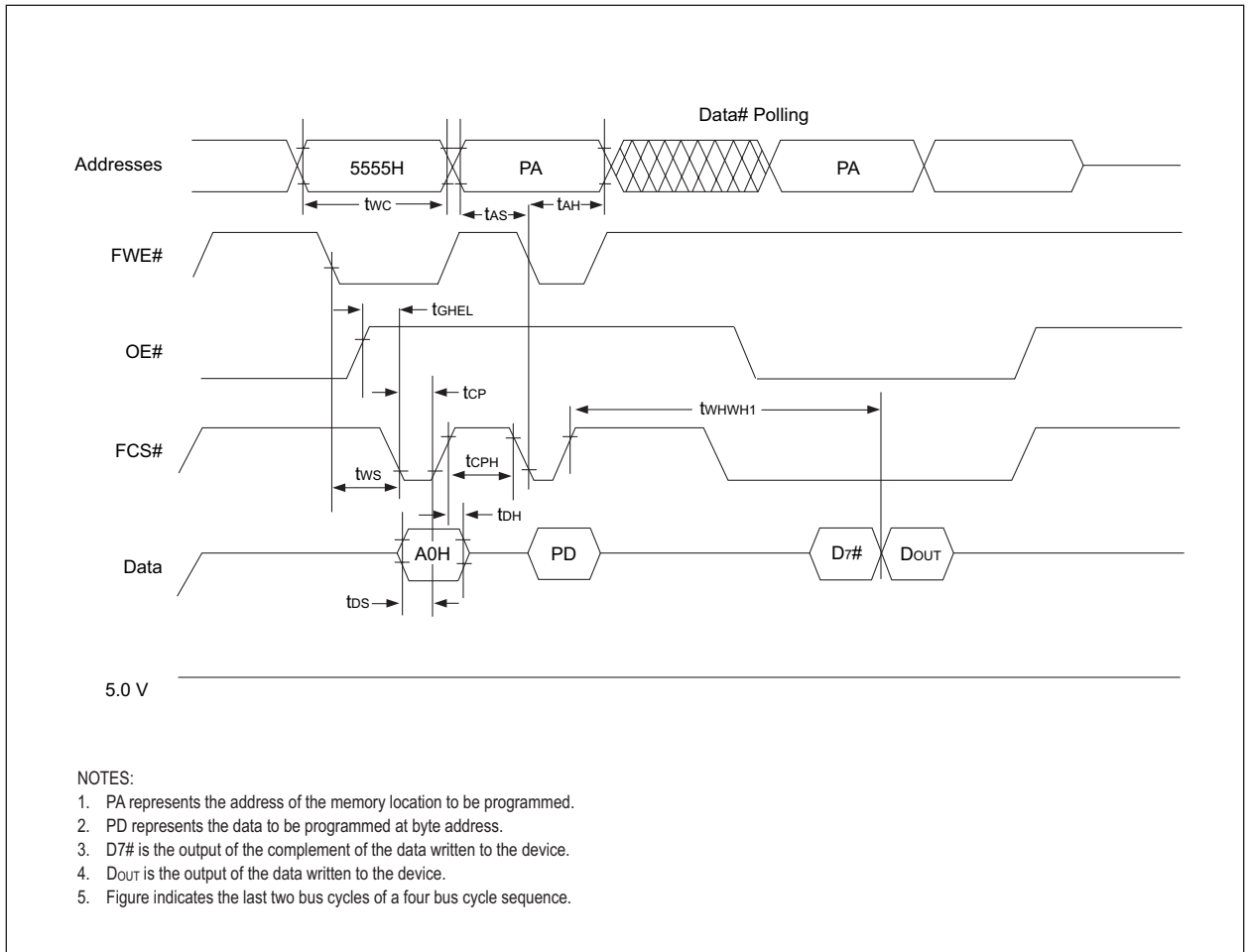


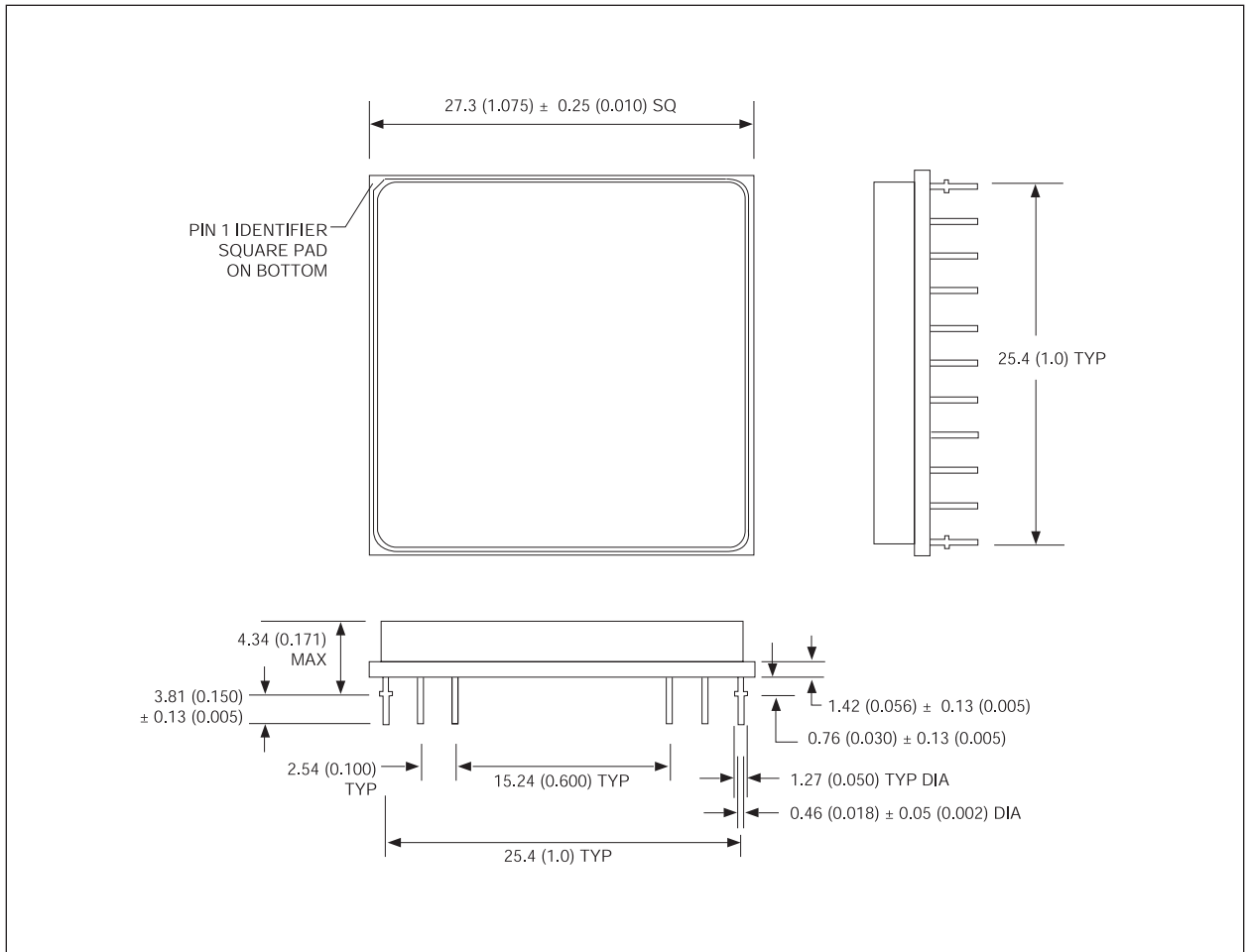


FIGURE 11 – WRITE/ERASE/PROGRAM OPERATION FOR FLASH MEMORY, CS# CONTROLLED





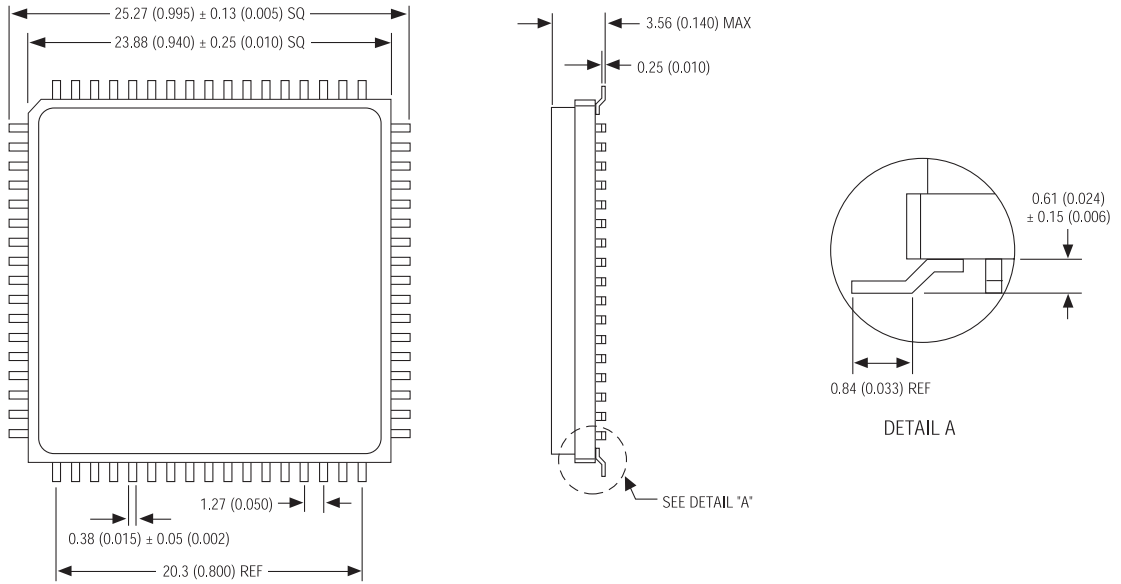
PACKAGE 400: 66 PIN, PGA TYPE, CERAMIC HEX-IN-LINE PACKAGE, HIP (H1)



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES



PACKAGE 519: 68 LEAD, CERAMIC QUAD FLAT PACK, CQFP (G1U)¹

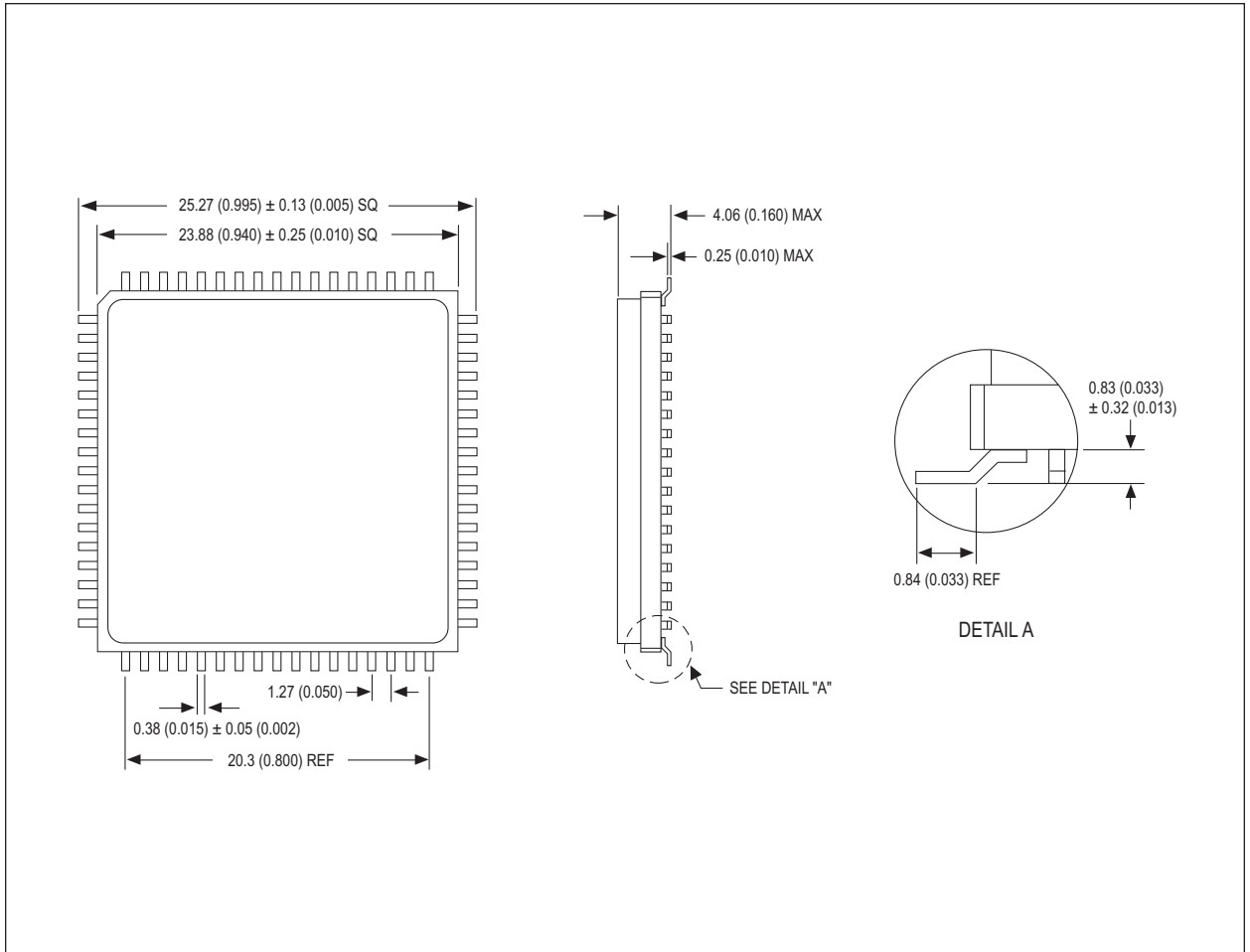


NOTE 1: Package not recommended for new designs

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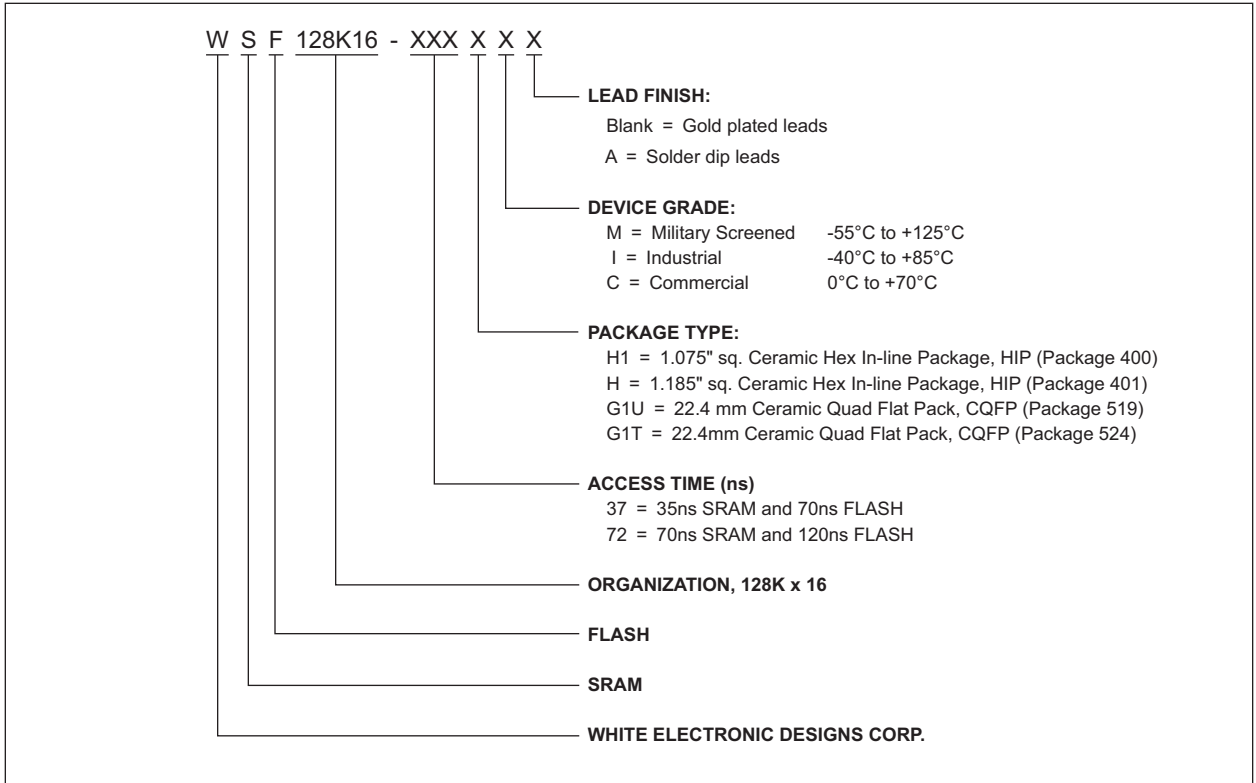
PACKAGE 524: 68 LEAD, CERAMIC QUAD FLAT PACK, LOW PROFILE CQFP (G1T)



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES



ORDERING INFORMATION



DEVICE TYPE	SRAM SPEED	FLASH SPEED	PACKAGE	SMD NO.
128K x 16 Mixed Module	70ns	120ns	66 pin HIP (H)	5962-96900 01HXX
128K x 16 Mixed Module	70ns	120ns	66 pin HIP (H1)	5962-96900 01HYX
128K x 16 Mixed Module	70ns	120ns	68 lead CQFP/J (G1U)	5962-96900 01H9X
128K x 16 Mixed Module	35ns	70ns	66 pin HIP (H)	5962-96900 02HXX
128K x 16 Mixed Module	35ns	70ns	66 pin HIP (H1)	5962-96900 02HYX
128K x 16 Mixed Module	35ns	70ns	68 lead CQFP/J (G1U)	5962-96900 02H9X