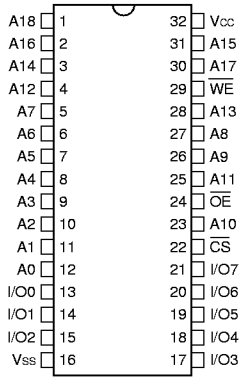
512Kx8 SRAM

*PRELIMINARY **

PIN CONFIGURATION
TOP VIEW



PIN DESCRIPTION

A_{0-18}	Address Inputs
I/O_{0-7}	Data Input/Output
$\overline{CS}$	Chip Select
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
V_{CC}	+5.0V Power
V_{SS}	Ground

PLASTIC PLUS™ FEATURES

- Access Times 55, 70, 85ns
- Standard Commercial Off-The-Shelf (COTS) Memory Devices for Extended Temperature Range
- JEDEC Standard Packages:
  - 32 Pin 600mil Plastic DIP
  - 32 Lead 525mil Plastic SOP
  - 32 Lead 400mil Plastic TSOP (II)
- Electrical and Speed Characteristics for:
  - Military Temperature (-55°C to +125°C)
  - Industrial Temperature (-40°C to +85°C)
- Burn-in and Temperature Cycling Available
- Organized as 512K x 8
- 5 Volt Power Supply
- Low Power CMOS
- Battery Back-Up Operation
- Reliability Test Data Available:
  - High Temperature Operating Life
  - High Temperature Storage
  - Pressure Cooker Test
  - Wet High Temperature Operating Life
  - Thermal Shock
  - Temperature Cycling

* *This data sheet describes a product under development, not fully characterized, and is subject to change without notice.*

PLASTIC PLUS SRAM

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Unit
Operating Temperature (Mil.)	T_A	-55	+125	°C
Operating Temperature (Ind.)	T_A	-40	+85	°C
Storage Temperature	T_{STG}	-65	+150	°C
Signal Voltage Relative to V_{SS}	V_G	-0.5	Vcc + 0.5	V
Supply Voltage	V_{CC}	-0.5	7.0	V

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V_{CC}	4.5	5.5	V
Input High Voltage	V_{IH}	2.2	Vcc + 0.5	V
Input Low Voltage	V_{IL}	-0.3	+0.8	V
Operating Temperature (Mil.)	T_A	-55	+125	°C
Operating Temperature (Ind.)	T_A	-40	+85	°C

TRUTH TABLE

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	Mode	I/O Pin	Vcc Current
H	X	X	Power Down	High-Z	I_{SB}
L	H	H	Out Disable	High-Z	I_{CC}
L	H	L	Read	D_{OUT}	I_{CC}
L	L	X	Write	D_{IN}	I_{CC}

CAPACITANCE

(T_A = +25°C)

Parameter	Symbol	Condition	Max	Unit
Input capacitance	C_{IN}	V_{IN} = 0V, f = 1.0MHz	8	pF
Output capicitance	C_{OUT}	V_{OUT} = 0V, f = 1.0MHz	10	pF

This parameter is guaranteed by design but not tested.

DC CHARACTERISTICS

(V_{CC} = 5V, V_{SS} = 0V, T_A = -55°C to +125°C)

Parameter	Symbol	Conditions	Min	Max	Units
Input Leakage Current	I_{LI}	V_{CC} = 5.5, V_{IN} = V_{SS} to V_{CC}		10	µA
Output Leakage Current	I_{LO}	$\overline{CS}$ = V_{IH}, $\overline{OE}$ = V_{IH}, V_{OUT} = V_{SS} to V_{CC}		10	µA
Operating Supply Current	I_{CC}	$\overline{CS}$ = V_{IL}, $\overline{OE}$ = V_{IH}, f = 5MHz, Vcc = 5.5		85	mA
Standby Current	I_{SB}	$\overline{CS}$ = V_{CC}, $\overline{OE}$ = V_{IH}, f = 5MHz		8	mA
Output Low Voltage	V_{OL}	I_{OL} = 2.1mA, Vcc = 4.5		0.4	V
Output High Voltage	V_{OH}	I_{OH} = -1.0mA, Vcc = 4.5	2.4		V

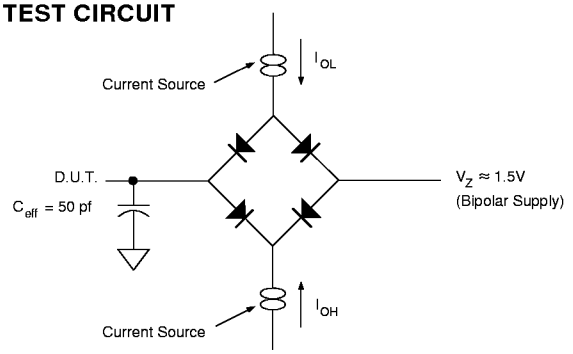
NOTE: DC test conditions: V_{IL} = 0.3V, V_{IH} = Vcc -0.3V

DATA RETENTION CHARACTERISTICS

(T_A = -55°C to +125°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Data Retention Supply Voltage	V_{DR}	$\overline{CS}$ ≥ Vcc - .2V	2.0		5.5	V
Data Retention Current	I_{CCDR}	Vcc = 3V		10	150	µA

AC TEST CIRCUIT



AC TEST CONDITIONS

Parameter	Typ	Unit
Input Pulse Levels	V_{IL} = 0, V_{IH} = 3.0	V
Input Rise and Fall	5	ns
Input and Output Reference Level	1.5	V
Output Timing Reference Level	1.5	V

NOTES:
V_Z is programmable from -2V to +7V.
I_{OL} & I_{OH} programmable from 0 to 16mA.
Tester Impedance Z_0 = 75 Ω.
V_Z is typically the midpoint of V_{OH} and V_{OL}.
I_{OL} & I_{OH} are adjusted to simulate a typical resistive load circuit.
ATE tester includes jig capacitance.

AC CHARACTERISTICS

(V_{CC} = 5.0V, V_{SS} = 0V, T_A = -55°C to +125°C)

Parameter Read Cycle	Symbol	-55		-70		-85		Units
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	55		70		85		ns
Address Access Time	t_{AA}		55		70		85	ns
Output Hold from Address Change	t_{OH}	5		5		5		ns
Chip Select Access Time	t_{ACS}		55		70		85	ns
Output Enable to Output Valid	t_{OE}		25		35		45	ns
Chip Select to Output in Low Z	t_{CLZ}[1]	10		10		10		ns
Output Enable to Output in Low Z	t_{OLZ}[1]	5		5		5		ns
Chip Disable to Output in High Z	t_{CHZ}[1]		20		25		30	ns
Output Disable to Output in High Z	t_{OHZ}[1]		20		25		30	ns

1. This parameter is guaranteed by design but not tested.

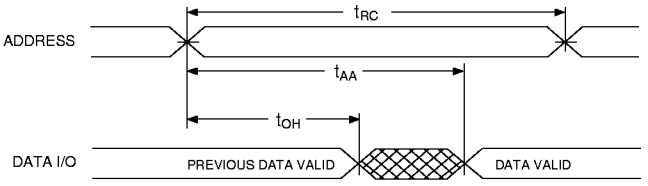
AC CHARACTERISTICS

(V_{CC} = 5.0V, V_{SS} = 0V, T_A = -55°C to +125°C)

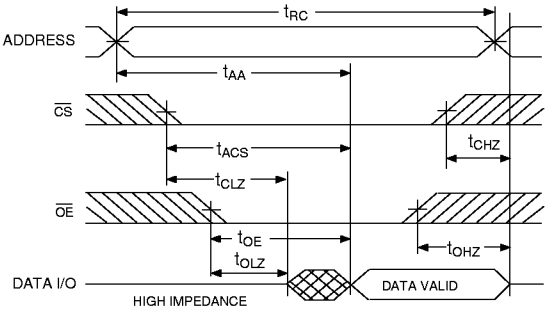
Parameter Write Cycle	Symbol	-55		-70		-85		Units
		Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{WC}	55		70		85		ns
Chip Select to End of Write	t_{CW}	45		60		70		ns
Address Valid to End of Write	t_{AW}	45		60		70		ns
Data Valid to End of Write	t_{DW}	25		30		35		ns
Write Pulse Width	t_{WP}	40		50		55		ns
Address Setup Time	t_{AS}	0		0		0		ns
Address Hold Time	t_{AH}	0		0		0		ns
Output Active from End of Write	t_{OW}[1]	5		5		5		ns
Write Enable to Output in High Z	t_{WHZ}[1]		25		30		35	ns
Data Hold Time	t_{DH}	0		0		0		ns

1. This parameter is guaranteed by design but not tested.

TIMING WAVEFORM - READ CYCLE

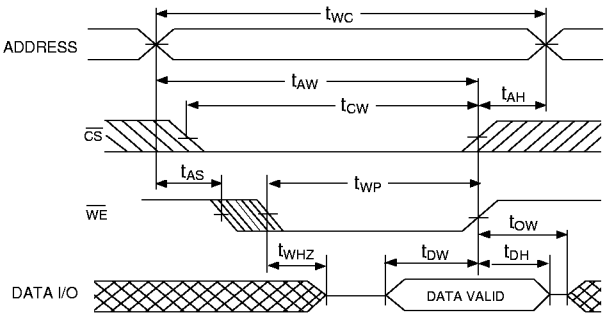


READ CYCLE 1 ($\overline{CS}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH})



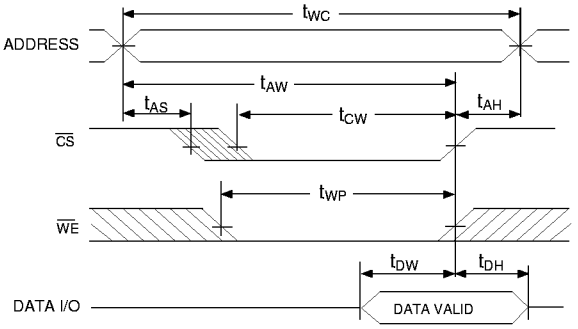
READ CYCLE 2 ($\overline{WE}$ = V_{IH})

WRITE CYCLE - $\overline{WE}$ CONTROLLED



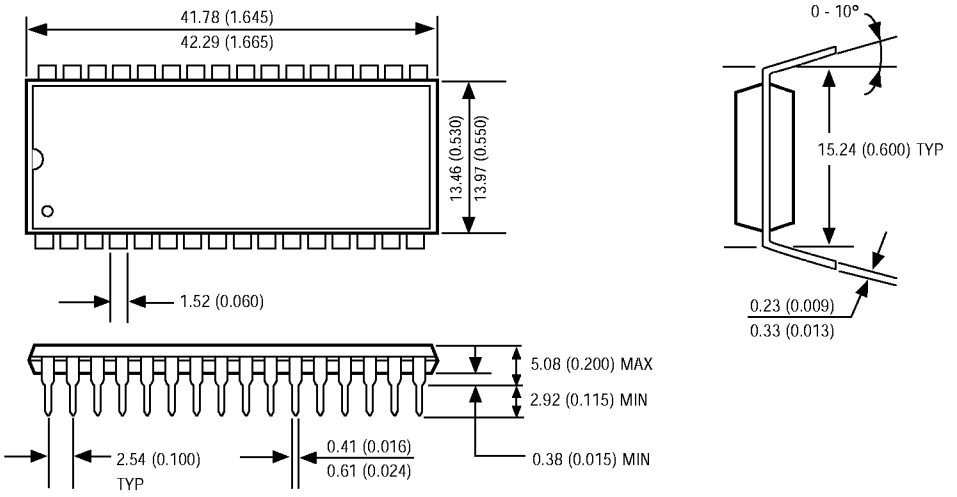
WRITE CYCLE 1, $\overline{WE}$ CONTROLLED

WRITE CYCLE - $\overline{CS}$ CONTROLLED



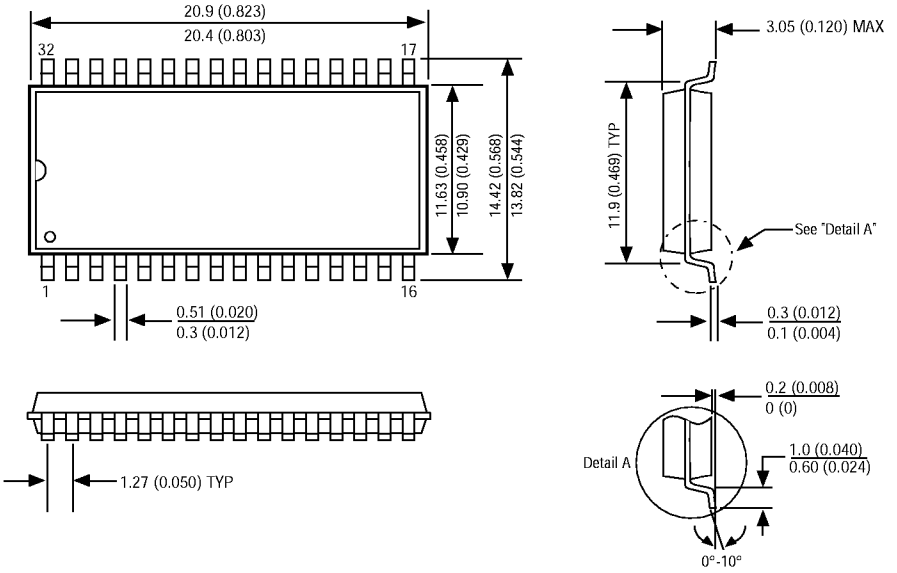
WRITE CYCLE 2, $\overline{CS}$ CONTROLLED

32 PIN, PLASTIC DIP PACKAGE DIMENSION



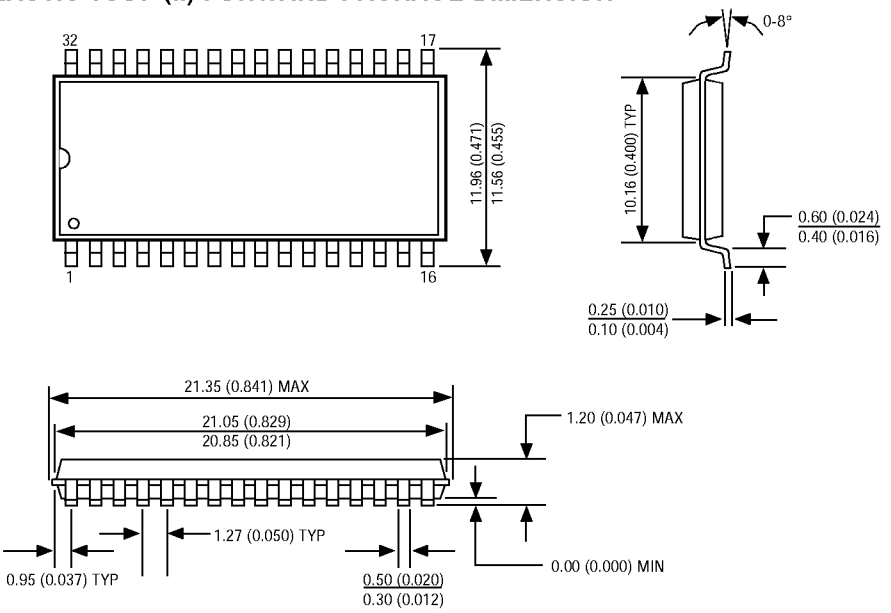
DIMENSIONS IN MILLIMETERS AND (INCHES)

32 LEAD, PLASTIC SOP PACKAGE DIMENSION



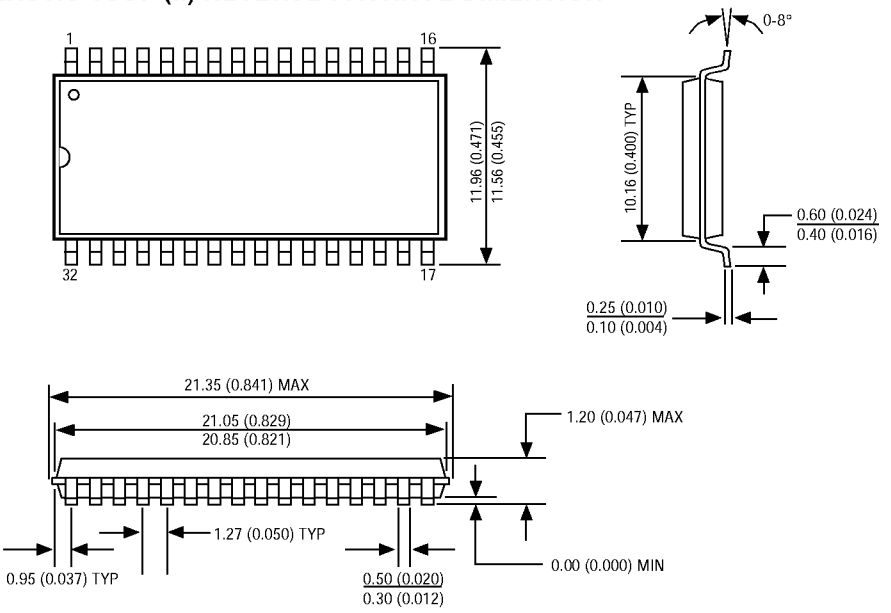
DIMENSIONS IN MILLIMETERS AND (INCHES)

32 LEAD, PLASTIC TSOP (II) FORWARD PACKAGE DIMENSION



DIMENSIONS IN MILLIMETERS AND (INCHES)

32 LEAD, PLASTIC TSOP (II) REVERSE PACKAGE DIMENSION



DIMENSIONS IN MILLIMETERS AND (INCHES)

ORDERING INFORMATION