Winbond Electronics Corp.

166MHZ CLOCK FOR SIS CHIPSET

1. GENERAL DESCRIPTION

The W83194R-630A is a Clock Synthesizer for SiS 540/630 chipset. W83194R-630A provides all clocks required for high-speed RISC or CISC microprocessor such as AMD,Cyrix,Intel Pentium, Pentium II and also provides 16 different frequencies of CPU clocks frequency setting. All clocks are externally selectable with smooth transitions. The W83194R-630A makes SDRAM in synchronous or asynchronous frequency with CPU clocks.

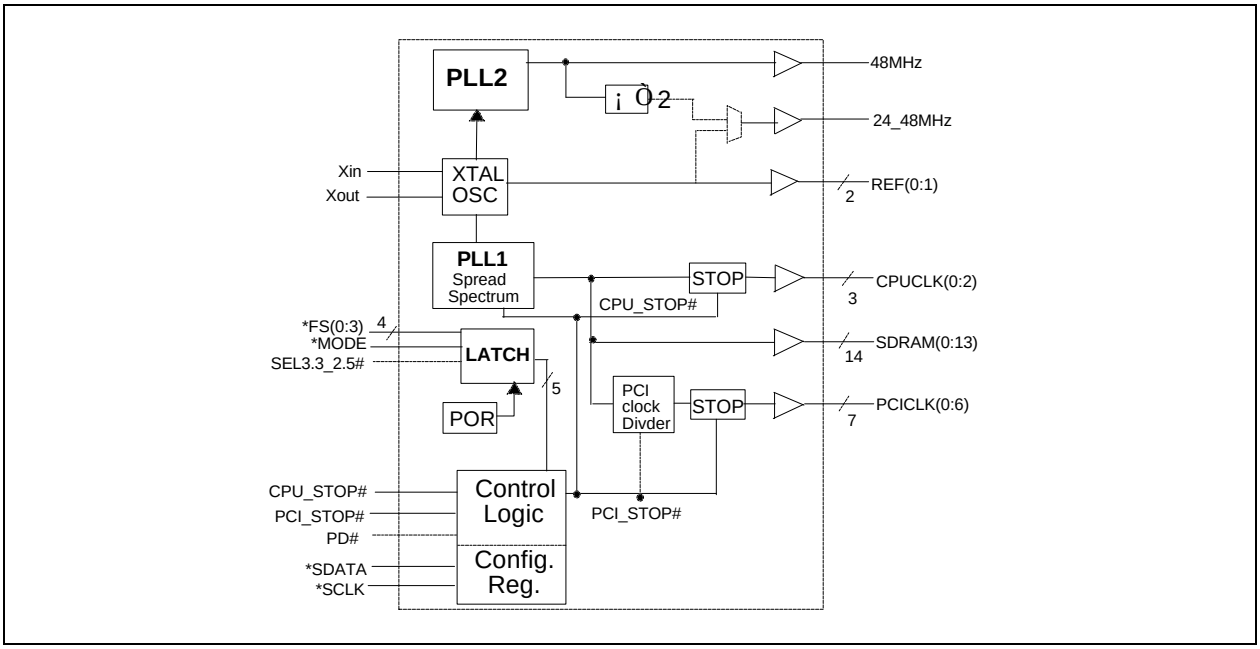
The W83194R-630A provides I^2C serial bus interface to program the registers to enable or disable each clock outputs and W83194R-630A provides the 0.5%, 0.75% center type and 0~0.5% down type spread spectrum to reduce EMI.

The W83194R-630A accepts a 14.318 MHz reference crystal as its input and runs on a 3.3V supply. High drive PCI and SDRAM CLOCK outputs typically provide greater than 1 V /ns slew rate into 30 pF loads. CPU CLOCK outputs typically provide better than 1 V /ns slew rate into 20 pF loads as maintaining 50± 5% duty cycle. The fixed frequency outputs as REF, 24MHz, and 48 MHz provide better than 0.5V /ns slew rate.

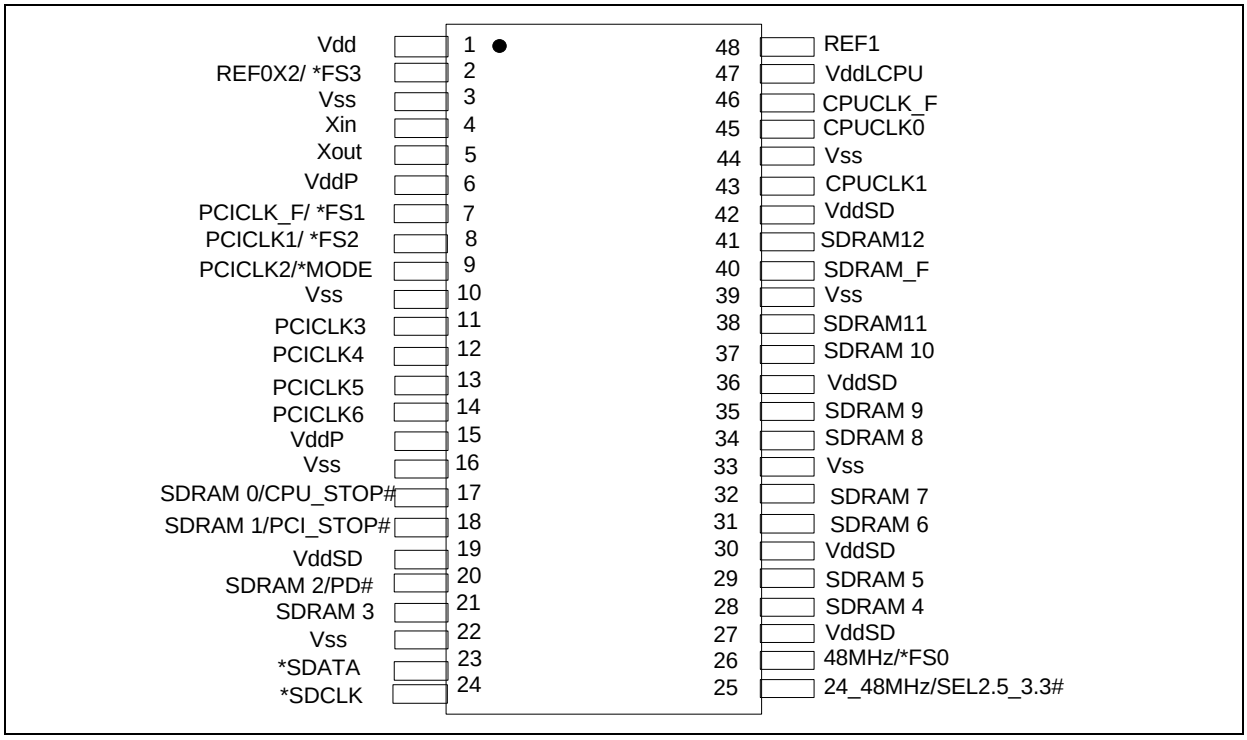
2. PRODUCT FEATURES

- Supports Pentium™, Pentium™ II, AMD and Cyrix CPUs with I^2C.
- 3 CPU clocks
- 14 SDRAM clocks for 3 DIMMs
- 7 PCI synchronous clocks.
- Optional single or mixed supply:
  (All Vdd = 3.3V) or (Other s Vdd = 3.3V, VddLCPU=2.5V)
- Skew form CPU to PCI clock 1 to 4 ns, center 2.6 ns
- SDRAM frequency synchronous or asynchronous to CPU clocks
- Smooth frequency switch with selections from 66 to 166mhz
- I^2C 2-Wire serial interface and I^2C read back
- **0.5%, 0.75%center type, 0~0.5% down type spread spectrum to reduce EMI**
- Programmable registers to enable/stop each output and select modes
  (mode as Tri-state or Normal)
- 48 MHz for USB
- 24 MHz for super I/O
- Packaged in 48-pin SSOP

3. BLOCK DIAGRAM



4. PIN CONFIGURATION



5. PIN DESCRIPTION

IN - Input
OUT - Output
I/O - Bi-directional Pin
- Active Low
* - Internal 250kΩ pull-up

5.1 Crystal I/O

SYMBOL	PIN	I/O	FUNCTION
Xin	4	IN	Crystal input with internal loading capacitors and feedback resistors.
Xout	5	OUT	Crystal output at 14.318MHz nominally.

5.2 CPU, SDRAM, PCI Clock Outputs

SYMBOL	PIN	I/O	FUNCTION
CPUCLK_F	46	OUT	Low skew (< 250ps) clock outputs for host frequencies such as CPU, Chipset and Cache. VddLCPU is the supply voltage for these outputs. This pin will not be stopped by CPU_STOP#
CPUCLK [0:1]	45,43	OUT	Low skew (< 250ps) clock outputs for host frequencies such as CPU, Chipset and Cache. VddLCPU is the supply voltage for these outputs.
SDRAM_F	40	OUT	SDRAM clock outputs which have syn. or asyn. frequencies as CPU clocks. This pin will not be stopped by CPU_STOP#
SDRAM0/CPU_STOP#	17	I/O	SDRAM clock outputs which have syn. or asyn. frequencies as CPU clocks. CPU_STOP# input pin when MODE=0.
SDRAM1/PCI_STOP#	18	I/O	SDRAM clock outputs which have syn. or asyn. frequencies as CPU clocks. PCI_STOP# input pin when MODE=0.
SDRAM2/PD#	20	I/O	SDRAM clock outputs which have syn. or asyn. frequencies as CPU clocks. PD# input pin when MODE=0.
SDRAM[3:12]	21,28,29,31,32,34,35,37,38,41	OUT	SDRAM clock outputs which have syn. or asyn. frequencies as CPU clocks.
PCICLK_F/ *FS1	7	I/O	Latched input for FS1 at initial power up for H/W selecting the output frequency of CPU, SDRAM and PCI clocks.

			PCI free-running clock during normal operation.
PCICLK 1/ *FS2	8	I/O	Latched input for FS2 at initial power up for H/W selecting the output frequency of CPU, SDRAM and PCI clocks. PCI clock during normal operation.
PCICLK 2/ *MODE	9	I/O	Latched input for MODE at initial power up for input selection of CPU_STOP#, PCI_STOP# and PD#. When MODE=1, the above pins are SDRAM clock outputs. When MODE=0, the pins are inputs ACPI pins. PCI clock during normal operation.
PCICLK [3:6]	11,12,13,14	OUT	Low skew (< 250ps) PCI clock outputs.

5.3 I^2C Control Interface

SYMBOL	PIN	I/O	FUNCTION
*SDATA	23	I/O	Serial data of I^2C 2-wire control interface
*SDCLK	24	IN	Serial clock of I^2C 2-wire control interface

5.4 Fixed Frequency Outputs

SYMBOL	PIN	I/O	FUNCTION
REF0X2 / *FS3	2	I/O	3.3V, 14.318MHz reference clock output . Internal 250kΩ pull-up. Latched input for FS3 at initial power up for H/W selecting the output frequency of CPU, SDRAM and PCI clocks.
REF1	48	I/O	3.3V , 14.318MHz reference clock output.
24_48MHz/ SEL2.5_3.3#	25	I/O	SEL2.5_3.3# controls the Vdd of CPU. If logic 0 at power on, VddLCPU=3.3V. If logic 1, VddLCPU=2.5 24MHz or 48MHz selected by I2C for Super I/O.
48MHz / *FS0	26	I/O	Internal 250kΩ pull-up. Latched input for FS0 at initial power up for H/W selecting the output frequency of CPU, SDRAM and PCI clocks. 48MHz output for USB during normal operation.

5.5 Power Pins

SYMBOL	PIN	FUNCTION
Vdd	1	Power supply for REF crystal and core logic.
VddLCPU	47	Power supply for CPUCLK_F and CPUCLK[0:1], either 2.5V or 3.3V.
VddP	6,15	Power supply for PCI outputs.
VddSD	19,27,30,36,42	Power supply for SDRAM and 48/24NHz outputs.
Vss	3,10,16,22,33,39,44	Circuit Ground.

6. FREQUENCY SELECTION BY HARDWARE

FS3	FS2	FS1	FS0	CPU (MHz)	SDRAM (MHz)	PCI (MHz)	REF (MHz) IOAPIC
0	0	0	0	66.8	100.2	33.4	14.318
0	0	0	1	100.2	100.2	33.4	14.318
0	0	1	0	83.3	83.3	33.2	14.318
0	0	1	1	133.6	100.2	33.4	14.318
0	**1**	**0**	**0**	**75**	**75**	**37.5**	**14.318**
0	1	0	1	100.2	133.6	33.4	14.318
0	1	1	0	100.2	150.3	33.4	14.318
0	1	1	1	133.6	133.6	33.4	14.318
1	0	0	0	66.8	66.8	33.4	14.318
1	0	0	1	97	97	32.3	14.318
1	0	1	0	97	129.3	32.3	14.318
1	0	1	1	95.2	95.2	31.7	14.318
1	1	0	0	140	140	35	14.318
1	1	0	1	112	112	37.3	14.318
1	1	1	0	96.2	96.2	32.1	14.318
1	1	1	1	166	166	33.3	14.318

7. SEL3.3_2.5# BUFFER SELECTION

SEL3.3_2.5# (Pin 25) Input Level	CPU Operate at
1	VDDLCPU = 2.5V
0	VDDLCPU = 3.3V

8. FUNCTION DESCRIPTION

8.1 2-WIRE I²C CONTROL INTERFACE

The clock generator is a slave I2C component which can be read back the data stored in the latches for verification. All proceeding bytes must be sent to change one of the control bytes. The 2-wire control interface allows each clock output individually enabled or disabled. On power up, the W83194R-630A initializes with default register settings, and then it帰 ptional to use the 2-wire control interface.

The SDATA signal only changes when the SDCLK signal is low, and is stable when SDCLK is high during normal data transfer. There are only two exceptions. One is a high-to-low transition on SDATA while SDCLK is high used to indicate the beginning of a data transfer cycle. The other is a low-to-high transition on SDATA while SDCLK is high used to indicate the end of a data transfer cycle. Data is always sent as complete 8-bit bytes followed by an acknowledge generated.

Byte writing starts with a start condition followed by 7-bit slave address [1101 0010], command code checking [0000 0000], and byte count checking. After successful reception of each byte, an acknowledge (low) on the SDATA wire will be generated by the clock chip. Controller can start to write to internal I²C registers after the string of data. The sequence order is as follows:

Bytes sequence order for I²C controller :

Clock Address A(6:0) & R/W	**Ack**	**8 bits dummy Command code**	**Ack**	**8 bits dummy Byte count**	**Ack**	**Byte0,1,2... until Stop**

Set R/W to 1 when read back the data sequence is as follows, [1101 0011] :

Clock Address A(6:0) & R/W	**Ack**	**Byte 0**	**Ack**	**Byte 1**	**Ack**	**Byte2, 3, 4... until Stop**

8.2 SERIAL CONTROL REGISTERS

The Pin column lists the affected pin number and the @PowerUp column gives the state at true power up. Registers are set to the values shown only on true power up. "Command Code" byte and "Byte Count" byte must be sent following the acknowledge of the Address Byte. Although the data (bits) in these two bytes are considered "don't care", they must be sent and will be acknowledge. After that, the below described sequence (Register 0, Register 1, Register 2, ...) will be valid and acknowledged.

Frequency table by I2C

SSEL3	SSEL2	SSEL1	SSEL0	CPU (MHz)	SDRAM (MHz)	PCI (MHz)	REF (MHz) IOAPIC
0	0	0	0	66.8	100.2	33.4	14.318
0	0	0	1	100.2	100.2	33.4	14.318
0	0	1	0	83.3	124.9	33.2	14.318
0	0	1	1	133.6	100.2	33.4	14.318
0	**1**	**0**	**0**	**75**	**75**	**37.5**	14.318
0	1	0	1	100.2	133.6	33.4	14.318
0	1	1	0	100.2	150.3	33.4	14.318
0	1	1	1	133.6	133.6	33.4	14.318
1	0	0	0	66.8	66.8	33.4	14.318
1	0	0	1	97	97	32.3	14.318
1	0	1	0	97	129.3	32.3	14.318
1	0	1	1	95.2	95.2	31.7	14.318
1	1	0	0	140	140	35	14.318
1	1	0	1	112	112	37.3	14.318
1	1	1	0	96.2	96.2	32.1	14.318
1	1	1	1	166	166	33.3	14.318

8.2.1 Register 0: CPU Frequency Select Register (default = 0)

Bit	@PowerUp	Pin	Description
7	0	-	0 = ±0.5% Center type Spread Spectrum Modulation 1 = ±0.75% Center type Spread Spectrum Modulation
6	0	-	SSEL2 (for frequency table selection by software via I^2C)
5	0	-	SSEL1 (for frequency table selection by software via I^2C)
4	0	-	SSEL0 (for frequency table selection by software via I^2C)
3	0	-	0 = Selection by hardware 1 = Selection by software I^2C - Bit 2, 6:4
2	0	-	SSEL3 (for frequency table selection by software via I^2C)
1	0	-	0 = Normal 1 = Spread Spectrum enabled
0	0	-	0 = Running 1 = Tristate all outputs

8.2.2 Register 1 : CPU Clock Register (1 = Active, 0 = Inactive)

Bit	@PowerUp	Pin	Description
7	x	-	Latched FS2#
6	1	-	Reserved
5	1	-	0 = 0.5% down type spread, overrides Byte0-bit7. 1= Center type spread.
4	1	-	Reserved
3	1	43	CPUCLK2 (Active / Inactive)
2	1	45	CPUCLK1 (Active / Inactive)
1	1	46	CPUCLK0 (Active / Inactive)
0	1	-	Reserved

8.2.3 Register 2: PCI Clock Register (1 = Active, 0 = Inactive)

Bit	@PowerUp	Pin	Description
7	1	-	Reserved
6	1	14	PCICLK6 (Active / Inactive)
5	1	13	PCICLK5 (Active / Inactive)
4	1	12	PCICLK4 (Active / Inactive)
3	1	11	PCICLK3 (Active / Inactive)
2	1	9	PCICLK2 (Active / Inactive)
1	1	8	PCICLK1 (Active / Inactive)
0	1	7	PCICLK0 (Active / Inactive)

8.2.4 Register 3: Control Register (1 = Active, 0 = Inactive)

Bit	@PowerUp	Pin	Description
7	1	-	1 Pin25 24_48MHz = 24MHz 0 Pin25 24_48MHz = 48MHz
6	x	-	Latched FS0#
5	1	26	48MHz (Active / Inactive)
4	1	25	24-48MHz (Active / Inactive)
3	1	-	Reserved
2	1	-	Reserved
1	1	48	REF1 (Active / Inactive)
0	1	2	REF0X2 (Active / Inactive)

8.2.5 Register 4: SDRAM Register (1 = Active, 0 = Inactive)

Bit	@PowerUp	Pin	Description
7	1	41	SDRAM13 (Active / Inactive)
6	1	40	SDRAM12 (Active / Inactive)
5	1	38	SDRAM11 (Active / Inactive)
4	1	37	SDRAM10 (Active / Inactive)
3	x	X	Latched FS1#
2	1	35	SDRAM9 (Active / Inactive)
1	x	X	Latched FS3#
0	1	34	SDRAM8 (Active / Inactive)

8.2.6 Register 5: SDRAM Register(1 = Active, 0 = Inactive)

Bit	@PowerUp	Pin	Description
7	1	32	SDRAM7 (Active / Inactive)
6	1	31	SDRAM6 (Active / Inactive)
5	1	29	SDRAM5 (Active / Inactive)
4	1	28	SDRAM4 (Active / Inactive)
3	1	21	SDRAM3 (Active / Inactive)
2	1	20	SDRAM2 (Active / Inactive)
1	1	18	SDRAM1 (Active / Inactive)
0	1	17	SDRAM0 (Active / Inactive)

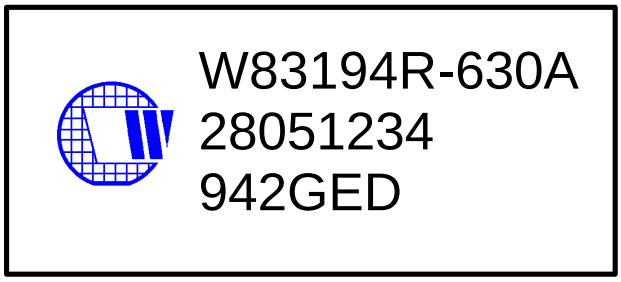
8.2.7 Register 6: Winbond Chip ID Register (Read Only)

Bit	@PowerUp	Pin	Description
7	0	-	Winbond Chip ID
6	1	-	Winbond Chip ID
5	0	-	Winbond Chip ID
4	1	-	Winbond Chip ID
3	1	-	Winbond Chip ID
2	0	-	Winbond Chip ID
1	0	-	Winbond Chip ID
0	1	-	Winbond Chip ID

9. ORDERING INFORMATION

Part Number	Package Type	Production Flow
W83194R-630A	48 PIN SSOP	Commercial, 0°C to +70°C

10. HOW TO READ THE TOP MARKING



1st line: Winbond logo and the type number: W83194R-630A

2nd line: Tracking code 2 8051234

2: wafers manufactured in Winbond FAB 2

8051234: wafer production series lot number

3rd line: Tracking code 942 G E D

942: packages made in '99, week 42

G: assembly house ID; O means OSE, G means GR

E: Internal use code

D: IC revision

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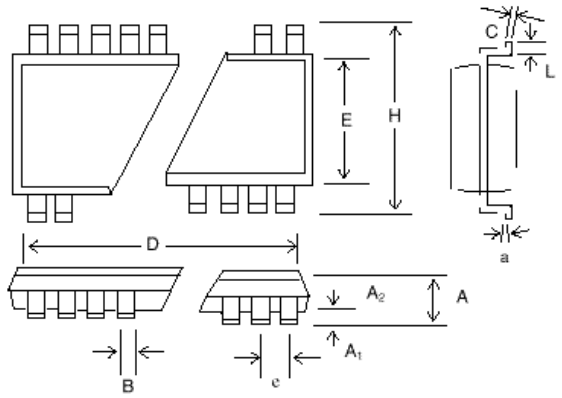
11. PACKAGE DRAWING AND DIMENSIONS



48 PIN SSOP OUTLINE DIMENSIONS

SYMBOL	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	-	-	0.110	0	0	2.79
A_1	0.008	0.012	0.016	0.20	0.30	0.41
A2	0.085	0.090	0.095	2.16	2.29	2.41
b	0.008	0.010	0.013	0.20	0.25	0.33
C	0.006	0.008	0.010	0.15	0.20	0.25
D	-	0.625	0.637	-	15.88	16.18
E	0.291	0.295	0.299	7.39	7.49	7.59
e	0.025 BSC			0.64 BSC		
H	0.395	0.408	0.420	10.03	10.36	10.67
L	0.025	0.030	0.040	0.64	0.76	1.02
a	0°	5°	8°	0°	5°	8°

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