100 MHZ AGP CLOCK FOR VIA CHIPSET

1.0 GENERAL DESCRIPTION

The W83194R-37/-58 is a Clock Synthesizer for VIA chipset. W83194R-37 provides all clocks required for high-speed RISC or CISC microprocessor such as Intel PentiumPro, AMD or Cyrix. Eight different frequencies of CPU, W83194R-58 provides all clocks required for high-speed RISC or CISC microprocessor such as Intel PentiumII and also provides 16 different frequencies of CPU clocks by software setting (additional register0 bit2). AGP and PCI clocks are externally selectable with smooth transitions. The W83194R-37/-58 provides AGP clocks especially for clone chipset, and makes SDRAM in synchronous frequency with CPU or AGP clocks.

The W83194R-37/-58 provides I^2C serial bus interface to program the registers to enable or disable each clock outputs and choose the 0.25%, 0.5% or 0.5%,1.5% center type spread spectrum to reduce EMI.

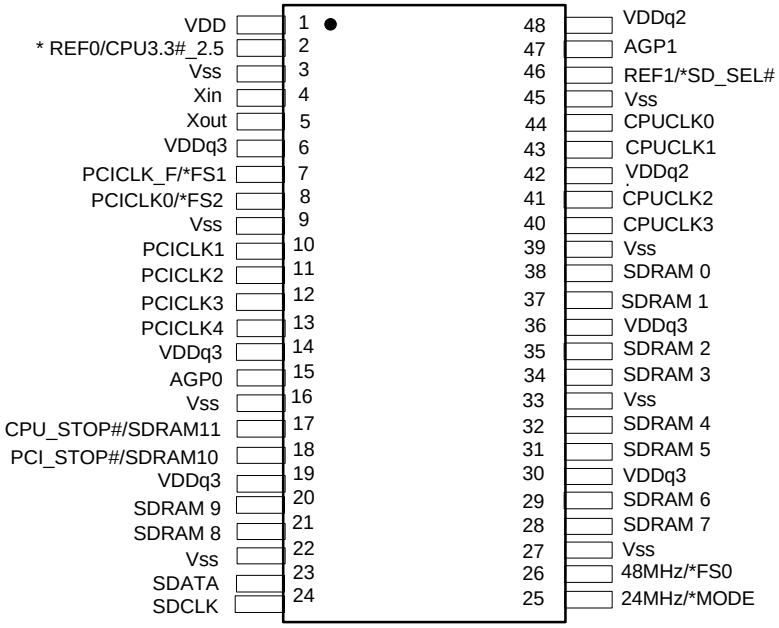
The W83194R-37/-58 accepts a 14.318 MHz reference crystal as its input and runs on a 3.3V supply. High drive PCI and SDRAM CLOCK outputs typically provide greater than 1V /nS slew rate into 30 pF loads. CPU CLOCK outputs typically provide better than 1V /nS slew rate into 20 pF loads as maintaining 50 ±5% duty cycle. The fixed frequency outputs as REF, 24 MHz, and 48 MHz provide better than 0.5V /nS slew rate.

2.0 FEATURES

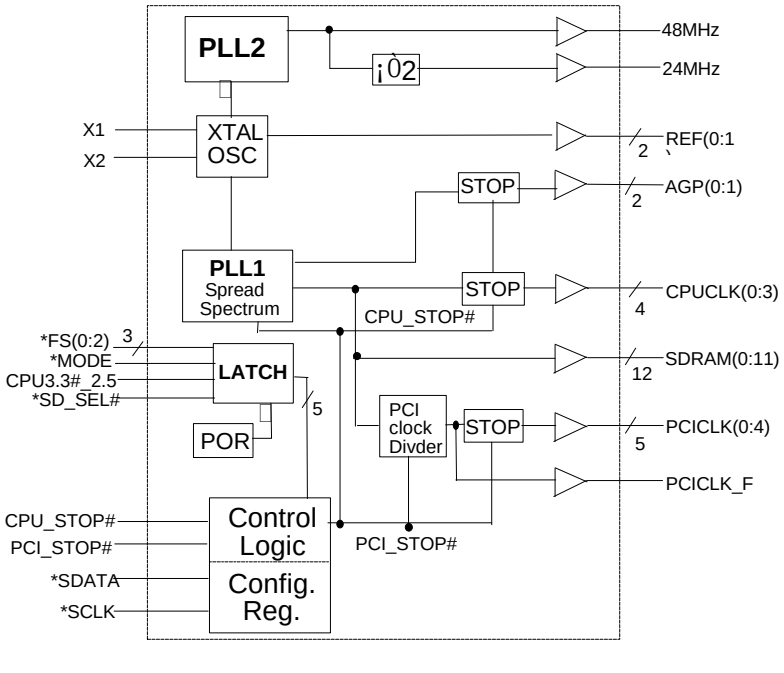
- Supports Pentium™, Pentium™ Pro, Pentium™ II, AMD and Cyrix CPUs with I^2C.
- 4 CPU clocks
- 12 SDRAM clocks for 3 DIMs
- Two AGP clocks
- 6 PCI synchronous clocks.
- Optional single or mixed supply:

  (V_{DD} = V_{DD}q3 = V_{DD}q2 = V_{DD}q2b = 3.3V) or (V_{DD} = V_{DD}q3 = V_{DD}q2 = 3.3V, V_{DD}q2b = 2.5V)
- Skew form CPU to PCI clock -1 to 4 nS, center 2.6 nS, AGP to CPU sync. skew 0 nS (250 pS)
- SDRAM frequency synchronous to CPU or AGP clocks
- Smooth frequency switch with selections from 60 to 100 MHz CPU (-37) and 66 to 150 MHz (-58)
- I^2C 2-Wire serial interface and I^2C read back
- ±0.5% or ±1.5% (-37) and 0.25%, 0.5% (-58) center type spread spectrum to reduce EMI
- Programmable registers to enable/stop each output and select modes (mode as Tri-state or Normal)
- MODE pin for power Management
- 48 MHz for USB
- 24 MHz for super I/O
- Packaged in 48-pin SSOP

3.0 PIN CONFIGURATION



4.0 BLOCK DIAGRAM



5.0 PIN DESCRIPTION

IN - Input
OUT - Output
I/O - Bi-directional Pin
- Active Low
* - Internal 250kΩ pull-up

5.1 Crystal I/O

SYMBOL	PIN	I/O	FUNCTION
Xin	4	IN	Crystal input with internal loading capacitors and feedback resistors.
Xout	5	OUT	Crystal output at 14.318 MHz nominally.

5.2 CPU, SDRAM, PCI Clock Outputs

SYMBOL	PIN	I/O	FUNCTION
CPUCLK [0:3]	40, 41, 43, 44	OUT	Low skew (< 250 pS) clock outputs for host frequencies such as CPU, Chipset and Cache. VDDq2b is the supply voltage for these outputs.
AGP[0:1]	15, 47	OUT	Accelerate Graphic Port clock outputs
SDRAM11/ CPU_STOP#	17	I/O	If MODE = 1 (default), then this pin is a SDRAM clock buffered output of the crystal. If MODE = 0, then this pin is CPU_STOP# input used in power management mode for synchronously stopping the all CPU clocks.
SDRAM10/ PCI_STOP#	18	I/O	If MODE = 1 (default), then this pin is a SDRAM clock output. If MODE = 0, then this pin is PCI_STOP # and used in power management mode for synchronously stopping the all PCI clocks.
SDRAM [0:9]	20, 21, 28, 29, 31, 32, 34, 35, 37, 38	O	SDRAM clock outputs which have the same frequency as CPU clocks.
PCICLK_F/ *FS1	7	I/O	Latched input for FS1 at initial power up for H/W selecting the output frequency of CPU, SDRAM and PCI clocks. Free running PCI clock during normal operation.
PCICLK 0/ *FS2	8	I/O	Latched input for FS2 at initial power up for H/W selecting the output frequency of CPU, SDRAM and PCI clocks. PCI clock during normal operation.
PCICLK [1:4]	10, 11, 12, 13	OUT	Low skew (< 250 pS) PCI clock outputs.

5.3 I²C Control Interface

SYMBOL	PIN	I/O	FUNCTION
SDATA	23	I/O	Serial data of I²C 2-wire control interface
SDCLK	24	IN	Serial clock of I²C 2-wire control interface

5.4 Fixed Frequency Outputs

SYMBOL	PIN	I/O	FUNCTION
REF0/ CPU3.3#_2.5	2	I/O	Internal 250 KΩ pull-up. Latched input for CPU3.3#_2.5 at initial power up. Reference clock during normal operation. Latched high - VDDq2b = 2.5V Latched low - VDDq2b = 3.3V
REF1/*SD_SEL#	46	I/O	Internal 250 KΩ pull-up. Latched input at Power On selects either CPU(SDSEL = 1) or AGP(SD_SEL = 0) frequencies for SDRAM clock outputs.
24MHz/ *MODE	25	I/O	Internal 250 KΩ pull-up. Latched input for MODE at initial power up. 24 MHz output for super I/O during normal operation.
48MHz/ *FS0	26	I/O	Internal 250 KΩ pull-up. Latched input for FS0 at initial power up for H/W selecting the output frequency of CPU, SDRAM and PCI clocks. 48 MHz output for USB during normal operation.

5.5 Power Pins

SYMBOL	PIN	FUNCTION
VDD	1	Power supply for Ref [0:1] crystal and core logic.
VDDq2	42	Power supply for AGP1 and REF1 output, either 2.5V or 3.3V.
VDDq2b	48	Power supply for CPUCLK[0:3], either 2.5V or 3.3V.
VDDq3	6, 14, 19, 30, 36	Power supply for SDRAM, PCICLK and 48/24 MHz outputs.
Vss	3, 9, 16, 22, 27, 33, 39, 45	Circuit Ground.

6.0 FREQUENCY SELECTION BY HARDWARE

6.1 W83194R-37 Frequency Selection Table

FS2	FS1	FS0	CPU (MHz)	SDRAM (MHz)		PCI (MHz)	AGP (MHz)	REF (MHz)
				SD_SEL = 1	SD_SEL = 0			
0	0	0	60	60	60	30	60	14.318
0	0	1	66.8	66.8	66.8	33.4	66.8	14.318
0	1	0	68.5	68.5	68.5	34.25	68.5	14.318
0	1	1	75	75	75	37.5	75	14.318
1	0	0	75	75	60	30	60	14.318
1	0	1	83.3	83.3	66.6	33.3	66.6	14.318
1	1	0	95	95	63.4	31.7	63.4	14.318
1	1	1	100	100	66.6	33.3	66.6	14.318

6.2 W83194R-58 Frequency Selection Table

FS2	FS1	FS0	CPU (MHz)	SDRAM (MHz)		PCI (MHz)	AGP (MHz)	REF (MHz)
				SD_SEL = 1	SD_SEL = 0			
0	0	0	112	112	74.7	37.3	74.7	14.318
0	0	1	66.8	66.8	66.8	33.4	66.8	14.318
0	1	0	124	124	82.5	41.3	82.5	14.318
0	1	1	75	75	75	37.5	75	14.318
1	0	0	133.3	133.3	88.7	44.3	88.7	14.318
1	0	1	83.3	83.3	66.6	33.3	66.6	14.318
1	1	0	95.25	95.25	63.5	31.75	63.5	14.318
1	1	1	100.2	100.2	66.8	33.4	66.8	14.318

7.0 CPU 3.3#_2.5 BUFFER SELECTION

CPU 3.3#_2.5 (Pin 2) Input Level	CPU Operate at
1	V_{DD} = 2.5V
0	V_{DD} = 3.3V

8.0 FUNCTION DESCRIPTION

8.1 Power Management Functions

All clocks can be individually enabled or disabled via the 2-wire control interface. On power up, external circuitry should allow 3 mS for the VCO to stabilize prior to enabling clock outputs to assure correct pulse widths. When MODE = 0, pins 18 and 17 are inputs (PCI_STOP#), (CPU_STOP#), when MODE = 1, these functions are not available. A particular clock could be enabled as both the 2-wire serial control interface and one of these pins indicate that it should be enabled.

The W83194R-37/-58 may be disabled in the low state according to the following table in order to reduce power consumption. All clocks are stopped in the low state, but maintain a valid high period on transitions from running to stop. The CPU and PCI clocks transform between running and stop by waiting for one positive edge on PCICLK_F followed by negative edge on the clock of interest, after which high levels of the output are either enabled or disabled.

CPU_STOP#	PCI_STOP#	CPU & AGP	PCI	OTHER CLKs	XTAL & VCOs
0	0	Low	Low	Running	Running
0	1	Low	Running	Running	Running
1	0	Running	Low	Running	Running
1	1	Running	Running	Running	Running

8.2 2-Wire I^{2}C Control Interface

The clock generator is a slave I^{2}C component which can be read back the data stored in the latches for verification. All proceeding bytes must be sent to change one of the control bytes. The 2-wire control interface allows each clock output individually enabled or disabled. On power up, the W83194R-37/-58 initializes with default register settings, and then it optional to use the 2-wire control interface.

The SDATA signal only changes when the SDCLK signal is low, and is stable when SDCLK is high during normal data transfer. There are only two exceptions. One is a high-to-low transition on SDATA while SDCLK is high used to indicate the beginning of a data transfer cycle. The other is a low-to-high transition on SDATA while SDCLK is high used to indicate the end of a data transfer cycle. Data is always sent as complete 8-bit bytes followed by an acknowledge generated.

Byte writing starts with a start condition followed by 7-bit slave address [1101 0010], command code checking [0000 0000], and byte count checking. After successful reception of each byte, an acknowledge (low) on the SDATA wire will be generated by the clock chip. Controller can start to write to internal I^{2}C registers after the string of data. The sequence order is as follows:

Bytes sequence order for I^{2}C controller:

Clock Address A(6:0) & R/W	**Ack**	**8 bits dummy Command code**	**Ack**	**8 bits dummy Byte count**	**Ack**	**Byte0,1,2... until Stop**

Set R/W to 1 when read back the data sequence is as follows:

Clock Address A(6:0) & R/W	**Ack**	**Byte 0**	**Ack**	**Byte 1**	**Ack**	**Byte2, 3, 4... until Stop**

8.3 Serial Control Registers

The Pin column lists the affected pin number and the @PowerUp column gives the state at true power up. Registers are set to the values shown only on true power up. "Command Code" byte and "Byte Count" byte must be sent following the acknowledge of the Address Byte. Although the data (bits) in these two bytes are considered "don't care", they must be sent and will be acknowledge. After that, the below described sequence (Register 0, Register 1, Register 2, ...) will be valid and acknowledged.

8.3.1 Register 0: CPU Frequency Select Register

BIT	@POWERUP	PIN	DESCRIPTION
7	0	-	0 = ±1.5% Spread Spectrum Modulation (W83194R-37) 1 = ±0.5% Spread Spectrum Modulation 0 = ±0.25% Center Type Spread Spectrum Modulation (W83194R-58) 1 = ±0.5% Center Type Spread Spectrum Modulation
6	0	-	SSEL2 (Frequency table selection by software via I^2C)
5	0	-	SSEL1 (Frequency table selection by software via I^2C)
4	0	-	SSEL0 (Frequency table selection by software via I^2C)
3	0	-	0 = Selection by hardware 1 = Selection by software I^2C - Bit 6:4
2	0	-	SSEL3 (Frequency table selection by software via I^2C for W83194R-58)
2	0	-	0 = Spread spectrum center type (W83194R-37) 1 = Spread spectrum down type (W83194R-37)
1	0	-	0 = Normal 1 = Spread Spectrum enabled
0	0	-	0 = Running 1 = Tristate all outputs

W83194R-37 Frequency table selection by software via I^2C

SSEL2	SSEL1	SSEL0	CPU(MHz)	SDRAM (MHz)		PCI (MHz)	AGP (MHz)	REF (MHz)
				SD_SEL=1	SD_SEL=0			
0	0	0	60	60	60	30	60	14.318
0	0	1	66.8	66.8	66.8	33.4	66.8	14.318
0	1	0	68.5	68.5	68.5	34.25	68.5	14.318
0	1	1	75	75	75	37.5	75	14.318
1	0	0	75	75	60	30	60	14.318
1	0	1	83.3	83.3	66.6	33.3	66.6	14.318
1	1	0	95	95	63.4	31.7	63.4	14.318
1	1	1	100	100	66.6	33.3	66.6	14.318

W83194R-58 Frequency table selection by software via I^2C

SSEL2	SSEL1	SSEL0	Register0 Bit2	CPU	SDRAM	(MHz)	PCI	AGP	REF
			SSEL3	(MHz)	SD_SEL=1	SD_SEL=0	(MHz)	(MHz)	(MHz)
0	0	0	0	112	112	74.7	37.3	74.7	14.318
0	0	1	0	66.8	66.8	66.8	33.4	66.8	14.318
0	1	0	0	124	124	82.7	41.3	82.7	14.318
0	1	1	0	75	75	75	37.5	75	14.318
1	0	0	0	133.3	133.3	88.7	44..3	88.7	14.318
1	0	1	0	83.3	83.3	66.6	33.3	66.6	14.318
1	1	0	0	95.25	95.25	63.5	31.75	63.5	14.318
1	1	1	0	100.2	100.2	66.8	33.4	66.8	14.318
0	0	0	1	103	103	68.7	34.3	68.7	14.318
0	0	1	1	112	112	74.7	37.3	74.7	14.318
0	1	0	1	115	115	76.6	38.3	76.6	14.318
0	1	1	1	120	120	80	40	80	14.318
1	0	0	1	124	124	82	31	82	14.318
1	0	1	1	133.3	133.3	66.6	33.3	66.6	14.318
1	1	0	1	140	140	70	35	70	14.318
1	1	1	1	150	150	75	37.5	75	14.318

FUNCTION TABLE

FUNCTION	OUTPUTS				
DESCRIPTION	CPU	PCI	SDRAM	REF	IOAPIC
TRI-STATE	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
NORMAL	See table	See table	CPU	14.318	14.318

8.3.2 Register 1: CPU, 48/24 MHz Clock Register (1 = Active, 0 = Inactive)

BIT	@POWERUP	PIN	DESCRIPTION
7	1	-	Reserved
6	1	-	Reserved
5	1	-	Reserved
4	1	-	Reserved

8.3.2 Register 1: CPU, 48/24 MHz Clock Register (1 = Active, 0 = Inactive), continued

BIT	@POWERUP	PIN	DESCRIPTION
3	1	40	CPUCLK3 (Active/Inactive)
2	1	41	CPUCLK2 (Active/Inactive)
1	1	43	CPUCLK1 (Active/Inactive)
0	1	44	CPUCLK0 (Active/Inactive)

8.3.3 Register 2: PCI Clock Register (1 = Active, 0 = Inactive)

BIT	@POWERUP	PIN	DESCRIPTION
7	x	-	Reserved
6	1	7	PCICLK_F (Active/Inactive)
5	1	15	AGP0 (Active/Inactive)
4	1	14	PCICLK4 (Active/Inactive)
3	1	12	PCICLK3 (Active/Inactive)
2	1	11	PCICLK2 (Active/Inactive)
1	1	10	PCICLk1 (Active/Inactive)
0	1	8	PCICLK0 (Active/Inactive)

8.3.4 Register 3: SDRAM Clock Register (1 = Active, 0 = Inactive)

BIT	@POWERUP	PIN	DESCRIPTION
7	1	28	SDRAM7 (Active/Inactive)
6	1	29	SDRAM6 (Active/Inactive)
5	1	31	SDRAM5 (Active/Inactive)
4	1	32	SDRAM4 (Active/Inactive)
3	1	34	SDRAM3 (Active/Inactive)
2	1	35	SDRAM2 (Active/Inactive)
1	1	37	SDRAM1 (Active/Inactive)
0	1	38	SDRAM0 (Active/Inactive)

8.3.5 Register 4: Additional SDRAM Clock Register (1 = Active, 0 = Inactive)

BIT	@POWERUP	PIN	DESCRIPTION
7	x	-	Reserved
6	x	-	Reserved

8.3.5 Register 4: Additional SDRAM Clock Register (1 = Active, 0 = Inactive), continued

BIT	@POWERUP	PIN	DESCRIPTION
5	x	-	Reserved
4	x	-	Reserved
3	1	17	SDRAM11 (Active/ Inactive)
2	1	18	SDRAM10 (Active/ Inactive)
1	1	20	SDRAM9 (Active/ Inactive)
0	1	21	SDRAM8 (Active/ Inactive)

8.3.6 Register 5: Peripheral Control (1 = Active, 0 = Inactive)

BIT	@POWERUP	PIN	DESCRIPTION
7	x	-	Reserved
6	x	-	Reserved
5	x	-	Reserved
4	1	47	AGP1 (Active/ Inactive)
3	x	-	Reserved
2	x	-	Reserved
1	1	46	REF1 (Active/ Inactive)
0	1	2	REF0 (Active/ Inactive)

8.3.7 Register 6: Reserved Register

BIT	@POWERUP	PIN	DESCRIPTION
7	x	-	Reserved
6	x	-	Reserved
5	x	-	Reserved
4	x	-	Reserved
3	x	-	Reserved
2	x	-	Reserved
1	x	-	Reserved
0	x	-	Reserved

9.0 SPECIFICATIONS

9.1 Absolute Maximum Ratings

Stresses greater than those listed in this table may cause permanent damage to the device. Precautions should be taken to avoid application of any voltage higher than the maximum rated voltages to this circuit. Maximum conditions for extended periods may affect reliability. Unused inputs must always be tied to an appropriate logic voltage level (Ground or V_{DD}).

PARAMETER	SYMBOL	RATING
Voltage on any pin with respect to GND	V_{DD}, V_{IN}	- 0.5V to +7.0V
Storage Temperature	T_{STG}	- 65°C to +150°C
Ambient Temperature	T_B	- 55°C to +125°C
Operating Temperature	T_A	0°C to +70°C

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

9.2 AC Characteristics

$V_{DD}q2 = V_{DD} = V_{DD}q3 = 3.3V \pm 5\%$, $V_{DD}q2b = 2.375V \sim 2.9V$, $T_A = 0$ °C to +70 °C

PARAMETER	SYM.	MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
Output Duty Cycle		45	50	55	%	Measured at 1.5V
CPU/SDRAM to PCI Offset	t_{OFF}	1		4	nS	15 pF Load Measured at 1.5V
Skew (CPU-CPU), (PCI-PCI), (SDRAM-SDRAM)	t_{SKEW}			250	pS	15 pF Load Measured at 1.5V
CPU/SDRAM Cycle to Cycle Jitter	t_{CCJ}			±250	pS	
CPU/SDRAM Absolute Jitter	t_{JA}			500	pS	
Jitter Spectrum 20 dB Bandwidth from Center	BW_J			500	KHz	
Output Rise (0.4V–2.0V) & Fall (2.0V–0.4V) Time	t_{TLH} t_{THL}	0.4		1.6	nS	15 pF Load on CPU and PCI outputs
Overshoot/Undershoot Beyond Power Rails	Vover	0.7		1.5	V	22 Ω at source of 8 inch PCB run to 15 pF load
Ring Back Exclusion	V_{RBE}	0.7		2.1	V	Ring Back must not enter this range.

9.3 DC Characteristics

$V_{DD}q2 = V_{DD} = V_{DD}q3 = 3.3V \pm 5\%$, $V_{DD}q2b = 2.375V \sim 2.9V$, $T_A = 0\ °C$ to $+70\ °C$

PARAMETER	SYM.	MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
Input Low Voltage	V_{IL}			0.8	V_{dc}	
Input High Voltage	V_{IH}	2.0			V_{dc}	
Input Low Current	I_{IL}			-66	µA	
Input High Current	I_{IH}			5	µA	
Output Low Voltage I_{OL} = 4 mA	V_{OL}			0.4	V_{dc}	All outputs
Output High Voltage I_{OH} = 4 mA	V_{OH}	2.4			V_{dc}	All outputs using 3.3V power
Tri-State leakage Current	I_{OZ}			10	µA	
Dynamic Supply Current for V_{DD} + $V_{DD}q3$	I_{DD3}				mA	CPU = 66.6 MHz PCI = 33.3 MHz with load
Dynamic Supply Current for $V_{DD}q2$ + $V_{DD}q2b$	I_{DD2}				mA	Same as above
CPU Stop Current for V_{DD} + $V_{DD}q3$	I_{CPUS3}				mA	Same as above
CPU Stop Current for $V_{DD}q2$ + $V_{DD}q2b$	I_{CPUS2}				mA	Same as above
PCI Stop Current for V_{DD} + $V_{DD}q3$	I_{PD3}				mA	

9.4 Buffer Characteristics

9.4.1 Type 1 Buffer for CPU (0:3)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
Pull-up Current Min.	I_{OH} (min.)	-27			mA	Vout = 1.0V
Pull-up Current Max.	I_{OH} (max.)			-27	mA	Vout = 2.0V
Pull-down Current Min.	I_{OL} (min.)				mA	Vout = 1.2V
Pull-down Current Max.	I_{OL} (max.)			27	mA	Vout = 0.3V
Rise/Fall Time Min. Between 0.4V and 2.0V	T_{RF} (min.)	0.4			nS	10 pF Load
Rise/Fall Time Max. Between 0.4V and 2.0V	T_{RF} (max.)			1.6	nS	20 pF Load

9.4.2 Type 2 Buffer for IOAPIC

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
Pull-up Current Min.	IOH (min.)				mA	Vout = 1.4V
Pull-up Current Max.	IOH (max.)			-29	mA	Vout = 2.7V
Pull-down Current Min.	IOL (min.)				mA	Vout = 1.0V
Pull-down Current Max.	IOL (max.)			28	mA	Vout = 0.2V
Rise/Fall Time Min. Between 0.7V and 1.7V	TRF (min.)	0.4			nS	10 pF Load
Rise/Fall Time Max. Between 0.7V and 1.7V	TRF (max.)			1.8	nS	20 pF Load

9.4.3 Type 3 Buffer for REF(0:1), 24 MHz, 48 MHz

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
Pull-up Current Min.	IOH (min.)	-29			mA	Vout = 1.0V
Pull-up Current Max.	IOH (max.)			-23	mA	Vout = 3.135V
Pull-down Current Min.	IOL (min.)	29			mA	Vout = 1.95V
Pull-down Current Max.	IOL (max.)				mA	Vout = 0.4V
Rise/Fall Time Min. Between 0.8V and 2.0V	TRF (min.)	1.0			nS	10 pF Load
Rise/Fall Time Max. Between 0.8V and 2.0V	TRF (max.)			4.0	nS	20 pF Load

9.4.4 Type 4 Buffer for REF0 and SDRAM (0:11)

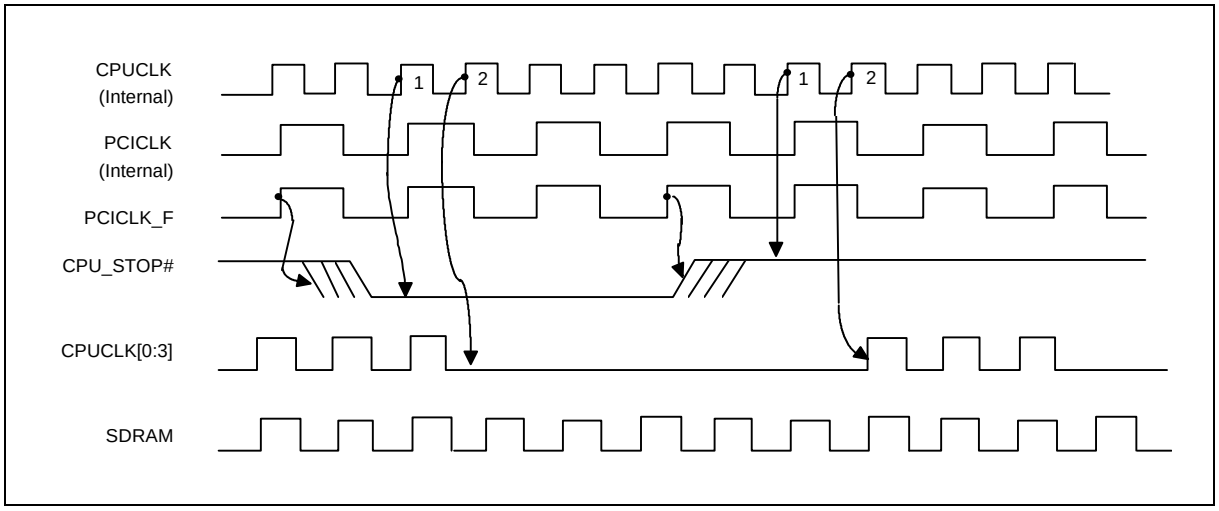
PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
Pull-up Current Min.	IOH (min.)				mA	Vout = 1.65V
Pull-up Current Max.	IOH (max.)			-46	mA	Vout = 3.135V
Pull-down Current Min.	IOL (min.)				mA	Vout = 1.65V
Pull-down Current Max.	IOL (max.)			53	mA	Vout = 0.4V
Rise/Fall Time Min. Between 0.8V and 2.0V	TRF (min.)	0.5			nS	20 pF Load
Rise/Fall Time Max. Between 0.8V and 2.0V	TRF (max.)			1.3	nS	30 pF Load

9.4.5 Type 5 Buffer for PCICLK(0:4,F)

PARAMETER	SYM.	MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
Pull-up Current Min.	IOH (min.)	-33			mA	Vout = 1.0V
Pull-up Current Max.	IOH (max.)			-33	mA	Vout = 3.135V
Pull-down Current Min.	IOL (min.)	30			mA	Vout = 1.95V
Pull-down Current Max.	IOL (max.)			38	mA	Vout = 0.4V
Rise/Fall Time Min. Between 0.8V and 2.0V	TRF (min.)	0.5			nS	15 pF Load
Rise/Fall Time Max. Between 0.8V and 2.0V	TRF (max.)			2.0	nS	30 pF Load

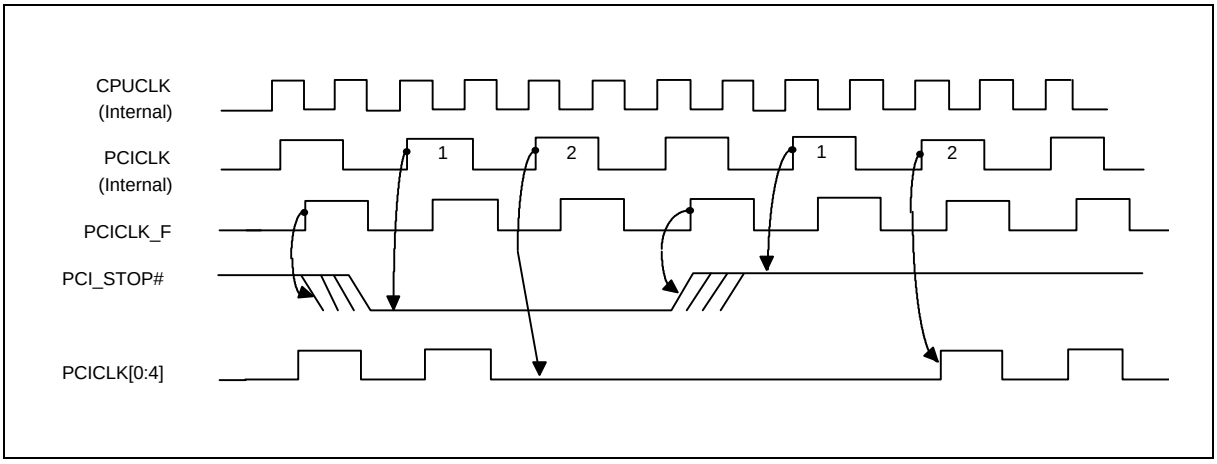
10.0 POWER MANAGEMENT TIMING

10.1 CPU_STOP# Timing Diagram



For synchronous Chipset, CPU_STOP# pin is a synchronous "active low" input pin used to stop the CPU clocks for low power operation. This pin is asserted synchronously by the external control logic at the rising edge of free running PCI clock(PCICLK_F). All other clocks will continue to run while the CPU clocks are stopped. The CPU clocks will always be stopped in a low state and resume output with full pulse width. In this case, CPU "clocks on latency" is less than 2 CPU clocks and clocks off latency is less then 2 CPU clocks.

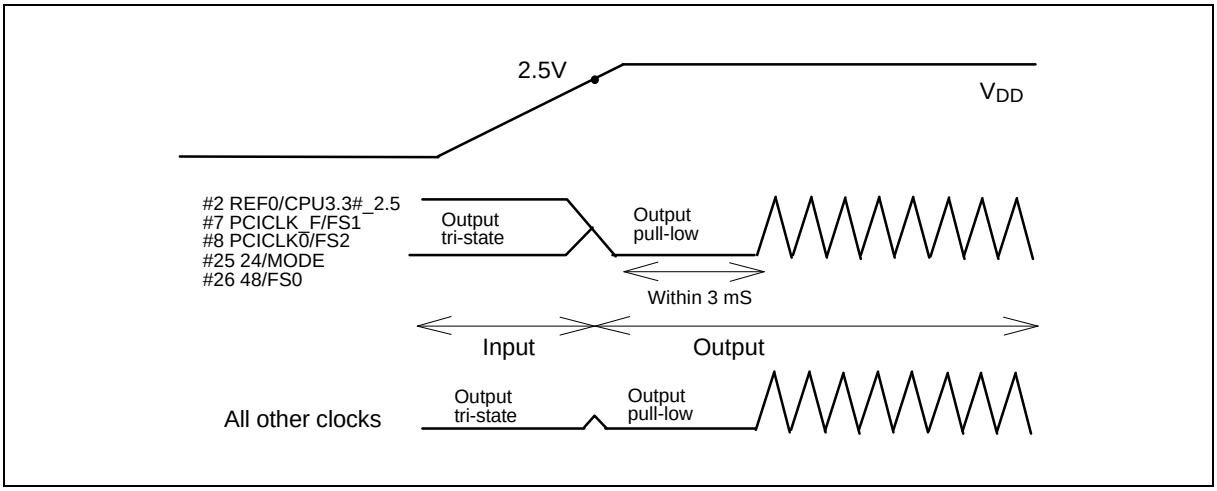
10.2 PCI_STOP# Timing Diagram



For synchronous Chipset, PCI_STOP# pin is a synchronous "active low" input pin used to stop the PCICLK [0:4] for low power operation. This pin is asserted synchronously by the external control logic at the rising edge of free running PCI clock (PCICLK_F). All other clocks will continue to run while the PCI clocks are stopped. The PCI clocks will always be stopped in a low state and resume output with full pulse width. In this case, PCI "clocks on latency" is less than 1 PCI clocks and clocks off latency is less then 1 PCI clocks.

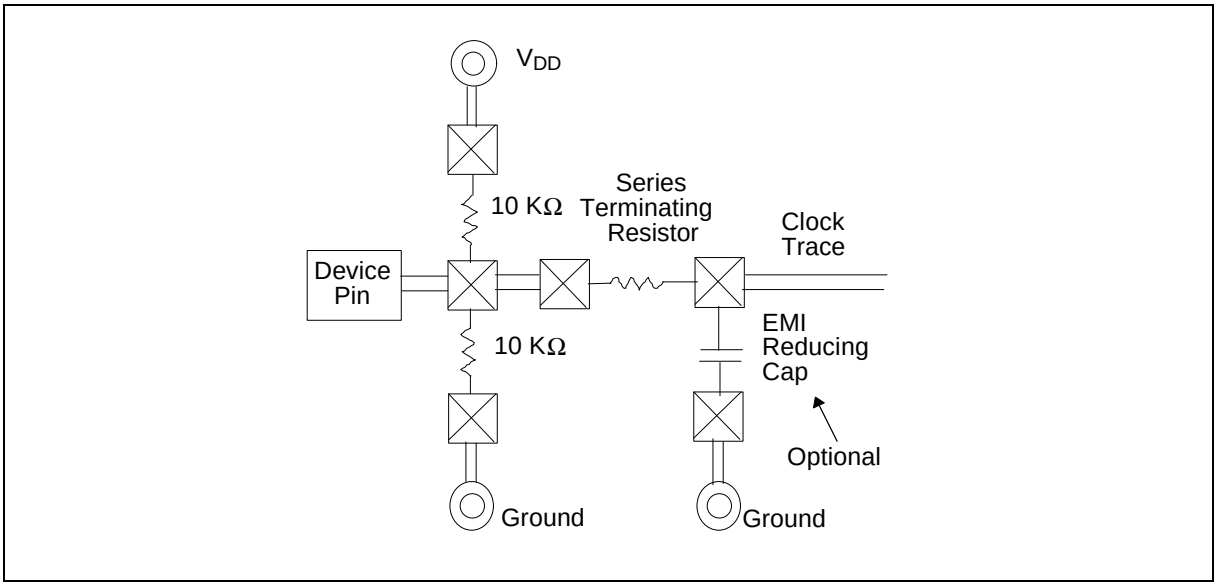
11.0 OPERATION OF DUAL FUCTION PINS

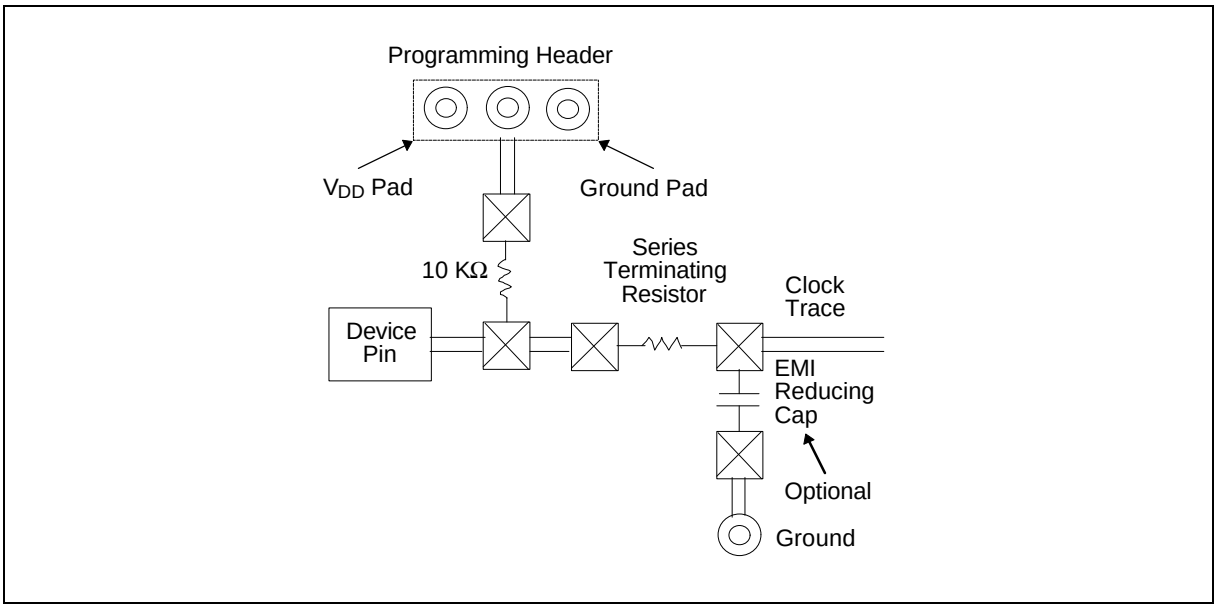
Pins 2, 7, 8, 25 and 26 are dual function pins and are used for selecting different functions in this device (see Pin description). During power up, these pins are in input mode (see Figure 1), therefore, and are considered input select pins. When V_{DD} reaches 2.5V, the logic level that is present on these pins are latched into their appropriate internal registers. Once the correct information are properly latched, these pins will change into output pins and will be pulled low by default. At the end of the power up timer (within 3 mS) outputs starts to toggle at the specified frequency.



Each of these pins are a large pull-up resistor (250 KΩ @3.3V) inside. The default state will be logic 1, but the internal pull-up resistor may be too large when long traces or heavy load appear on these dual function pins. Under these conditions, an external 10 KΩ resistor is recommended to be connected to V_{DD} if logic 1 is expected. Otherwise, the 10 KΩ resistor is connected to ground if a logic 0 is desired. The 10 KΩ resistor should be place before the serious terminating resistor. Note that these logic will only be latched at initial power on.

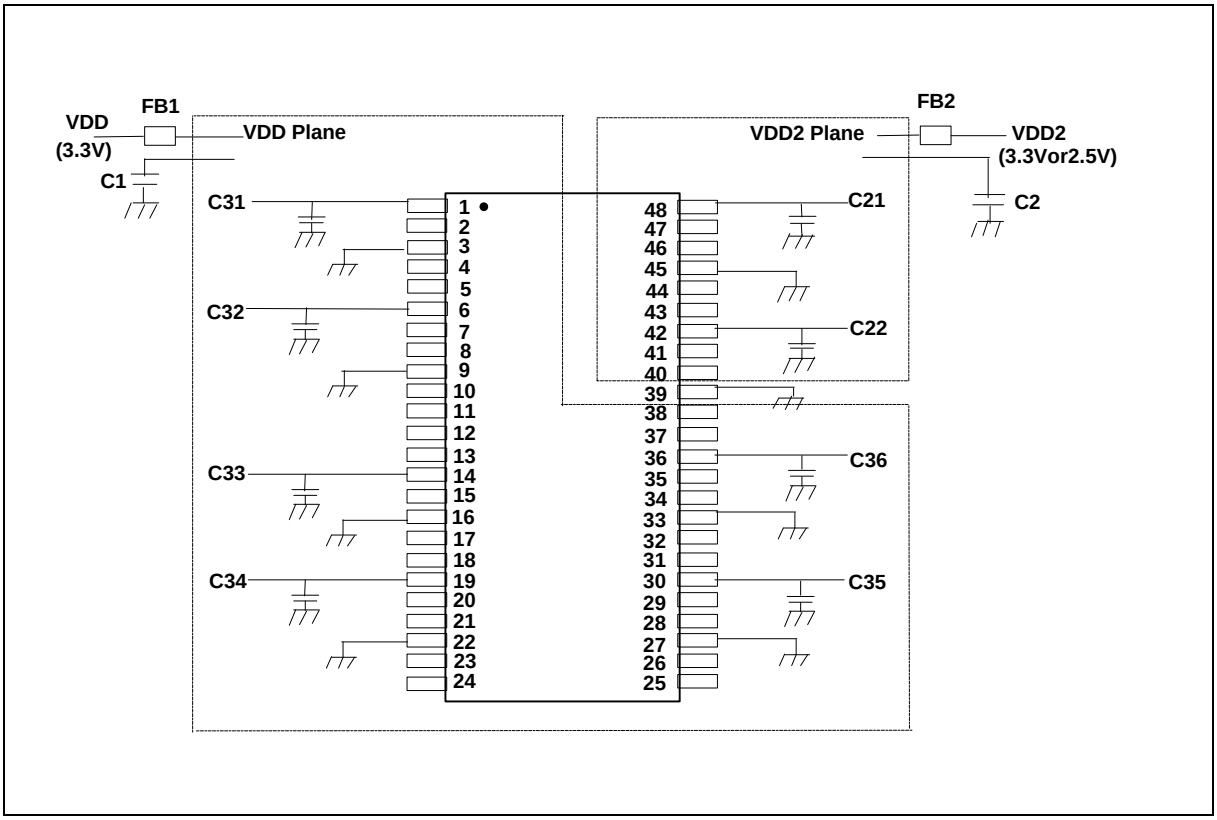
If optional EMI reducing capacitor are needed, they should be placed as close to the series terminating resistor as possible and after the series terminating resistor. These capacitor has typical values ranging from 4.7 pF to 22 pF.





12.0 POWER SUPPLY SUGGESTION

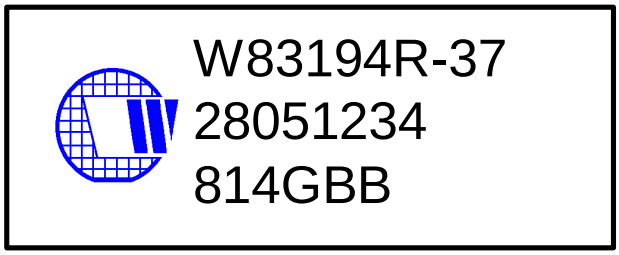
1. A solid ground plane should be placed around the clock device. Ground connections should be tied to this main ground plane as short as possible. No cuts should be made in the ground plane around the device.
2. C21, C22, C31, C36 are decoupling capacitors (0.1 µF surface mount, low ESR, ceramic capacitors.) They should be placed as possible as the VDD pin and the ground via.
3. C1 and C2 are supply filtering capacitors for low frequency power supply noise. A 22 µF (or 10 µF) tantalum capacitor is recommended.
4. Use of Ferrite Bead (FB) are recommended to further reduce the power supply noise.
5. The power supply race to the VDD pins must be thick enough so that voltage drops across the trace resistance is negligible.

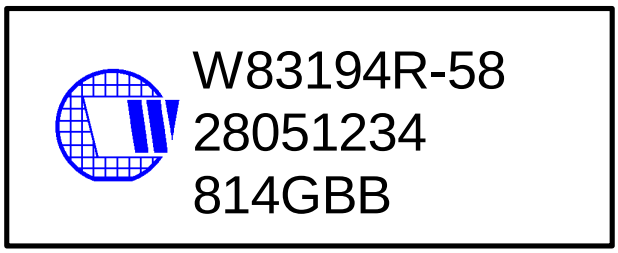


13.0 ORDERING INFORMATION

PART NUMBER	PACKAGE TYPE	PRODUCTION FLOW
W83194R-37/-58	48-pin SSOP	Commercial, 0° C to +70° C

14.0 HOW TO READ THE TOP MARKING





1st line: Winbond logo and the type number: W83194R-37/-58

2nd line: Tracking code 2 8051234

2: wafers manufactured in Winbond FAB 2

8051234: wafer production series lot number

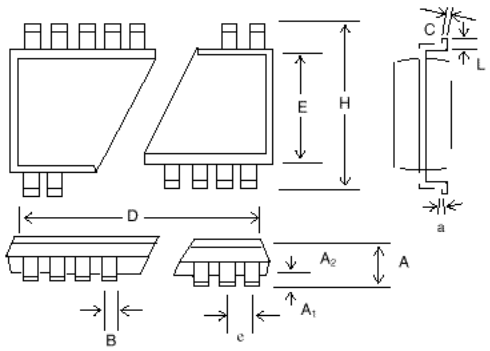
3rd line: Tracking code 814 G B B

814: packages made in '98, week 14

G: assembly house ID; A means ASE, S means SPIL, G means GR

BB: IC revision

15.0 PACKAGE DRAWING AND DIMENSIONS



48 PIN SSOP OUTLINE DIMENSIONS

SYMBOL	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	-	-	0.110	0	0	2.79
A_1	0.008	0.012	0.016	0.20	0.30	0.41
A2	0.085	0.090	0.095	2.16	2.29	2.41
b	0.008	0.010	0.013	0.20	0.25	0.33
C	0.006	0.008	0.010	0.15	0.20	0.25
D	-	0.625	0.637	-	15.88	16.18
E	0.291	0.295	0.299	7.39	7.49	7.59
e	0.025 BSC			0.64 BSC		
H	0.395	0.408	0.420	10.03	10.36	10.67
L	0.025	0.030	0.040	0.64	0.76	1.02
a	0°	5°	8°	0°	5°	8°

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Note: All data and specifications are subject to change without notice.