PRELIMINARY

W48C101-01

Spread Spectrum BX System Frequency Generator

Features

- **Maximized EMI suppression using Cypress's Spread Spectrum technology**
- **Four copies of CPU output**
- **Eight copies of PCI output (Synchronous w/CPU output)**
- **Two copies of 14.318-MHz IOAPIC output**
- **Two copies of 48-MHz USB output**
- **Three buffered copies of 14.318-MHz reference input**
- **Input is a 14.318-MHz XTAL or reference signal**
- **Selectable 100-MHz or 66-MHz CPU outputs**
- **Power management control input pins**
- **Test mode and output three-state capability**

Key Specifications

Supply Voltages: .... V_{DDQ3} = 3.3V±5%
V_{DDQ2} = 2.5V±5%

CPU0:3 Jitter (Cycle to Cycle): .... 200 ps

CPU0:3 Clock Skew: ....175 ps

PCI_F, PCI1:7 Clock Skew: ....500 ps

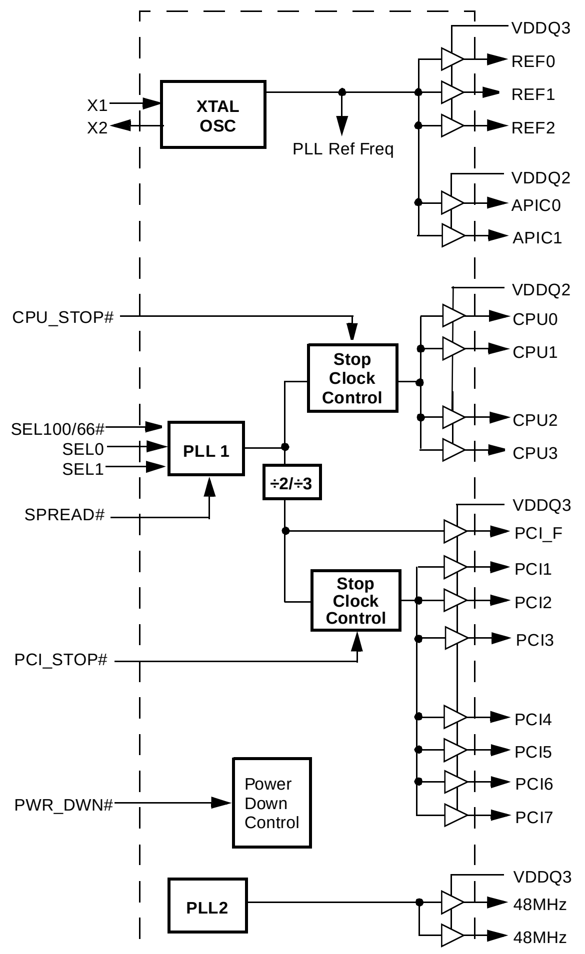
CPU to PCI Clock Skew: .... 1.5 to 4.0 ns (CPU Leads)

Logic inputs have 250-kΩ pull-up resistors except SEL100/66#.

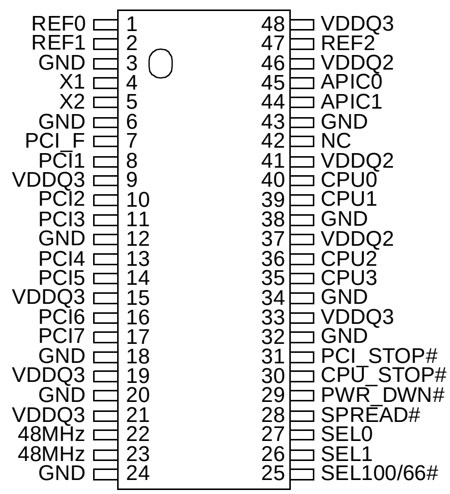
Table 1. Pin Selectable Frequency

SEL 100/66#	SEL1	SEL0	CPU (MHz)	PCI (MHz)	SPREAD#=0
0	0	0	HI-Z	HI-Z	Don't Care
0	0	1	66.6	33.3	±0.9% Center
0	1	0	66.6	33.3	–1% Down
0	1	1	66.6	33.3	–0.5% Down
1	0	0	X1/2	X1/6	Don't Care
1	0	1	100	33.3	±0.9% Center
1	1	0	100	33.3	–1% Down
1	1	1	100	33.3	–0.5% Down

Block Diagram



Pin Configuration



Pin Definitions

Pin Name	Pin No.	Pin Type	Pin Description
CPU0:3	40, 39, 36, 35	O	***CPU Clock Outputs 0 through 3:*** These four CPU clock outputs are controlled by the CPU_STOP# control pin. Output voltage swing is controlled by voltage applied to VDDQ2.
PCI1:7	8, 10, 11, 13, 14, 16, 17	O	***PCI Bus Clock Outputs 1 through 7:*** These seven PCI clock outputs are controlled by the PCI_STOP# control pin. Output voltage swing is controlled by voltage applied to VDDQ3.
PCI_F	7	O	***Fixed PCI Clock Output:*** Unlike PCI1:7 outputs, this output is not controlled by the PCI_STOP# control pin. Output voltage swing is controlled by voltage applied to VDDQ3.
CPU_STOP#	30	I	***CPU_STOP# Input:*** When brought LOW, clock outputs CPU0:3 are stopped LOW after completing a full clock cycle (2–3 CPU clock latency). When brought HIGH, clock outputs CPU0:3 start beginning with a full clock cycle (2–3 CPU clock latency).
PCI_STOP#	31	I	***PCI_STOP# Input:*** The PCI_STOP# input enables the PCI 1:7 outputs when HIGH and causes them to remain at logic 0 when LOW. The PCI_STOP signal is latched on the rising edge of PCI_F. Its effects take place on the next PCI_F clock cycle.
SPREAD#	28	I	***SPREAD# Input:*** When brought LOW this pin activates Spread Spectrum clocking.
APIC0:1	45, 44	O	***I/O APIC Clock Outputs:*** Provides 14.318-MHz fixed frequency. The output voltage swing is controlled by VDDQ2.
48MHz	22, 23	O	***48-MHz Outputs:*** Fixed clock outputs at 48 MHz. Output voltage swing is controlled by voltage applied to VDDQ3.
REF0:2	1, 2, 47	O	***Fixed 14.318-MHz Outputs 0 through 2:*** Used for various system applications. Output voltage swing is controlled by voltage applied to VDDQ3.
SEL100/66# SEL1:0	25, 26, 27	I	***Frequency Selection Input:*** Selects power-up default CPU clock frequency as shown in *Table 1* on page 1.
X1	4	I	***Crystal Connection or External Reference Frequency Input:*** Connect to either a 14.318-MHz crystal or reference signal.
X2	5	I	***Crystal Connection:*** An input connection for an external 14.318-MHz crystal. If using an external reference, this pin must be left unconnected.
PWR_DWN#	29	I	***Power Down Control:*** When this input is LOW, device goes into a low-power condition. All outputs are held LOW while in power-down. CPU and PCI clock outputs are stopped LOW after completing a full clock cycle (2–3 CPU clock cycle latency). When brought HIGH, CPU, SDRAM and PCI outputs start with a full clock cycle at full operating frequency (3 ms maximum latency).
VDDQ3	9, 15, 19, 21, 33, 48	P	***Power Connection:*** Connect to 3.3V supply.
VDDQ2	37,41,46	P	***Power Connection:*** Power supply for CPU0:3 and APIC0:1 output buffers. Connect to 2.5V supply.
GND	3, 6, 12, 18, 20, 24, 32, 34, 38, 43	G	***Ground Connection:*** Connect all ground pins to the common system ground plane.
NC	42	-	***No Connect:*** Do not connect.

Spread Spectrum Clocking

The device generates a clock that is frequency modulated in order to increase the bandwidth that it occupies. By increasing the bandwidth of the fundamental and its harmonics, the amplitudes of the radiated electromagnetic emissions are reduced. This effect is depicted in *Figure 1*.

As shown in *Figure 1*, a harmonic of a modulated clock has a much lower amplitude than that of an unmodulated signal. The reduction in amplitude is dependent on the harmonic number and the frequency deviation or spread. The equation for the reduction is:

$$dB = 6.5 + 9*\log_{10}(P) + 9*\log_{10}(F)$$

Where *P* is the percentage of deviation and *F* is the frequency in MHz where the reduction is measured.

The output clock is modulated with a waveform depicted in *Figure 2*. This waveform, as discussed in “Spread Spectrum Clock Generation for the Reduction of Radiated Emissions” by Bush, Fessler, and Hardin produces the maximum reduction in the amplitude of radiated electromagnetic emissions. The deviation selected for this chip is –0.5%, –1.0%, or ±0.9% of the selected frequency. *Figure 2* details the Cypress spreading pattern. Cypress does offer options with more spread and greater EMI reduction. Contact your local Sales representative for details on these devices.

Spread Spectrum clocking is activated or deactivated by selecting the appropriate values for SPREAD#.

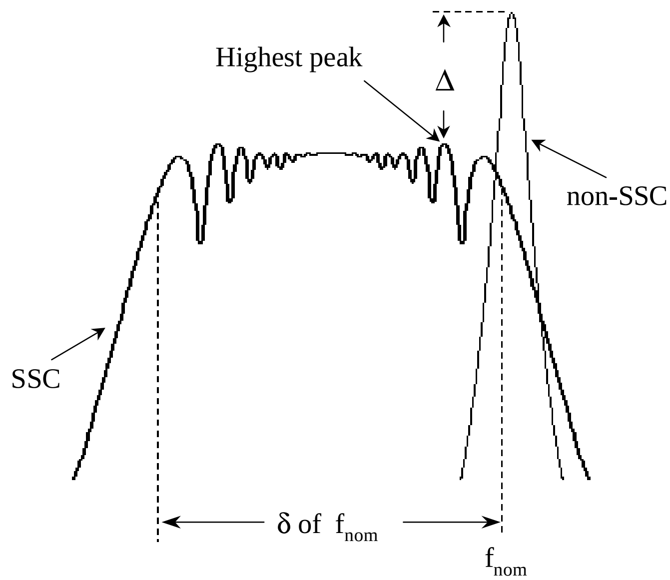


Figure 1. Clock Harmonic with and without SSCG Modulation Frequency Domain Representation

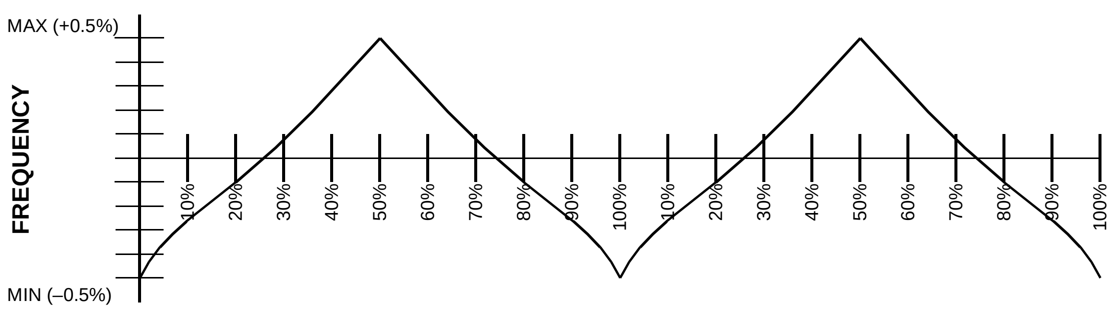


Figure 2. Typical Modulation Profile

Absolute Maximum Ratings

Stresses greater than those listed in this table may cause permanent damage to the device. These represent a stress rating only. Operation of the device at these or any other conditions above those specified in the operating sections of this specification is not implied. Maximum conditions for extended periods may affect reliability.

Parameter	Description	Rating	Unit
V_{DD}, V_{IN}	Voltage on any pin with respect to GND	–0.5 to +7.0	V
T_{STG}	Storage Temperature	–65 to +150	°C
T_A	Operating Temperature	0 to +70	°C
T_B	Ambient Temperature under Bias	–55 to +125	°C
ESD_{PROT}	Input ESD Protection	2 (min.)	kV

DC Electrical Characteristics: T_A = 0°C to +70°C, V_{DDQ3} = 3.3V±5%, V_{DDQ2} = 2.5V±5%

Parameter	Description		Test Condition	Min.	Typ.	Max.	Unit
Supply Current							
I_{DDQ3}	3.3V Supply Current		CPU0:3 = 100 MHz Outputs Loaded[1]			120	mA
I_{DDQ2}	2.5V Supply Current		CPU0:3 = 100 MHz Outputs Loaded[1]			65	mA
Logic Inputs							
V_{IL}	Input Low Voltage			GND – 0.3		0.8	V
V_{IH}	Input High Voltage			2.0		V_{DD} + 0.3	V
I_{IL}	Input Low Current[2]					–25	µA
I_{IH}	Input High Current[2]					10	µA
I_{IL}	Input Low Current (SEL100/66#)					–5	µA
I_{IH}	Input High Current (SEL100/66#)					5	µA
Clock Outputs							
V_{OL}	Output Low Voltage		I_{OL} = 1 mA			50	mV
V_{OH}	Output High Voltage		I_{OH} = –1 mA	3.1			V
V_{OH}	Output High Voltage	CPU0:3, APIC0:1	I_{OH} = –1 mA	2.2			V
I_{OL}	Output Low Current	CPU0:3	V_{OL} = 1.25V	45	65	100	mA
		PCI_F, PCI1:7	V_{OL} = 1.5V	70	100	145	mA
		APIC0:1	V_{OL} = 1.25V	60	90	140	mA
		REF0:2	V_{OL} = 1.5V	45	65	100	mA
		48MHz	V_{OL} = 1.5V	45	65	100	mA
I_{OH}	Output High Current	CPU0:3	V_{OL} = 1.25V	45	65	100	mA
		PCI_F, PCI1:7	V_{OL} = 1.5V	65	95	135	mA
		APIC0:1	V_{OL} = 1.25V	55	80	115	mA
		REF0:2	V_{OL} = 1.5V	45	65	100	mA
		48MHz	V_{OL} = 1.5V	45	65	100	mA

Notes:
1. All clock outputs loaded with 6" 60Ω transmission lines with 20-pF capacitors.
2. W48C101-01 logic inputs have internal pull-up devices, except SEL100/66# (pull-ups not full CMOS level).

DC Electrical Characteristics: T_A = 0°C to +70°C, V_{DDQ3} = 3.3V±5%, V_{DDQ2} = 2.5V±5% (continued)

Parameter	Description	Test Condition	Min.	Typ.	Max.	Unit
Crystal Oscillator						
V_{TH}	X1 Input Threshold Voltage[3]			1.65		V
C_{LOAD}	Load Capacitance, as seen by External Crystal[4]			14		pF
$C_{IN,X1}$	X1 Input Capacitance[5]	Pin X2 unconnected		28		pF
Pin Capacitance/Inductance						
C_{IN}	Input Pin Capacitance	Except X1 and X2			5	pF
C_{OUT}	Output Pin Capacitance				6	pF
L_{IN}	Input Pin Inductance				7	nH

Notes:

3. X1 input threshold voltage (typical) is $V_{DD}/2$.
4. The W48C101-01 contains an internal crystal load capacitor between pin X1 and ground and another between pin X2 and ground. Total load placed on crystal is 14 pF; this includes typical stray capacitance of short PCB traces to crystal.
5. X1 input capacitance is applicable when driving X1 with an external clock source (X2 is left unconnected).

AC Electrical Characteristics

T_A = 0°C to +70°C, V_{DDQ3} = 3.3V±5%, V_{DDQ2} = 2.5V± 5%, f_{XTL} = 14.31818 MHz

AC clock parameters are tested and guaranteed over stated operating conditions using the stated lump capacitive load at the clock output; Spread Spectrum clocking is disabled.

CPU Clock Outputs, CPU0:3 (Lump Capacitance Test Load = 20 pF)

Parameter	Description	Test Condition/Comments	CPU = 66.6 MHz			CPU = 100 MHz			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
t_P	Period	Measured on rising edge at 1.25V	15		15.5	10		10.5	ns
t_H	High Time	Duration of clock cycle above 2.0V	5.2			3.0			ns
t_L	Low Time	Duration of clock cycle below 0.4V	5.0			2.8			ns
t_R	Output Rise Edge Rate	Measured from 0.4V to 2.0V	1		4	1		4	V/ns
t_F	Output Fall Edge Rate	Measured from 2.0V to 0.4V	1		4	1		4	V/ns
t_D	Duty Cycle	Measured on rising and falling edge at 1.25V	45		55	45		55	%
t_{JC}	Jitter, Cycle-to-Cycle	Measured on rising edge at 1.25V. Maximum difference of cycle time between two adjacent cycles.			200			200	ps
t_{SK}	Output Skew	Measured on rising edge at 1.25V			175			175	ps
f_{ST}	Frequency Stabilization from Power-up (cold start)	Assumes full supply voltage reached within 1 ms from power-up. Short cycles exist prior to frequency stabilization.			3			3	ms
Z_o	AC Output Impedance	Average value during switching transition. Used for determining series termination value.		20			20		Ω

PCI Clock Outputs, PCI1:7 and PCI_F (Lump Capacitance Test Load = 30 pF

Parameter	Description	Test Condition/Comments	CPU = 66.6/100 MHz			Unit
			Min.	Typ.	Max.	
t_P	Period	Measured on rising edge at 1.5V	30			ns
t_H	High Time	Duration of clock cycle above 2.4V	12			ns
t_L	Low Time	Duration of clock cycle below 0.4V	12			ns
t_R	Output Rise Edge Rate	Measured from 0.4V to 2.4V	1		4	V/ns
t_F	Output Fall Edge Rate	Measured from 2.4V to 0.4V	1		4	V/ns
t_D	Duty Cycle	Measured on rising and falling edge at 1.5V	45		55	%
t_{JC}	Jitter, Cycle-to-Cycle	Measured on rising edge at 1.5V. Maximum difference of cycle time between two adjacent cycles.			250	ps
t_{SK}	Output Skew	Measured on rising edge at 1.5V			500	ps
t_O	CPU to PCI Clock Skew	Covers all CPU/PCI outputs. Measured on rising edge at 1.5V. CPU leads PCI output.	1.5		4	ns
f_{ST}	Frequency Stabilization from Power-up (cold start)	Assumes full supply voltage reached within 1 ms from power-up. Short cycles exist prior to frequency stabilization.			3	ms
Z_o	AC Output Impedance	Average value during switching transition. Used for determining series termination value.		15		Ω

APIC0:1 Clock Outputs (Lump Capacitance Test Load = 20 pF)

Parameter	Description	Test Condition/Comments	CPU = 66.6/100MHz			Unit
			Min.	Typ.	Max.	
f	Frequency, Actual	Frequency generated by crystal oscillator		14.31818		MHz
t_R	Output Rise Edge Rate	Measured from 0.4V to 2.0V	1		4	V/ns
t_F	Output Fall Edge Rate	Measured from 2.0V to 0.4V	1		4	V/ns
t_D	Duty Cycle	Measured on rising and falling edge at 1.25V	45		55	%
f_{ST}	Frequency Stabilization from Power-up (cold start)	Assumes full supply voltage reached within 1 ms from power-up. Short cycles exist prior to frequency stabilization.			1.5	ms
Z_o	AC Output Impedance	Average value during switching transition. Used for determining series termination value.		15		Ω

REF0:2 Clock Outputs (Lump Capacitance Test Load = 20 pF)

Parameter	Description	Test Condition/Comments	CPU = 66.6/100 MHz			Unit
			Min.	Typ.	Max.	
f	Frequency, Actual	Frequency generated by crystal oscillator		14.318		MHz
t_R	Output Rise Edge Rate	Measured from 0.4V to 2.4V	0.5		2	V/ns
t_F	Output Fall Edge Rate	Measured from 2.4V to 0.4V	0.5		2	V/ns
t_D	Duty Cycle	Measured on rising and falling edge at 1.5V	45		55	%
f_{ST}	Frequency Stabilization from Power-up (cold start)	Assumes full supply voltage reached within 1 ms from power-up. Short cycles exist prior to frequency stabilization.			3	ms
Z_o	AC Output Impedance	Average value during switching transition. Used for determining series termination value.		25		Ω

48-MHz Clock Outputs (Lump Capacitance Test Load = 20 pF = 66.6/100 MHz)

Parameter	Description	Test Condition/Comments	CPU = 66.6/100 MHz			Unit
			Min.	Typ.	Max.	
f	Frequency, Actual	Determined by PLL divider ratio (see m/n below)		48.008		MHz
f_D	Deviation from 48 MHz	(48.008 – 48)/48		+167		ppm
m/n	PLL Ratio	(14.31818 MHz x 57/17 = 48.008 MHz)		57/17		
t_R	Output Rise Edge Rate	Measured from 0.4V to 2.4V	1		4	V/ns
t_F	Output Fall Edge Rate	Measured from 2.4V to 0.4V	1		4	V/ns
t_D	Duty Cycle	Measured on rising and falling edge at 1.5V	45		55	%
f_{ST}	Frequency Stabilization from Power-up (cold start)	Assumes full supply voltage reached within 1 ms from power-up. Short cycles exist prior to frequency stabilization.			3	ms
Z_o	AC Output Impedance	Average value during switching transition. Used for determining series termination value.		25		Ω

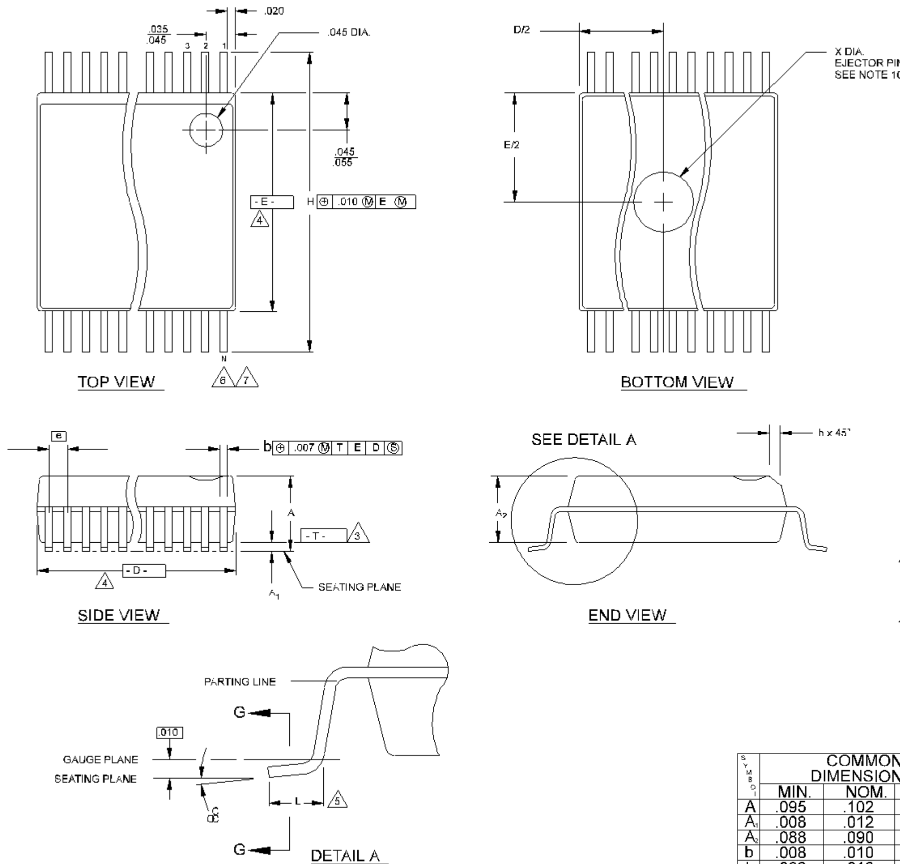
Ordering Information

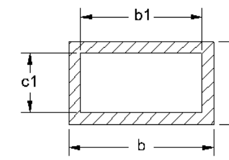
Ordering Code	Freq. Mask Code	Package Name	Package Type
W48C101	-01	H	48-pin SSOP (300 mils)

Document #: 38-00852

Package Diagram

48-Pin Small Shrink Outline Package (SSOP, 300 mils)





SECTION G-G ⚠11
SCALE: NONE

NOTES:

1. ⚠ MAXIMUM DIE THICKNESS ALLOWABLE IS .025.
2. ⚠ DIMENSIONING & TOLERANCING PER ANSI Y14.5M - 1982.
3. ⚠ "T" IS A REFERENCE DATUM.
4. ⚠ "D" & "E" ARE REFERENCE DATUMS AND DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS, BUT DOES INCLUDE MOLD MISMATCH AND ARE MEASURED AT THE MOLD PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .006 INCHES PER SIDE.
5. ⚠ "L" IS THE LENGTH OF TERMINAL FOR SOLDERING TO A SUBSTRATE.
6. ⚠ "N" IS THE NUMBER OF TERMINAL POSITIONS.
7. ⚠ TERMINAL POSITIONS ARE SHOWN FOR REFERENCE ONLY.
8. ⚠ FORMED LEADS SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITHIN .003 INCHES AT SEATING PLANE.
9. ⚠ CONTROLLING DIMENSION: INCHES.
10. COUNTRY OF ORIGIN LOCATION AND EJECTOR PIN ON PACKAGE BOTTOM IS OPTIONAL AND DEPENDS ON ASSEMBLY LOCATION.
11. ⚠ THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .005 INCHES AND .010 INCHES FROM THE LEAD TIPS.
12. THIS PART IS COMPLIANT WITH JEDEC SPECIFICATION MO-118, VARIATIONS AA, AB, EXCEPT CHAMFER DIMENSION h. JEDEC SPECIFICATION FOR h IS .015"/.025".

SYMBOL	COMMON DIMENSIONS MIN.	NOM.	MAX.	NOTE
A	.095	.102	.110	
A_1	.008	.012	.016	
A_2	.088	.090	.092	
b	.008	.010	.0135	
b_1	.008	.010	.012	
c	.005	-	.010	
c_1	.005	.006	.0085	
D	SEE VARIATIONS			4
E	.292	.296	.299	
e	.025 BSC			
H	.400	.406	.410	
h	.010	.013	.016	
L	.024	.032	.040	
N	SEE VARIATIONS			6
X	.085	.093	.100	10
α	0°	5°	8°	

NOTE	4			6
VARIATIONS	D MIN.	NOM.	MAX.	N
AA	.620	.625	.630	48
AB	.720	.725	.730	56

THIS TABLE IN INCHES

SYMBOL	COMMON DIMENSIONS MIN.	NOM.	MAX.	NOTE
A	2.41	2.59	2.79	
A_1	0.20	0.31	0.41	
A_2	2.24	2.29	2.34	
b	0.203	0.254	0.343	
b_1	0.203	0.254	0.305	
c	0.127	-	0.254	
c_1	0.127	0.152	0.216	
D	SEE VARIATIONS			4
E	7.42	7.52	7.59	
e	0.635 BSC			
H	10.16	10.31	10.41	
h	0.25	0.33	0.41	
L	0.61	0.81	1.02	
N	SEE VARIATIONS			6
X	2.16	2.36	2.54	10
α	0°	5°	8°	

NOTE	4			6
VARIATIONS	D MIN.	NOM.	MAX.	N
AA	15.75	15.88	16.00	48
AB	18.29	18.42	18.54	56

THIS TABLE IN MILLIMETERS

Summary of nominal dimensions in inches:

Body Width: 0.296
Lead Pitch: 0.025
Body Length: 0.625
Body Height: 0.102