Notebook PC System Frequency Generator for K6 Processors

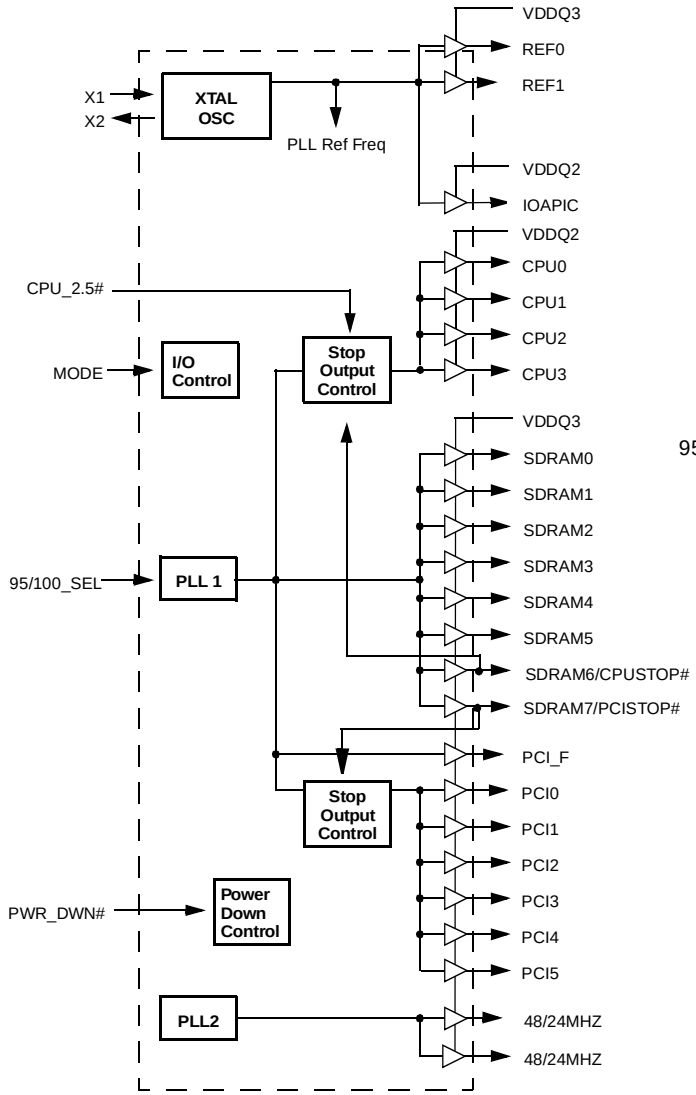
Features

- Generates system clocks for CPU, IOAPIC, SDRAM, PCI, USB plus 14.318 MHz (REF0:1)
- MODE input pin selects optional power management input control pins (reconfigures pins 26 and 27)
- Two fixed outputs separately selectable as 24-MHz or 48-MHz (default = 48-MHz)
- V_{DDQ3} = 3.3V±5%, V_{DDQ2} = 3.3V±5%
- Uses external 14.318-MHz crystal
- Available in 48-pin TSSOP (6.1-mm)
- 10Ω CPU output impedance

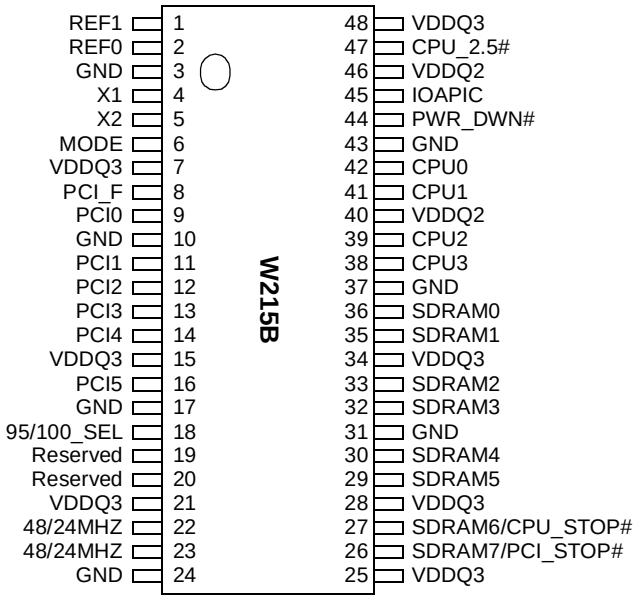
Table 1. Pin Selectable Frequency

95/100_SEL	CPU, SDRAM Clocks (MHz)	PCI Clocks
0	95.0	CPU/3
1	100.0	CPU/3

Block Diagram



Pin Configuration



Pin Definitions

Pin Name	Pin No.	Pin Type	Pin Description
CPU0:3	42, 41, 39, 38	O	***CPU Outputs 0 through 3:*** These four CPU outputs are controlled by the CPU_STOP# control pin. Output voltage swing is controlled by voltage applied to VDDQ2.
PCI0:5	9, 11, 12, 13, 14, 16	O	***PCI Bus Outputs 0 through 5:*** These six PCI outputs are controlled by the PCI_STOP# control pin. Output voltage swing is controlled by voltage applied to VDDQ3.
PCI_F	8	O	***Free Running PCI Output:*** Unlike PCI0:5 outputs, this output is not controlled by the PCI_STOP# control pin. Output voltage swing is controlled by voltage applied to VDDQ3.
SDRAM0:5	36, 35, 33, 32, 30, 29	O	***SDRAM Clock Outputs 0 through 5:*** These six SDRAM clock outputs run synchronous to the CPU clock outputs. Output voltage swing is controlled by voltage applied to VDDQ3.
SDRAM6/ CPU_STOP#	27	I/O	***SDRAM Clock Output 6 or CPU Clock Output Stop Control:*** This pin has dual functions, selectable by the MODE input pin. When MODE = 0, this pin becomes the CPU_STOP# input. When MODE = 1, this pin becomes SDRAM clock output 6. Regarding use as a CPU_STOP# input: When brought LOW, clock outputs CPU0:3 are stopped LOW after completing a full clock cycle (2–3 CPU clock latency). When brought HIGH, clock outputs CPU0:3 are started beginning with a full clock cycle (2–3 CPU clock latency). Regarding use as a SDRAM clock: Output voltage swing is controlled by voltage applied to VDDQ3.
SDRAM7/ PCI_STOP#	26	I/O	***SDRAM Clock Output 7 or PCI Clock Output Stop Control:*** This pin has dual functions, selectable by the MODE input pin. When MODE = 0, this pin becomes the PCI_STOP# input. When MODE = 1, this pin becomes SDRAM clock output 7. PCI_STOP# input: When brought LOW, clock outputs PCI0:5 are stopped LOW after completing a full clock cycle. When brought HIGH, clock outputs PCI0:5 are started beginning with a full clock cycle. Clock latency provides one PCI_F rising edge of PCI clock following PCI_STOP# state change. Regarding use as a SDRAM clock: Output voltage swing is controlled by voltage applied to VDDQ3.
IOAPIC	45	O	***I/O APIC Clock Output:*** Provides 14.318-MHz fixed frequency. The output voltage swing is controlled by VDDQ2.
48/24MHz	22, 23	O	***48-MHz / 24-MHz Output:*** Fixed clock outputs that default to 48 MHz following device power-up. Either or both can be changed to 24 MHz through use of the serial data interface (Byte 0, bits 2 and 3). Output voltage swing is controlled by voltage applied to VDDQ3
REF0:1	2, 1	O	***Fixed 14.318-MHz Outputs 0 through 1:*** Used for various system applications. Output voltage swing is controlled by voltage applied to VDDQ3. REF0 is stronger than REF1 and should be used for driving ISA slots.
CPU_2.5#	47	I	Set to logic 1 for 3.3V CPU I/O.
95/100_SEL	18	I	***95- or 100-MHz Input Selection:*** Selects power-up default CPU clock frequency as shown in *Table 1* on page 1 (also determines SDRAM and PCI clock frequency selections).
X1	4	I	***Crystal Connection or External Reference Frequency Input:*** This pin has dual functions. It can be used as an external 14.318-MHz crystal connection or as an external reference frequency input.
X2	5	I	***Crystal Connection:*** An input connection for an external 14.318-MHz crystal. If using an external reference, this pin must be left unconnected.

Pin Definitions

Pin Name	Pin No.	Pin Type	Pin Description
PWR_DWN#	44	I	***Power-Down Control:*** When this input is LOW, device goes into a low-power standby condition. All outputs are actively held LOW while in power-down. CPU, SDRAM, and PCI clock outputs are stopped LOW after completing a full clock cycle (2–4 CPU clock cycle latency). When brought HIGH, CPU, SDRAM, and PCI outputs start with a full clock cycle at full operating frequency (3 ms maximum latency).
MODE	6	I	***Mode Control:*** This input selects the function of device pin 26 (SDRAM7/PCI_STOP#) and pin 27 (SDRAM6/CPU_STOP#). Refer to description for those pins.
VDDQ3	7, 15, 21, 25 28, 34, 48	P	***Power Connection:*** Power supply for PCI0:5, REF0:1, and 48-/24-MHz output buffers. Connected to 3.3V supply.
VDDQ2	46, 40	P	***Power Connection:*** Power supply for IOAPIC0, CPU0:3 output buffer. Connected to 3.3V supply.
GND	3, 10, 17, 24, 31, 37, 43	G	***Ground Connection:*** Connect all ground pins to the common system ground plane.
Reserved	19, 20	I	***Reserved Pins:*** Connect to Logic 1.

Absolute Maximum Ratings

Stresses greater than those listed in this table may cause permanent damage to the device. These represent a stress rating only. Operation of the device at these or any other conditions above those specified in the operating sections of this specification is not implied. Maximum conditions for extended periods may affect reliability.

Parameter	Description	Rating	Unit
V_{DD}, V_{IN}	Voltage on any pin with respect to GND	–0.5 to +7.0	V
T_{STG}	Storage Temperature	–65 to +150	°C
T_B	Ambient Temperature under Bias	–55 to +125	°C
T_A	Operating Temperature	0 to +70	°C
ESD_{PROT}	Input ESD Protection	2 (min.)	kV

DC Electrical Characteristics

T_A = 0°C to +70°C, V_{DDQ3} = 3.3V±5% (3.135–3.465V), f_{XTL} = 14.31818 MHz, V_{DDQ2} = 3.3V±5%

Parameter	Description		Test Condition	Min.	Typ.	Max.	Unit
Supply Current							
I_{DDQ3}	Supply Current (3.3V)		CPU0:3 = 100 MHz Outputs Loaded[1]		150		mA
I_{DDQ2}	Supply Current (3.3V)		CPU0:3 = 100 MHz Outputs Loaded[1]		80		mA
Logic Inputs							
V_{IL}	Input Low Voltage					0.8	V
V_{IH}	Input High Voltage			2.0			V
I_{IL}	Input Low Current[2]					10	µA
I_{IH}	Input High Current[2]					10	µA
Clock Outputs							
V_{OL}	Output Low Voltage		I_{OL} = 2 mA			50	mV
V_{OH}	Output High Voltage		I_{OH} = –1 mA	3.1			V
I_{OL}	Output Low Current	CPU0:3	V_{OL} = 1.5V		140		mA
		SDRAM0:7	V_{OL} = 1.5V		110		mA
		PCI_F, PCI0:5	V_{OL} = 1.5V		110		mA
		IOAPIC	V_{OL} = 1.5V		95		mA
		REF0	V_{OL} = 1.5V		75		mA
		REF1	V_{OL} = 1.5V		70		mA
		48/24MHZ	V_{OL} = 1.5V		70		mA
I_{OH}	Output High Current	CPU0:3	V_{OL} = 1.5V		120		mA
		SDRAM0:7	V_{OL} = 1.5V		95		mA
		PCI_F, PCI0:5	V_{OL} = 1.5V		95		mA
		IOAPIC	V_{OL} = 1.5V		95		mA
		REF0	V_{OL} = 1.5V		80		mA
		REF1	V_{OL} = 1.5V		62		mA
		48/24MHZ	V_{OL} = 1.5V		60		mA

Notes:
1. All clock outputs loaded with maximum lump capacitance test load specified in AC Electrical Characteristics section.
2. W215B logic inputs have internal pull-up devices (not CMOS level).

DC Electrical Characteristics (continued)

T_A = 0°C to +70°C, V_{DDQ3} = 3.3V±5% (3.135–3.465V), f_{XTL} = 14.31818 MHz, V_{DDQ2} = 3.3V±5%

Parameter	Description	Test Condition	Min.	Typ.	Max.	Unit
Crystal Oscillator						
V_{TH}	X1 Input Threshold Voltage[3]	V_{DDQ3} = 3.3V		1.65		V
C_{LOAD}	Load Capacitance, Imposed on External Crystal[4]			14		pF
$C_{IN,X1}$	X1 Input Capacitance[5]	Pin X2 unconnected		28		pF
Pin Capacitance/Inductance						
C_{IN}	Input Pin Capacitance	Except X1 and X2			5	pF
C_{OUT}	Output Pin Capacitance				6	pF
L_{IN}	Input Pin Inductance				7	nH

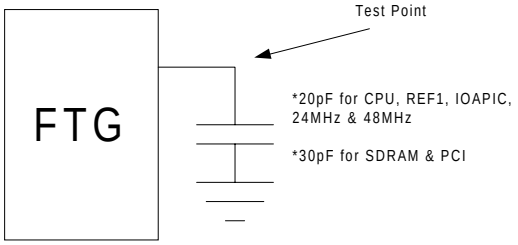
Notes:

3. X1 input threshold voltage (typical) is $V_{DDQ3}/2$.
4. The W215B contains an internal crystal load capacitor between pin X1 and ground and another between pin X2 and ground. Total load placed on crystal is 14 pF; this includes typical stray capacitance of short PCB traces to crystal.
5. X1 input capacitance is applicable when driving X1 with an external clock source (X2 is left unconnected).

AC Electrical Characteristics (Lump Load Model)

T_A = 0°C to +70°C, V_{DDQ3} = 3.3V±5% (3.135–3.465V) f_{XTL} = 14.31818 MHz, V_{DDQ2} = 3.3V±5%

AC clock parameters are tested and guaranteed over stated operating conditions using the stated lump capacitive load at the clock output.



CPU Clock Outputs, CPU0:3 (Lump Capacitance Test Load = 20 pF)

Parameter	Description	Test Condition/Comments	CPU = 100 MHz			Unit
			Min.	Typ.	Max.	
t_P	Period	Measured on rising edge at 1.5V		10		ns
f	Frequency, Actual	Determined by PLL divider ratio		100		MHz
t_H	High Time	Duration of clock cycle above 2.4V		5		ns
t_L	Low Time	Duration of clock cycle below 0.4V		5		ns
t_R	Output Rise Edge Rate	Measured from 0.4V to 2.4V	1		4	V/ns
t_F	Output Fall Edge Rate	Measured from 2.4V to 0.4V	1		4	V/ns
t_D	Duty Cycle	Measured on rising and falling edge at 1.5V	45	50	55	%
t_{JC}	Jitter, Cycle-to-Cycle	Measured on rising edge at 1.5V. Maximum difference of cycle time between two adjacent cycles.			500	ps
t_{SK}	Output Skew	Measured on rising edge at 1.5V			250	ps
f_{ST}	Frequency Stabilization from Power-up (cold start)	Assumes full supply voltage reached within 1 ms from power-up. Short cycles exist prior to frequency stabilization.			3	ms
Z_o	AC Output Impedance	Average value during switching transition. Used for determining series termination value.		10		Ω

SDRAM Clock Outputs, SDRAM0:7 (Lump Capacitance Test Load = 30 pF)

Parameter	Description	Test Condition/Comments	CPU = 100 MHz			Unit
			Min.	Typ.	Max.	
t_P	Period	Measured on rising edge at 1.5V		10		ns
f	Frequency, Actual	Determined by PLL divider ratio		100		MHz
t_R	Output Rise Edge Rate	Measured from 0.4V to 2.4V	1		4	V/ns
t_F	Output Fall Edge Rate	Measured from 2.4V to 0.4V	1		4	V/ns
t_D	Duty Cycle	Measured on rising and falling edge at 1.5V	45	50	55	%
t_{JC}	Jitter, Cycle-to-Cycle	Measured on rising edge at 1.5V. Maximum difference of cycle time between two adjacent cycles.			500	ps
t_{SK}	Output Skew	Measured on rising edge at 1.5V		100		ps
t_{SK}	CPU to SDRAM Clock Skew	Covers all CPU/SDRAM outputs. Measured on rising edge at 1.5V.			1.5	ns
f_{ST}	Frequency Stabilization from Power-up (cold start)	Assumes full supply voltage reached within 1 ms from power-up. Short cycles exist prior to frequency stabilization.			3	ms
Z_o	AC Output Impedance	Average value during switching transition. Used for determining series termination value.		16		Ω

PCI Clock Outputs, PCI0:5 (Lump Capacitance Test Load = 30 pF)

Parameter	Description	Test Condition/Comments	CPU = 100 MHz			Unit
			Min.	Typ.	Max.	
t_P	Period	Measured on rising edge at 1.5V		30		ns
f	Frequency, Actual	Determined by PLL divider ratio		33.3		MHz
t_H	High Time	Duration of clock cycle above 2.4V	12			ns
t_L	Low Time	Duration of clock cycle below 0.4V	12			ns
t_R	Output Rise Edge Rate		1		4	V/ns
t_F	Output Fall Edge Rate		1		4	V/ns
t_D	Duty Cycle	Measured on rising and falling edge at 1.5V	45	50	55	%
t_{JC}	Jitter, Cycle-to-Cycle	Measured on rising edge at 1.5V. Maximum difference of cycle time between two adjacent cycles.			500	ps
t_{SK}	Output Skew	Measured on rising edge at 1.5V			250	ps
t_O	CPU to PCI Clock Skew	Covers all CPU/PCI outputs. Measured on rising edge at 1.5V. CPU leads PCI output.	1		4	ns
f_{ST}	Frequency Stabilization from Power-up (cold start)	Assumes full supply voltage reached within 1 ms from power-up. Short cycles exist prior to frequency stabilization.			3	ms
Z_o	AC Output Impedance	Average value during switching transition. Used for determining series termination value.		15		Ω

I/O APIC Clock Output (Lump Capacitance Test Load = 20 pF)

Parameter	Description	Test Condition/Comments	CPU = 100 MHz			Unit
			Min.	Typ.	Max.	
f	Frequency, Actual	Frequency generated by crystal oscillator		14.31818		MHz
t_R	Output Rise Edge Rate		1		4	V/ns
t_F	Output Fall Edge Rate		1		4	V/ns
t_D	Duty Cycle	Measured on rising and falling edge at 1.5V	45	50	55	%
f_{ST}	Frequency Stabilization from Power-up (cold start)	Assumes full supply voltage reached within 1 ms from power-up. Short cycles exist prior to frequency stabilization.			1.5	ms
Z_o	AC Output Impedance	Average value during switching transition. Used for determining series termination value.		15		Ω

REF0 Clock Output (Lump Capacitance Test Load = 45 pF)

Parameter	Description	Test Condition/Comments	CPU = 100 MHz			Unit
			Min.	Typ.	Max.	
f	Frequency, Actual	Frequency generated by crystal oscillator		14.318		MHz
t_R	Output Rise Edge Rate		1		4	V/ns
t_F	Output Fall Edge Rate		1		4	V/ns
t_D	Duty Cycle	Measured on rising and falling edge at 1.5V	45	50	55	%
f_{ST}	Frequency Stabilization from Power-up (cold start)	Assumes full supply voltage reached within 1 ms from power-up. Short cycles exist prior to frequency stabilization.			1.5	ms
Z_o	AC Output Impedance	Average value during switching transition. Used for determining series termination value.		16		Ω

REF1 Clock Output (Lump Capacitance Test Load = 20 pF)

Parameter	Description	Test Condition/Comments	CPU = 100 MHz			Unit
			Min.	Typ.	Max.	
f	Frequency, Actual	Frequency generated by crystal oscillator		14.318		MHz
t_R	Output Rise Edge Rate		0.5		2	V/ns
t_F	Output Fall Edge Rate		0.5		2	V/ns
t_D	Duty Cycle	Measured on rising and falling edge at 1.5V	45		55	%
f_{ST}	Frequency Stabilization from Power-up (cold start)	Assumes full supply voltage reached within 1 ms from power-up. Short cycles exist prior to frequency stabilization.			1.5	ms
Z_o	AC Output Impedance	Average value during switching transition. Used for determining series termination value.		25		Ω

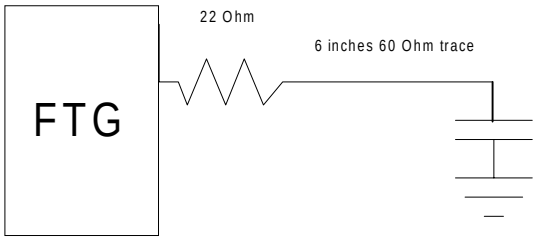
48-/24-MHz Clock Output (Lump Capacitance Test Load = 20 pF)

Parameter	Description	Test Condition/Comments	CPU = 100 MHz			Unit
			Min.	Typ.	Max.	
m/n	PLL Ratio			57/17		
t_R	Output Rise Edge Rate		0.5		2	V/ns
t_F	Output Fall Edge Rate		0.5		2	V/ns
t_D	Duty Cycle	Measured on rising and falling edge at 1.5V	45	50	55	%
f_{ST}	Frequency Stabilization from Power-up (cold start)	Assumes full supply voltage reached within 1 ms from power-up. Short cycles exist prior to frequency stabilization.			3	ms
Z_o	AC Output Impedance	Average value during switching transition. Used for determining series termination value.		25		Ω

AC Electrical Characteristics (Transmission Line Model)

T_A = 0°C to +70°C, V_{DDQ3} = 3.3V±5% (3.135–3.465V), f_{XTL} = 14.31818 MHz, V_{DDQ2} = 3.3±5%

AC clock parameters are tested and guaranteed over stated operating conditions using the stated transmission line load at the clock output.



CPU Clock Outputs, CPU0:3 (Test Load: R = 33Ω; C = 22 pF)

Parameter	Description	Test Condition/Comments	CPU = 100 MHz			Unit
			Min.	Typ.	Max.	
t_P	Period	Measured on rising edge at 1.5V		10		ns
f	Frequency, Actual	Determined by PLL divider ratio		100		MHz
t_H	High Time	Duration of clock cycle above 2.4V		5		ns
t_L	Low Time	Duration of clock cycle below 0.4V		5		ns
t_R	Output Rise Edge Rate	Measured from 0.4V to 2.4V	1		4	V/ns
t_F	Output Fall Edge Rate	Measured from 2.4V to 0.4V	1		4	V/ns
t_D	Duty Cycle	Measured on rising and falling edge at 1.5V	45	50	55	%
t_{JC}	Jitter, Cycle-to-Cycle	Measured on rising edge at 1.5V. Maximum difference of cycle time between two adjacent cycles.			250	ps
t_{SK}	Output Skew	Measured on rising edge at 1.5V			250	ps
f_{ST}	Frequency Stabilization from Power-up (cold start)	Assumes full supply voltage reached within 1 ms from power-up. Short cycles exist prior to frequency stabilization.			3	ms
Z_o	AC Output Impedance	Average value during switching transition. Used for determining series termination value.		10		Ω

SDRAM Clock Outputs, SDRAM0:7 (Test Load: R = 22Ω; C = 22 pF)

Parameter	Description	Test Condition/Comments	CPU = 100 MHz			Unit
			Min.	Typ.	Max.	
t_P	Period	Measured on rising edge at 1.5V		10		ns
f	Frequency, Actual	Determined by PLL divider ratio		100		MHz
t_R	Output Rise Edge Rate	Measured from 0.4V to 2.4V	1		4	V/ns
t_F	Output Fall Edge Rate	Measured from 2.4V to 0.4V	1		4	V/ns
t_D	Duty Cycle	Measured on rising and falling edge at 1.5V	45	50	55	%
t_{JC}	Jitter, Cycle-to-Cycle	Measured on rising edge at 1.5V. Maximum difference of cycle time between two adjacent cycles.			250	ps
t_{SK}	Output Skew	Measured on rising edge at 1.5V		100		ps
t_{SK}	CPU to SDRAM Clock Skew	Covers all CPU/SDRAM outputs. Measured on rising edge at 1.5V.			850	ps
f_{ST}	Frequency Stabilization from Power-up (cold start)	Assumes full supply voltage reached within 1 ms from power-up. Short cycles exist prior to frequency stabilization.			3	ms
Z_o	AC Output Impedance	Average value during switching transition. Used for determining series termination value.		16		Ω

PCI Clock Outputs, PCI0:5 (Test Load: R = 22Ω; C = 22 pF)

Parameter	Description	Test Condition/Comments	CPU = 100 MHz			Unit
			Min.	Typ.	Max.	
t_P	Period	Measured on rising edge at 1.5V		30		ns
f	Frequency, Actual	Determined by PLL divider ratio		33.3		MHz
t_H	High Time	Duration of clock cycle above 2.4V	12			ns
t_L	Low Time	Duration of clock cycle below 0.4V	12			ns
t_R	Output Rise Edge Rate		1		4	V/ns
t_F	Output Fall Edge Rate		1		4	V/ns
t_D	Duty Cycle	Measured on rising and falling edge at 1.5V	45	50	55	%
t_{JC}	Jitter, Cycle-to-Cycle	Measured on rising edge at 1.5V. Maximum difference of cycle time between two adjacent cycles.			250	ps
t_{SK}	Output Skew	Measured on rising edge at 1.5V			250	ps
t_O	CPU to PCI Clock Skew	Covers all CPU/PCI outputs. Measured on rising edge at 1.5V. CPU leads PCI output.	1		4	ns
f_{ST}	Frequency Stabilization from Power-up (cold start)	Assumes full supply voltage reached within 1 ms from power-up. Short cycles exist prior to frequency stabilization.			3	ms
Z_o	AC Output Impedance	Average value during switching transition. Used for determining series termination value.		15		Ω

I/O APIC Clock Output (Test Load: R = 33Ω; C = 22 pF)

Parameter	Description	Test Condition/Comments	CPU = 100 MHz			Unit
			Min.	Typ.	Max.	
f	Frequency, Actual	Frequency generated by crystal oscillator		14.31818		MHz
t_R	Output Rise Edge Rate		1		4	V/ns
t_F	Output Fall Edge Rate		1		4	V/ns
t_D	Duty Cycle	Measured on rising and falling edge at 1.5V	45	50	55	%
f_{ST}	Frequency Stabilization from Power-up (cold start)	Assumes full supply voltage reached within 1 ms from power-up. Short cycles exist prior to frequency stabilization.			1.5	ms
Z_o	AC Output Impedance	Average value during switching transition. Used for determining series termination value.		15		Ω

REF0 Clock Output (Test Load: R = 33Ω; C = 22 pF)

Parameter	Description	Test Condition/Comments	CPU = 100 MHz			Unit
			Min.	Typ.	Max.	
f	Frequency, Actual	Frequency generated by crystal oscillator		14.318		MHz
t_R	Output Rise Edge Rate	Measured from 0.4V to 2.4V	1		4	V/ns
t_F	Output Fall Edge Rate	Measured from 2.4V to 0.4V	1		4	V/ns
t_D	Duty Cycle	Measured on rising and falling edge at 1.5V	45	50	55	%
f_{ST}	Frequency Stabilization from Power-up (cold start)	Assumes full supply voltage reached within 1 ms from power-up. Short cycles exist prior to frequency stabilization.			1.5	ms
Z_o	AC Output Impedance	Average value during switching transition. Used for determining series termination value.		16		Ω

REF1 Clock Output (Lump Capacitance Test Load = 20 pF)

Parameter	Description	Test Condition/Comments	CPU = 100 MHz			Unit
			Min.	Typ.	Max.	
f	Frequency, Actual	Frequency generated by crystal oscillator		14.318		MHz
t_R	Output Rise Edge Rate		0.5		2	V/ns
t_F	Output Fall Edge Rate		0.5		2	V/ns
t_D	Duty Cycle	Measured on rising and falling edge at 1.5V	45		55	%
f_{ST}	Frequency Stabilization from Power-up (cold start)	Assumes full supply voltage reached within 1 ms from power-up. Short cycles exist prior to frequency stabilization.			1.5	ms
Z_o	AC Output Impedance	Average value during switching transition. Used for determining series termination value.		25		Ω

48-/24-MHz Clock Output (Test Load: R = 33Ω; C = 22 pF)

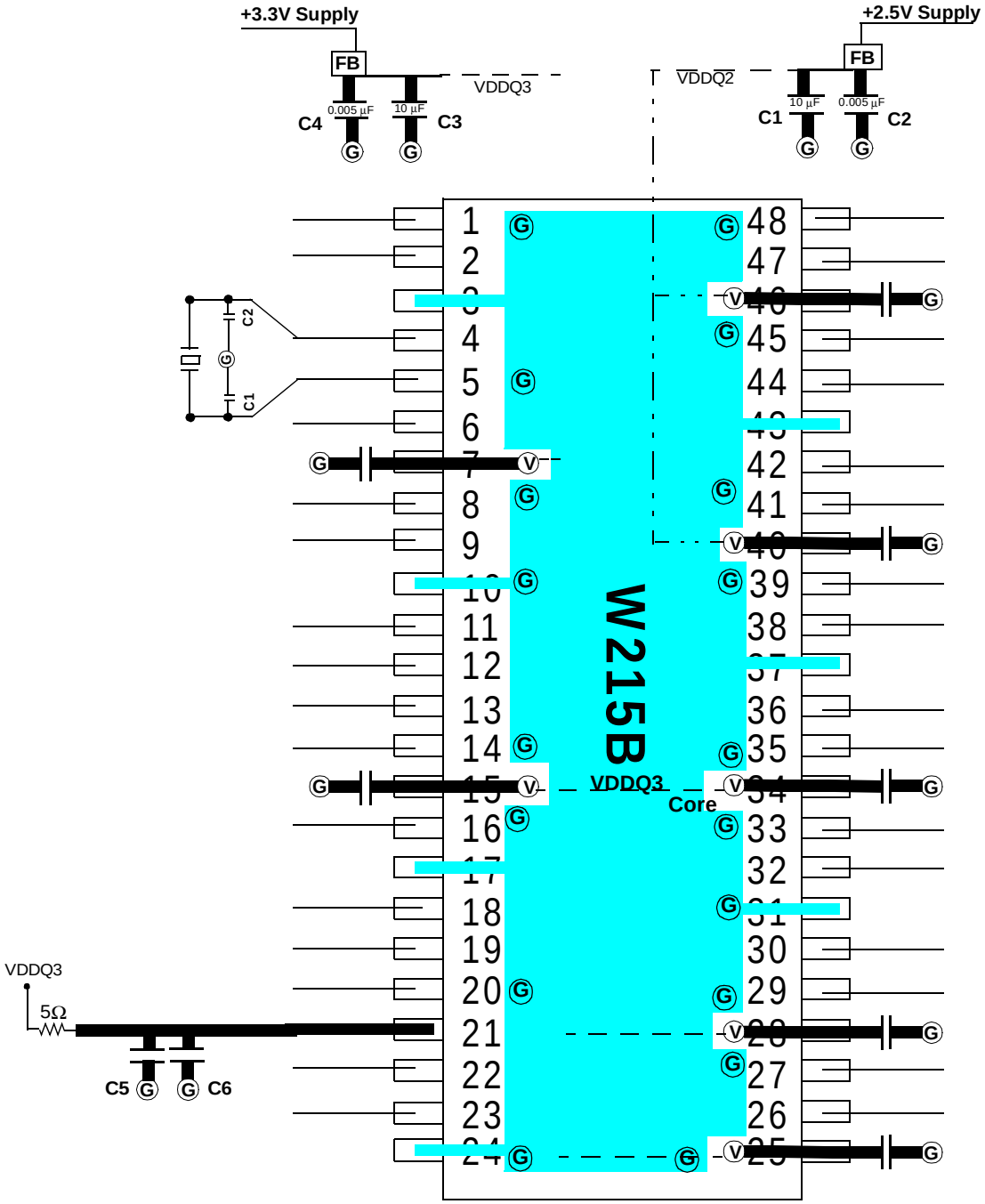
Parameter	Description	Test Condition/Comments	CPU = 100 MHz			Unit
			Min.	Typ.	Max.	
m/n	PLL Ratio			57/17		
t_R	Output Rise Edge Rate		0.5		2	V/ns
t_F	Output Fall Edge Rate		0.5		2	V/ns
t_D	Duty Cycle	Measured on rising and falling edge at 1.5V	45	50	55	%
f_{ST}	Frequency Stabilization from Power-up (cold start)	Assumes full supply voltage reached within 1 ms from power-up. Short cycles exist prior to frequency stabilization.			3	ms
Z_o	AC Output Impedance	Average value during switching transition. Used for determining series termination value.		25		Ω

Ordering Information

Ordering Code	Package Name	Package Type
W215B	X	48-pin TSSOP (6.1 mm)

Document #: 38-00886

Layout Example



FB = Dale ILB1206 - 300 (300Ω @ 100 MHz)

C1 & C3 = 10–22 µF C2 & C4 = 0.005 µF C5 = 47 µF C6 = 0.1 µF

Ⓖ = VIA to GND plane layer Ⓥ =VIA to respective supply plane layer

Note: Each supply plane or strip should have a **ferrite bead and capacitors**

Package Diagram

48-Pin Small Shrink Outline Package (TSSOP, 6.1 mm)