PRELIMINARY

W161

133-MHz Spread Spectrum FTG for Pentium® II Platforms

Features

- **Maximized EMI Suppression using Cypress's Spread Spectrum Technology**
- **Three copies of CPU outputs at 100 or 133 MHz**
- **Three copies of 66-MHz output at 3.3V**
- **Ten copies of PCI clocks at 33 MHz, 3.3V**
- **Two copies of 14.318-MHz reference output at 3.3V**
- **One copy of 48-MHz USB clock**
- **One copy of CPU-divide-by-2 output as reference input to Direct Rambus™ Clock Generator (Cypress W134)**
- **Available in 48-pin SSOP (300 mils)**

Key Specifications

Supply Voltages: ..... V_{DDQ2} = 2.5V±5%
V_{DDQ3} = 3.3V±5%

CPU, CPUdiv2 Output Jitter:..... 250 ps

CPU, CPUdiv2 Output Skew:..... 175 ps

IOAPIC, 3V66 Output Skew:..... 250 ps

PCI0:9 Output Skew: ..... 500 ps

Duty Cycle: 45/55

Spread Spectrum Modulation:..... –0.5%

CPU to 3V66 Output Offset:..... 0.0–1.5 ns (CPU leads)

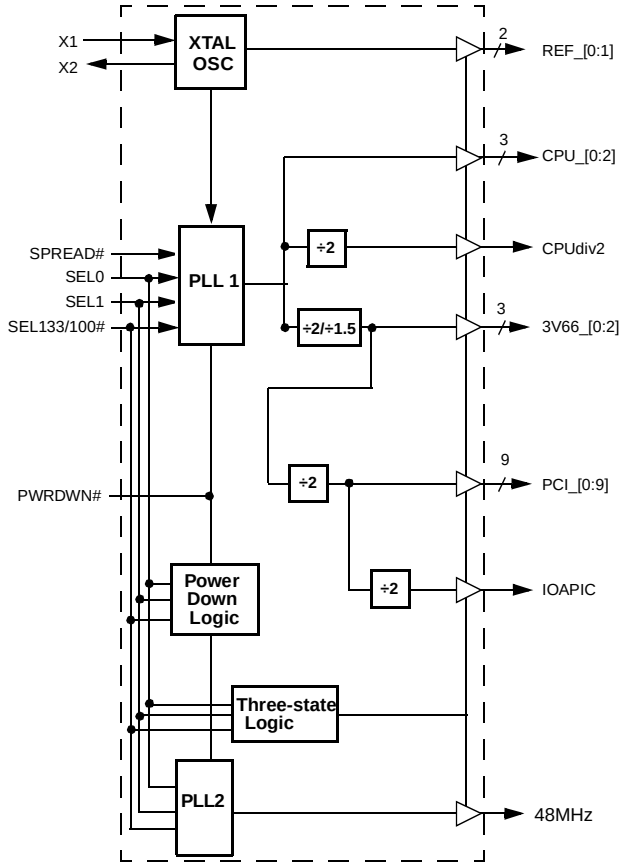
3V66 to PCI Output Offset:..... 1.5–3.0 ns (3V66 leads)

CPU to IOAPIC Output Offset: ..... 1.5–4.0 ns (CPU leads)

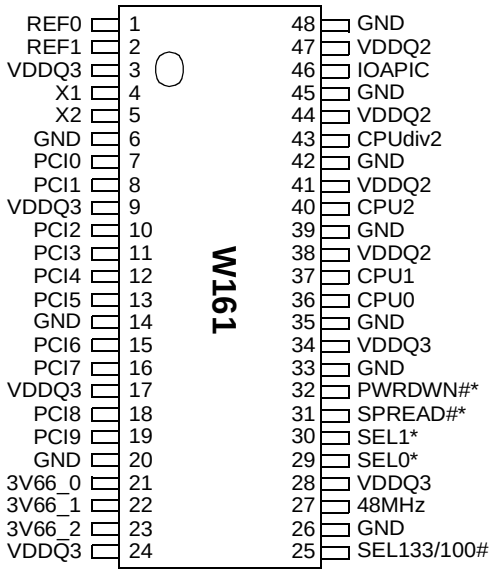
Table 1. Pin Selectable Frequency

SEL133/100#	SEL1	SEL0	Function
0	0	0	All outputs Three-State
0	0	1	(Reserved)
0	1	0	Active 100-MHz, 48-MHz PLL inactive
0	1	1	Active 100-MHz, 48-MHz PLL active
1	0	0	Test Mode
1	0	1	(Reserved)
1	1	0	Active 133-MHz, 48-MHz PLL inactive
1	1	1	Active 133-MHz, 48-MHz PLL active

Block Diagram



Pin Configuration[1]



Note:

1. Internal 250-kΩ pull-up resistors present on inputs marked with *. Design should not rely solely on internal pull-up resistor to set I/O pins HIGH.

Pin Definitions

Pin Name	Pin No.	Pin Type	Pin Description
CPU0:2	36, 37, 40	O	***CPU Clock Outputs 0 through 2:*** CPU clock outputs. Their output voltage swing is controlled by voltage applied to VDDQ2.
PCI0:9	7, 8, 10, 11, 12, 13, 15, 16, 18, 19	O	***PCI Clock Outputs 0 through 9:*** Output voltage swing is controlled by voltage applied to VDDQ3.
CPUdiv2	43	O	***CPU-Divide-By-2 Output:*** This serves as a reference input signal for Direct Rambus Clock Generator (Cypress W134). The output voltage is determined by VDDQ2.
3V66_0:2	21, 22, 23	O	***66-MHz Clock Outputs 0 through 2:*** Output voltage swing is controlled by voltage applied to VDDQ3.
IOAPIC	46	O	***I/O APIC Clock Output:*** Provides an output synchronous to CPU clock. See *Table 1* for their relation to other system clock outputs.
48 MHz	27	O	***48-MHz Output:*** Fixed clock output at 48 MHz.
SPREAD#	31	I	***Spread Spectrum Enable:*** This input enables spread spectrum modulation on the PLL1 generated frequency outputs of the W161. Modulation range is –0.5%.
PWRDWN#	32	I	***Power Down Control***
REF0:1	1, 2	I	***Fixed 14.318-MHz Output 0 and 1:*** Output voltage swing is controlled by voltage applied to VDDQ3.
SEL0:1	29, 30	I	***Mode Select Input 0 through 1:*** 3.3V LVTTL-compatible input for selecting clock output modes. As shown in *Table 1*.
SEL133/100#	25	I	***Frequency Selection Input:*** 3.3V LVTTL-compatible input that selects CPU output frequency as shown in *Table 1*.
X1	4	I	***Crystal Connection or External Reference Frequency Input:*** This pin has dual functions. It can be used as an external 14.318-MHz crystal connection or as an external reference frequency input.
X2	5	I	***Crystal Connection:*** An input connection for an external 14.318-MHz crystal. If using an external reference, this pin must be left unconnected.
VDDQ2	38, 41, 44, 47	P	***Power Connection:*** Connected to 2.5V power supply.
VDDQ3	3, 9, 17, 24, 28, 34	P	***Power Connection:*** Connected to 3.3V power supply.
GND	6, 14, 20, 26, 33, 35, 39, 42, 45, 48	G	***Ground Connection:*** Connect all ground pins to the common system ground plane.

Overview

The W161, a motherboard clock synthesizer, provides 2.5V CPU clock outputs for advanced CPU and a CPU-divide-by-2 reference frequency for Direct Rambus Clock Generator (such Cypress W134) interface. Fixed output frequencies are provided for other system functions.

CPU Frequency Selection

CPU frequency is selected with input pins 25, 29, and 30 (SEL133/100#, SEL0, and SEL1, respectively). Refer to *Table 1* for details.

Output Buffer Configuration

Clock Outputs

All clock outputs are designed to drive serial terminated clock lines. The W161 outputs are CMOS-type, which provide rail-to-rail output swing.

Crystal Oscillator

The W161 requires one input reference clock to synthesize all output frequencies. The reference clock can be either an externally generated clock signal or the clock generated by the internal crystal oscillator. When using an external clock signal, pin X1 is used as the clock input and pin X2 is left open.

The internal crystal oscillator is used in conjunction with a quartz crystal connected to device pins X1 and X2. This forms a parallel resonant crystal oscillator circuit. The W161 incorporates the necessary feedback resistor and crystal load capacitors. Including typical stray circuit capacitance, the total load presented to the crystal is approximately 18 pF. For optimum frequency accuracy without the addition of external capacitors, a parallel-resonant mode crystal specifying a load of 18 pF should be used. This will typically yield reference frequency accuracies within ±100 ppm.

Spread Spectrum Feature

The device generates a clock that is frequency modulated in order to increase the bandwidth that it occupies. By increasing the bandwidth of the fundamental and its harmonics, the amplitudes of the radiated electromagnetic emissions are reduced. This effect is depicted in *Figure 1*.

As shown in *Figure 1*, a harmonic of a modulated clock has a much lower amplitude than that of an unmodulated signal. The reduction in amplitude is dependent on the harmonic number and the frequency deviation or spread. The equation for the reduction is

$$dB = 6.5 + 9*\log_{10}(P) + 9*\log_{10}(F)$$

Where *P* is the percentage of deviation and *F* is the frequency in MHz where the reduction is measured.

The output clock is modulated with a waveform depicted in *Figure 2*. This waveform, as discussed in "Spread Spectrum Clock Generation for the Reduction of Radiated Emissions" by Bush, Fessler, and Hardin produces the maximum reduction in the amplitude of radiated electromagnetic emissions. The deviation selected for this chip is –0.5% downspread. *Figure 2* details the Cypress spreading pattern. Cypress does offer options with more spread and greater EMI reduction. Contact your local Sales representative for details on these devices.

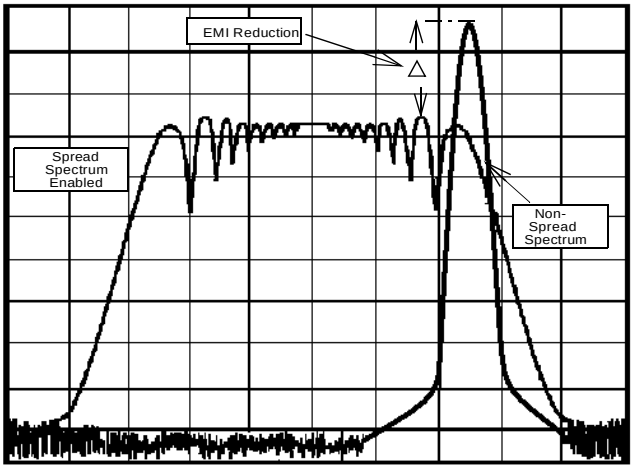


Figure 1. Typical Clock and SSFTG Comparison

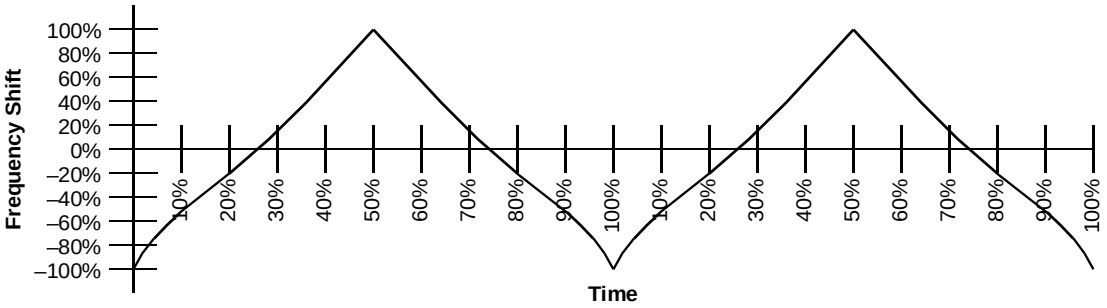


Figure 2. Typical Modulation Profile

Absolute Maximum Ratings

Stresses greater than those listed in this table may cause permanent damage to the device. These represent a stress rating only. Operation of the device at these or any other conditions above those specified in the operating sections of this specification is not implied. Maximum conditions for extended periods may affect reliability.

Parameter	Description	Rating	Unit
V_{DD}, V_{IN}	Voltage on any pin with respect to GND	–0.5 to +7.0	V
T_{STG}	Storage Temperature	–65 to +150	°C
T_A	Operating Temperature	0 to +70	°C
T_B	Ambient Temperature under Bias	–55 to +125	°C
ESD_{PROT}	Input ESD Protection	2 (min.)	kV

DC Electrical Characteristics: T_A = 0°C to +70°C, V_{DDQ3} = 3.3V±5%, V_{DDQ2} = 2.5V±5%

Parameter	Description	Test Condition	Min.	Typ.	Max.	Unit
Supply Current						
$I_{DD-3.3V}$	Combined 3.3V Supply Current	CPU0:3 =133 MHz[2]			160	mA
$I_{DD-2.5}$	Combined 2.5V Supply Current	CPU0:3 =133 MHz[2]			90	mA
Logic Inputs (All referenced to V_{DDQ3} = 3.3V)						
V_{IL}	Input Low Voltage		GND – 0.3		0.8	V
V_{IH}	Input High Voltage		2.0		V_{DD} + 0.3	V
I_{IL}	Input Low Current[3]				–25	µA
I_{IH}	Input High Current[3]				10	µA
I_{IL}	Input Low Current, SEL133/100#[3]				–5	µA
I_{IH}	Input High Current, SEL133/100#[3]				5	µA
Clock Outputs						
CPU, CPUdiv2, IOAPIC (Referenced to V_{DDQ2})		**Test Condition**	**Min.**	**Typ.**	**Max.**	**Unit**
V_{OL}	Output Low Voltage	I_{OL} = 1 mA			50	mV
V_{OH}	Output High Voltage	I_{OH} = –1 mA	2.2			V
I_{OL}	Output Low Current	V_{OL} = 1.25V	45	65	100	mA
I_{OH}	Output High Current	V_{OH} = 1.25V	45	65	100	mA
48MHz, REF (Referenced to V_{DDQ3})		**Test Condition**	**Min.**	**Typ.**	**Max.**	**Unit**
V_{OL}	Output Low Voltage	I_{OL} = 1 mA			50	mV
V_{OH}	Output High Voltage	I_{OH} = –1 mA	3.1			V
I_{OL}	Output Low Current	V_{OL} = 1.5V	45	65	100	mA
I_{OH}	Output High Current	V_{OH} = 1.5V	45	65	100	mA
PCI, 3V66 (Referenced to V_{DDQ3})		**Test Condition**	**Min.**	**Typ.**	**Max.**	**Unit**
V_{OL}	Output Low Voltage	I_{OL} = 1 mA			50	mV
V_{OH}	Output High Voltage	I_{OH} = –1 mA	3.1			V
I_{OL}	Output Low Current	V_{OL} = 1.5V	70	100	145	mA
I_{OH}	Output High Current	V_{OH} = 1.5V	65	95	135	mA

Notes:
2. All clock outputs loaded with 6" 60Ω transmission lines with 20-pF capacitors.
3. W161 logic inputs have internal pull-up devices, except SEL133/100# (pull-ups not CMOS level).

DC Electrical Characteristics: T_A = 0°C to +70°C, V_{DDQ3} = 3.3V±5%, V_{DDQ2} = 2.5V±5% (continued)

Parameter	Description	Test Condition	Min.	Typ.	Max.	Unit
Crystal Oscillator						
V_{TH}	X1 Input threshold Voltage[4]			1.65		V
C_{LOAD}	Load Capacitance, Imposed on External Crystal[5]			18		pF
$C_{IN,X1}$	X1 Input Capacitance[6]	Pin X2 unconnected		28		pF
Pin Capacitance/Inductance						
C_{IN}	Input Pin Capacitance	Except X1 and X2			5	pF
C_{OUT}	Output Pin Capacitance				6	pF
L_{IN}	Input Pin Inductance				7	nH

3.3V AC Electrical Characteristics

T_A = 0°C to +70°C, V_{DDQ3} = 3.3V±5%,V_{DDQ2} = 2.5V± 5%, f_{XTL} = 14.31818 MHz
Spread Spectrum function turned off

AC clock parameters are tested and guaranteed over stated operating conditions using the stated lump capacitive load at the clock output.[7]

3V66 Clock Outputs, 3V66_0:3 (Lump Capacitance Test Load = 30 pF)

Parameter	Description	Test Condition/Comments	Min.	Typ.	Max.	Unit
f	Frequency	Note 8		66.6		MHz
t_R	Output Rise Edge Rate	Measured from 0.4V to 2.4V	1		4	V/ns
t_F	Output Fall Edge Rate	Measured from 2.4V to 0.4V	1		4	V/ns
t_D	Duty Cycle	Measured on rising and falling edge at 1.5V	45		55	%
f_{ST}	Frequency Stabilization from Power-up (cold start)	Assumes full supply voltage reached within 1 ms from power-up. Short cycles exist prior to frequency stabilization.			3	ms
Z_o	AC Output Impedance	Average value during switching transition. Used for determining series termination value.		15		Ω

Notes:
4. X1 input threshold voltage (typical) is $V_{DD}/2$.
5. The W161 contains an internal crystal load capacitor between pin X1 and ground and another between pin X2 and ground. Total load placed on crystal is 18 pF; this includes typical stray capacitance of short PCB traces to crystal.
6. X1 input capacitance is applicable when driving X1 with an external clock source (X2 is left unconnected).
7. Period, jitter, offset, and skew measured on rising edge at 1.5V.
8. 3V66 is CPU/2 for CPU =133 MHz and (2 x CPU)/3 for CPU = 100 MHz.

PCI Clock Outputs, PCI0:9 (Lump Capacitance Test Load = 30 pF

Parameter	Description	Test Condition/Comments	Min.	Typ.	Max.	Unit
t_P	Period	Measured on rising edge at 1.5V[9]	30			ns
t_H	High Time	Duration of clock cycle above 2.4V	12			ns
t_L	Low Time	Duration of clock cycle below 0.4V	12			ns
t_R	Output Rise Edge Rate	Measured from 0.4V to 2.4V	1		4	V/ns
t_F	Output Fall Edge Rate	Measured from 2.4V to 0.4V	1		4	V/ns
t_D	Duty Cycle	Measured on rising and falling edge at 1.5V	45		55	%
t_{JC}	Jitter, Cycle-to-Cycle	Measured on rising edge at 1.5V. Maximum difference of cycle time between two adjacent cycles.			500	ps
t_{SK}	Output Skew	Measured on rising edge at 1.5V.			500	ps
t_O	3V66 to PCI Clock Skew	Covers all 3V66/PCI outputs. Measured on rising edge at 1.5V. 3V66 leads PCI output.	1.5		3	ns
f_{ST}	Frequency Stabilization from Power-up (cold start)	Assumes full supply voltage reached within 1 ms from power-up. Short cycles exist prior to frequency stabilization.			3	ms
Z_o	AC Output Impedance	Average value during switching transition. Used for determining series termination value.		15		Ω

REF Clock Outputs, REF0:1 (Lump Capacitance Test Load = 20 pF)

Parameter	Description	Test Condition/Comments	Min.	Typ.	Max.	Unit
f	Frequency, Actual	Frequency generated by crystal oscillator		14.318		
t_R	Output Rise Edge Rate	Measured from 0.4V to 2.4V	0.5		2	V/ns
t_F	Output Fall Edge Rate	Measured from 2.4V to 0.4V	0.5		2	V/ns
t_D	Duty Cycle	Measured on rising and falling edge at 1.5V	45		55	%
f_{ST}	Frequency Stabilization from Power-up (cold start)	Assumes full supply voltage reached within 1 ms from power-up. Short cycles exist prior to frequency stabilization.			3	ms
Z_o	AC Output Impedance	Average value during switching transition. Used for determining series termination value.		25		Ω

48-MHZ Clock Output (Lump Capacitance Test Load = 20 pF)

Parameter	Description	Test Condition/Comments	Min.	Typ.	Max.	Unit
f	Frequency, Actual	Determined by PLL divider ratio (see m/n below)		48.008		MHz
f_D	Deviation from 48 MHz	(48.008 – 48)/48		+167		ppm
m/n	PLL Ratio	(14.31818 MHz x 57/17 = 48.008 MHz)		57/17		
t_R	Output Rise Edge Rate	Measured from 0.4V to 2.4V	0.5		2	V/ns
t_F	Output Fall Edge Rate	Measured from 2.4V to 0.4V	0.5		2	V/ns
t_D	Duty Cycle	Measured on rising and falling edge at 1.5V	45		55	%
f_{ST}	Frequency Stabilization from Power-up (cold start)	Assumes full supply voltage reached within 1 ms from power-up. Short cycles exist prior to frequency stabilization.			3	ms
Z_o	AC Output Impedance	Average value during switching transition. Used for determining series termination value.		25		Ω

Note:

9. PCI clock is CPU/4 for CPU = 133 MHz and CPU/3 for CPU = 100 MHz.

2.5V AC Electrical Characteristics

T_A = 0°C to +70°C, V_{DDQ3} = 3.3V±5%, V_{DDQ2}= 2.5V±5%
f_{XTL} = 14.31818 MHz
Spread Spectrum function turned off

AC clock parameters are tested and guaranteed over stated operating conditions using the stated lump capacitive load at the clock output.[10]

CPU Clock Outputs, CPU0:2 (Lump Capacitance Test Load = 20 pF)

Parameter	Description	Test Condition/Comments	CPU = 133 MHz			CPU = 100 MHz			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
t_P	Period	Measured on rising edge at 1.25V	7.5		7.65	10		10.2	ns
t_H	High Time	Duration of clock cycle above 2.0V	1.87			3.0			ns
t_L	Low Time	Duration of clock cycle below 0.4V	1.67			2.8			ns
t_R	Output Rise Edge Rate	Measured from 0.4V to 2.0V	1		4	1		4	V/ns
t_F	Output Fall Edge Rate	Measured from 2.0V to 0.4V	1		4	1		4	V/ns
t_D	Duty Cycle	Measured on rising and falling edge at 1.25V	45		55	45		55	%
t_{JC}	Jitter, Cycle-to-Cycle	Measured on rising edge at 1.25V. Maximum difference of cycle time between two adjacent cycles.			250			250	ps
t_{SK}	Output Skew	Measured on rising edge at 1.25V			175			175	ps
f_{ST}	Frequency Stabilization from Power-up (cold start)	Assumes full supply voltage reached within 1 ms from power-up. Short cycles exist prior to frequency stabilization.			3			3	ms

CPUdiv2 Clock Outputs, CPUdiv2 (Lump Capacitance Test Load = 20 pF)

Parameter	Description	Test Condition/Comments	CPU = 133 MHz			CPU = 100 MHz			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
t_P	Period	Measured on rising edge at 1.25V	15		15.3	20		20.4	ns
t_H	High Time	Duration of clock cycle above 2.0V	5.25			7.5			ns
t_L	Low Time	Duration of clock cycle below 0.4V	5.05			7.3			ns
t_R	Output Rise Edge Rate	Measured from 0.4V to 2.0V	1		4	1		4	V/ns
t_F	Output Fall Edge Rate	Measured from 2.0V to 0.4V	1		4	1		4	V/ns
t_D	Duty Cycle	Measured on rising and falling edge at 1.25V	45		55	45		55	%
t_{JC}	Jitter, Cycle-to-Cycle	Measured on rising edge at 1.25V. Maximum difference of cycle time between two adjacent cycles.			250			250	ps
t_{SK}	Output Skew	Measured on rising edge at 1.25V			175			175	ps
f_{ST}	Frequency Stabilization from Power-up (cold start)	Assumes full supply voltage reached within 1 ms from power-up. Short cycles exist prior to frequency stabilization.			3			3	ms
Z_o	AC Output Impedance	Average value during switching transition. Used for determining series termination value.		20			20		Ω

Note:
10. Period, Jitter, offset. and skew measured on rising edge at 1.25V.

IOAPIC Clock Output, IOAPIC (Lump Capacitance Test Load = 20 pF)

Parameter	Description	Test Condition/Comments	Min	Typ	Max	Unit
f	Frequency	Note 11		16.67		MHz
t_R	Output Rise Edge Rate	Measured from 0.4V to 2.0V	1		4	V/ns
t_F	Output Fall Edge Rate	Measured from 2.0V to 0.4V	1		4	V/ns
t_D	Duty Cycle	Measured on rising and falling edge at 1.25V	45		55	%
f_{ST}	Frequency Stabilization from Power-up (cold start)	Assumes full supply voltage reached within 1 ms from power-up. Short cycles exist prior to frequency stabilization.			3	ms
Z_o	AC Output Impedance	Average value during switching transition. Used for determining series termination value.		20		Ω

Note:

11. IOAPIC clock is CPU/8 for CPU = 133 MHz and CPU/6 for CPU = 100 MHz.

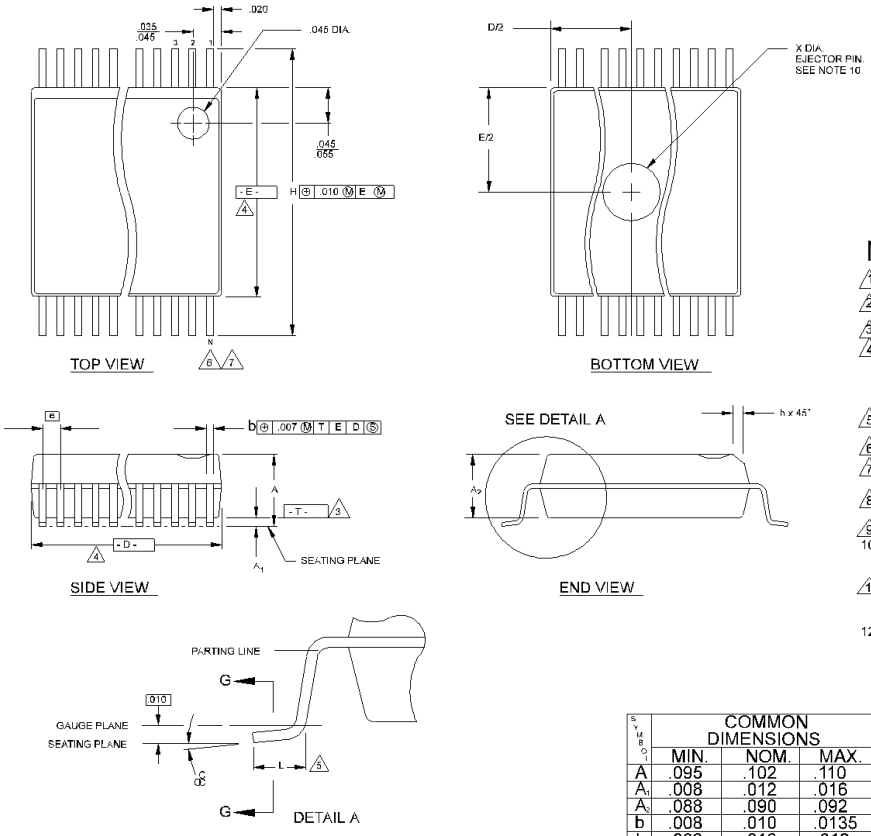
Ordering Information

Ordering Code	Package Name	Package Type
W161	H	48-pin SSOP (300 mils)

Document #: 38-00817

Package Diagram

48-Pin Small Shrink Outline Package (SSOP, 300 mils)



NOTES:

1. MAXIMUM DIE THICKNESS ALLOWABLE IS .025.
2. DIMENSIONING & TOLERANCING PER ANSI Y14.5M - 1982.
3. "T" IS A REFERENCE DATUM.
4. "D" & "E" ARE REFERENCE DATUMS AND DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS, BUT DOES INCLUDE MOLD MISMATCH AND ARE MEASURED AT THE MOLD PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .006 INCHES PER SIDE.
5. "L" IS THE LENGTH OF TERMINAL FOR SOLDERING TO A SUBSTRATE.
6. "N" IS THE NUMBER OF TERMINAL POSITIONS.
7. TERMINAL POSITIONS ARE SHOWN FOR REFERENCE ONLY.
8. FORMED LEADS SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITHIN .003 INCHES AT SEATING PLANE.
9. CONTROLLING DIMENSION: INCHES.
10. COUNTRY OF ORIGIN LOCATION AND EJECTOR PIN ON PACKAGE BOTTOM IS OPTIONAL AND DEPENDS ON ASSEMBLY LOCATION.
11. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .005 INCHES AND .010 INCHES FROM THE LEAD TIPS.
12. THIS PART IS COMPLIANT WITH JEDEC SPECIFICATION MO-118, VARIATIONS AA, AB, EXCEPT CHAMFER DIMENSION h. JEDEC SPECIFICATION FOR h IS .015"/.025".

SYMBOL	COMMON DIMENSIONS			NOTE	NOTE VARIATIONS	4 D			6 N
	MIN.	NOM.	MAX.			MIN.	NOM.	MAX.	
A	.095	.102	.110		AA	.620	.625	.630	48
A_1	.008	.012	.016		AB	.720	.725	.730	56
A_2	.088	.090	.092						
b	.008	.010	.0135						
b_1	.008	.010	.012						
c	.005	-	.010						
c_1	.005	.006	.0085						
D	SEE VARIATIONS			4					
E	.292	.296	.299						
e	.025 BSC								
H	.400	.406	.410						
h	.010	.013	.016						
L	.024	.032	.040						
N	SEE VARIATIONS			6					
X	.085	.093	.100	10					
α	0°	5°	8°						

THIS TABLE IN INCHES

Summary of nominal dimensions in inches:

Body Width: 0.296
Lead Pitch: 0.025
Body Length: 0.625
Body Height: 0.102

SYMBOL	COMMON DIMENSIONS			NOTE	NOTE VARIATIONS	4 D			6 N
	MIN.	NOM.	MAX.			MIN.	NOM.	MAX.	
A	2.41	2.59	2.79		AA	15.75	15.88	16.00	48
A_1	0.20	0.31	0.41		AB	18.29	18.42	18.54	56
A_2	2.24	2.29	2.34						
b	0.203	0.254	0.343						
b_1	0.203	0.254	0.305						
c	0.127	-	0.254						
c_1	0.127	0.152	0.216						
D	SEE VARIATIONS			4					
E	7.42	7.52	7.59						
e	0.635 BSC								
H	10.16	10.31	10.41						
h	0.25	0.33	0.41						
L	0.61	0.81	1.02						
N	SEE VARIATIONS			6					
X	2.16	2.36	2.54	10					
α	0°	5°	8°						

THIS TABLE IN MILLIMETERS