

440BX AGPset Spread Spectrum Frequency Synthesizer

Features

- Maximized electromagnetic interference (EMI) suppression using Cypress's Spread Spectrum technology
- Single-chip system frequency synthesizer for Intel® 440BX AGPset
- Three copies of CPU output
- Seven copies of PCI output
- One 48 MHz output for USB/one 24 MHz for SIO
- Two buffered reference outputs
- Two IOAPIC outputs
- 17 SDRAM outputs provide support for four DIMMs
- Supports frequencies up to 150 MHz
- SMBus interface for programming
- Power management control inputs

Key Specifications

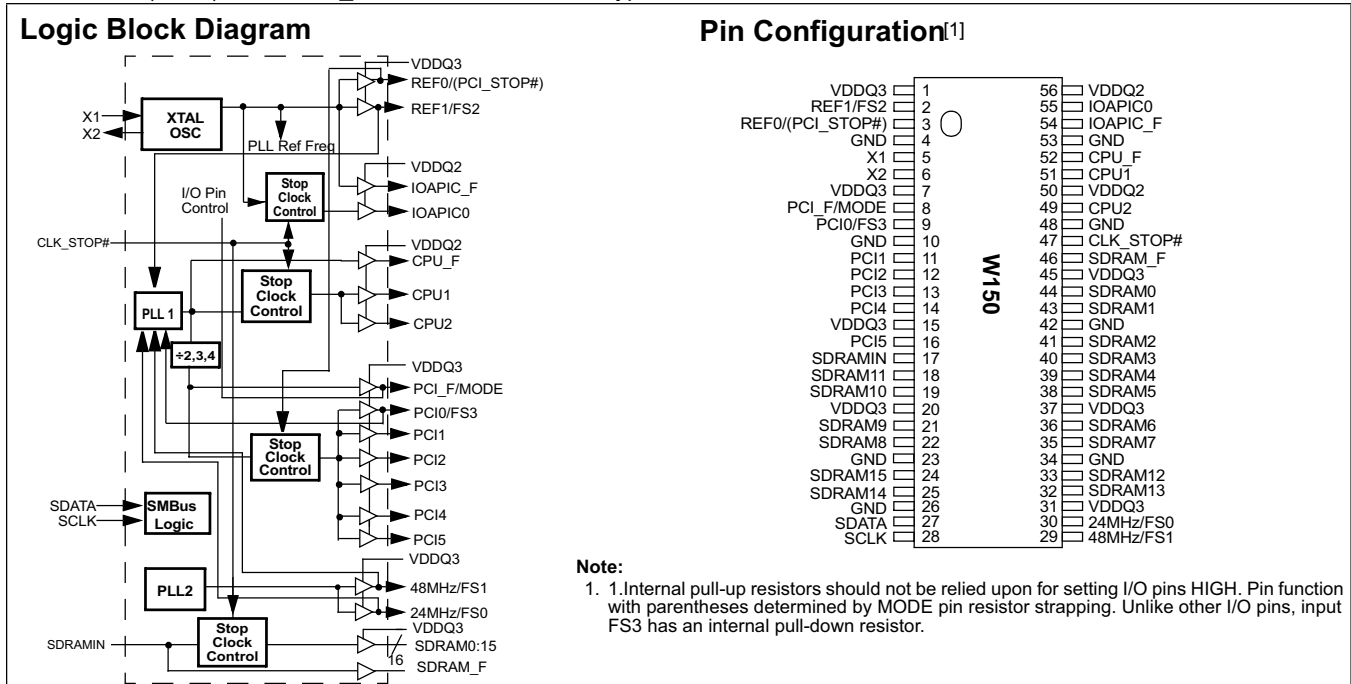
CPU Cycle-to-Cycle Jitter: 250 ps
 CPU to CPU Output Skew: 175 ps
 PCI to PCI Output Skew: 500 ps
 SDRAMIN to SDRAM0:15 Delay: 3.7 ns typ.
 V_{DDQ3} : $3.3V \pm 5\%$
 V_{DDQ2} : $2.5V \pm 5\%$
 SDRAM0:15 (leads) to SDRAM_F Skew: 0.4 ns typ.

Table 1. Mode Input Table

| Mode | Pin 3 |
|------|-----------|
| 0 | PCI_STOP# |
| 1 | REF0 |

Table 2. Pin Selectable Frequency

| Input Address | | | | CPU F, 1:2 (MHz) | PCI F, 0:5 (MHz) |
|---------------|-----|-----|-----|------------------|------------------|
| FS3 | FS2 | FS1 | FS0 | | |
| 1 | 1 | 1 | 1 | 133.3 | 33.3 (CPU/4) |
| 1 | 1 | 1 | 0 | 124 | 31 (CPU/4) |
| 1 | 1 | 0 | 1 | 150 | 37.5 (CPU/4) |
| 1 | 1 | 0 | 0 | 140 | 35 (CPU/4) |
| 1 | 0 | 1 | 1 | 105 | 35 (CPU/3) |
| 1 | 0 | 1 | 0 | 110 | 36.7 (CPU/3) |
| 1 | 0 | 0 | 1 | 115 | 38.3 (CPU/3) |
| 1 | 0 | 0 | 0 | 120 | 40 (CPU/3) |
| 0 | 1 | 1 | 1 | 100 | 33.3 (CPU/3) |
| 0 | 1 | 1 | 0 | 133.3 | 44.43 (CPU/3) |
| 0 | 1 | 0 | 1 | 112 | 37.3 (CPU/3) |
| 0 | 1 | 0 | 0 | 103 | 34.3 (CPU/3) |
| 0 | 0 | 1 | 1 | 66.8 | 33.4 (CPU/2) |
| 0 | 0 | 1 | 0 | 83.3 | 41.7 (CPU/2) |
| 0 | 0 | 0 | 1 | 75 | 37.5 (CPU/2) |
| 0 | 0 | 0 | 0 | 124 | 41.3 (CPU/3) |



Pin Definitions

| Pin Name | Pin No. | Pin Type | Pin Description |
|---------------------|--|----------|---|
| CPU1:2 | 51, 49 | O | CPU Outputs 1 and 2: Frequency is set by the FS0:3 inputs or through serial input interface, see <i>Table 2</i> and <i>Table 6</i> . These outputs are affected by the CLK_STOP# input. |
| CPU_F | 52 | O | Free-Running CPU Output: Frequency is set by the FS0:3 inputs or through serial input interface, see <i>Table 2</i> and <i>Table 6</i> . This output is not affected by the CLK_STOP# input. |
| PCI1:5 | 11, 12, 13, 14, 16 | O | PCI Outputs 1 through 5: Frequency is set by the FS0:3 inputs or through serial input interface, see <i>Table 2</i> and <i>Table 6</i> . These outputs are affected by the PCI_STOP# input. |
| PCI0/FS3 | 9 | I/O | PCI Output/Frequency Select Input: As an output, frequency is set by the FS0:3 inputs or through serial input interface, see <i>Table 2</i> and <i>Table 6</i> . This output is affected by the PCI_STOP# input. When an input, latches data selecting the frequency of the CPU and PCI outputs. |
| PCI_F/MODE | 8 | I/O | Free Running PCI Output: Frequency is set by the FS0:3 inputs or through serial input interface, see <i>Table 2</i> and <i>Table 6</i> . This output is not affected by the PCI_STOP# input. When an input, selects function of pin 3 as described in <i>Table 1</i> . |
| CLK_STOP# | 47 | I | CLK_STOP# Input: When brought LOW, affected outputs are stopped LOW after completing a full clock cycle (2–3 CPU clock latency). When brought HIGH, affected outputs start beginning with a full clock cycle (2–3 CPU clock latency). |
| IOAPIC_F | 54 | O | Free-running IOAPIC Output: This output is a buffered version of the reference input which is not affected by the CPU_STOP# logic input. Its swing is set by voltage applied to VDDQ2. |
| IOAPIC0 | 55 | O | IOAPIC Output: Provides 14.318 MHz fixed frequency. The output voltage swing is set by voltage applied to VDDQ2. This output is disabled when CLK_STOP# is set LOW. |
| 48MHz/FS1 | 29 | I/O | 48 MHz Output: 48 MHz is provided in normal operation. In standard systems, this output can be used as the reference for the Universal Serial Bus. Upon power up, FS1 input will be latched, setting output frequencies as described in <i>Table 2</i> . |
| 24MHz/FS0 | 30 | I/O | 24 MHz Output: 24 MHz is provided in normal operation. In standard systems, this output can be used as the clock input for a Super I/O chip. Upon power up, FS0 input will be latched, setting output frequencies as described in <i>Table 2</i> . |
| REF1/FS2 | 2 | I/O | Reference Output: 14.318 MHz is provided in normal operation. Upon power-up, FS2 input will be latched, setting output frequencies as described in <i>Table 2</i> . |
| REF0 (PCI_STOP#) | 3 | I/O | Fixed 14.318 MHz Output 0 or PCI_STOP# Pin: Function determined by MODE pin. The PCI_STOP# input enables the PCI 0:5 outputs when HIGH and causes them to remain at logic 0 when LOW. The PCI_STOP signal is latched on the rising edge of PCI_F. Its effects take place on the next PCI_F clock cycle. As an output, this pin provides a fixed clock signal equal in frequency to the reference signal provided at the X1/X2 pins (14.318 MHz). |
| SDRAMIN | 17 | I | Buffered Input Pin: The signal provided to this input pin is buffered to 17 outputs (SDRAM0:15, SDRAM_F). |
| SDRAM0:15 | 44, 43, 41, 40, 39, 38, 36, 35, 22, 21, 19, 18, 33, 32, 25, 24 | O | Buffered Outputs: These sixteen dedicated outputs provide copies of the signal provided at the SDRAMIN input. The swing is set by VDDQ3, and they are deactivated when CLK_STOP# input is set LOW. |
| SDRAM_F | 46 | O | Free-Running Buffered Output: This output provides a single copy of the SDRAMIN input. The swing is set by VDDQ3; this signal is unaffected by the CLK_STOP# input. |
| SCLK | 28 | I | Clock pin for SMBus circuitry. |
| SDATA | 27 | I/O | Data pin for SMBus circuitry. |
| X1 | 5 | I | Crystal Connection or External Reference Frequency Input: This pin has dual functions. It can be used as an external 14.318 MHz crystal connection or as an external reference frequency input. |
| X2 | 6 | I | Crystal Connection: An input connection for an external 14.318-MHz crystal. If using an external reference, this pin must be left unconnected. |
| VDDQ3 | 1, 7, 15, 20, 31, 37, 45 | P | Power Connection: Power supply for core logic, PLL circuitry, SDRAM output buffers, PCI output buffers, reference output buffers, and 48 MHz/24 MHz output buffers. Connect to 3.3V. |

Pin Definitions (continued)

| Pin Name | Pin No. | Pin Type | Pin Description |
|----------|-------------------------------|----------|---|
| VDDQ2 | 50, 56 | P | Power Connection: Power supply for IOAPIC and CPU output buffers. Connect to 2.5V or 3.3V. |
| GND | 4, 10, 23, 26, 34, 42, 48, 53 | G | Ground Connections: Connect all ground pins to the common system ground plane. |

Overview

The W150 was designed as a single-chip alternative to the standard two-chip Intel 440BX AGPset clock solution. It provides sufficient outputs to support most single-processor, four SDRAM DIMM designs.

Functional Description
I/O Pin Operation

Pins 2, 8, 9, 29, and 30 are dual-purpose I/O pins. Upon power-up these pins act as logic inputs, allowing the determination of assigned device functions. A short time after power-up, the logic state of each pin is latched and the pins become clock outputs. This feature reduces device pin count by combining clock outputs with input select pins.

An external 10-k Ω "strapping" resistor is connected between the I/O pin and ground or V_{DD} . Connection to ground sets a latch to "0," connection to V_{DD} sets a latch to "1." *Figure 1* and *Figure 2* show two suggested methods for strapping resistor connections.

Upon W150 power-up, the first 2 ms of operation are used for input logic selection. During this period, the five I/O pins (2, 8, 9, 29, 30) are three-stated, allowing the output strapping

resistor on the I/O pins to pull the pins and their associated capacitive clock load to either a logic HIGH or LOW state. At the end of the 2-ms period, the established logic "0" or "1" condition of the I/O pin is latched. Next the output buffer is enabled, converting the I/O pins into operating clock outputs. The 2-ms timer starts when V_{DD} reaches 2.0V. The input bits can only be reset by turning V_{DD} off and then back on again.

It should be noted that the strapping resistors have no significant effect on clock output signal integrity. The drive impedance of clock output (< 40 Ω , nominal) is minimally affected by the 10-k Ω strap to ground or V_{DD} . As with the series termination resistor, the output strapping resistor should be placed as close to the I/O pin as possible in order to keep the interconnecting trace short. The trace from the resistor to ground or V_{DD} should be kept less than two inches in length to minimize system noise coupling during input logic sampling.

When the clock outputs are enabled following the 2-ms input period, the corresponding specified output frequency is delivered on the pins, assuming that V_{DD} has stabilized. If V_{DD} has not yet reached full value, output frequency initially may be below target but will increase to target once V_{DD} voltage has stabilized. In either case, a short output clock cycle may be produced from the CPU clock outputs when the outputs are enabled.

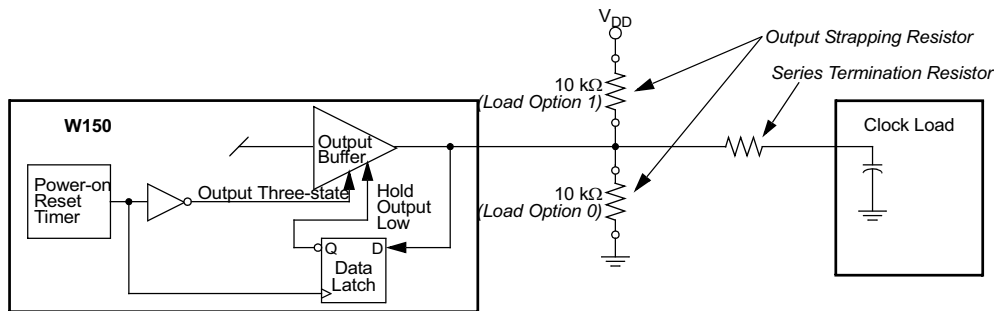


Figure 1. Input Logic Selection Through Resistor Load Option

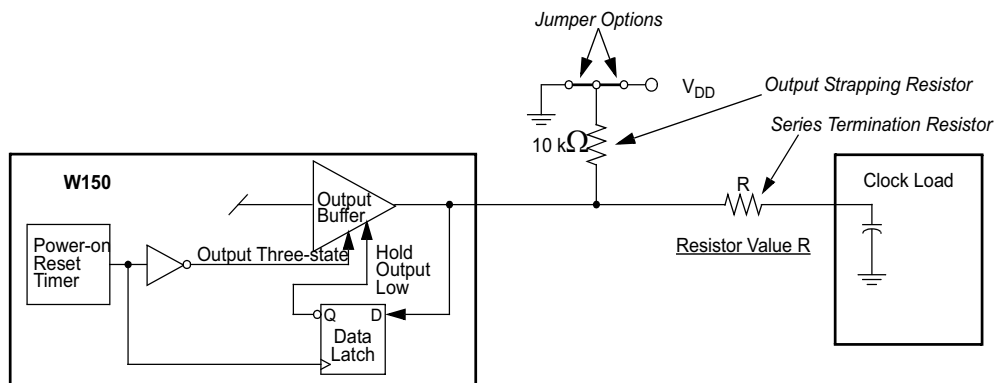


Figure 2. Input Logic Selection Through Jumper Option

Spread Spectrum Generator

The device generates a clock that is frequency modulated in order to increase the bandwidth that it occupies. By increasing the bandwidth of the fundamental and its harmonics, the amplitudes of the radiated electromagnetic emissions are reduced. This effect is depicted in *Figure 3*.

As shown in *Figure 3*, a harmonic of a modulated clock has a much lower amplitude than that of an unmodulated signal. The reduction in amplitude is dependent on the harmonic number and the frequency deviation or spread. The equation for the reduction is

$$dB = 6.5 + 9 \cdot \log_{10}(P) + 9 \cdot \log_{10}(F)$$

Where P is the percentage of deviation and F is the frequency in MHz where the reduction is measured.

The output clock is modulated with a waveform depicted in *Figure 4*. This waveform, as discussed in "Spread Spectrum Clock Generation for the Reduction of Radiated Emissions" by Bush, Fessler, and Hardin produces the maximum reduction in the amplitude of radiated electromagnetic emissions. The deviation selected for this chip is specified in *Table 6*. *Figure 4* details the Cypress spreading pattern. Cypress does offer options with more spread and greater EMI reduction. Contact your local Sales representative for details on these devices.

Spread Spectrum clocking is activated or deactivated by selecting the appropriate values for bits 1–0 in data byte 0 of the SMBus data stream. Refer to *Table 7* for more details.

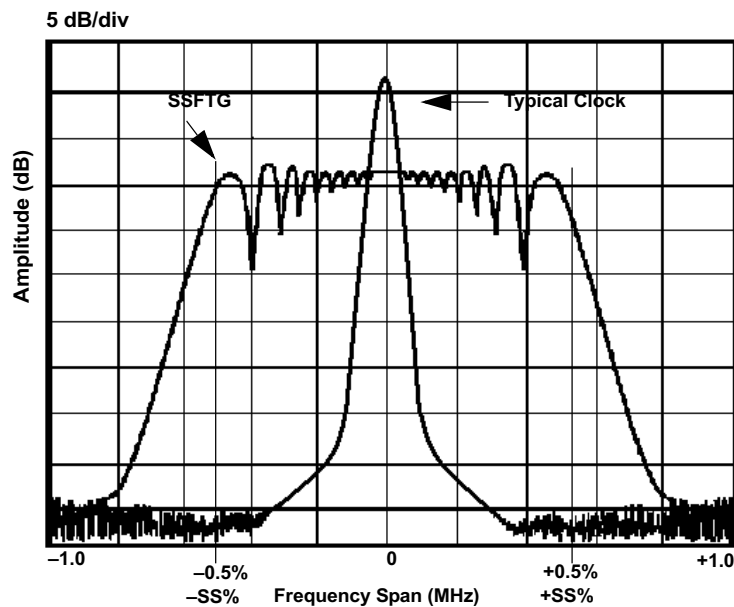


Figure 3. Clock Harmonic with and without SSCG Modulation Frequency Domain Representation

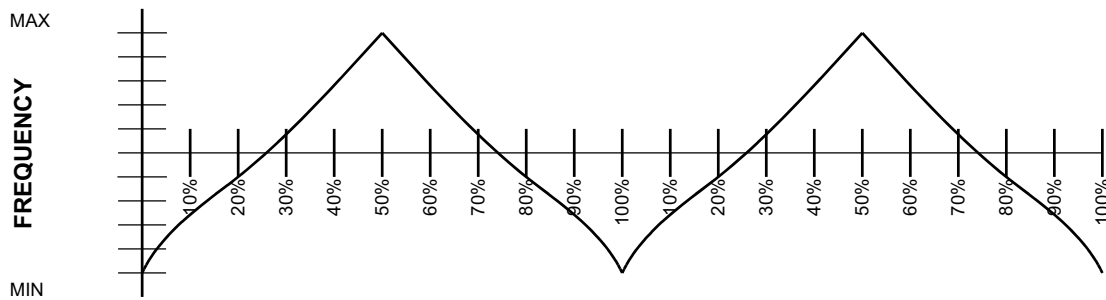


Figure 4. Typical Modulation Profile

Serial Data Interface

The W150 features a two-pin, serial data interface that can be used to configure internal register settings that control particular device functions. Upon power-up, the W150 initializes with default register settings, therefore the use of this serial data interface is optional. The serial interface is write-only (to the clock chip) and is the dedicated function of device pins SDATA and SCLOCK. In motherboard applications, SDATA and SCLOCK are typically driven by two logic

outputs of the chipset. If needed, clock device register changes are normally made upon system initialization. The interface can also be used during system operation for power management functions. *Table 3* summarizes the control functions of the serial data interface.

Operation

Data is written to the W150 in eleven bytes of eight bits each. Bytes are written in the order shown in *Table 4*.

Table 3. Serial Data Interface Control Functions Summary

| Control Function | Description | Common Application |
|-------------------------------|--|--|
| Clock Output Disable | Any individual clock output(s) can be disabled. Disabled outputs are actively held LOW. | Unused outputs are disabled to reduce EMI and system power. Examples are clock outputs to unused PCI slots. |
| CPU Clock Frequency Selection | Provides CPU/PCI frequency selections through software. Frequency is changed in a smooth and controlled fashion. | For alternate microprocessors and power management options. Smooth frequency transition allows CPU frequency change under normal system operation. |
| Spread Spectrum Enabling | Enables or disables spread spectrum clocking. | For EMI reduction. |
| Output Three-state | Puts clock output into a high-impedance state. | Production PCB testing. |
| Test Mode | All clock outputs toggle in relation to X1 input, internal PLL is bypassed. Refer to <i>Table 5</i> . | Production PCB testing. |
| (Reserved) | Reserved function for future device revision or production device testing. | No user application. Register bit must be written as 0. |

Table 4. Byte Writing Sequence

| Byte Sequence | Byte Name | Bit Sequence | Byte Description |
|---------------|---------------|--------------|---|
| 1 | Slave Address | 11010010 | Commands the W150 to accept the bits in Data Bytes 0–7 for internal register configuration. Since other devices may exist on the same common serial data bus, it is necessary to have a specific slave address for each potential receiver. The slave receiver address for the W150 is 11010010. Register setting will not be made if the Slave Address is not correct (or is for an alternate slave receiver). |
| 2 | Command Code | Don't Care | Unused by the W150, therefore bit values are ignored ("Don't Care"). This byte must be included in the data write sequence to maintain proper byte allocation. The Command Code Byte is part of the standard serial communication protocol and may be used when writing to another addressed slave receiver on the serial data bus. |
| 3 | Byte Count | Don't Care | Unused by the W150, therefore bit values are ignored ("Don't Care"). This byte must be included in the data write sequence to maintain proper byte allocation. The Byte Count Byte is part of the standard serial communication protocol and may be used when writing to another addressed slave receiver on the serial data bus. |

Table 4. Byte Writing Sequence (continued)

| Byte Sequence | Byte Name | Bit Sequence | Byte Description |
|---------------|-------------|-------------------------|--|
| 4 | Data Byte 0 | Refer to <i>Table 5</i> | The data bits in Data Bytes 0–5 set internal W150 registers that control device operation. The data bits are only accepted when the Address Byte bit sequence is 11010010, as noted above. For description of bit control functions, refer to <i>Table 5</i> , Data Byte Serial Configuration Map. |
| 5 | Data Byte 1 | | |
| 6 | Data Byte 2 | | |
| 7 | Data Byte 3 | | |
| 8 | Data Byte 4 | | |
| 9 | Data Byte 5 | | |
| 10 | Data Byte 6 | Don't Care | Unused by the W150, therefore bit values are ignored (Don't Care). |
| 11 | Data Byte 7 | | |

Writing Data Bytes

Each bit in Data Bytes 0–7 control a particular device function except for the “reserved” bits which must be written as a logic 0. Bits are written MSB (most significant bit) first, which is bit 7.

Table 5 gives the bit formats for registers located in Data Bytes 0–7.

Table 6 details additional frequency selections that are available through the serial data interface.

Table 7 details the select functions for Byte 0, bits 1 and 0.

Table 5. Data Bytes 0–5 Serial Configuration Map

| Bit(s) | Affected Pin | | Control Function | Bit Control | | Default | | | | | | | | | | | | | | | |
|--------------------|--------------|---|---|---|--|---|---|---|------------------|---|---|------------|---|---|--------------------|---|---|--------------------------|--|--|----|
| | Pin No. | Pin Name | | 0 | 1 | | | | | | | | | | | | | | | | |
| Data Byte 0 | | | | | | | | | | | | | | | | | | | | | |
| 7 | – | – | (Reserved) | – | – | 0 | | | | | | | | | | | | | | | |
| 6 | – | – | SEL_2 | See <i>Table 6</i> | | 0 | | | | | | | | | | | | | | | |
| 5 | – | – | SEL_1 | See <i>Table 6</i> | | 0 | | | | | | | | | | | | | | | |
| 4 | – | – | SEL_0 | See <i>Table 6</i> | | 0 | | | | | | | | | | | | | | | |
| 3 | – | – | Frequency Table Selection | Frequency Controlled by FS (3:0) <i>Table 2</i> | Frequency Controlled by SEL (3:0) <i>Table 6</i> | 0 | | | | | | | | | | | | | | | |
| 2 | – | – | SEL3 | Refer to <i>Table 6</i> | | 0 | | | | | | | | | | | | | | | |
| 1–0 | – | – | <table border="0"> <tr> <td><u>Bit 1</u></td> <td><u>Bit 0</u></td> <td><u>Function (See <i>Table 7</i> for function details)</u></td> </tr> <tr> <td>0</td> <td>0</td> <td>Normal Operation</td> </tr> <tr> <td>0</td> <td>1</td> <td>(Reserved)</td> </tr> <tr> <td>1</td> <td>0</td> <td>Spread Spectrum On</td> </tr> <tr> <td>1</td> <td>1</td> <td>All Outputs Three-stated</td> </tr> </table> | <u>Bit 1</u> | <u>Bit 0</u> | <u>Function (See <i>Table 7</i> for function details)</u> | 0 | 0 | Normal Operation | 0 | 1 | (Reserved) | 1 | 0 | Spread Spectrum On | 1 | 1 | All Outputs Three-stated | | | 00 |
| <u>Bit 1</u> | <u>Bit 0</u> | <u>Function (See <i>Table 7</i> for function details)</u> | | | | | | | | | | | | | | | | | | | |
| 0 | 0 | Normal Operation | | | | | | | | | | | | | | | | | | | |
| 0 | 1 | (Reserved) | | | | | | | | | | | | | | | | | | | |
| 1 | 0 | Spread Spectrum On | | | | | | | | | | | | | | | | | | | |
| 1 | 1 | All Outputs Three-stated | | | | | | | | | | | | | | | | | | | |
| Data Byte 1 | | | | | | | | | | | | | | | | | | | | | |
| 7 | – | – | – | – | – | 0 | | | | | | | | | | | | | | | |
| 6 | – | – | – | – | – | 0 | | | | | | | | | | | | | | | |
| 5 | – | – | – | – | – | 0 | | | | | | | | | | | | | | | |
| 4 | – | – | – | – | – | 0 | | | | | | | | | | | | | | | |
| 3 | 46 | SDRAM_F | Clock Output Disable | Low | Active | 1 | | | | | | | | | | | | | | | |
| 2 | 49 | CPU2 | Clock Output Disable | Low | Active | 1 | | | | | | | | | | | | | | | |
| 1 | 51 | CPU1 | Clock Output Disable | Low | Active | 1 | | | | | | | | | | | | | | | |
| 0 | 52 | CPU_F | Clock Output Disable | Low | Active | 1 | | | | | | | | | | | | | | | |
| Data Byte 2 | | | | | | | | | | | | | | | | | | | | | |
| 7 | – | – | (Reserved) | – | – | 0 | | | | | | | | | | | | | | | |
| 6 | 8 | PCI_F | Clock Output Disable | Low | Active | 1 | | | | | | | | | | | | | | | |
| 5 | 16 | PCI5 | Clock Output Disable | Low | Active | 1 | | | | | | | | | | | | | | | |

Table 5. Data Bytes 0–5 Serial Configuration Map (continued)

| Bit(s) | Affected Pin | | Control Function | Bit Control | | Default |
|--------------------|-------------------|------------|----------------------|-------------|--------|---------|
| | Pin No. | Pin Name | | 0 | 1 | |
| 4 | 14 | PCI4 | Clock Output Disable | Low | Active | 1 |
| 3 | 13 | PCI3 | Clock Output Disable | Low | Active | 1 |
| 2 | 12 | PCI2 | Clock Output Disable | Low | Active | 1 |
| 1 | 11 | PCI1 | Clock Output Disable | Low | Active | 1 |
| 0 | 9 | PCI0 | Clock Output Disable | Low | Active | 1 |
| Data Byte 3 | | | | | | |
| 7 | – | – | (Reserved) | – | – | 0 |
| 6 | – | – | (Reserved) | – | – | 0 |
| 5 | 29 | 48MHz | Clock Output Disable | Low | Active | 1 |
| 4 | 30 | 24MHz | Clock Output Disable | Low | Active | 1 |
| 3 | 33, 32, 25, 24 | SDRAM12:15 | Clock Output Disable | Low | Active | 1 |
| 2 | 22, 21, 19, 18 | SDRAM8:11 | Clock Output Disable | Low | Active | 1 |
| 1 | 39, 38, 36, 35 | SDRAM4:7 | Clock Output Disable | Low | Active | 1 |
| 0 | 44, 43, 41, 40 | SDRAM0:3 | Clock Output Disable | Low | Active | 1 |
| Data Byte 4 | | | | | | |
| 7 | – | – | (Reserved) | – | – | 0 |
| 6 | – | – | (Reserved) | – | – | 0 |
| 5 | – | – | (Reserved) | – | – | 0 |
| 4 | – | – | (Reserved) | – | – | 0 |
| 3 | – | – | (Reserved) | – | – | 0 |
| 2 | – | – | (Reserved) | – | – | 0 |
| 1 | – | – | (Reserved) | – | – | 0 |
| 0 | – | – | (Reserved) | – | – | 0 |
| Data Byte 5 | | | | | | |
| 7 | – | – | (Reserved) | – | – | 0 |
| 6 | – | – | (Reserved) | – | – | 0 |
| 5 | 54 | IOAPIC_F | Disabled | Low | Active | 1 |
| 4 | 55 | IOAPICO | Disabled | Low | Active | 1 |
| 3 | – | – | (Reserved) | – | – | 0 |
| 2 | – | – | (Reserved) | – | – | 0 |
| 1 | 2 | REF1 | Clock Output Disable | Low | Active | 1 |
| 0 | 3 | REF0 | Clock Output Disable | Low | Active | 1 |

Table 6. Frequency Selections through Serial Data Interface Data Bytes

| Input Conditions | | | | Output Frequency | | Spread On |
|------------------------|----------------|----------------|----------------|----------------------------|---------------------|-------------------|
| Data Byte 0, Bit 3 = 1 | | | | CPU, SDRAM Clocks (MHz) | PCI Clocks (MHz) | Spread Percentage |
| Bit 2 SEL_3 | Bit 6 SEL_2 | Bit 5 SEL_1 | Bit 4 SEL_0 | | | |
| 1 | 1 | 1 | 1 | 133.3 | 33.3 (CPU/4) | ± 0.5% Center |
| 1 | 1 | 1 | 0 | 124 | 31 (CPU/4) | ± 0.5% Center |
| 1 | 1 | 0 | 1 | 150 | 37.5 (CPU/4) | ± 0.5% Center |
| 1 | 1 | 0 | 0 | 140 | 35 (CPU/4) | ± 0.5% Center |
| 1 | 0 | 1 | 1 | 105 | 35 (CPU/3) | ± 0.5% Center |
| 1 | 0 | 1 | 0 | 110 | 36.7 (CPU/3) | ± 0.9% Center |
| 1 | 0 | 0 | 1 | 115 | 38.3 (CPU/3) | ± 0.5% Center |
| 1 | 0 | 0 | 0 | 120 | 40 (CPU/3) | ± 0.5% Center |
| 0 | 1 | 1 | 1 | 100 | 33.3 (CPU/3) | ± 0.5% Center |
| 0 | 1 | 1 | 0 | 133.3 | 44.43 (CPU/3) | ± 0.5% Center |
| 0 | 1 | 0 | 1 | 112 | 37.3 (CPU/3) | ± 0.5% Center |
| 0 | 1 | 0 | 0 | 103 | 34.3 (CPU/3) | ± 0.5% Center |
| 0 | 0 | 1 | 1 | 66.8 | 33.4 (CPU/2) | ± 0.5% Center |
| 0 | 0 | 1 | 0 | 83.3 | 41.7 (CPU/2) | ± 0.9% Center |
| 0 | 0 | 0 | 1 | 75 | 37.5 (CPU/2) | ± 0.5% Center |
| 0 | 0 | 0 | 0 | 124 | 41.3 (CPU/3) | ± 0.5% Center |

Table 7. Select Function for Data Byte 0, Bits 0:1

| Function | Input Conditions | | Output Conditions | | | | |
|------------------|------------------|-------|-------------------|---------------|-----------------------|--------|--------|
| | Data Byte 0 | | CPU_F, 1:2 | PCI_F, PCI0:5 | REF0:1, IOAPIC0,_F | 48 MHZ | 24 MHZ |
| | Bit 1 | Bit 0 | | | | | |
| Normal Operation | 0 | 0 | Note 2 | Note 2 | 14.318 MHz | 48 MHz | 24 MHz |
| Test Mode | 0 | 1 | X1/2 | CPU/(2 or 3) | X1 | X1/2 | X1/4 |
| Spread Spectrum | 1 | 0 | Note 2 | Note 2 | 14.318 MHz | 48 MHz | 24 MHz |
| Tristate | 1 | 1 | Hi-Z | Hi-Z | Hi-Z | Hi-Z | Hi-Z |

Note:

 2. CPU and PCI frequency selections are listed in *Table 2* and *Table 6*.

Absolute Maximum Ratings^[3]

Stresses greater than those listed in this table may cause permanent damage to the device. These represent a stress rating only. Operation of the device at these or any other conditions above those specified in the operating sections of this specification is not implied. Maximum conditions for extended periods may affect reliability.

| Parameter | Description | Rating | Unit |
|------------------|--|--------------|------|
| V_{DD}, V_{IN} | Voltage on any pin with respect to GND | -0.5 to +7.0 | V |
| T_{STG} | Storage Temperature | -65 to +150 | °C |
| T_B | Ambient Temperature under Bias | -55 to +125 | °C |
| T_A | Operating Temperature | 0 to +70 | °C |
| ESD_{PROT} | Input ESD Protection | 2 (min) | kV |

DC Electrical Characteristics ($T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$; $V_{DDQ3} = 3.3\text{V} \pm 5\%$; $V_{DDQ2} = 2.5\text{V} \pm 5\%$)

| Parameter | Description | Test Condition | Min. | Typ. | Max. | Unit | |
|-----------------------|-----------------------------------|--|-------------------------|------|----------------|-------|----|
| Supply Current | | | | | | | |
| I_{DD} | 3.3V Supply Current | CPU_F, 1:2= 100 MHz Outputs Loaded ^[4] | | 320 | | mA | |
| I_{DD} | 2.5V Supply Current | CPU_F, 1:2= 100 MHz Outputs Loaded ^[4] | | 40 | | mA | |
| Logic Inputs | | | | | | | |
| V_{IL} | Input Low Voltage | | GND - 0.3 | | 0.8 | V | |
| V_{IH} | Input High Voltage | | 2.0 | | $V_{DD} + 0.3$ | V | |
| I_{IL} | Input Low Current ^[5] | | | | -25 | μA | |
| I_{IH} | Input High Current ^[5] | | | | 10 | μA | |
| I_{IL} | Input Low Current (SEL100/66#) | | | | -5 | μA | |
| I_{IH} | Input High Current (SEL100/66#) | | | | +5 | μA | |
| Clock Outputs | | | | | | | |
| V_{OL} | Output Low Voltage | | $I_{OL} = 1\text{ mA}$ | | | 50 mV | |
| V_{OH} | Output High Voltage | | $I_{OH} = 1\text{ mA}$ | 3.1 | | V | |
| V_{OH} | Output High Voltage | CPU_F, 1:2, IOAPIC | $I_{OH} = -1\text{ mA}$ | 2.2 | | V | |
| I_{OL} | Output Low Current | CPU_F, 1:2 | $V_{OL} = 1.25\text{V}$ | 60 | 73 | 85 | mA |
| | | PCI_F, PCI1:5 | $V_{OL} = 1.5\text{V}$ | 96 | 110 | 130 | mA |
| | | IOAPIC0, IOAPIC_F | $V_{OL} = 1.25\text{V}$ | 72 | 92 | 110 | mA |
| | | REF0:1 | $V_{OL} = 1.5\text{V}$ | 61 | 71 | 80 | mA |
| | | 48-MHz | $V_{OL} = 1.5\text{V}$ | 60 | 70 | 80 | mA |
| | | 24-MHz | $V_{OL} = 1.5\text{V}$ | 60 | 70 | 80 | mA |
| | | SDRAM0:15, _F | $V_{OL} = 1.5\text{V}$ | 95 | 110 | 130 | |
| I_{OH} | Output High Current | CPU_F, 1:2 | $V_{OH} = 1.25\text{V}$ | 43 | 60 | 80 | mA |
| | | PCI_F, PCI1:5 | $V_{OH} = 1.5\text{V}$ | 76 | 96 | 120 | mA |
| | | IOAPIC | $V_{OH} = 1.25\text{V}$ | 60 | 90 | 130 | mA |
| | | REF0:1 | $V_{OH} = 1.5\text{V}$ | 50 | 60 | 72 | mA |
| | | 48-MHz | $V_{OH} = 1.5\text{V}$ | 50 | 60 | 72 | mA |
| | | 24-MHz | $V_{OH} = 1.5\text{V}$ | 50 | 60 | 72 | mA |
| | | SDRAM0:15, _F | $V_{OH} = 1.5\text{V}$ | 75 | 95 | 120 | |

Notes:

- Multiple Supplies: The voltage on any input or I/O pin cannot exceed the power pin during power-up. Power supply sequencing is NOT required.
- All clock outputs loaded with 6" 60Ω traces with 22-pF capacitors.
- W150 logic inputs have internal pull-up devices (not to full CMOS level). Logic input FS3 has an internal pull-down device.

DC Electrical Characteristics ($T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$; $V_{DDQ3} = 3.3\text{V} \pm 5\%$; $V_{DDQ2} = 2.5\text{V} \pm 5\%$) (continued)

| Parameter | Description | Test Condition | Min. | Typ. | Max. | Unit |
|-----------------------------------|--|--------------------------|------|------|------|------|
| Crystal Oscillator | | | | | | |
| V_{TH} | X1 Input threshold Voltage ^[6] | $V_{DDQ3} = 3.3\text{V}$ | | 1.65 | | V |
| C_{LOAD} | Load Capacitance, Imposed on External Crystal ^[7] | | | 14 | | pF |
| $C_{IN,X1}$ | X1 Input Capacitance ^[8] | Pin X2 unconnected | | 28 | | pF |
| Pin Capacitance/Inductance | | | | | | |
| C_{IN} | Input Pin Capacitance | Except X1 and X2 | | | 5 | pF |
| C_{OUT} | Output Pin Capacitance | | | | 6 | pF |
| L_{IN} | Input Pin Inductance | | | | 7 | nH |

AC Electrical Characteristics

$T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$; $V_{DDQ3} = 3.3\text{V} \pm 5\%$; $V_{DDQ2} = 2.5\text{V} \pm 5\%$; $f_{XTL} = 14.31818$ MHz. AC clock parameters are tested and guaranteed over stated operating conditions using the stated lump capacitive load at the clock output; Spread Spectrum clocking is disabled.

CPU Clock Outputs, CPU_F, 1:2 (Lump Capacitance Test Load = 20 pF)

| Parameter | Description | Test Condition/Comments | CPU = 66.8 MHz | | | CPU = 100 MHz | | | Unit |
|-----------|--|---|----------------|------|------|---------------|------|------|----------|
| | | | Min. | Typ. | Max. | Min. | Typ. | Max. | |
| t_P | Period | Measured on rising edge at 1.25 | 15 | | 15.5 | 10 | | 10.5 | ns |
| t_H | High Time | Duration of clock cycle above 2.0V | 5.2 | | | 3.0 | | | ns |
| t_L | Low Time | Duration of clock cycle below 0.4V | 5.0 | | | 2.8 | | | ns |
| t_R | Output Rise Edge Rate | Measured from 0.4V to 2.0V | 1 | | 4 | 1 | | 4 | V/ns |
| t_F | Output Fall Edge Rate | Measured from 2.0V to 0.4V | 1 | | 4 | 1 | | 4 | V/ns |
| t_D | Duty Cycle | Measured on rising and falling edge at 1.25V | 45 | | 55 | 45 | | 55 | % |
| t_{JC} | Jitter, Cycle-to-Cycle | Measured on rising edge at 1.25V. Maximum difference of cycle time between two adjacent cycles. | | | 250 | | | 250 | ps |
| t_{SK} | Output Skew | Measured on rising edge at 1.25V | | | 175 | | | 175 | ps |
| f_{ST} | Frequency Stabilization from Power-up (cold start) | Assumes full supply voltage reached within 1 ms from power-up. Short cycles exist prior to frequency stabilization. | | | 3 | | | 3 | ms |
| Z_o | AC Output Impedance | Average value during switching transition. Used for determining series termination value. | | 20 | | | 20 | | Ω |

PCI Clock Outputs, PCI_F and PCI0:5 (Lump Capacitance Test Load = 30 pF)

| Parameter | Description | Test Condition/Comments | CPU = 66.6/100 MHz | | | Unit |
|-----------|-----------------------|------------------------------------|--------------------|------|------|------|
| | | | Min. | Typ. | Max. | |
| t_P | Period | Measured on rising edge at 1.5V | 30 | | | ns |
| t_H | High Time | Duration of clock cycle above 2.4V | 12.0 | | | ns |
| t_L | Low Time | Duration of clock cycle below 0.4V | 12.0 | | | ns |
| t_R | Output Rise Edge Rate | Measured from 0.4V to 2.4V | 1 | | 4 | V/ns |

Notes:

6. X1 input threshold voltage (typical) is $V_{DDQ3}/2$.
7. The W150 contains an internal crystal load capacitor between pin X1 and ground and another between pin X2 and ground. Total load placed on crystal is 14 pF; this includes typical stray capacitance of short PCB traces to crystal.
8. X1 input capacitance is applicable when driving X1 with an external clock source (X2 is left unconnected).

| | | | | | | |
|-------|-----------------------|----------------------------|---|--|---|------|
| t_F | Output Fall Edge Rate | Measured from 2.4V to 0.4V | 1 | | 4 | V/ns |
|-------|-----------------------|----------------------------|---|--|---|------|

PCI Clock Outputs, PCI_F and PCI0:5 (Lump Capacitance Test Load = 30 pF) (continued)

| Parameter | Description | Test Condition/Comments | CPU = 66.6/100 MHz | | | Unit |
|-----------------|--|---|--------------------|------|------|------|
| | | | Min. | Typ. | Max. | |
| t _D | Duty Cycle | Measured on rising and falling edge at 1.5V | 45 | | 55 | % |
| t _{JC} | Jitter, Cycle-to-Cycle | Measured on rising edge at 1.5V. Maximum difference of cycle time between two adjacent cycles. | | | 250 | ps |
| t _{SK} | Output Skew | Measured on rising edge at 1.5V | | | 500 | ps |
| t _O | CPU to PCI Clock Skew | Covers all CPU/PCI outputs. Measured on rising edge at 1.5V. CPU leads PCI output. | 1.5 | | 4 | ns |
| f _{ST} | Frequency Stabilization from Power-up (cold start) | Assumes full supply voltage reached within 1 ms from power-up. Short cycles exist prior to frequency stabilization. | | | 3 | ms |
| Z _O | AC Output Impedance | Average value during switching transition. Used for determining series termination value. | | 15 | | Ω |

IOAPIC0 and IOAPIC_F Clock Outputs (Lump Capacitance Test Load = 20 pF)

| Parameter | Description | Test Condition/Comments | CPU = 66.6/100 MHz | | | Unit |
|-----------------|--|---|--------------------|------|------|------|
| | | | Min. | Typ. | Max. | |
| f | Frequency, Actual | Frequency generated by crystal oscillator | 14.31818 | | | MHz |
| t _R | Output Rise Edge Rate | Measured from 0.4V to 2.0V | 1 | | 4 | V/ns |
| t _F | Output Fall Edge Rate | Measured from 2.0V to 0.4V | 1 | | 4 | V/ns |
| t _D | Duty Cycle | Measured on rising and falling edge at 1.25V | 45 | | 55 | % |
| f _{ST} | Frequency Stabilization from Power-up (cold start) | Assumes full supply voltage reached within 1 ms from power-up. Short cycles exist prior to frequency stabilization. | | | 1.5 | ms |
| Z _O | AC Output Impedance | Average value during switching transition. Used for determining series termination value. | | 15 | | Ω |

REF0:1 Clock Outputs (Lump Capacitance Test Load = 20 pF)

| Parameter | Description | Test Condition/Comments | CPU = 66.6/100 MHz | | | Unit |
|-----------------|--|---|--------------------|------|------|------|
| | | | Min. | Typ. | Max. | |
| f | Frequency, Actual | Frequency generated by crystal oscillator | 14.318 | | | MHz |
| t _R | Output Rise Edge Rate | Measured from 0.4V to 2.4V | 0.5 | | 2 | V/ns |
| t _F | Output Fall Edge Rate | Measured from 2.4V to 0.4V | 0.5 | | 2 | V/ns |
| t _D | Duty Cycle | Measured on rising and falling edge at 1.5V | 45 | | 55 | % |
| f _{ST} | Frequency Stabilization from Power-up (cold start) | Assumes full supply voltage reached within 1 ms from power-up. Short cycles exist prior to frequency stabilization. | | | 3 | ms |
| Z _O | AC Output Impedance | Average value during switching transition. Used for determining series termination value. | | 25 | | Ω |

SDRAM 0:15, _F Clock Outputs (Lump Capacitance Test Load = 30 pF)

| Parameter | Description | Test Condition/Comments | CPU = 66.8 MHz | | | CPU = 100 MHz | | | Unit |
|----------------|-----------------------|------------------------------------|----------------|------|------|---------------|------|------|------|
| | | | Min. | Typ. | Max. | Min. | Typ. | Max. | |
| t _P | Period | Measured on rising edge at 1.5V | 15 | | 15.5 | 10 | | 10.5 | ns |
| t _H | High Time | Duration of clock cycle above 2.4V | 5.2 | | | 3.0 | | | ns |
| t _L | Low Time | Duration of clock cycle below 0.4V | 5.0 | | | 2.0 | | | ns |
| t _R | Output Rise Edge Rate | Measured from 0.4V to 2.4V | 1 | | 4 | 1 | | 4 | V/ns |
| t _F | Output Fall Edge Rate | Measured from 2.4V to 0.4V | 1 | | 4 | 1 | | 4 | V/ns |

SDRAM 0:15, _F Clock Outputs (Lump Capacitance Test Load = 30 pF) (continued)

| Parameter | Description | Test Condition/Comments | CPU = 66.8 MHz | | | CPU = 100 MHz | | | Unit |
|-----------------|---------------------|---|----------------|------|------|---------------|------|------|------|
| | | | Min. | Typ. | Max. | Min. | Typ. | Max. | |
| t _D | Duty Cycle | Measured on rising and falling edge at 1.5V | 45 | | 55 | 45 | | 55 | % |
| t _{SK} | Output Skew | Measured on rising and falling edge at 1.5V | | | 250 | | | 250 | ps |
| t _{PD} | Propagation Delay | Measured from SDRAMIN | | 3.7 | | | 3.7 | | ns |
| Z _o | AC Output Impedance | Average value during switching transition. Used for determining series termination value. | | 15 | | | 15 | | Ω |

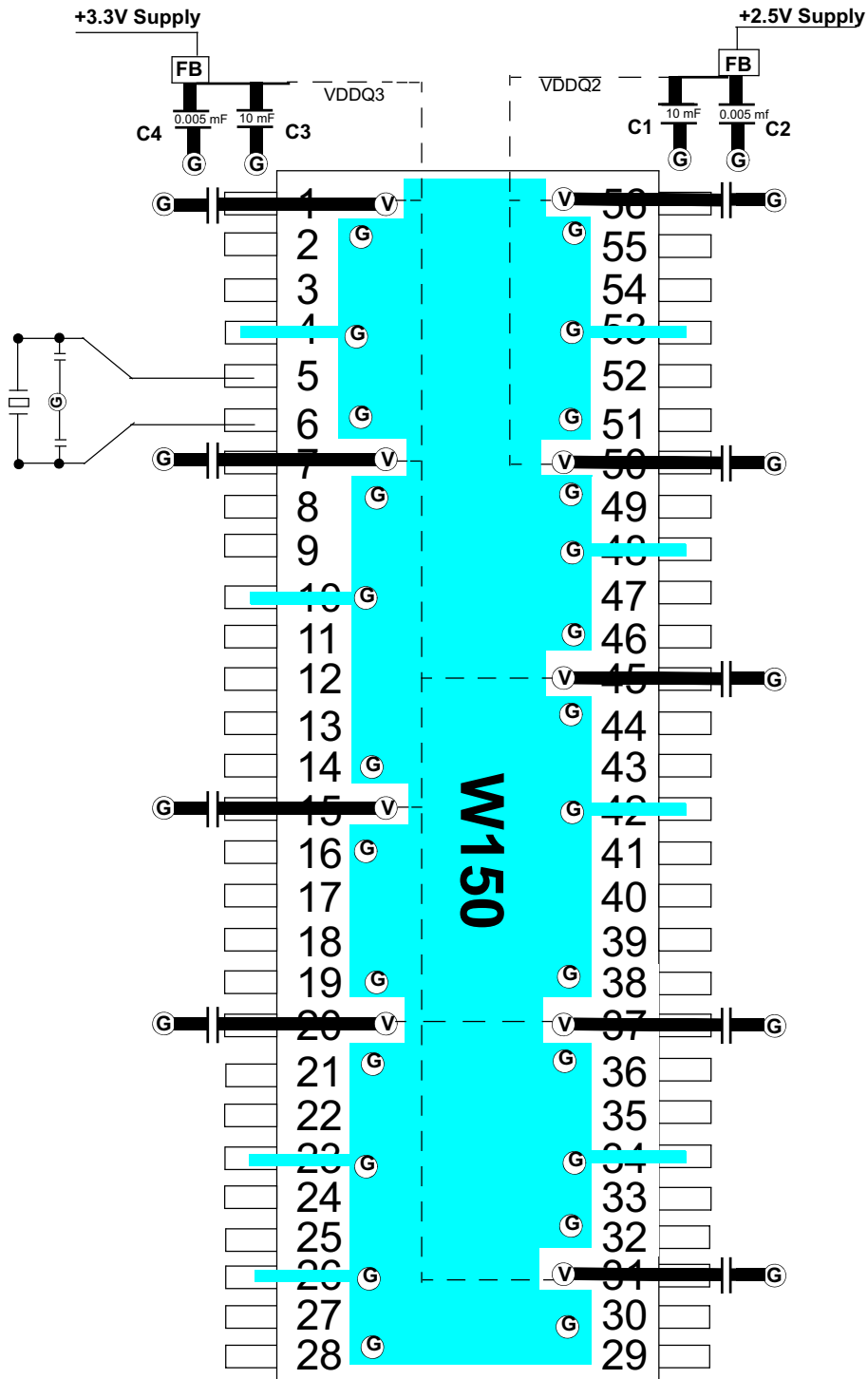
48-MHz Clock Output (Lump Capacitance Test Load = 20 pF)

| Parameter | Description | Test Condition/Comments | CPU = 66.8/100 MHz | | | Unit |
|-----------------|--|---|--------------------|------|------|------|
| | | | Min. | Typ. | Max. | |
| f | Frequency, Actual | Determined by PLL divider ratio (see m/n below) | 48.008 | | | MHz |
| f _D | Deviation from 48 MHz | (48.008 – 48)/48 | +167 | | | ppm |
| m/n | PLL Ratio | (14.31818 MHz x 57/17 = 48.008 MHz) | 57/17 | | | |
| t _R | Output Rise Edge Rate | Measured from 0.4V to 2.4V | 0.5 | | 2 | V/ns |
| t _F | Output Fall Edge Rate | Measured from 2.4V to 0.4V | 0.5 | | 2 | V/ns |
| t _D | Duty Cycle | Measured on rising and falling edge at 1.5V | 45 | | 55 | % |
| f _{ST} | Frequency Stabilization from Power-up (cold start) | Assumes full supply voltage reached within 1 ms from power-up. Short cycles exist prior to frequency stabilization. | | | 3 | ms |
| Z _o | AC Output Impedance | Average value during switching transition. Used for determining series termination value. | | 25 | | Ω |

24-MHz Clock Output (Lump Capacitance Test Load = 20 pF)

| Parameter | Description | Test Condition/Comments | CPU = 66.8/100 MHz | | | Unit |
|-----------------|--|---|--------------------|------|------|------|
| | | | Min. | Typ. | Max. | |
| f | Frequency, Actual | Determined by PLL divider ratio (see m/n below) | 24.004 | | | MHz |
| f _D | Deviation from 24 MHz | (24.004 – 24)/24 | +167 | | | ppm |
| m/n | PLL Ratio | (14.31818 MHz x 57/34 = 24.004 MHz) | 57/34 | | | |
| t _R | Output Rise Edge Rate | Measured from 0.4V to 2.4V | 0.5 | | 2 | V/ns |
| t _F | Output Fall Edge Rate | Measured from 2.4V to 0.4V | 0.5 | | 2 | V/ns |
| t _D | Duty Cycle | Measured on rising and falling edge at 1.5V | 45 | | 55 | % |
| f _{ST} | Frequency Stabilization from Power-up (cold start) | Assumes full supply voltage reached within 1 ms from power-up. Short cycles exist prior to frequency stabilization. | | | 3 | ms |
| Z _o | AC Output Impedance | Average value during switching transition. Used for determining series termination value. | | 25 | | Ω |

Layout Example



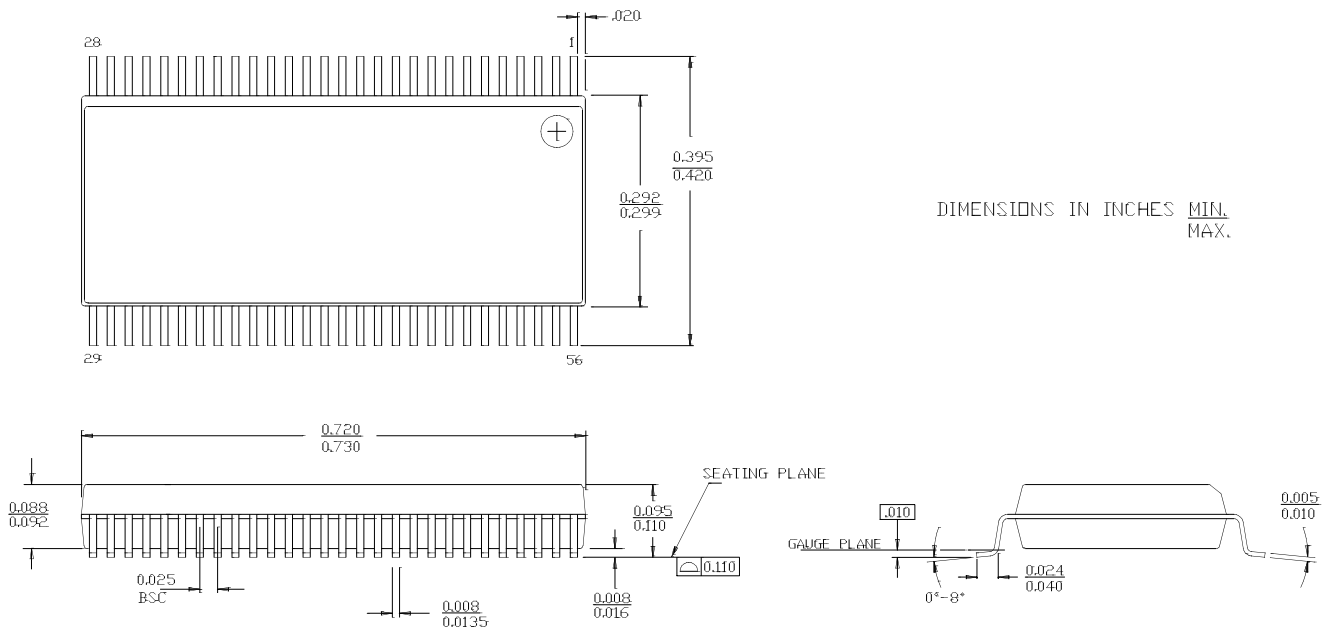
FB = Dale ILB1206 - 300 (300Ω @ 100 MHz)
 Cermaic Caps C1 & C3 = 10 – 22 μF C2 & C4 = 0.005 μF

ⓐ = VIA to GND plane layer Ⓥ =VIA to respective supply plane layer

Note: Each supply plane or strip should have a ferrite bead and capacitors
 All bypass caps = 0.1 μF ceramic

Ordering Information

| Ordering Code | Package Type | Industrial Product Flow |
|---------------|-----------------------------|-------------------------|
| W150H | 56-pin SSOP | Commercial, 0 to 70°C |
| W150HT | 56-pin SSOP – Tape and Reel | Commercial, 0 to 70°C |

Package Drawing and Dimensions
56-Lead Shrunken Small Outline Package O56


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