VISION VV6850 & VV5850 Monolithic Sensors

High resolution CMOS Image Sensor with support for external FPN cancellation and serial interface control, available in colour (6850) and monochrome (5850) versions.

PRODUCT DATASHEET Revision 1.0

DISTINCTIVE CHARACTERISTICS

- High resolution (800K) CMOS sensor designed for use in Digital Colour Stills Cameras and Machine Vision applications
- Versatile operating modes, including Live Video/'Cine' mode for viewfinder applications, and exposure monitoring modes
- Digital control of pixel reading for flexibility, including external ADC interface
- Control/configuration via serial interface
- External frame/line buffering schemes offer effective pixel offset cancellation and low noise operation
- Bayer pattern R,G,B colourisation (other patterns/colours can be accommodated)
- Monochrome version available - VV5850 - functionally identical to the VV6850, but with higher sensitivity
- Low power operation (125mW Typical)
- Industry standard 84 pin LCC package

GENERAL DESCRIPTION

The VV6850 and VV5850 are highly integrated CMOS camera devices. The devices both incorporate a 1016 x 804 pixel array image sensor configured to produce line by line pixel output for external digitisation and storage.

The VV6850 is colourised in a Red, Green, Blue Bayer pattern, whereas the VV5850 is uncolourised. Both are suitable for still image capture applications, and applications requiring digitisation of the pixel image.

All clocking and sequencing control signals are user-defined, giving maximum flexibility of use. A two way serial interface and internal Control Register provide further control and monitoring of camera functions, giving many image capture operating modes.

Exposure control can be achieved with or without an electromechanical shutter, and (external) frame/line buffering and processing enables effective Fixed Pattern Noise cancellation.

BLOCK DIAGRAM

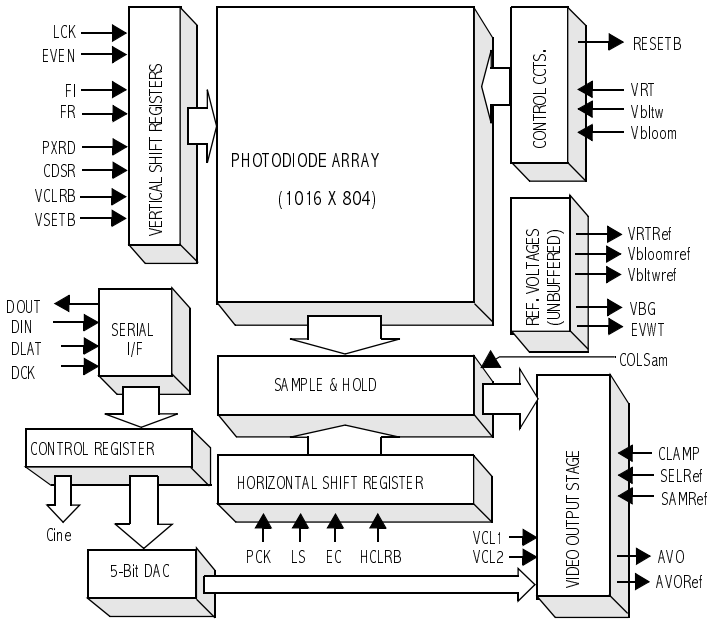
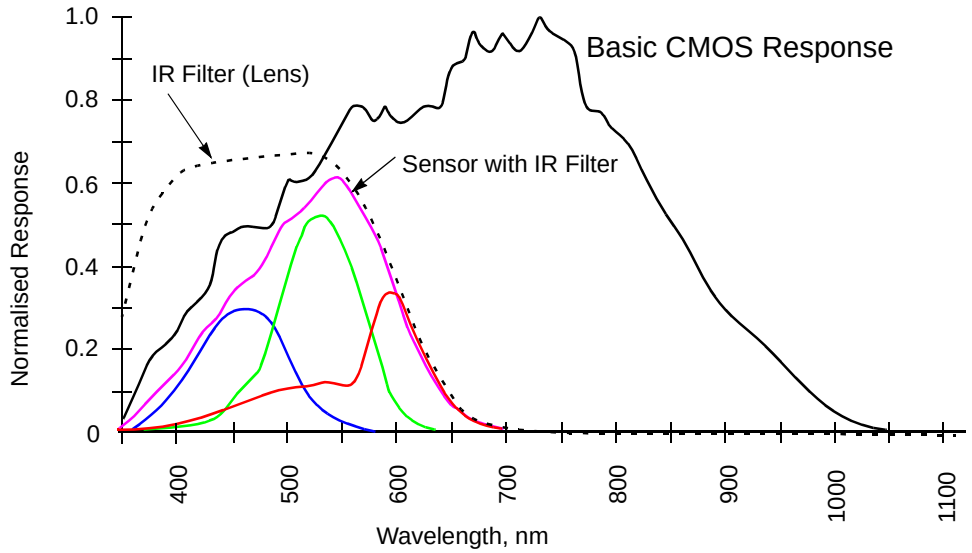
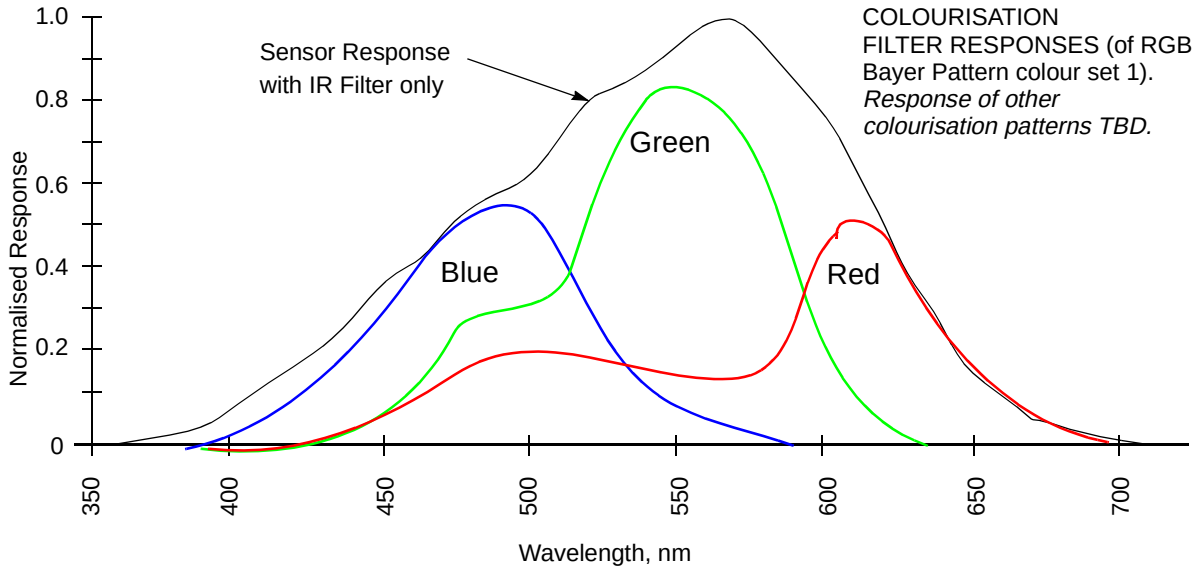


Image Format	800 x 992 pixels
Pixel Size	10.8µm x 10.8µm
Array Size	8.640mm x 10.951mm
Sensitivity (colour)	50mV/lux @ 50ms exp.
S/N	Typically 66dB (with FPN cancellation)
Max. pixel rate	10Mpix/s (5Mpix/s for 0.1% settling)
Power Supply	5v ±5%
Power	< 150 mW
Temperature	0^{o}C - 40^{o}C

Spectral Response





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MAIN FEATURES

The VV6850 sensor has been developed specifically for use in image processing applications requiring pixel by pixel access. Flexible control options allow many operating modes, but the VV6850 is ideally suited to Digital Stills Cameras with electromechanical shutter exposure control and a frame store memory available for pixel offset cancellation.

Note: The VV5850 monochrome sensor is identical in operation to the VV6850, but with higher sensitivity and simpler image processing, due to the absence of colour filters.

Pixel Array

The pixel array is colourised in a four pixel, Red, Green, Blue 'Bayer' arrangement. This provides high colour fidelity images with low colour aliasing. (Other colourisation schemes can be produced to suit specific application needs.) The pixel array includes a number of reference lines, and a useable image area of 992 x 800 'valid video' pixels.

Pixel access is by row and column shift registers. Each row of pixels, or line, is read at the same instant, and stored in a sample-and-hold stage. The columns are then read out alternately, and multiplexed through four output channels to the AVO output stage. The image can then be unshuffled and reconstructed in external buffering and processing circuits.

This scheme provides AVO settling to better than 0.1% at a sampling rate of 5 Msps. (Higher sampling rates are possible, with reduced settling accuracy.

Video Output

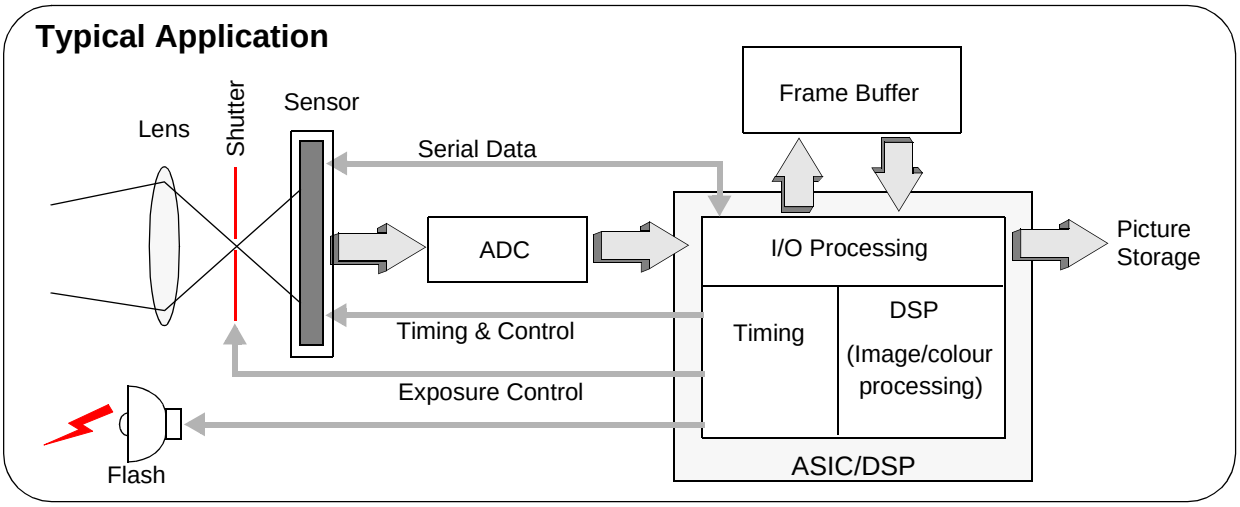
The multiplexed column outputs are buffered to the Analogue Video Output (AVO) pin, as 'inverted' video, that is Black is higher than White. An AVORef output is also generated, from the internal black reference level, to provide a pseudo differential output pair.

A DC component is added to the AVO and AVORef signals at the AC coupled output stages by CLAMPing these to VCL1 and VCL2, one of which can be set by an internal DAC. This allows the AVO level to be matched to the input range of an external ADC.

Serial Interface

The serial interface allows an external controller to set certain parameters and to determine the VV6850's current state. This is done through the Control Register, which is loaded from DIN and examined at DOUT.

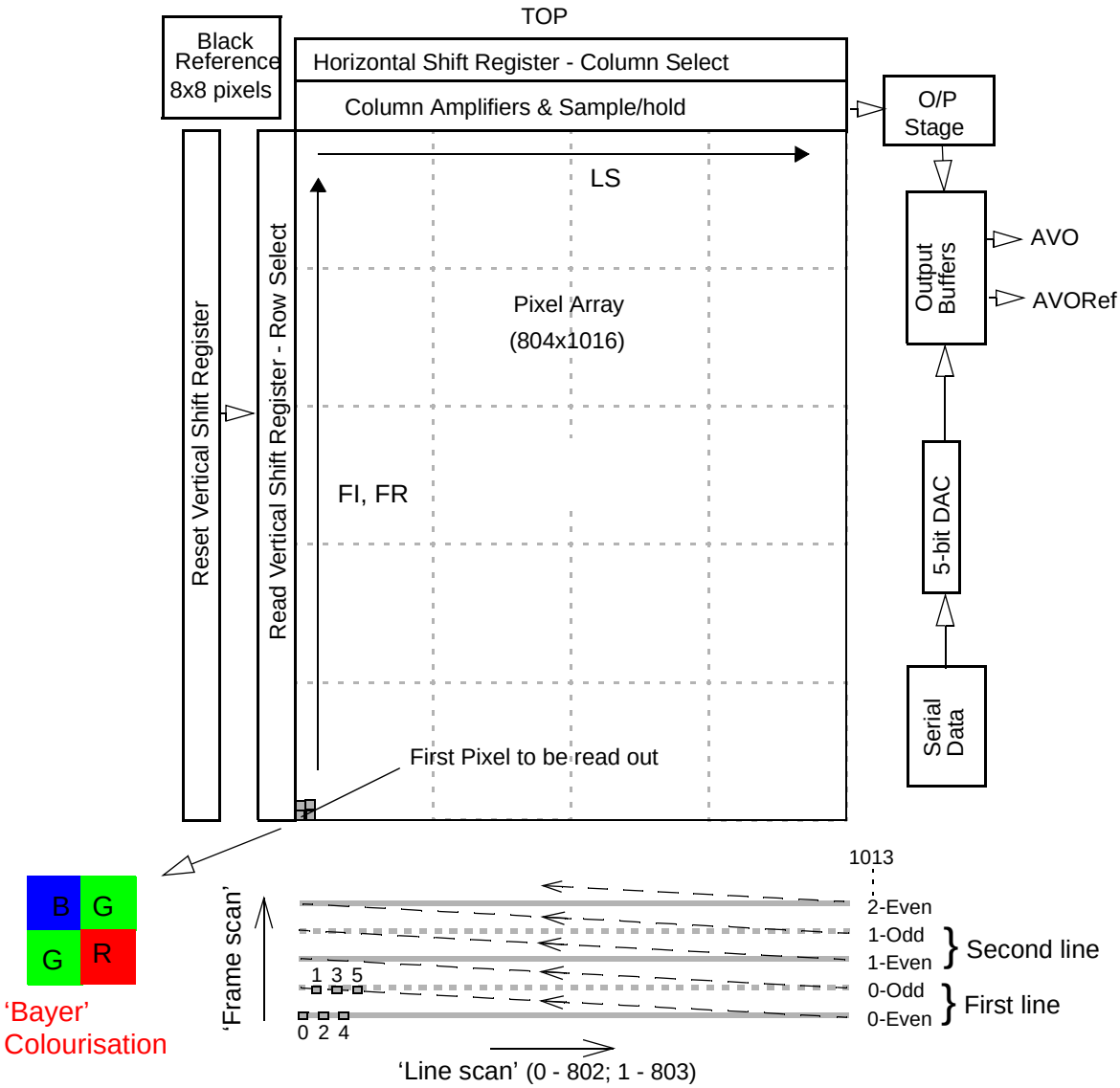
The VV6850 receives serial data as one 22-bit data word, the 20 msb of which are clocked into a shift register. The shift register contents can then be latched into the Control Register.



SENSOR ARCHITECTURE

The VV6850 image sensor comprises an array of 1016 (vertical, ‘lines’) by 804 (horizontal) active photodiode cells feeding into a row of column source followers at the top of the pixel array. These columns are then in turn multiplexed on to four output channels, and finally onto the AVO output. Exposure, that is pixel integration time, is controlled by a ‘Reset Vertical’ shift register with pixel readout controlled by the ‘Read Vertical’ and ‘Horizontal’ shift registers.

The first (‘bottom’) line of the array is used internally, and is not read out. The next 6 lines are black reference lines. Then there are 8 colour characterisation lines, 992 valid video lines and 8 more colour characterisation lines. At the top of the pixel array there is one more extra line which is not read out. The outer two columns on the left and right sides of the pixel array are also internal references, and not read out. Thus the usable image area of the 1016 x 804 array is 992 x 800 pixels.

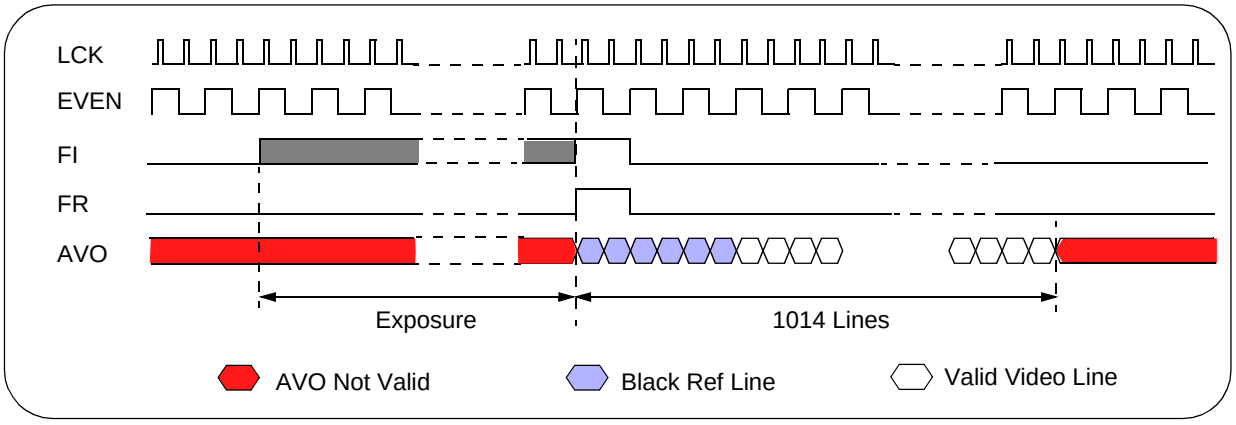


Reset and Read Vertical Shift Registers

The resetting and reading of pixels is performed on a line by line basis, that is a row of column amplifiers reads a whole line of pixel voltages in parallel. The reset/integrate/read cycle for a line of pixels is controlled by the Reset Vertical and Read Vertical shift registers (VSRs).

The length of the 'Frame Integrate' pulse, FI, propagating along the Reset Vertical shift register sets the pixel integration time. FI going high at a point along the VSR releases that line of pixels from RESET, starting the integration period. The two-line 'Frame Read' pulse, FR, which comes at the end of the integrate period, starts the field readout, which proceeds from 'bottom' to 'top'. As FR propagates along the Read Vertical shift register, it controls which line is to be read. For exposure control by means of a shutter mechanism, FI should be held high throughout the frame integrate/read cycle.

The Vertical Shift Registers are clocked by the Line Clock pulse, LCK. Within a frame, first an even line, then an odd line is read. This is controlled by the EVEN clock, which must be half the LCK frequency and change two PCKs before LS (Line Start) rises. A pair of lines may be 'skipped over' (for example as in 'Cine' mode—see: **HORIZONTAL SHIFT REGISTER**), by inserting two LCK pulses and one EVEN pulse between line readout sequences. .



Note: If FR does not rise with the rising edge of EVEN, that is if EVEN is high during the second line period of the FR pulse, the AVO-valid line readout sequence is offset by one line.

Further control of the VSRs is effected by: VCLRB (Clear Reset and Read); VSETB (preset Reset to ones); CDSR (reset row, but do not advance VSRs). The PXRD input to the Read VSR enables a line of pixels to be read out. (See: **OPERATING MODES** for more details.)

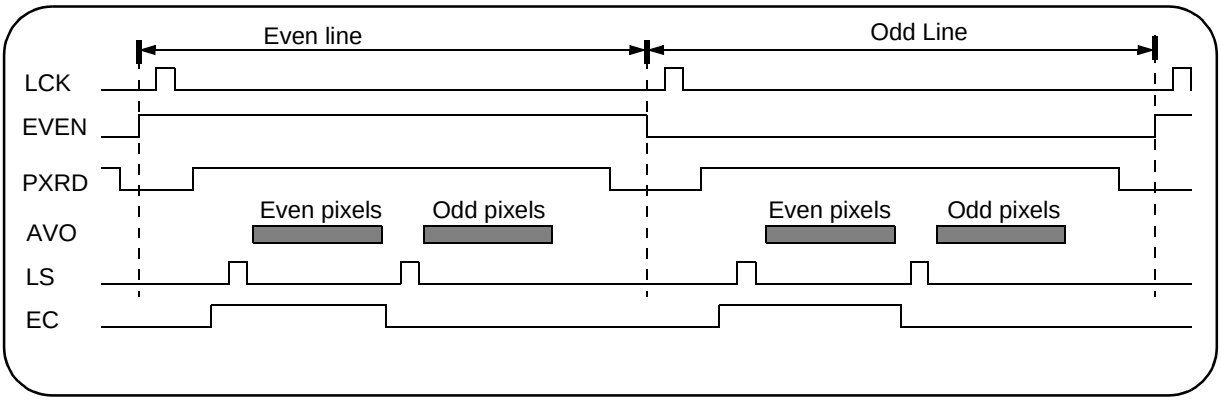
The first six lines in the array are black reference lines. The reset/integrate cycle for these lines is controlled by a third shift register, defined by bits CR[4] and CR[3] in the Control Register (see: **CONTROL REGISTER/SERIAL DATA INTERFACE**). This shift register can either hold the black reference lines in permanent reset, allow minimum exposure or have the same integration time (exposure) as the rest of the array.

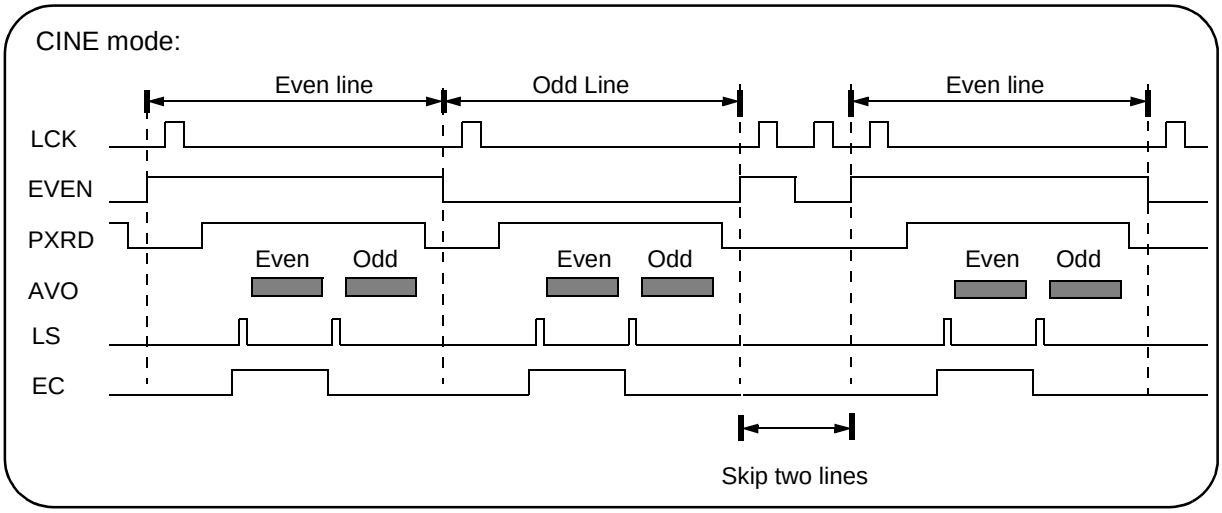
The readout sequence, initiated by FR going high, is therefore: six black lines followed by eight colour characterisation lines, 992 valid video lines and another eight colour characterisation lines. For Cine this becomes: four black lines, four colour characterisation, 496 valid video lines and four colour characterisation lines

Horizontal Shift Register

The Horizontal Shift Register is clocked by the Pixel Clock, PCK. Columns are read out, from left to right, by the Line Start pulse, LS, propagating along the Horizontal Shift Register. The LS pulse must be four PCK periods long, with the first valid pixel being sampled after the falling edge (see **DETAILED TIMING** for exact relationship). To avoid bandwidth limitations within the output stage causing cross talk problems between the colours in a colour pixelated sensor, the horizontal shift register either reads out the odd or the even columns, under control of the EC signal.

In order to read valid pixel data, the Pixel Read input to the Read VSR, PXRD, must be high. (To 'skip' lines, for example as in Cine mode, PXRD must be held low during the two extra LCK periods.) When reading out either the even columns (EC=1) or the odd columns (EC=0) it is the central 400 pixels of the 402 pixels read out that are valid. In Cine mode (Selected with bit CR[3] in the Control Register), every second pixel within a row is read out; of the 202 pixels read out for either EC=1 or EC=0, the central 200 pixels are valid.

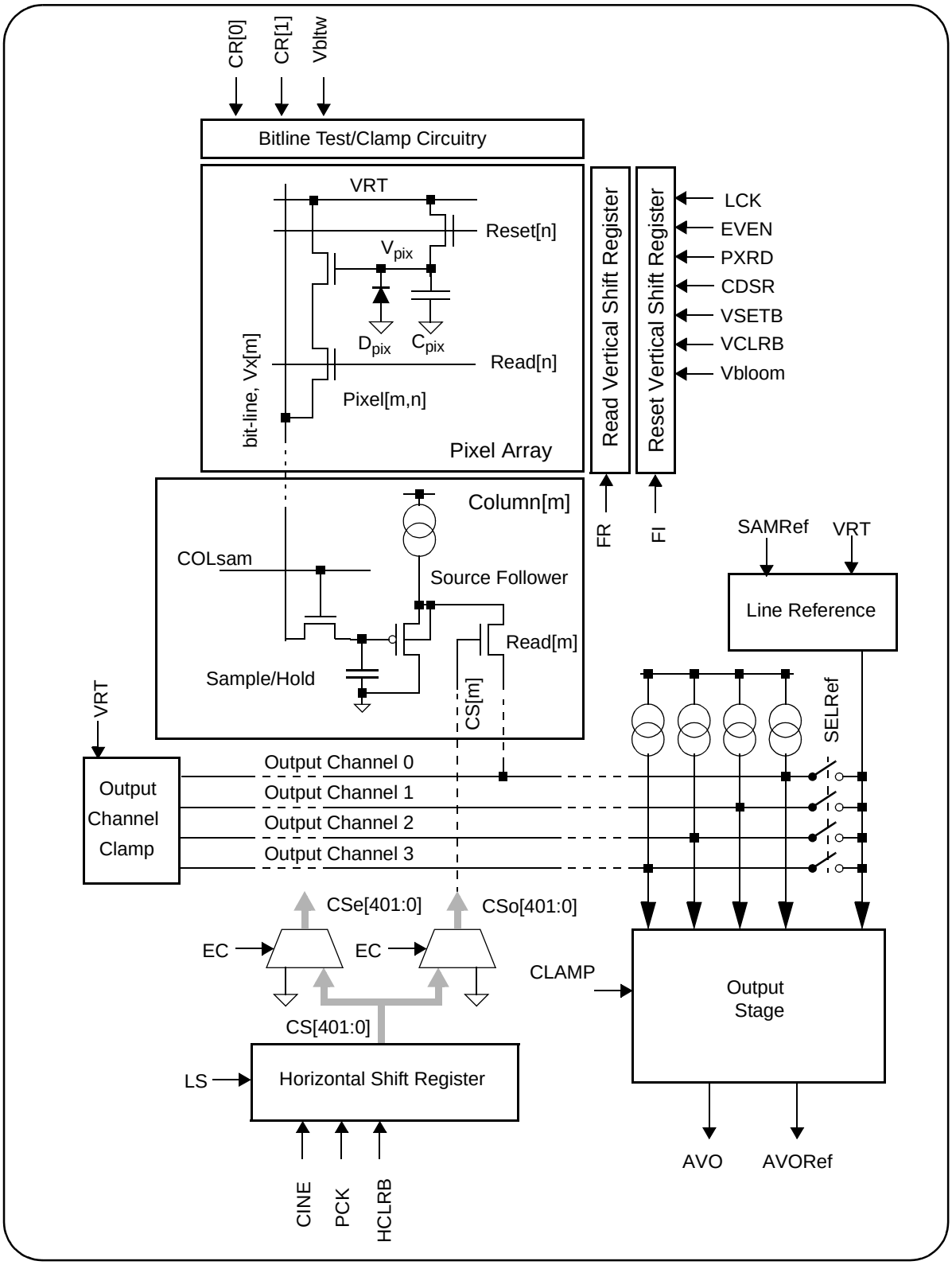




The HCLRB input (active low) clears the HSR to all zeros. HCLRB can also be used, for example, to prematurely end a line scan, perhaps when only part of the image is required.

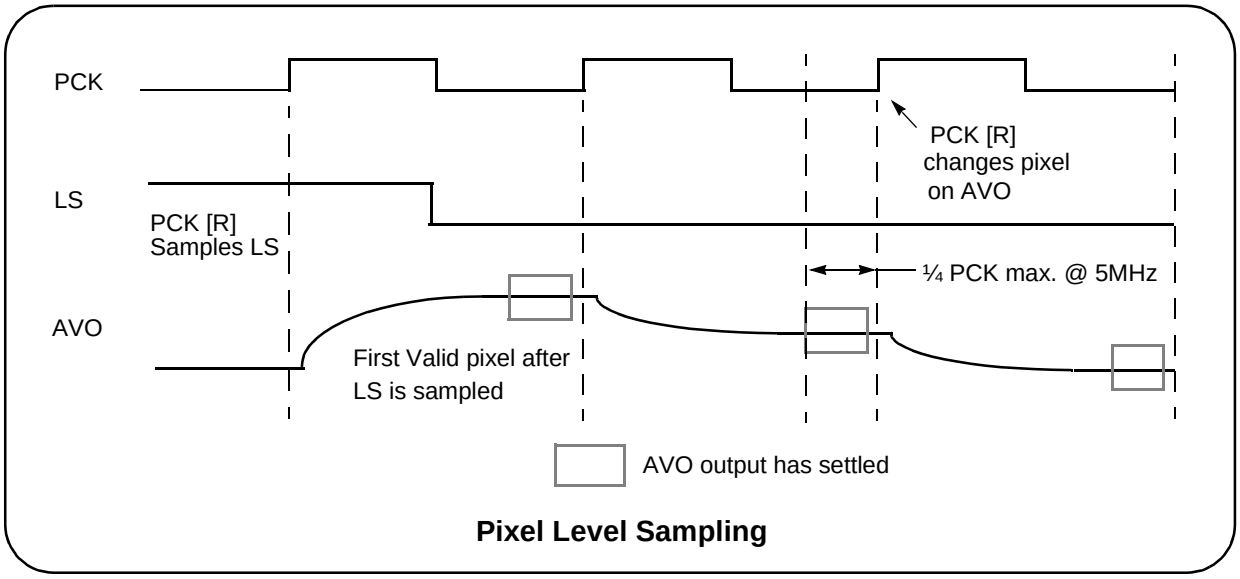
Note: The power-on reset signal, RSTB, should be used to drive HCLRB (and VCLRB for the Vertical Shift Registers) at power up.

Pixel Read Schematic



VIDEO OUTPUT

The four-PCK long LS pulse initiates output of a line of video, with the first valid pixel being sampled after LS falls, and subsequent pixels appearing at AVO as LS propagates along the Horizontal Shift Register. The AVO output for each pixel should then be sampled as close to the end of the PCK cycle as possible to allow maximum settling time.



Pixel Level Sampling

The Video Output Chain

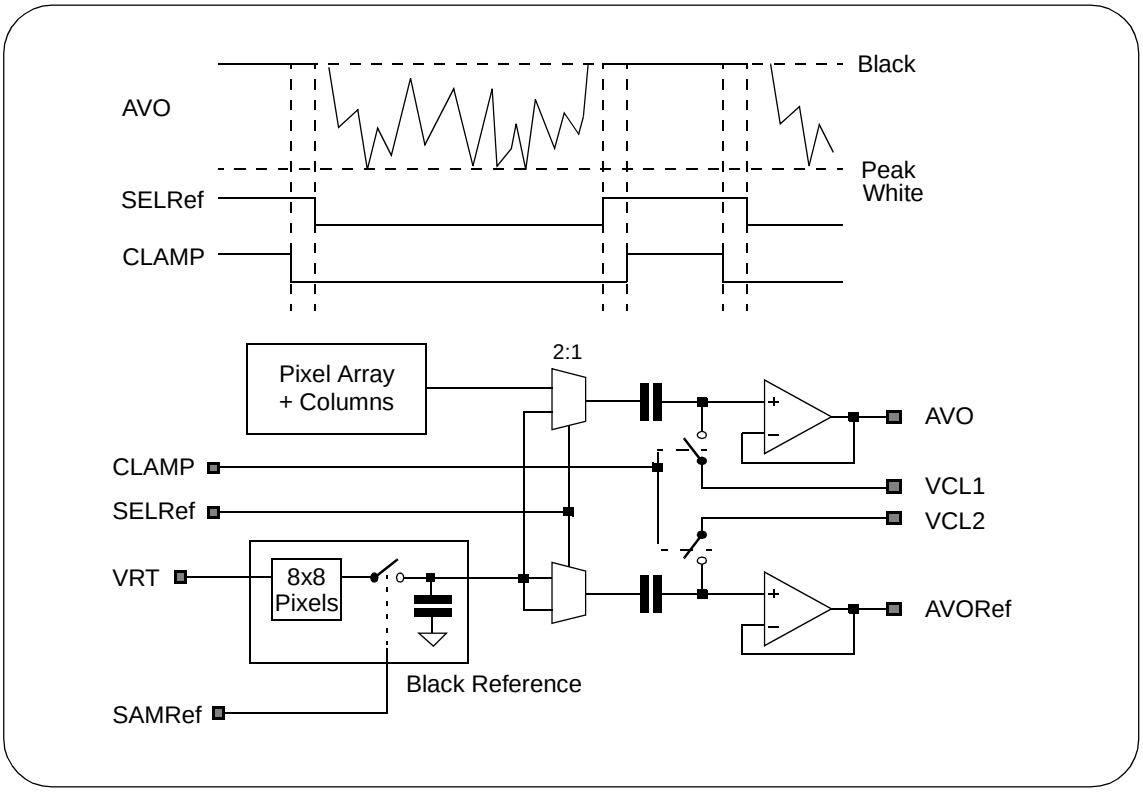
At the top of each column of the array is a sample and hold stage (controlled by COLsam), which drives the output stage. The purpose of the sample & hold is to ensure that all the pixels in a line have the same exposure, as the outputs of a row of pixels are sampled at the same instant. If COLsam is not used then each pixel will carry on integrating until it is read out. Therefore, since all pixels within a line are released from reset at the same time, each pixel will have a different integration time, and hence exposure value.

The columns are read out via four output channels. Each channel is multiplexed onto the AVO pin via an AC coupling stage to restore the DC content. The AVORef pin provides a pseudo-differential output, obtained from an internal black reference. (The pseudo-differential output stage cancels out leakage across the coupling capacitors since both output channels experience the same rate of decay.)

Note: The video at AVO is ‘inverted’, that is Black is higher than White.

AVO Reference

The DC content of the output stage is set by using the SELRef signal to simultaneously put the internal reference on the AVO and AVORef output channels, and then the CLAMP signal to charge the amplifier side of the coupling stages to VCL1 and VCL2 respectively. The integrated 5-bit DAC, controlled by Control Register bits CR[15..11], can be used to adjust one or other of these clamping voltages. The CLAMP signal must fall before SELRef falls. The AC Coupling Capacitors must be refreshed at least once every still image capture sequence, or every frame of a live video.



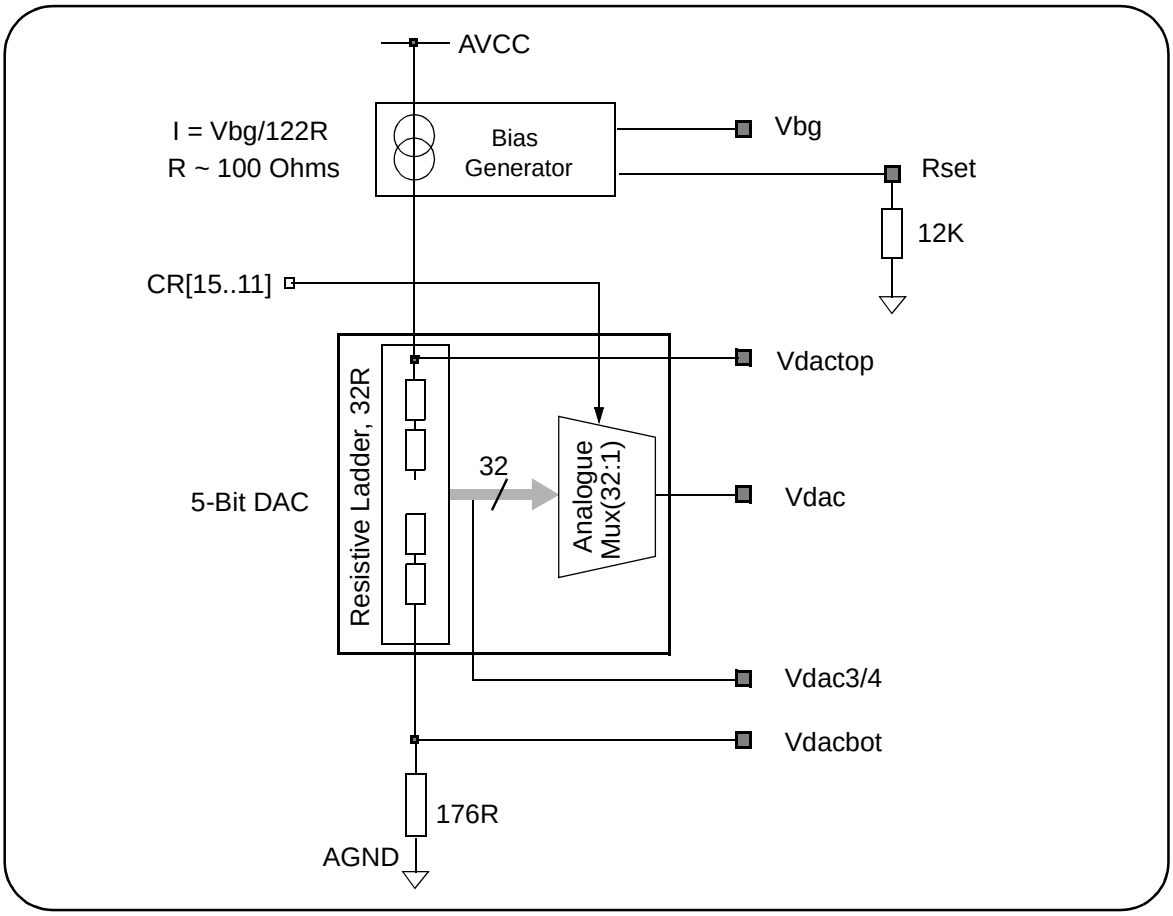
The sensor's internal black reference, which drives the AVORef output path, is derived from a separate 8 by 8 array of pixels connected in parallel. The input voltage to all pixels in the 8 by 8 array is VRT, that is the pixels are in reset. A sample & hold stage controlled by SAMRef allows the VRT voltage driving the black reference pixels to be sampled, freezing the black reference value.

Normally the black level reference should be updated between every still image capture sequence or between every frame in live video mode. Under very high illumination, however, the black reference should be sampled between every line in live video mode.

The internal black reference can be sampled at the beginning of a frame using SAMRef. It can also be observed line by line by asserting SELRef (without CLAMP) in the dead period between reading rows of pixels out onto AVO.

The 5-Bit DAC

The internal five bit resistive ladder DAC is energised by a Bias Generator that is set by the internal Bandgap Voltage Reference, Vbg, and the external 12K resistor connected from Rset to AGND. The Vdac output of the DAC, which can be used to set either VCL1 or VCL2, is adjusted by bits 11 to 15 of the Control Register/Serial Interface.



Note: The Vbg pin is a high impedance output, and can be over-ridden within the VCL input limits.

Parameter	Definition	Value	Comment
Vdactop	208/122 * Vbg	2.08V	
Vdacbot	176/122 * Vbg	1.76V	
Vdac3/4	199/122 * Vbg	1.99V	
Vdac	CR[15..11] * (32/122 * Vbg)	-	
Zdac	Vdac Output Impedance	21K	Ohms ±25%

5-Bit DAC Parameters

Black Reference Lines

There are six lines at the bottom of the pixel array that are covered with opaque masking. These black reference lines have their own reset shift register. A four to one multiplexer, controlled by Control Register bits CR[4] and CR[3], selects the input to this shift register (FBCK), and hence the operating mode. The four modes of operation are:

1. Permanent Reset - By setting FBCK low, the black lines are permanently reset to VRT.
2. Minimum Integration - FBCK follows the field read pulse, FR; the black reference lines are held in minimum exposure.
3. Integration - FBCK follows the field read pulse, FI; the black reference lines therefore have the same exposure time as the array.
4. Permanent integration; the reference lines continue to integrate until reset as in 1.

Option 1. is the most stable as it does not depend on either the quality of the black shield above the black pixels or any light incident on the pixels. However it is also the least accurate as it does not allow for dark current or the breakthrough of the falling edge of the pixel reset signal onto the pixel capacitance. The resulting reference value will be ‘blacker’ than black due to the above errors.

Option 2. is more accurate than option 1. as the effect of the pixel reset signal breakthrough is included, but the effect of total dark current is not included since the black reference pixels are not integrating for the same time as the image section of the pixel array. The reference is, also, now sensitive to the effects of light reaching the black line pixels.

Option 3. includes the effect of dark current since the black reference pixels are integrating for the same time as the image section of the pixel array. The validity of the reference is, however, now even more sensitive to the effects of light reaching the pixel.

Option 4. in combination with option 1 allows the exposure time for the black reference lines to be controlled independently of the exposure of the rest of the image.

Note: For best results, it is recommended that the average of the four central lines of the black reference line group is used to characterise ‘Black’ for the frame.

Exposure Control

Exposure control is achieved either electronically by varying the FI pulse duration, or directly by means of a shutter arrangement (mechanical, electro-mechanical, electro-optical, and so on). The correct exposure level for any scene can be assessed by processing a ‘trial exposure’ of the scene, or by utilising the ‘Accumulate’ or ‘Parallel Integration’ operating mode.

See: **OPERATING MODES** for a full description of exposure control.

OPERATING MODES

There are five main operating modes for the sensor:

- Still Image Capture with a Frame Buffer
- Correlated Double Sampling (line by line FPN cancellation)
- Live-Video/Cine Modes
- Accumulate
- Parallel Integration

These are explained below in outline. The following Section provides detailed timing requirements for the various control signals necessary to operate the sensor.

Removing Noise

In order to obtain high quality, low noise images from the VV6850 sensor pixel to pixel offset variations, or Fixed Pattern Noise (FPN), must be removed. This can be done by reading the image array more than once, for example reading in the dark to establish a reference for each pixel, then reading the exposed array to collect ‘image plus offset’ data, then subtracting to remove the offsets. To obtain the lowest noise operation the random pixel ‘reset’ noise must also be removed.

Sources of Fixed Pattern Noise

The major sources of Fixed Pattern Noise in the sensor that can be cancelled are:

- Transistor Threshold Offsets
- Dark Current

Each of the above can be effectively cancelled to a much lower residual random noise level by using the techniques described below. The residual noise sources in the sensor, such as flicker noise, dark current shot noise, thermal noise and ADC Quantisation noise, that cannot be cancelled, or are a function of the cancellation techniques, define the overall camera noise performance.

Methods of Removing Fixed Pattern Noise

Transistor Threshold Offsets

Each pixel amplifier, each column source follower and each output channel multiplexer, has a unique offset caused by process variations in the threshold voltage of the transistors. This offset is independent of exposure, and will be relatively stable with respect to temperature and operating conditions.To remove Transistor Threshold FPN, the VV6850 is used in conjunction with an ADC and either a frame buffer or a line buffer:

- **Pixel offset removal frame by frame with a shutter:** A frame buffer is used to obtain the pixel to pixel DC offsets for the whole image. The offsets are obtained by capturing a dark (FPN) frame with the shutter closed, and an ‘image’ frame with the shutter open. The ‘clean’ image data can then be extracted by subtraction. (This technique can only be used with a physical shutter, and with at least one extra dark frame acquisition period.)

- **Pixel offset removal frame by frame with a reference frame:** A non-volatile frame buffer is used to obtain the pixel to pixel DC offsets for the whole image at camera build. These offsets are then subtracted from the exposed ‘image’ as it is read to obtain the ‘clean’ image data. (This technique gives the fastest frame acquisition time at the expense of accuracy.)
- **Pixel offset removal line by line:** A line of pixel information is read and stored in a line buffer. The line is then reset to black using the CDSR signal, before being re-read to obtain the pixel to pixel DC offsets for that line. As the line is re-read the offset data for each pixel is subtracted from the value stored in the line buffer, the result being the ‘image’ data. (The COLsam signal must be used to ensure that samples in the same line have the same integration period.)

With line by line offset removal the time for reading out a complete frame is doubled, since each line has to be read twice. It is also not possible to remove pixel reset noise or dark current, thus there is a trade off between the frame rate and image quality, and the amount of memory required.

Full frame offset removal can be achieved in many ways, depending on what ancillary devices are available in the camera system, and constraints such as image quality required and acceptable minimum frame rate.

Dark Current

The ‘dark current’ in a pixel photodiode is the inherent leakage that discharges the integrating capacitance in the same way as incident light. Hence, Dark Current FPN builds up on the array whenever the array is released from reset, that is when FI is high. This means that the amount of dark signal depends on exposure time, and varies from pixel to pixel.

The same degree of dark current charge build-up occurs in the array whether or not the array is exposed to light. Therefore, if the array is allowed to integrate (FI high) with no incident light for the same length of time as for the image exposure, the dark current element of the exposed image data can be ascertained and removed from the image data by subtraction, leaving behind the dark current shot noise.

Since dark current also depends on temperature the dark frame should be taken close in time to the image frame, in order to avoid ambient temperature variations.

‘Reset Noise’ Cancellation

One random noise source that can be cancelled is ‘reset noise’ (or ‘kTC’ noise), which is due to the switching of the photodiode capacitance when the pixel is released from reset. This is present in all subsequent reads of the array (without reset) to the same extent. These can therefore be extracted by reading the array immediately after reset (when FI goes high) and subtracting the value obtained from the ‘exposed’ array data. This operation also cancels Pixel Threshold Offsets.

To achieve reset noise cancellation, FR should be taken high for two LCK periods when FI goes high, and 1014 lines read *before* the array is exposed to the required image. The pixel data from this pass of FR through the VSRs must be stored in a frame buffer, and subtracted from the exposed image data. The exposed image is obtained when FR is pulsed high again, coincident with the last two LCK periods of FI being high after the exposure period.

It is not possible to describe all of the many operating schemes that can be devised for image capture and FPN reduction. The basic recommended modes for camera operation are described below, with detailed timing requirements in the following Section.

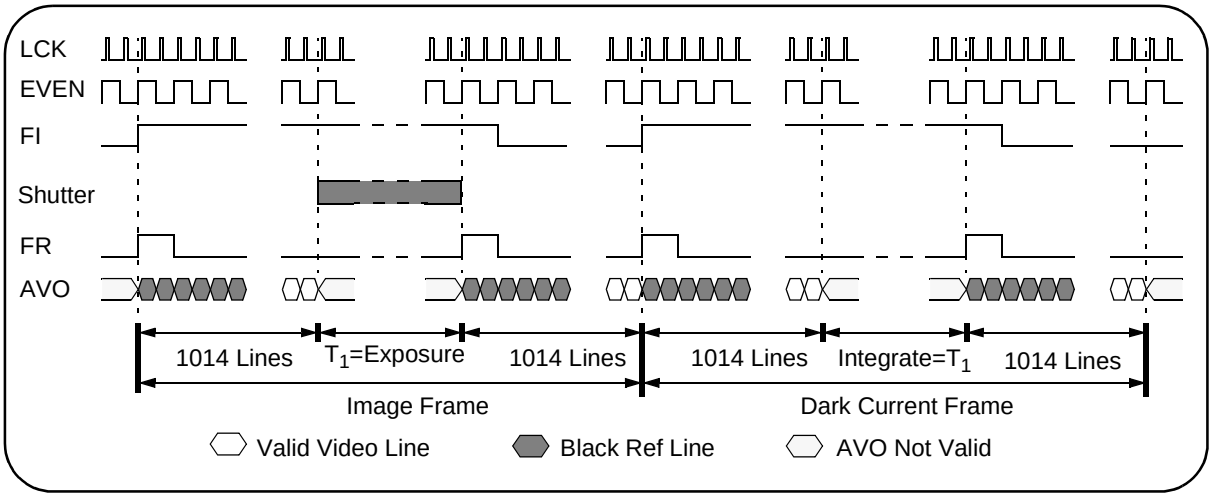
Still Image Capture with a Frame Buffer

This is the recommended operational mode for high quality still image capture in camera systems where there is an electro-mechanical shutter in front of the sensor and a Frame Buffer for temporary image storage. FPN cancellation is central to this mode of operation, and is described in detail. Other operational schemes that may be devised can include all or some of the techniques employed in this example, but the elements are essentially the same. (See: **APPENDIX, APPLICATION NOTES,** for a discussion of variations to this FPN cancellation scheme.)

Note: For the simplest possible image capture mode, with no FPN cancellation, see the description of the Vertical Shift Registers above.

The basic still image capture cycle starts with the shutter closed. The array is released from reset by taking the input to the reset vertical shift registers, FI, high. The system controlling the camera must then wait for 1014 lines to allow this “integrate wavefront” to propagate through the shift register, before opening the shutter. When FI goes high FR should also be pulsed high for 2 lines to initiate the Read sequence. Reading each pixel as soon as it is released from reset yields a reset image which contains both the fixed pattern noise component for each pixel and the random reset noise due to that particular reset operation. This image should be stored in a frame buffer.

When the shutter has closed after exposure FR must be pulsed high again for 2 lines to re-read the array and obtain the exposed image data. Again, it will take 1014 lines to read all of the array pixels. FI should fall when FR falls, to return the active pixel array into reset. As the image frame is read out the appropriate pixel reset value, as stored in the frame buffer, is subtracted from the current pixel value and the result written to the frame store. This removes both pixel reset noise and pixel to pixel DC offsets from the image.



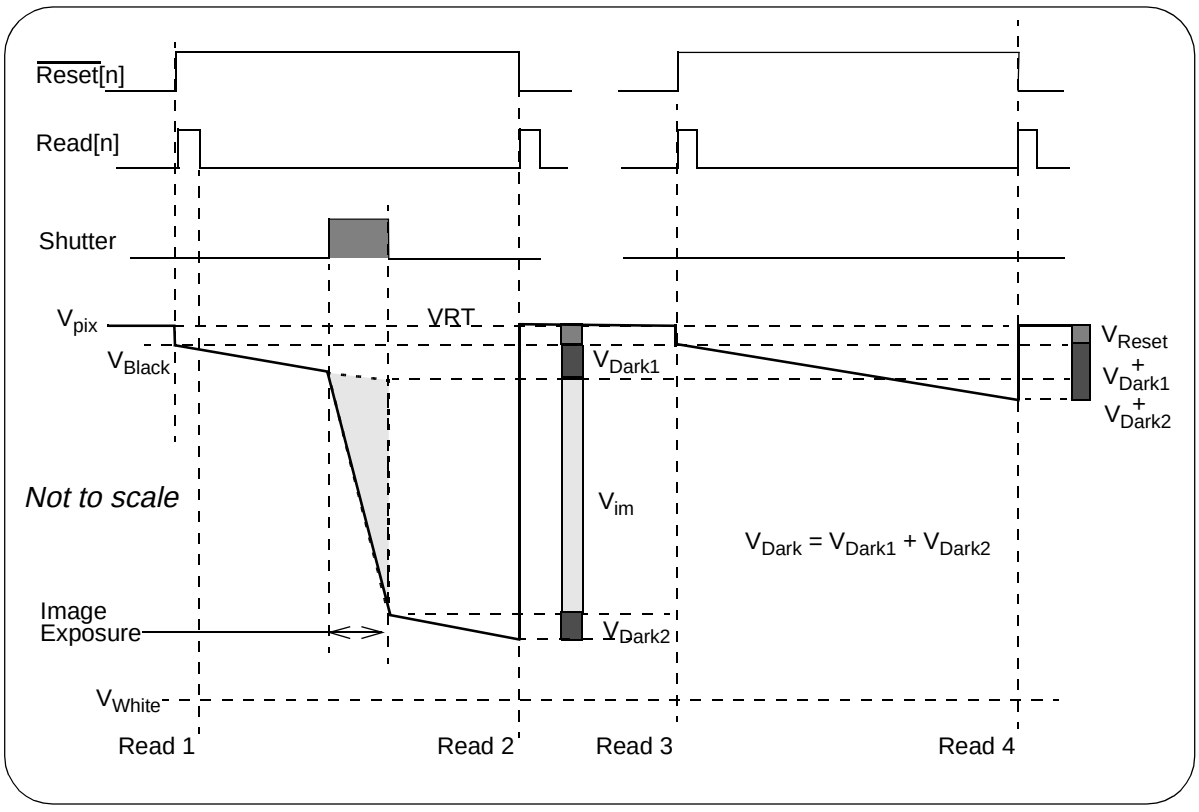
(See **DETAILED OPERATIONAL TIMING** below for exact relationships.)

Due to the relatively long time taken to read out an image (200 ms, assuming a 5 MHz clock rate), the dark current in each pixel is a significant part of the image data. To remove the fixed pattern noise injected by the dark current a ‘dark image’ must be captured with the same integration time as the exposed image but with the shutter closed. Subtracting the dark image from the exposed image removes the dark current fixed pattern noise, leaving a ‘clean’ image. This process can be summarised as follows:

1. With the shutter closed, release the sensor from reset and immediately read a frame into the buffer memory; this captures the array threshold FPN and reset noise ('V_{Reset}')
2. After 1014 line periods, open the shutter and expose the sensor to the required scene (the exposure time can be determined by 'Parallel Integration' or 'Accumulate' — see below)
3. Close the shutter and immediately read the array; as each pixel is read, subtract the value for that position stored in the frame buffer, and overwrite that pixel location with the difference — the memory now contains the image plus dark current FPN (V_{im} + V_{Dark})
4. After the 1014 line periods of the second read, repeat the image capture cycle, but do not open the shutter; this time, load a *second* frame buffer with first the V_{Reset} value and then the V_{Dark} value (after subtraction)
5. After the second integration period, subtract the V_{Dark} value for each pixel that is stored in the second frame buffer from the (V_{im} + V_{Dark}) value for that position stored in the first frame buffer and overwrite that pixel location with the result.

The frame buffer now contains the corrected image values, which can be processed for colour and so on, then transferred to permanent image storage memory.

The pixel voltages for this method are illustrated schematically below:



Note: Since the 'integrate wavefront' must propagate through the VSR, the point at which the open shutter exposure occurs will vary progressively from line to line of the array — from close to 'Read2' on the bottom line to close to 'Read1' at the top.

Correlated Double Sampling (line by line)

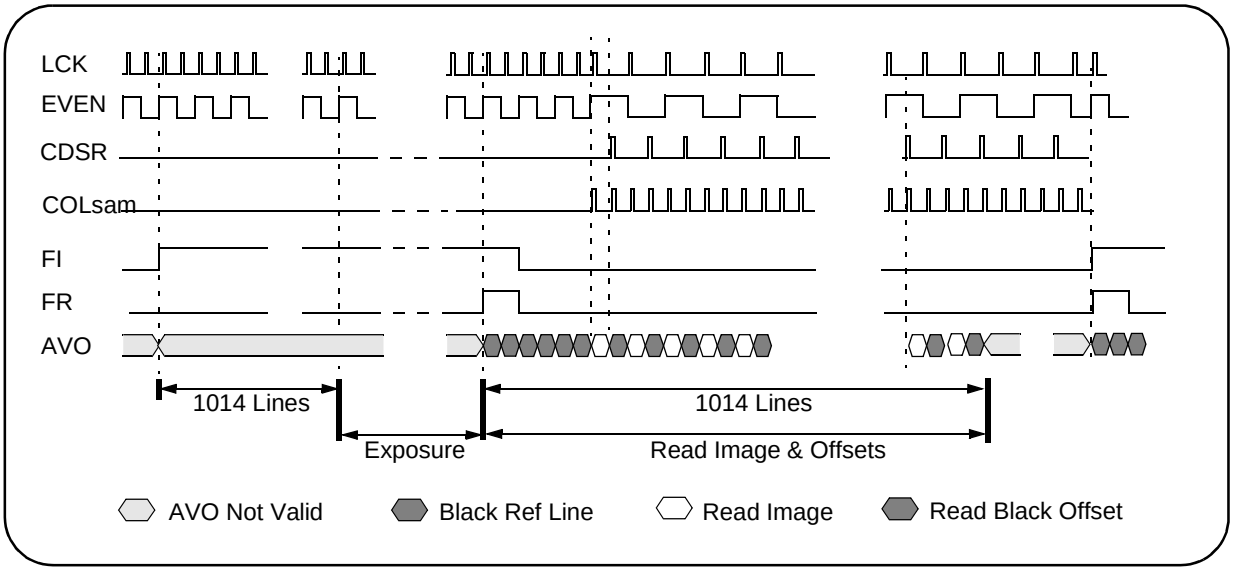
This is an alternative FPN cancellation mode for camera systems where there is only a Line Buffer available for temporary image capture, and not necessarily a mechanical shutter in front of the sensor. The method outlined below, using the CDSR signal, relates to a still image capture in a shuttered camera system, but the same principle could also be applied to exposure control with the FI pulse duration in Still Frame and Live Video modes.

Note: This method does not cancel dark current FPN, and as the pixel is reset twice, has two lots of 'reset' noise sources.

The array is released from reset by taking the input to the reset vertical shift registers, FI, high. The system controlling the camera must then wait for 1014 lines to allow this "integrate wavefront" to propagate through the shift register, before opening the shutter (or further extending the FI pulse). After the sensor has been exposed for the appropriate time, FR must be pulsed high for 2 lines to read the pixel array and obtain the exposed image data, which is loaded into the Line Buffer line by line.

When a line of 804 pixels of image data has been read, the CDSR signal is pulsed high to reset the line of pixels to Black (without advancing the HSR). COLSam is then pulsed to resample the row, and as each pixel is read out this 'Black Offset' value is subtracted from the value stored in the line buffer and the result passed on as corrected image data.

Note: During the 992-line image data readout, LCK and EVEN must be at least twice their minimum periods (with maximum PCK rate of 5.0MHz), to allow for the second line read.



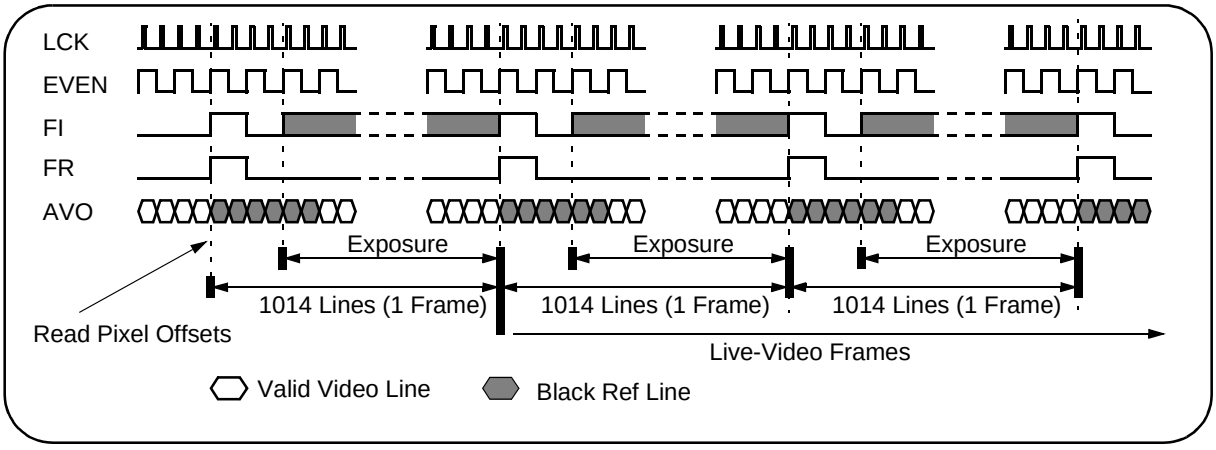
(See **DETAILED OPERATIONAL TIMING** below for the exact relationships, and also how CDSR, COLSam and PXRD should interact.)

Live-Video & Cine Modes

In the ‘Live Video’ mode the effect is similar to a conventional video camera, with a frame rate of just under five frames/second (with a 5 MHz pixel clock). This can be used, for example, to provide a moving ‘viewfinder’ display for a stills camera. ‘Cine’ mode is similar, but achieves higher frame rates.

In Live-Video mode the exposure level for a frame is controlled electronically by varying the high duration of the FI waveform. The high duration of FI can be varied from 2 lines (minimum exposure) in multiples of 2 lines up to 1012 lines (maximum exposure). The falling edge of FI is fixed within the frame, therefore it is the leading edge of FI that must be moved to vary exposure.

The field read pulse, FR, must be set high for the 2 lines preceding the falling edge of FI; this means that the FR waveform is identical to the FI waveform for minimum exposure. The necessary signal relationships are illustrated below:



If a frame buffer is being used to store the pixel to pixel DC offsets the first image captured on entering Live-Video mode should have minimum exposure to obtain and store pixel offset data. However, if the offset data already exists in memory this step is not required.

Cine Mode

Selecting Cine mode via the Serial Data Control Register (CR[2]) subsamples the pixels in a line, reading out only every other pixel pair. (See: **HORIZONTAL SHIFT REGISTER** for details.) ‘Cine’ mode enables higher frame rates to be achieved, for example 20 frames per second (at 5MHz) by also only reading every other *line pair*. To achieve this, the Vertical Shift Registers must read out 2 lines and then skip the next 2 lines, by inserting 2 extra LCK pulses and one extra EVEN pulse between every second line read out. (See: **VERTICAL SHIFT REGISTERS** for details.)

Note: It is not essential to skip line pairs in Cine mode, if aspect ratio need not be preserved. It is possible to skip more than one line pair, an also to increase PCK (up to 10MHz) to further increase frame rate.

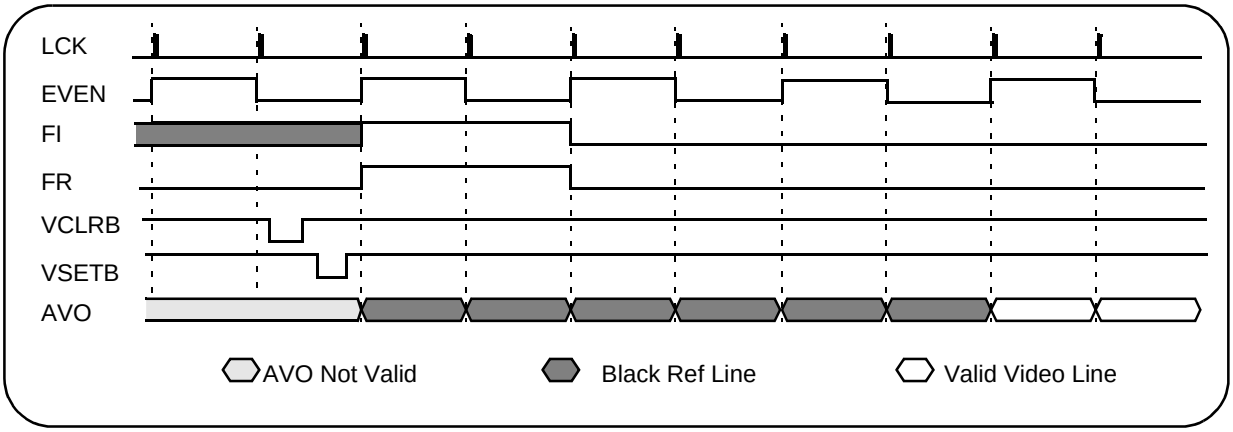
For high frame rates, it is also best to read a dark frame into memory and subtract the Fixed Pattern Noise as the array is read in order to reduce the frame overhead of either line-rate CDS or the Shuttered Frame-rate cancellation schemes.

Parallel Integration

In this mode all of the pixels in the array are released from reset at the same time. This is achieved using the VCLRB and VSETB signals for the vertical shift registers. (VSETB only effects the reset shift register). This can be used to give a quick but crude estimate of correct exposure by, for example, counting lines until a line is reached where all pixels in the line are saturated, then setting exposure to, say, 50% of the integration time taken to reach that line.

The sequence of operations is as follows:

1. Pulse VCLRB low to reset the Read and Reset vertical shift registers to all zeros; this forces all pixels into reset
2. Pulse VSETB low, this loads the Reset shift register with all ones, which starts all of the pixels integrating.
3. Then FR should be pulsed high for 2 lines to start the array readout.



Note: VCLRB and VSETB must NEVER be taken low at the same time.

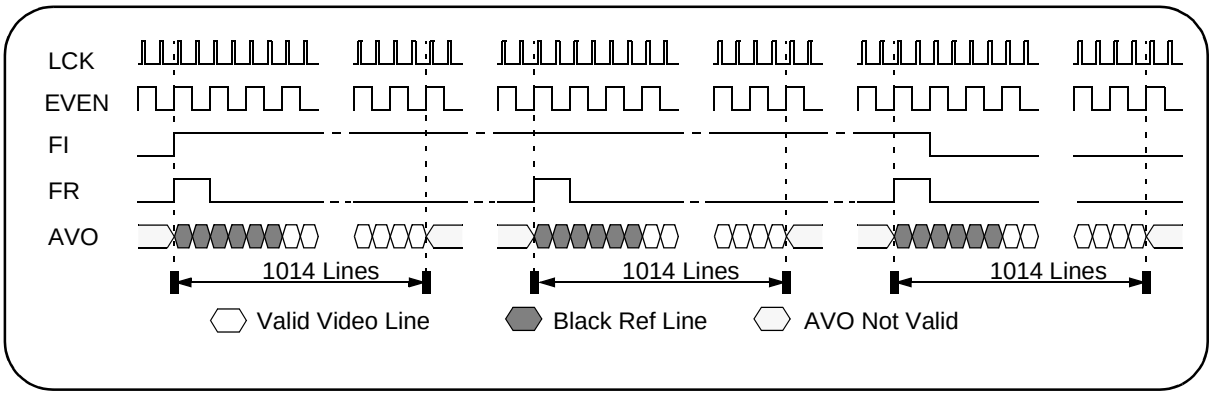
Since all pixels start to integrate at the same time and readout is sequential (line by line), each line of pixels represents a different exposure value. If the FR pulse occurs on the next video line after VSETB goes high then the first valid video line readout will have been exposed for 6 lines (the black reference lines), and the last line of valid video will have been exposed for 1014 lines.

Accumulate

In ‘Accumulate’ mode the pixel array is repeatedly re-read without resetting the pixels. This mode is intended for exposure monitoring in conjunction with a flash when light levels are low, and more than one frame time is required to obtain sufficient integration.

The array is released from reset by taking FI high. At the same time FR is pulsed high for 2 lines to read out the pixel reset values. Then at the required intervals (of not less than 1014 line periods) FR is pulsed high for 2 lines to re-read the array. While the array is being repeatedly re-read FI must stay high. Effectively, the successive reads of the array are monitoring the rate of charge accumulation in the pixels.

When sufficient integration has occurred to produce, say 50% average saturation, reading can be terminated. The number of frames of exposure required to achieve this can then be used to calculate the flash energy required to correctly expose the scene. On the falling edge of FR for the final array read, FI should go low, to return the pixel array into reset.



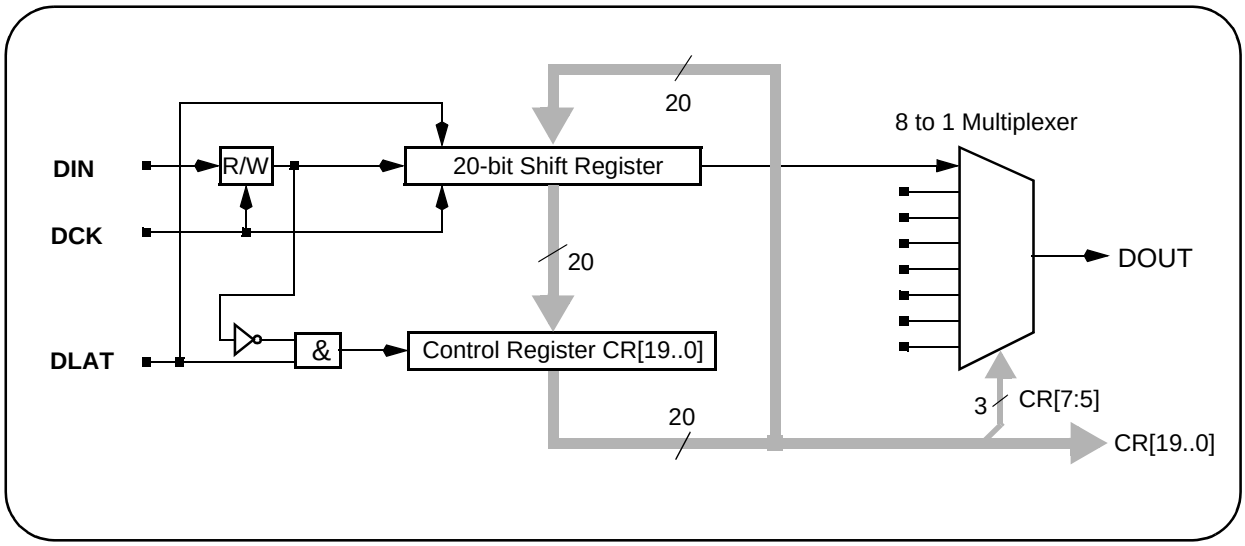
THE CONTROL REGISTER & SERIAL COMMUNICATION

The VV6850 includes a full duplex serial interface, and can be controlled and configured by a host processor. Data describing the current configuration of the camera is stored in a 20-bit control register. This register can be read from the camera on the serial interface, and can also be written to from the serial interface to change camera operation.

When a 22-bit serial interface data word arrives at the camera on DIN, the first 20 (msb) bits are loaded into a shift register, and the last two bits ('R/W') are examined to ascertain if a 'read' operation or a 'write' operation is required. If a 'write' is required ('R/W' = "00") the contents of the input shift register are transferred to the control register. Otherwise, the current contents of the control register is output on DOUT. (Note: In 'test mode', that is with CR[7..5]>0, certain other signals are monitored by DOUT and CR[19..0] is not transmitted.)

The signals used to effect the serial data interface are:

- DIN Serial Data In; DIN is sampled on the rising edge of DCK
- DOUTSerial Data Output
- DCK Serial Data Clock
- DLAT Serial Data Latch; transfers the input data word to the control register (for 'write'), and initiates control register output on DOUT (for CR[7..5]=0)

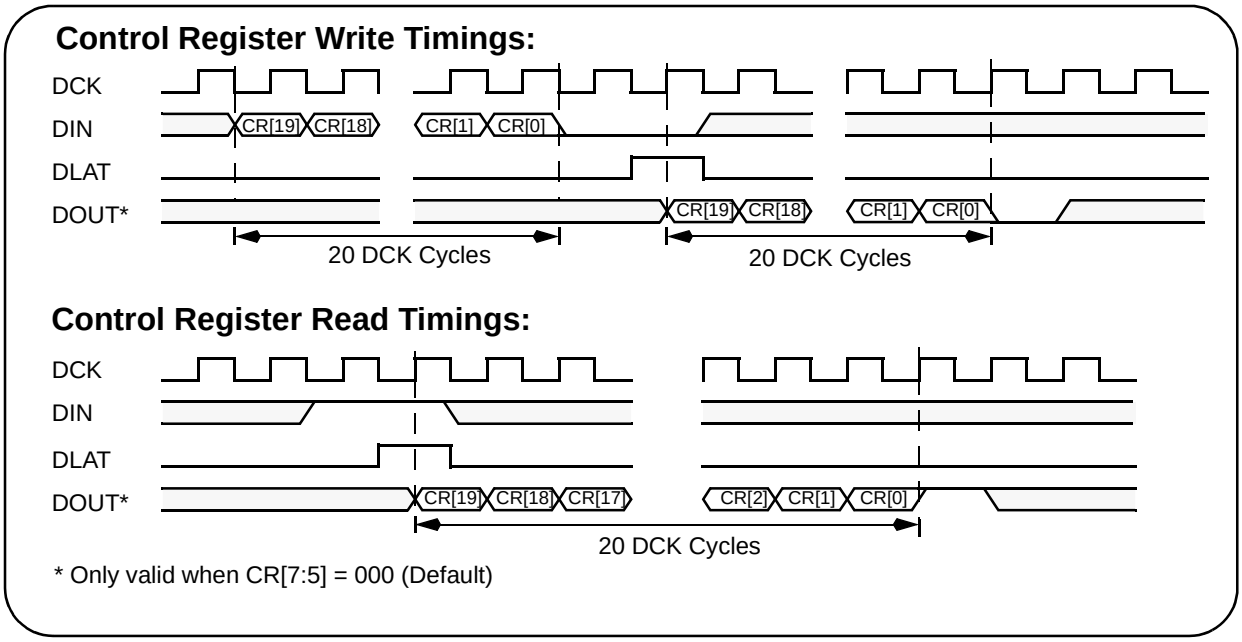


Serial Communication Protocol

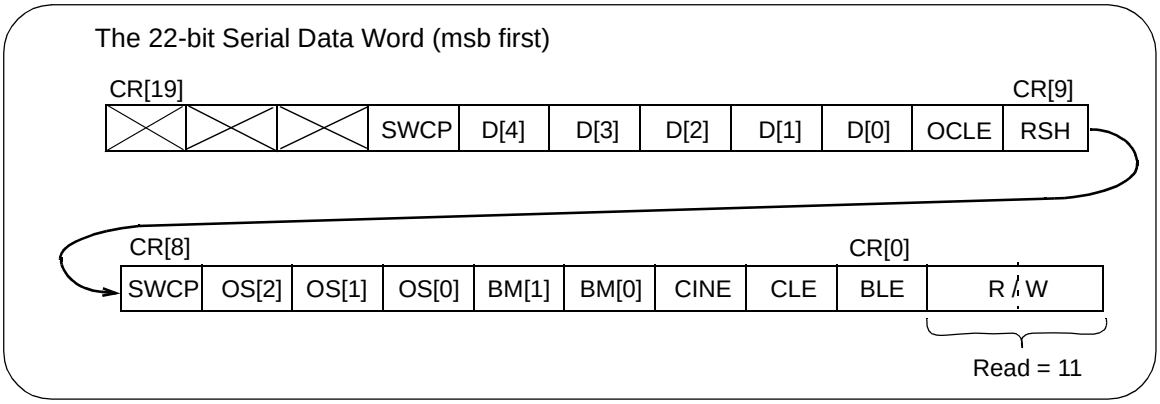
The host must perform the role of a communications master, while the camera acts as a slave receiver and transmitter. Communication from host to camera takes the form of a 22-bit data word, with a 20-bit data word returned to the host. Since the serial clock (DCK, maximum frequency 100kHz,) is generated by the host, the host determines the data transfer rate.

The host sends the 20 bit control word, most significant bit first, then either holds DIN high for two clock cycles, to indicate a ‘read’, or holds DIN low for two clock cycles, to indicate a ‘write’. The host also takes DLAT high for one clock cycle, corresponding to the last bit of the R/W pair. This defines the end of the transfer and latches the data word to the Control Register, if required (R/W=00). DLAT also (on the next rising edge of DCK) transfers the contents of the Control Register to the Shift Register, which is then output to DOUT if CR[7..5] = 0.

The data transfer protocol is illustrated below:



The Serial Data Word



Read Data Format

The 22-bit Serial Data Word consists of the two-bit wide R/W flag, and the 20 bits of Control Register data (CR[0..19]. The following tables defines the CR information contained in the messages:

CR Bit	Function/Comment	Default
0	Bit-line Test Enable	0
1	Bit-line Clamp Enable	1
2	Select ‘Cine’ mode: only every other ‘colour’ pixel column is output	0
4,3	Controls the integration mode for black reference lines	0
7..5	Selects the node that DOUT is monitoring	0
8	Enables the Sample & Hold circuits on the four output channels	0
9	Connects the four black reference output channels together; the default is AVORef cycling through the four channels	0
10	Enable clamping circuitry on the four output channels	1
15..11	D[4..0] - 5-bit Resistive DAC value; D[4] is msb	16
16	Switch in the Output Stage Sample&Hold Capacitors	0
19..17	Reserved	0

Control Register Definitions

The various bits in the Control Register define operating modes and parameters as follows:

CR[0] - Bit-line Test Enable

Enables testing of the pixel column interconnections. This bit should always be 0.

CR[1] - Bit-Line Clamp Enable

The default is the bit-line clamp enabled, CR[1] = 1, which ensures that if a bit-line goes too low due to a pixel being heavily over-exposed, the bit-line is clamped to Vbltw-Vtn.

Note: Due to internal variations, the absolute clamp voltage will vary from column to column. Thus, care must be taken to ensure that the ADC value clips before the bit-line clamp circuits operate otherwise column to column fixed pattern noise will appear in the saturated white regions of the image.

CR[2] - 'Cine' Mode

Setting CR[2] = 1 forces the horizontal shift register to read out every second red, green or blue pixel in each odd and even field. In this mode 202 pixels instead of 404 pixels are read out per colour per line. (Note: The buffer columns on the left and right side of the pixel array are always read out.)

CR[8] and CR[16] should also both be low for Cine mode.

CR[4:3] - Black Reference Line Integration Mode Select

CR[4] and CR[3] control the selection of the four possible integration modes to the black reference lines. The Table below defines the code associated with each of the four modes.

CR[4]	CR[3]	Integration Mode for Black reference Lines
0	0	Permanent Reset.
0	1	Minimum Integration (FR)
1	0	Same integration time as main array (FI)
1	1	Always integrating.

(See: **VIDEO OUTPUT - BLACK REFERENCE LINES** for details of these modes.)

CR[7:5] - Select DOUT output

Output to the DOUT pin is multiplexed under the control of CR[7], CR[6] and CR[5] for test purposes. All three of these bits must be set to zero for image data to be observed on DOUT.

CR[8] - Output Channel Sample & Hold Enable

The sample and hold circuits in the AVO and AVORef output stages isolate the capacitive back injection which occurs when an output channel is multiplexed onto the AC Coupling capacitor, which changes the nature of the back injection:

- Without sample and hold (CR[8] = 0 (default)), the interaction of the back injection and the column output results in the AVO overshooting slightly before settling to the desired value
- With sample and hold enabled (CR[8] = 1) the overshoot is eliminated, but the current pixel value will contain a very small contribution from the previous pixel value read out on AVO

Note: CR[16] allows the output channel sample /hold capacitor to be isolated from the signal path.

CR[9] - Common Up the Black Reference Channels

There are two options for operating the four black reference output channels:

1. CR[9]=0 : Operate with the AVORef cycling between each of the four black output channels. AVORef will follow the shape of AVO as the AC coupling capacitor is cycling in the same way within both output stages. Any mismatch between the black reference output channels will appear as a four-cycle pattern on AVORef.
2. CR[9]=1 : Parallel up the operation of the black output channels. AVORef represents the average of the four black output channels.

CR[10] - Output Channel Clamp Enable

Setting CR[10] = 1 (default) clamps the four output channels that are multiplexed onto AVO to prevent them going beyond the designed operating voltage range. This ensures that each output channel always has enough time to recover from being inactive before outputing pixel data.

CR[15:11] - 5-Bit Resistive DAC Data Value (D[5:0])

Data for the internal 5-bit Resistive Ladder DAC (default = 16). CR[15] is the MSB.

CR[16] - Switch in Output Stage Sample/Hold Capacitors

Setting CR[16] high isolates the output channel sample/hold capacitors from the signal path. By isolating these capacitors the output channels settle to the desired value in a shorter time.

Note: CR[16] should only be set high when the output channel sample/holds are disabled.

The primary use of this function is in Cine mode. In this mode only two of the four output channels are in use. As the two output channels have only half the time to settle, compared with the normal readout sequence, CR[16] should be set high to improve settling of the output channels.

CR[19:17] - Reserved for future use

DETAILED OPERATIONAL TIMING

The following Section describes in detail the recommended timing for the primary operating modes. There are many possible timing schemes, with more flexible setup and holds, but the recommended timings are safe. Specifically, timing diagrams and tables are given for:

- Normal Array Read
- Correlated Double Sampling (line by line)

System Clocks

Line and pixel timing is done in PCK's, and all signals should change on the falling edge of PCK.

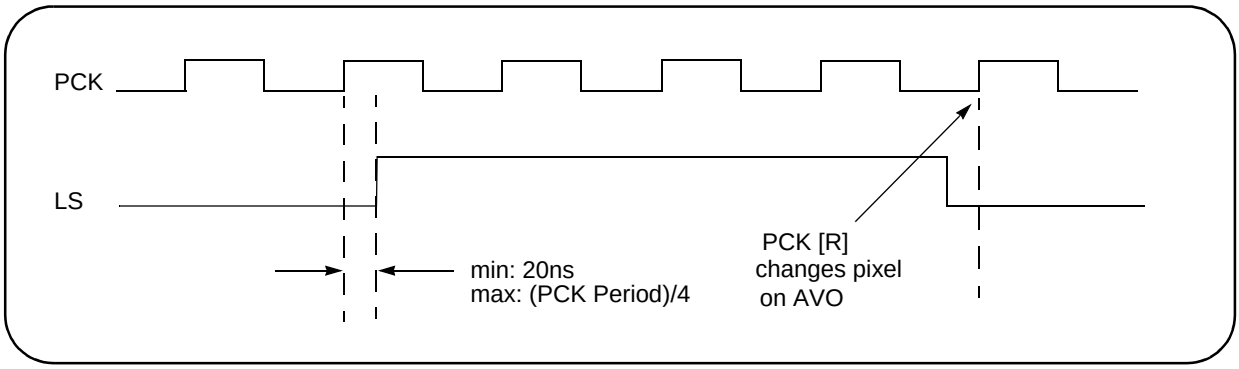
	Min	Typ	Max	Units
PCK Period	100	200	-	nS
PCK Duty Cycle	40	-	60	%
Line Period	1024	1024	-	PCK's
Line Period (CINE Mode)	624	624	-	PCK's

System Clocks.

The timings in the following tables have been expressed for a 5MHz PCK. The symbols [T],[R],[F],[H],[L] signify Transitional edge, Rising edge, Falling edge, High Level and Low Level respectively.

Line Start to PCK Timing

The relative timing of the Line Start pulse, LS, and the Pixel Clock, PCK, is extremely important for correct sensor operation. LS must be set up at least 20ns after the rising edge of PCK, no later than (PCK Period)/4 after the rising edge of PCK, and must be held for four PCK cycles. This is illustrated below:

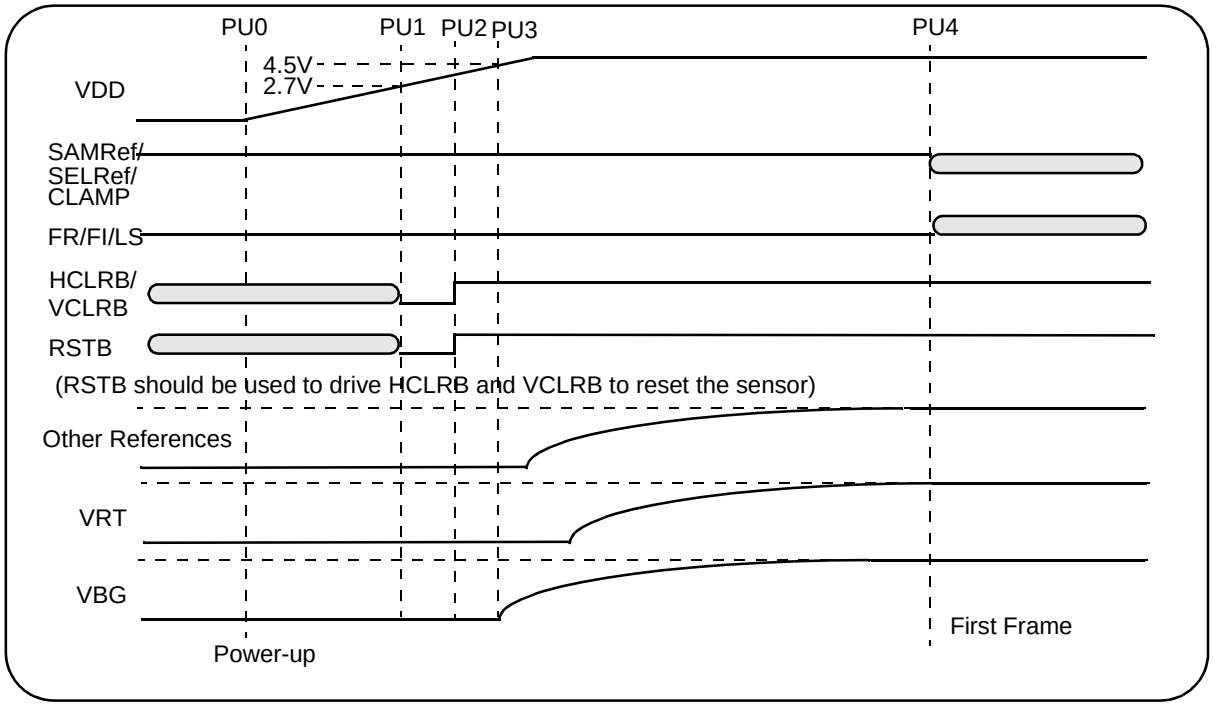


Initial Power Up Timing

- On powering up the array should be reset by VCLRB and HCLRB, to help the settling of the internal references. An internal power-on-reset circuit generates RSTB, which can be used to reset the sensor.
- The references VRT and Vbg must be stable before the first frame; this will be a function of the decoupling.
- The internal reference and AC coupling stages should be put into sample mode by making SELRef, SAMRef, and CLAMP high.
- To ensure that the array is inactive until the first frame on power up FI, FR, LS, PCK, LCK and EVEN should all be low.

Event	Timing	Min	Typ	Max	Units
Power On Reset trigger Voltage	PU1	-	2.7	-	V
RSTB pulse width	PU2-PU1	100	-	-	uS
Settling Time	PU4-PU3	10	-	-	mS

Recommended Start-Up Timing.

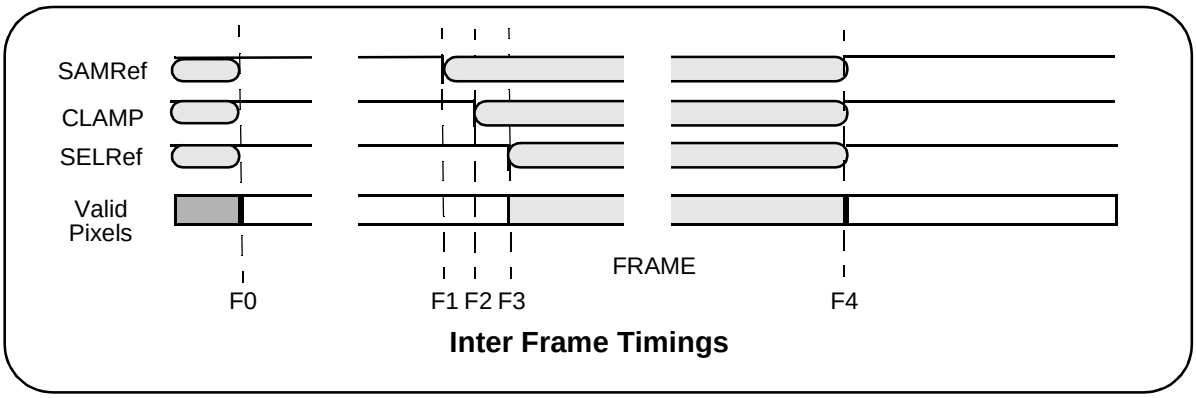


Note: Serial Data can only be sent after RSTB rises.

Inter-Frame Timing

When a frame is to be taken, the first task is to sample the reference with SAMRef. This signal should be held high until the first line, which should be for at least 100uS.

If possible, SAMRef should be held high between acquisition of still frames. In order to also ensure that the AC coupling stages do not drift, SELRef and CLAMP should also be held high.



Inter Frame Timings

Event	Timing	Min	Typ	Max	Units
SAMRef Period	F1-F0	100	-	-	uS
CLAMP overlap of SAMRef[F]	F2-F1	1			uS
SELRef overlap of CLAMP[F}	F3-F2	0.200			uS

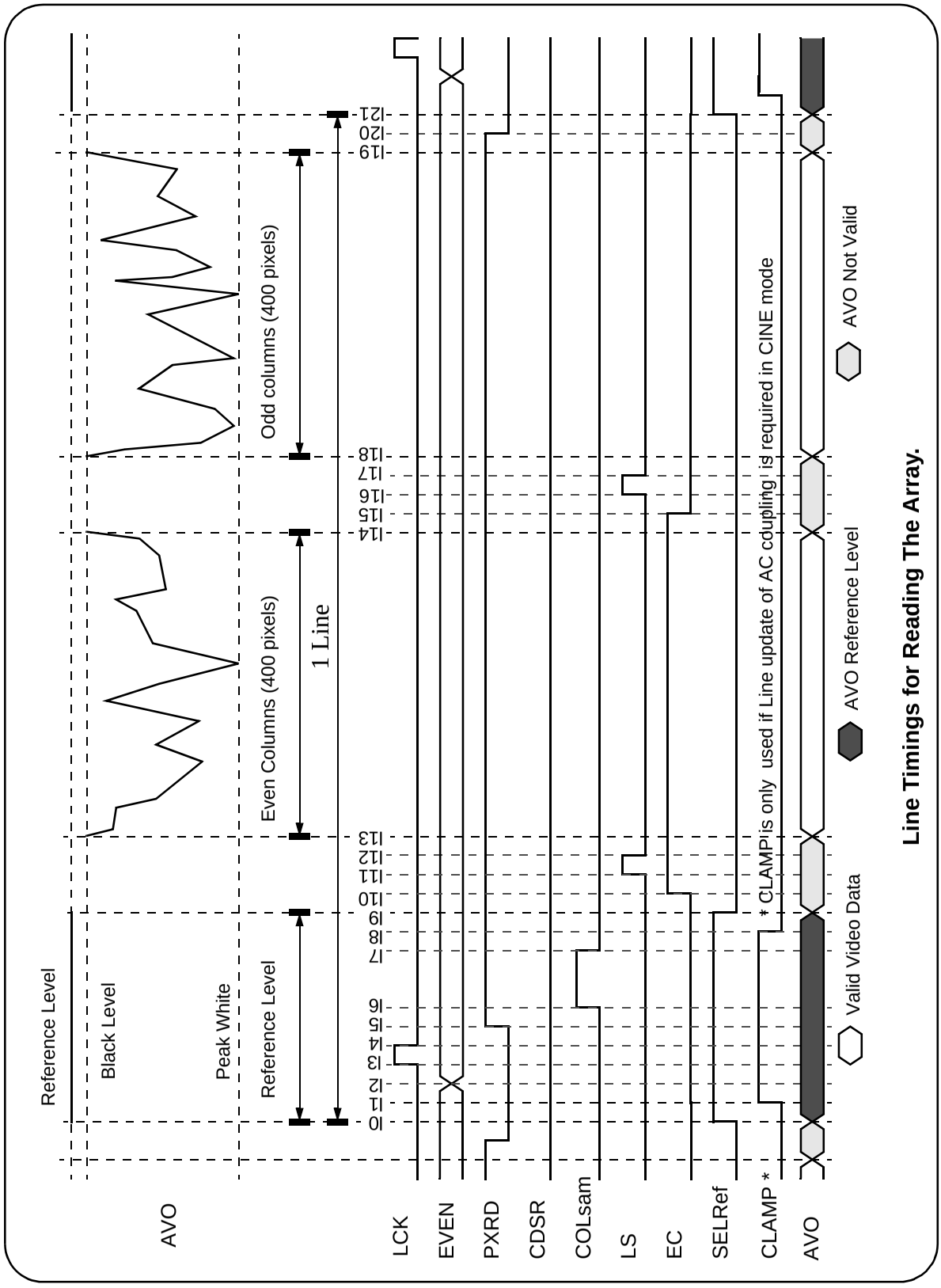
Inter Frame Timings

Line Read-Out Timing

The following diagrams and tables define the relative timings of the various control signals required to read a line of pixels. Not all of the signals shown will be required for all modes of operation, but where they are these timing constraints must be observed. Timings for Correlated Double Sampling (using CDSR) are given after the standard line read definitions.

LCK is the master clock for the vertical shift registers, for reading and resetting rows. LCK is a latching signal, and latches when high (to be reset on the next PCK).

The EVEN signal transitions must straddle LCK & PXRD, and FI & FR must straddle LCK. PXRD must be high when COLSam is pulsed. EC & EVEN are not latched, and must therefore remain high while reading valid pixels. The first line of pixel information is read out when the EVEN and FR signals are both high. If the EVEN signal is high during the second line period of FR pulse, the line readout sequence will be offset by one line relative to that outlined in the timing specification. This is due to the FR and FI inputs only being sampled when both LCK and EVEN are high.


Reference Level
Black Level
Peak White
Reference Level
Odd columns (400 pixels)
Even Columns (400 pixels)
1 Line
0
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
19
20
21
AVO
LCK
EVEN
PXRD
CDSR
COLsam
LS
EC
SELRef
CLAMP *
AVO
* CLAMP is only used if Line update of AC coupling is required in CINE mode
Valid Video Data
AVO Reference Level
AVO Not Valid
Line Timings for Reading The Array.

Description	#t	PCK Cycles	Time (us)
SELRef [R] - Start of Line	l0	0	0
CLAMP [R] (only if line CLAMPing is being done)	l1	1	0.2
EVEN [T]	l2	2	0.4
LCK [R])	l3	4	0.8
LCK [F]	l4	5	1.0
PXRD [R]	l5	10	2.0
COLsam [R]	l6	11	2.2
COLsam [F]	l7	206	41.2
CLAMP [F]	l8	207	41.4
SELRef [F]	l9	208	41.6
EC [R]	l10	209	41.8
LS [R] (even pixels)	l11	210	42.0
LS [F] (even pixels	l12	214	42.8
AVO valid, even pixels, start	l13	214.5	42.9
AVO valid, even pixels, end	l14	614.5	122.9
EC [F]	l15	616	123.2
LS [R] (odd pixels)	l16	617	123.4
LS [F] (odd pixels	l17	621	124.2
AVO valid, odd pixels, start	l18	621.5	124.3
AVO valid, odd pixels, end	l19	1021.5	204.3
PXRD [F]	l20	1023	204.6
End of line	l21	1024	204.8
Line Length	l21 - l0	1024	204.8
EVEN [T] - LCK [R] setup time	l3 - l2	2	0.4
LCK Duration	l4 - l3	1	0.2
LCK [F] - PXRD [R]	l5 - l4	5	1
PXRD [R] - COLsam [R], setup	l6 - l5	1	0.2
COLsam Duration	l7 - l6	195	39.0

Recommended Line timings

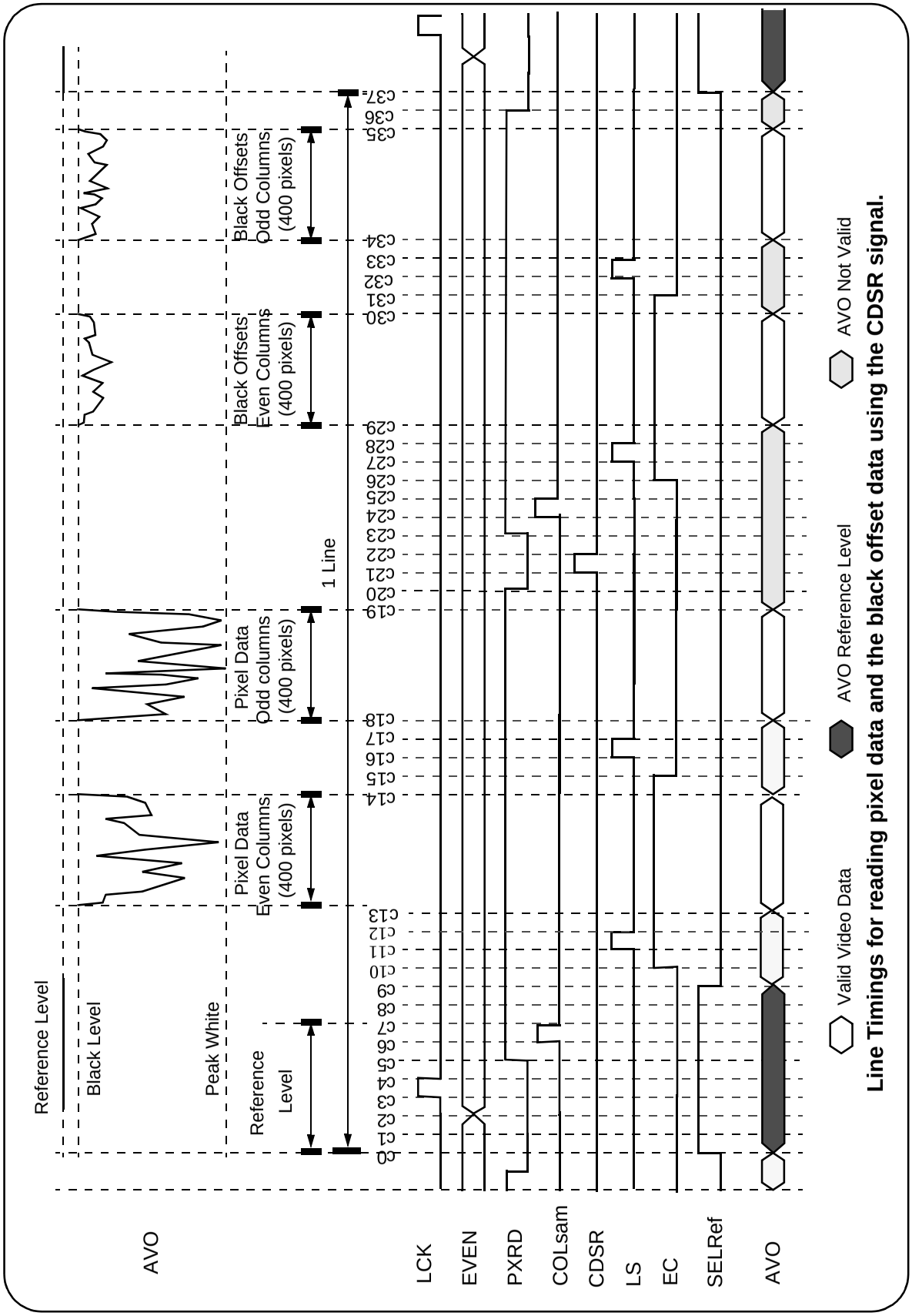
Description	#t	PCK Cycles	Time (us)
COLsam [R] - CLAMP [F]	l8 - l7	1	0.2
CLAMP [H] Duration	l8 - l1	206	41.2
SELRef [H] Duration	l9 - l0	208	41.6
SELRef overlap of CLAMP	l1 - l0 l9 - l8	1	0.2
SELRef [F] - EC [R]	l10 -l9	1	0.2
COLsam (F) - EC (R)	c10 -c7	3	0.6
EC [T] - LS [R] : even	l11 - l10 l16 - l15	1	0.2
LS [H] Duration 1 (even) Duration 2 (odd)	l12-l11 l17-l16	4 4	0.8 0.8
LS [F] - First Valid Even Pixel First Valid Odd Pixel	l13 - l12 l18 - l17	0.5	0.1
Valid pixels - even - odd	l14 - l13 l19 - l18	400	80.0
PXRD [F] - SELRef [R] (next line)	l21 - l20	1	0.2
NOTE 1: All input signals should change on the Falling Edge of PCK NOTE 2: For CINE mode the Valid pixels is reduced from 400 to 200, giving a reduction in Line time from 1024 to 624 PCK's, all other relative timings remain unchanged			

Recommended Line timings

Line Timing using CDSR

The following timing details relate to Correlated Double Sampling on a line by line basis, that is using the CDSR signal to reset a line of pixels without advancing the VSR. The image capture part of the double read is exactly as described above, and all setup times and durations other than CDSR specific times are also identical.

See: **OPERATING MODES - CORRELATED DOUBLE SAMPLING** for full details.



Line Timings for reading pixel data and the black offset data using the CDSR signal.

Description	#t	PCK Cycles	Time (us)
SELRef [R] - Start of Line	c0	0	0
Image Line data (exactly as single image capture)	c1	1023	204.6
CDSR [R]	c21	1028	205.6
CDSR [F]	c22	1053	210.6
PXRD [R]	c23	1058	211.6
COLsam [R}	c24	1059	211.8
COLsam [F}	c25	1254	250.8
EC [R]	c26	1257	251.4
LS [R] (even pixels, dark offsets)	c27	1258	251.6
LS [F] (even pixels, dark offsets)	c28	1262	252.4
AVO valid, dark offsets even pixels, start	c29	1262.5	252.5
AVO valid, dark offsets even pixels, end	c30	1662.5	332.5
EC [F]	c31	1664	332.8
LS [R] (odd pixels)	c32	1665	333.0
LS [F] (odd pixels	c33	1669	333.8
AVO valid, odd pixels, start	c34	1669.5	333.9
AVO valid, odd pixels, end	c35	2069.5	413.9
PXRD [F]	c36	2071	414.2
End of line	c37	2072	414.4
Line Length	c37 - c0	2072	414.4
CDSR Setup Times			
LS (F) - First Valid Pixel	c13 - c12 (etc.)	0.5	0.1
Valid exposed pixels - even - odd	c14 - c13 c19 - c18	400	80.0
Valid reset pixels - even - odd	c30 - c29 c35 - c34	400	80.0
CDSR [H] Duration	c22 - c21	25	5.0
NOTE: For CINE mode the Valid pixels is reduced from 400 to 200, giving a reduction in Line time from 2072 to 1272 PCK's, all other relative timings remain unchanged			

Recommended Line timings Using CDSR

SPECIFICATIONS

Absolute Maximum Ratings

Parameter	Value
Supply Voltage	-0.5 to +7.0 volts
Voltage on other input pins	-0.5 to V_{DD} + 0.5 volts
Temperature under bias	-15^{O}C to 85^{O}C
Storage Temperature	-30^{O}C to 125^{O}C
Maximum DC TTL output Current Magnitude	10mA (per o/p, one at a time, 1sec. duration)

Note: Stresses exceeding the Absolute Maximum Ratings may induce failure. Exposure to absolute maximum ratings for extended periods may reduce reliability. Functionality at or above these conditions is not implied.

DC Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Units	Notes
V_{DD}	Operating supply voltage	4.75	5.0	5.25	V	
I_{DD}	Overall supply current		35		mA	1
V_{IH}	Input Voltage Logic “1”	2.4		V_{DD}+0.5	V	
V_{IL}	Input Voltage Logic “0”	-0.5		0.5	V	
V_{OH}	Output Voltage Logic “1”	V_{DD}-0.5			V	I=1mA
V_{OL}	Output Voltage Logic “0”			0.5	V	I=1mA
I_{ILK}	Input Leakage current	-1			µA	V_{IH} on input
				1	µA	V_{IL} on input
C_{load}	Digital Input Cap. Load		10		pF	

Note 1.Digital and Analogue outputs unloaded.

AC Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Units	Notes
PCK	Pixel Clock frequency		5	10	MHz	1
DCK	Serial Data Clock			100	KHz	2

Note 1. Recommended clock rate for 0.1% settling of AVO is 5.0MHz.
Note 2. Serial Interface clock must be generated by host processor.

Electrical Characteristics

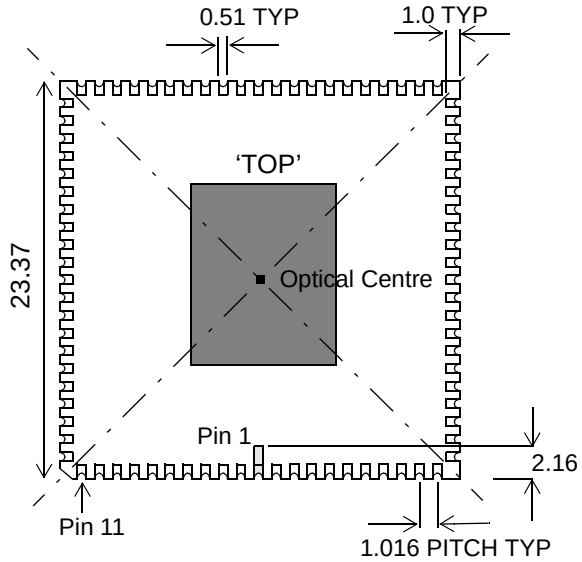
Symbol	Parameter	Min.	Typ.	Max.	Units	Notes
VRTref	Internal reference for VRT	2.85	3.0	3.15	V	Unbuffered
VBLOOMref	Internal reference for VBLOOM	1.90	2.0	2.10	V	Unbuffered
VBLTWref	Internal reference for VBLTW	1.35	1.50	1.65	V	Unbuffered
V_{BG}	Internal bandgap reference	1.15	1.23	1.30	V	Decouple with 0.1µF
VCL1,2	Video Output Clamp Voltages	1.30		2.30	V	An. Inputs
V_{DAC}	5-Bit DAC Output	1.76		2.08	V	For VCL1 or 2
R_{SET}	Resistor to set DAC bias current	-5%	12K	+5%	Ohms	
I_{VRT}	Load Current on VRT	1.5	2.5	4.0	mA	Buffered from VRTref

Typical conditions, V_{DD} = 5.0 V, T_A = 25^{o}C

Video Output Characteristics

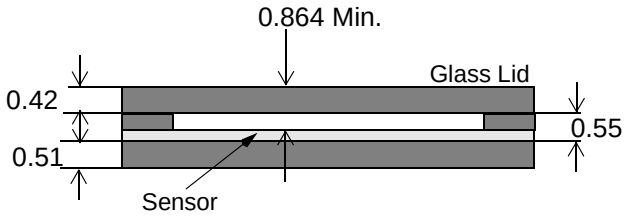
Symbol	Parameter	Min.	Typical	Max.	Units
V_{black}	AVO Black Level	VCL1-30mV	VCL1	VCL1+30mV	V
V_{white}	AVO Peak White	-	V_{black}-1.0V	-	V
	Pixel Reset to Pixel Reset	-0.125	0	0.125	V
AVORef	Pseudo-Diff. AVO Reference	VCL2-30mV	VCL2	VCL2+30mV	V
I_{AVO}	AVO output current	-2mA		4mA	mA
F_{AVO}	AVO bandwidth		33MHz		
C_{AVO}	AVO, AVOref Capacitive Loading			30	pF
R_{AVO}	AVO, AVOref Resistive loading			20K	Ohms

PACKAGE DETAILS



Viewed from below

Standard 84 Pin LCC

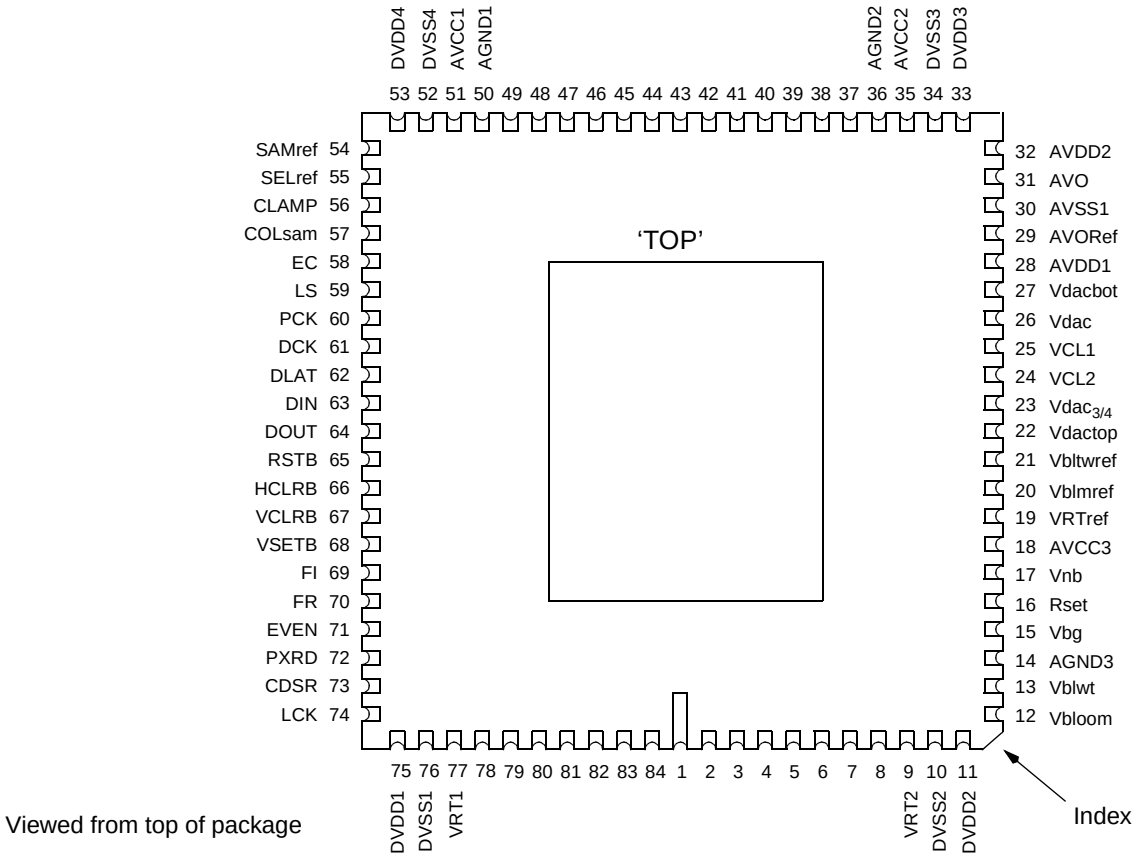


The optical array is centred within the package to a tolerance of +/- 0.2 mm, and rotated no more than +/- 0.5^{o}

Tolerances on package dimensions +/-0.2

All dimensions in millimetres

Pinout



Viewed from top of package

Pin List

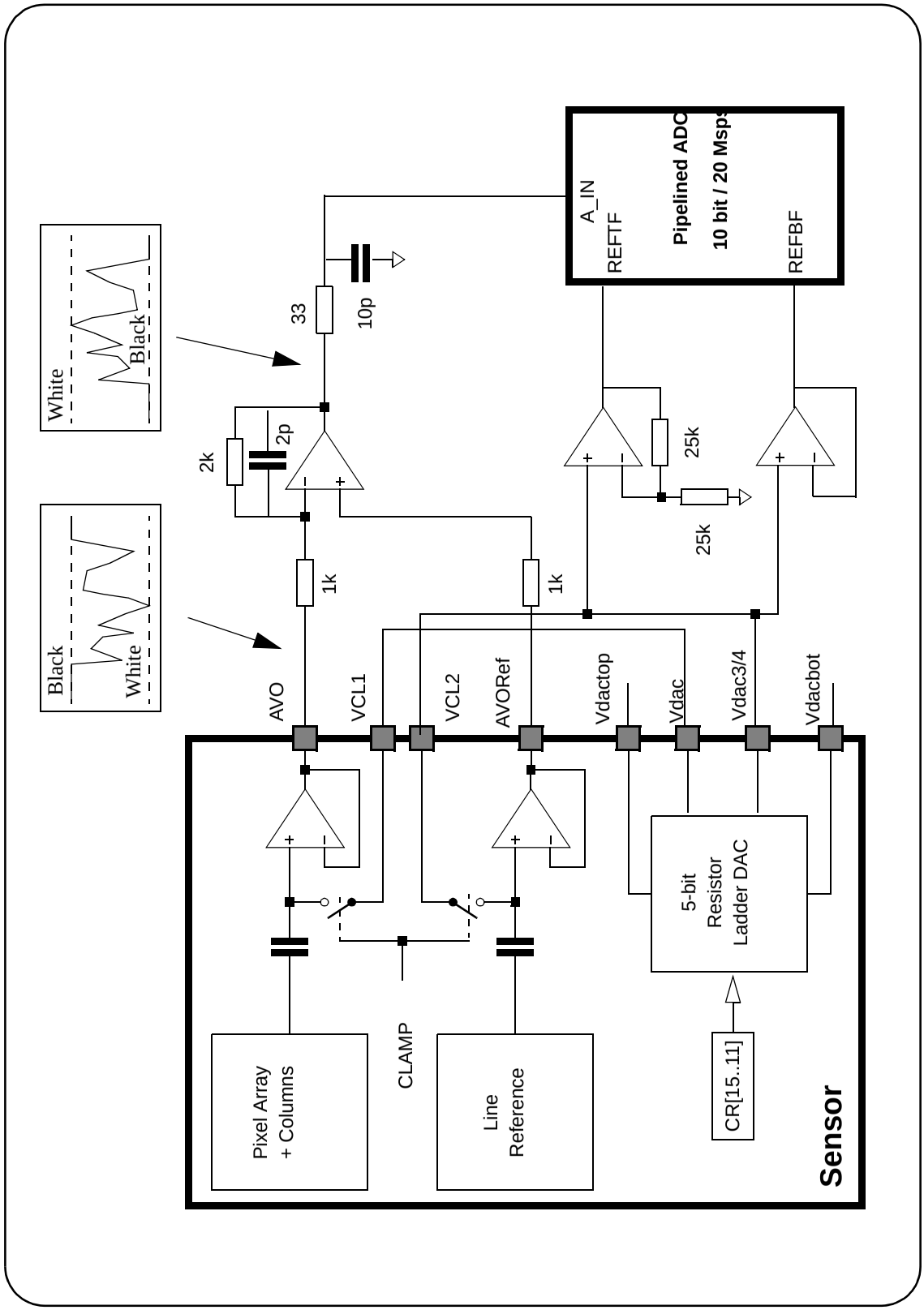
Pin	Name	Type	Function/Comment
POWER SUPPLIES			
51, 35, 18	AVCC1-3	PWR	5V supply for the Column Source Followers.
50,36, 14	AGND1-3	GND	Ground for the Substrate and the Column Source Followers.
28, 32	AVDD1,2	PWR	5V supply for the Output Stage.
30	AVSS1	GND	Ground supply for the Output Stage.
75, 11	DVDD1,2	PWR	5V supply for Vertical Shift Registers
76, 10	DVSS1,2	GND	Ground for Vertical Shift Registers
33	DVDD3	PWR	5V supply for Output Muxing.
34	DVSS3	GND	Ground for Output Muxing.
53	DVDD4	PWR	5V supply for Horizontal Shift Register.
52	DVSS4	GND	Ground for Horizontal Shift Register.
POWER-ON-RESET			
65	RSTB	OD	Output of internal power-on-reset cell. Should be applied to HCLRB and VCLRB at power up.
ANALOGUE VOLTAGE REFERENCES			
77, 9	VRT1,2	IA	Pixel Reset Voltage and Power Supply.
12	Vbloom	IA	Anti-blooming pixel reset voltage.
13	Vbltw	IA	Defines white level for the Bitline test.
19	VRTref	OA	Unbuffered Internally generated Reference for VRT
20	Vblmref	OA	Unbuffered Internally generated Reference for Vbloom
21	Vbltwref	OA	Unbuffered Internally generated Reference for Vbltw.
15	Vbg	OA	Internal bandgap voltage reference (1.22 V); decouple with 10nF
17	Vnb	IA	Decoupling (10nF) for internally generated bias current
16	Rset	IA	Sets internal master bias current; connect to AGND via 12K Res.
25	VCL1	IA	AC Clamp Voltage for AVO output.
26	VCL2	IA	AC Clamp Voltage for AVORef output.
ANALOGUE OUTPUT STAGE			
31	AVO	OA	Buffered analogue video output; Inverted - low = white
29	AVORef	OA	Buffered black level voltage reference.
55	SELRef	ID	SELRef=0 - Selects sensor output (video) at AVO. SELRef=1 - Selects ‘Line Reference’
54	SAMRef	ID	Samples the ‘Line Reference’ from VRT
56	CLAMP	ID	Controls AC Clamping circuit in output stage.

Pin	Name	Type	Function/Comment
RESET AND READ VERTICAL SHIFT REGISTERS (VSR)			
74	LCK	ID	Line clock input for Reset and Read Vertical Shift Registers
71	EVEN	ID	ODD/EVEN Line Clock.
72	PXRD	ID	Pixel Read: Control input to read a row of pixel voltages.
73	CDSR	ID↓	Correlated Double Sampling: Control input to allow the row of pixels currently being read to be reset without advancing the reset VSR.
67	VCLRB	ID↑	Clear Reset and Read VSR's.
68	VSETB	ID↑	Preset the Reset VSR to all ones. The Read VSR is not preset.
69	FI	ID	Field Integrate: Resets VSR. High duration sets exposure time.
70	FR	ID	Field Read: Reads VSR. Starts field read out.
HORIZONTAL SHIFT REGISTER (HSR)			
60	PCK	ID	Pixel clock
66	HCLRB	ID↑	Clear Horizontal Shift Register
59	LS	ID	Line Start: Starts horizontal scan/pixel output.
58	EC	ID	ODD/EVER Column Select.
57	COLsam	ID	Sample the Column Source Follower Inputs (pixel row).
SERIAL DATA INTERFACE (SDI)			
63	DIN	ID↓	Serial Data Input
64	DOUT	OD	Serial Data Output
62	DLAT	ID↓	Latch Serial Data into Control Register
61	DCK	ID↓	Serial Data Clock Must be generated by host.
5-BIT RESISTIVE LADDER DAC			
22	Vdactop	IA	Voltage reference for the top of the resistive ladder
23	Vdac3/4	OA	Three-Quarter-point of the resistive ladder (Unbuffered)
27	Vdacbot	IA	Voltage reference for the bottom of the resistive ladder
26	Vdac	OA	DAC Output Voltage (Unbuffered)

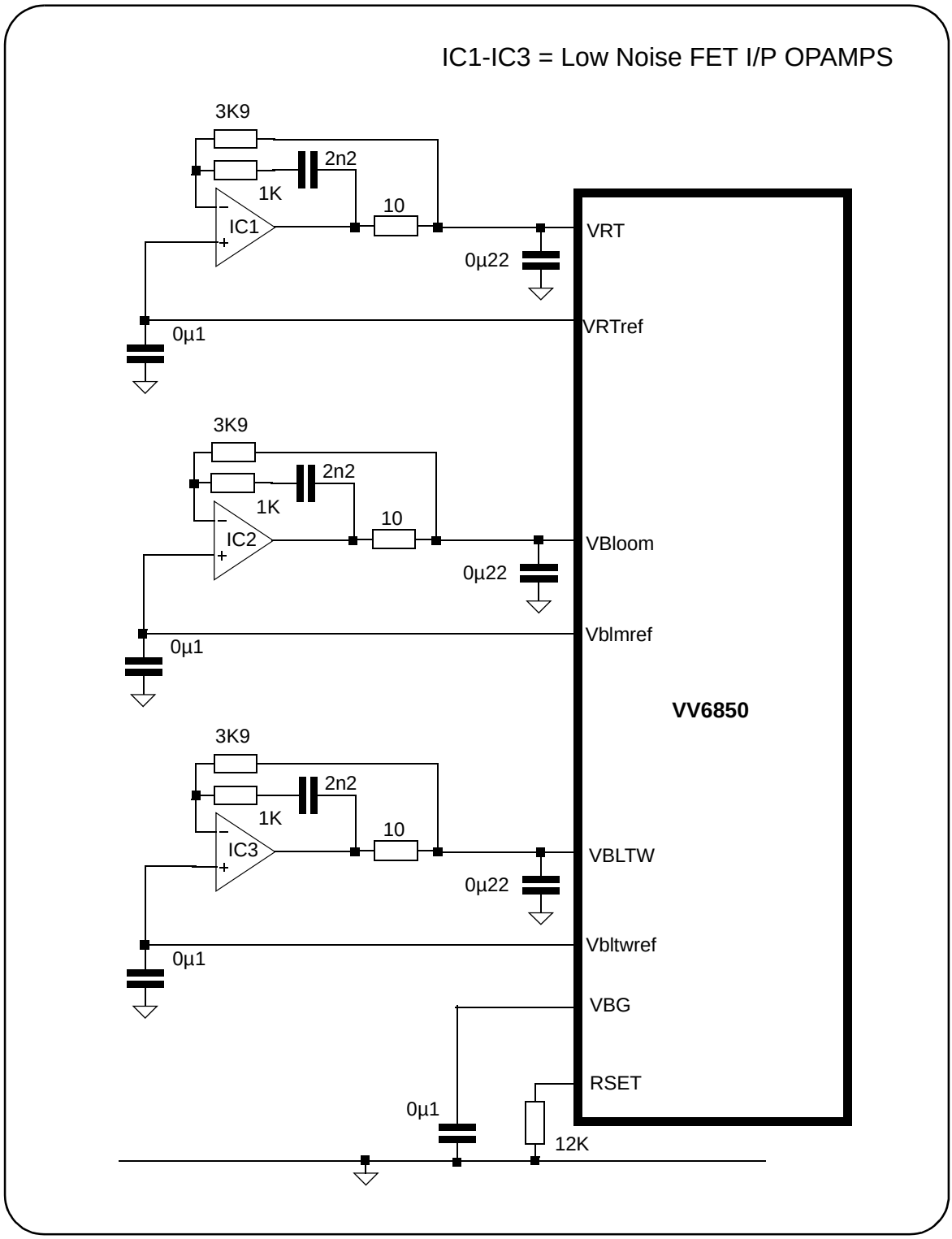
Key:

OA	Analogue output pad	ID	Digital input
IA	Analogue input pad	ID↑	Digital input with internal pull-up
OD	Digital output pad	OD↓	Digital output with internal pull-down

ADC INTERFACE CIRCUIT



ANALOGUE REFERENCE BUFFERING



APPENDIX A - FPN CANCELLATION SCHEMES

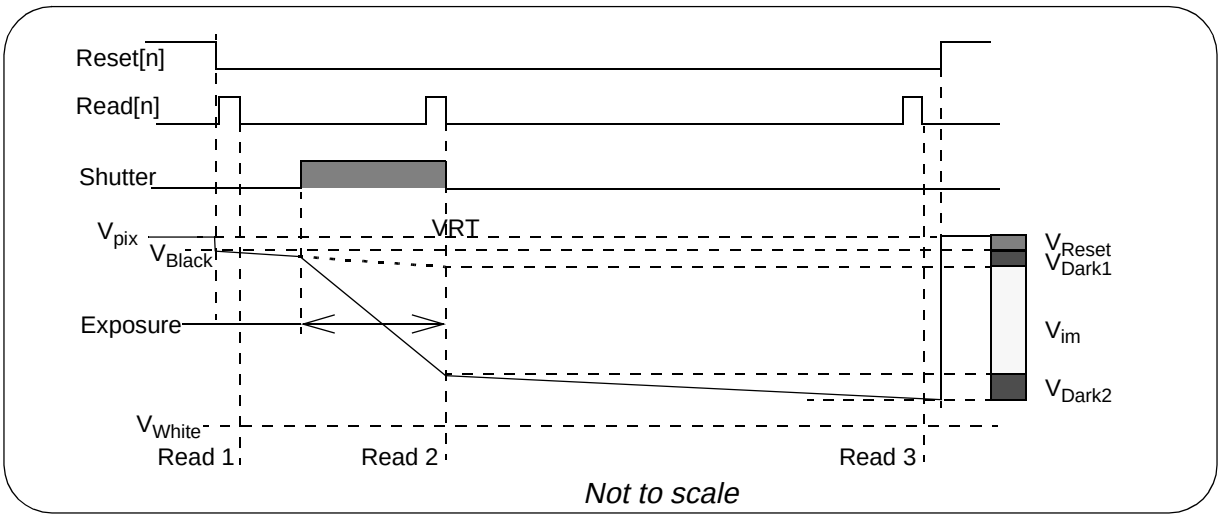
There are many possible ways achieve FPN cancellation in order to produce the highest quality stills images from the VV6850 sensor. The exact method chosen will depend on the intended use of the imager system, and the ancillary devices available in the system, such as the frame buffer and mechanical shutter typical of a Digital Stills Camera. A number of schemes are discussed.

Multiple Dark Current Periods

The basic FPN cancellation scheme outlined in **OPERATING MODES - STILL IMAGE CAPTURE** can be modified in many ways to suit a particular application. One such variation might be to extend the post image exposure 'dark image' capture period to some integral multiple of the image exposure period, in order to obtain a more accurate assessment of the dark current FPN:

1. With the shutter closed, release the sensor from reset and immediately read a frame into buffer 'A' memory; this captures the array threshold FPN and reset noise ('V_{Reset}')
2. Open the shutter and expose the sensor to the required scene
3. Close the shutter and immediately read the array; as each pixel is read, subtract the value for that position stored in the frame buffer to obtain the image plus dark current FPN (V_{im}+V_{Dark1}) value; store this value in *second* frame buffer, 'B'
4. After a further (say) four frame periods, read the array again; as each pixel is read, subtract the reset value for that position as stored in the 'A' frame buffer, and overwrite the position, leaving the V_{im} + V_{Dark1} + V_{Dark2} value in the buffer
5. For each pixel, subtract the value in 'B' from that in 'A' to give V_{Dark2} dark current value, which is equivalent to four times the V_{Dark1} value
6. Divide the V_{Dark2} values in 'A' by 4, then subtract them from the (V_{im} + V_{Dark1}) values in 'B' and store the result, which is the V_{im} image data

The frame buffer now contains the corrected image values, which can be transferred to image storage memory. This scheme is illustrated below:



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