

**VPS13**

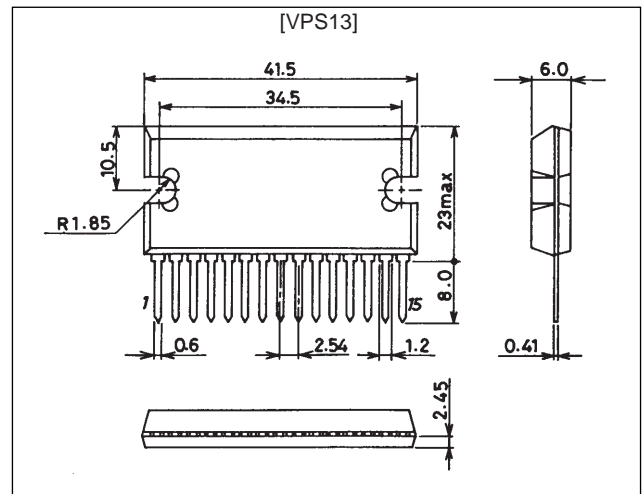
## CRT Display Video Output Amplifier, High-Voltage/Wideband Amplifier

### Features

- High output voltage and wide bandwidth; optimal for use in  $f_H$  (horizontal deflection frequency) = 100 kHz class monitors.  
( $f = 130$  MHz  $-3$  dB at  $V_{OUT} = 40$  V<sub>p-p</sub>)
- SIP molded 15-pin package houses three amplifier channels.

### Package Dimensions

unit: mm

**2127A**

### Specifications

#### Absolute Maximum Ratings at $T_a = 25^\circ\text{C}$

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	$V_{CC}$ max		90	V
	$V_{BB}$ max		15	V
Allowable power dissipation	$P_d$ max	With an ideal heat sink at $T_c = 25^\circ\text{C}$	30	W
Maximum junction temperature	$T_j$ max		150	$^\circ\text{C}$
Maximum case temperature	$T_c$ max		100	$^\circ\text{C}$
Storage temperature	$T_{stg}$		-20 to +110	$^\circ\text{C}$

#### Operating Conditions at $T_a = 25^\circ\text{C}$

Parameter	Symbol	Conditions	Ratings	Unit
Recommended supply voltage	$V_{CC}$		80	V
	$V_{BB}$		10	V

#### Electrical Characteristics at $T_a = 25^\circ\text{C}$ (for a single channel)

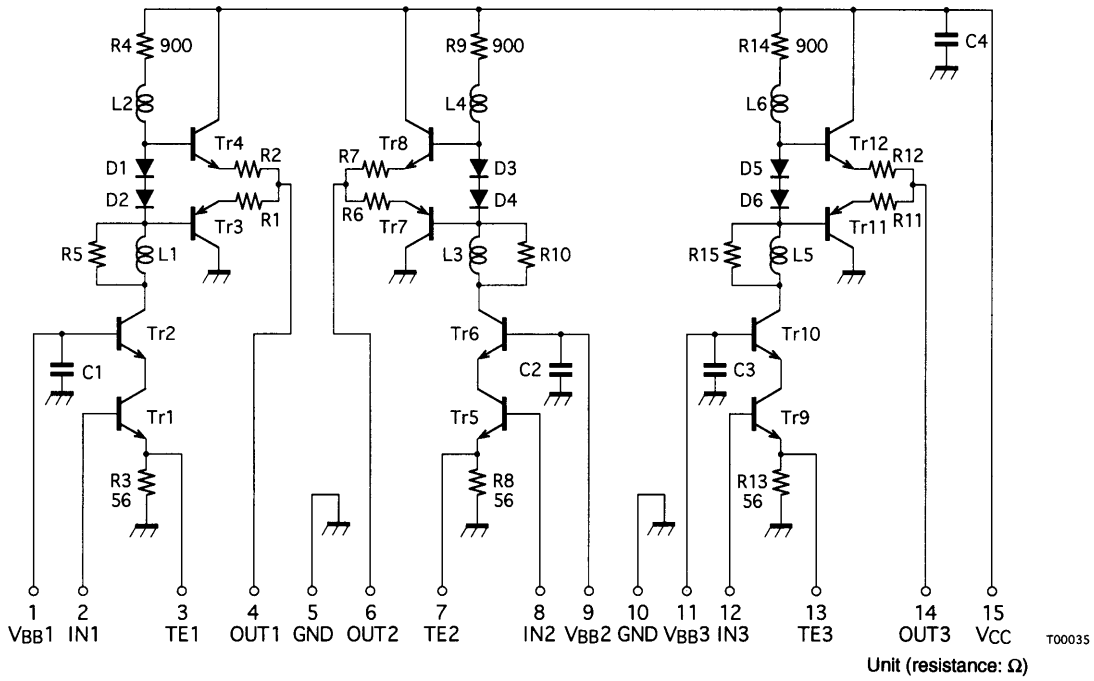
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Frequency band ( $-3$ dB)	$f_c$	$V_{CC} = 80$ V, $V_{BB} = 10$ V, $C_L = 10$ pF $V_{IN}$ (DC) = 3.2 V, $V_{OUT}$ (p-p) = 40 V		130		MHz
Impulse response	$t_r$	$V_{CC} = 80$ V, $V_{BB} = 10$ V, $C_L = 10$ pF		3.5		ns
	$t_f$	$V_{IN}$ (DC) = 3.2 V, $V_{OUT}$ (p-p) = 40 V		2.9		ns
Voltage gain	VG (DC)		13	15	17	double
Current drain	$I_{CC}(1)$	$V_{CC} = 80$ V, $V_{BB} = 10$ V, $V_{IN}$ (DC) = 2.9 V, $f = 10$ MHz clock, $C_L = 10$ pF, $V_{OUT}$ (p-p) = 40 V		47		mA
	$I_{CC}(2)$	$V_{CC} = 80$ V, $V_{BB} = 10$ V, $V_{IN}$ (DC) = 2.9 V, $f = 130$ MHz clock, $C_L = 10$ pF, $V_{OUT}$ (p-p) = 40 V		85		mA

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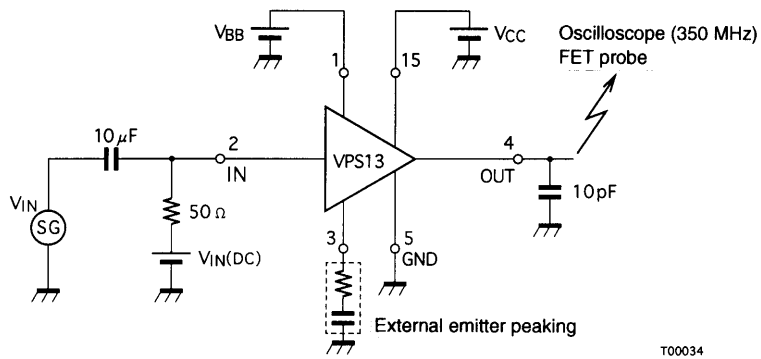
TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110 JAPAN

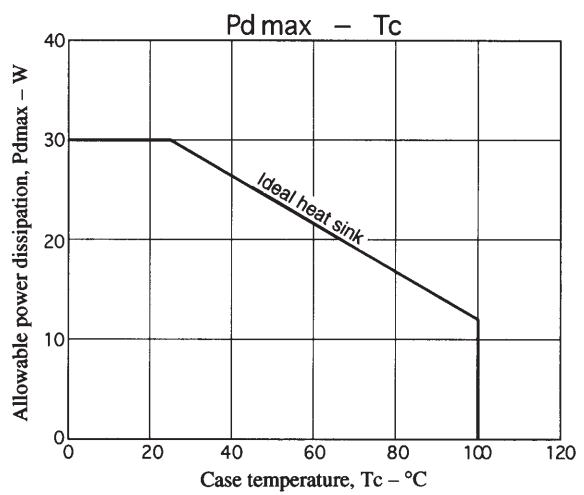
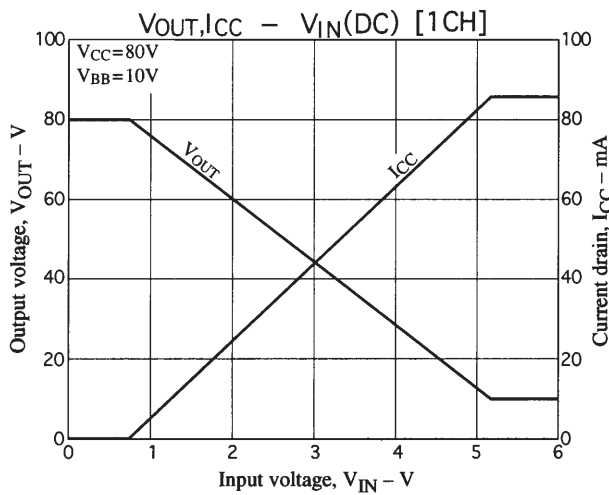
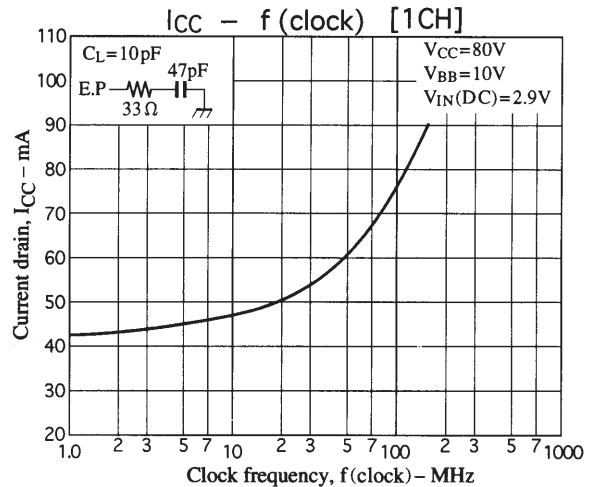
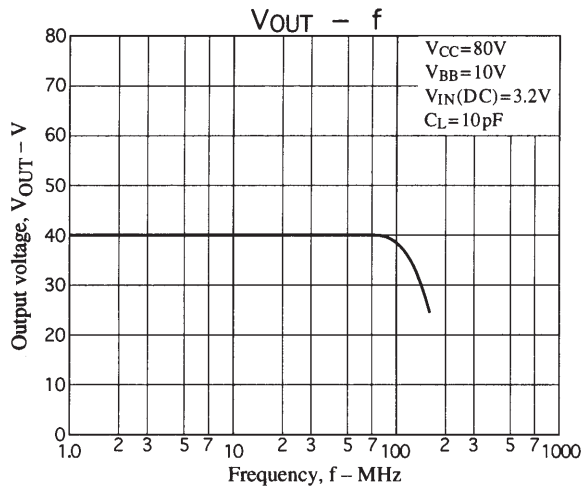
# VPS13

## Internal Equivalent Circuit



## Test Circuit (for a single channel)





**Thermal Design**

Since the VPS13 includes three channels as shown in the circuit diagram on page 2, we first consider a single channel. The chip temperature of each transistor under actual operating conditions is determined using the following formula.

$$T_j = (T_{ri}) = \theta_{j-c} (T_{ri}) \times P_c (T_{ri}) + \Delta T_c + T_a \text{ (}^\circ\text{C)} \dots\dots\dots(1)$$

$\theta_{j-c} (T_{ri})$  : Thermal resistance of an individual transistor

$P_c(T_{ri})$  : Collector loss for an individual transistor

$\Delta T_c$  : Case temperature rise

$T_a$  : Ambient temperature

The  $\theta_{j-c} (T_{ri})$  for each chip is:  $\theta_{j-c} (Tr1) = 35^\circ\text{C/W}$

$$\theta_{j-c} (Tr2) \text{ to } (Tr4) = 30^\circ\text{C/W} \dots\dots\dots(2)$$

Although the loss for each transistor in a video pack varies with frequency and is not uniform, if we assume the maximum operating frequency,  $f = 130 \text{ MHz}$  (clock), then the chip with the largest loss will be transistor 3 ( $Tr3$ ) of the emitter-follower stage. From the  $P_d - f$  (clock) figure we see that loss will be 22% of the total loss for a single channel:

$$P_c (\text{emitter-follower stage})_{(f=130 \text{ MHz})} = P_d (1ch)_{(f=130 \text{ MHz})} \times 0.22 \text{ [W]} \quad (3)$$

Here, we must select a heat sink with a capacity  $\theta_h$  such that the  $T_j$  of these transistors does not exceed  $150^\circ\text{C}$ . Equation (4) below gives the relationship between  $\theta_h$  and  $\Delta T_c$ .

$$\Delta T_c = P_d (\text{Total}) \times \theta_h \dots\dots\dots(4)$$

The required  $\theta_h$  is calculated using this equation and equation (1).

**VPS13 Thermal Design Example**

Conditions: Using an  $f_H = 100$  kHz class monitor,  $f_V = 130$  MHz (clock)

$$V_{CC} = 80 \text{ V}, V_{BB} = 10 \text{ V}, V_{OUT} = 40 \text{ V}_{p-p} (C_L = 10 \text{ pF})$$

Here we consider the case where this class of monitor is operated up to  $T_a = 60^\circ\text{C}$  at a maximum clock frequency of  $f = 130$  MHz.

As mentioned previously, the chip with the largest loss is transistor 3 (Tr3) of the emitter-follower stage. Determining that value gives:

$$P_c (\text{emitter-follower stage}) = 6.8 \times 0.22 \approx 1.5 \text{ [W]} \dots\dots\dots(5)$$

Now, determine  $\Delta T_j$  by substituting the value for  $\theta_{j-c}$  in equation (5).

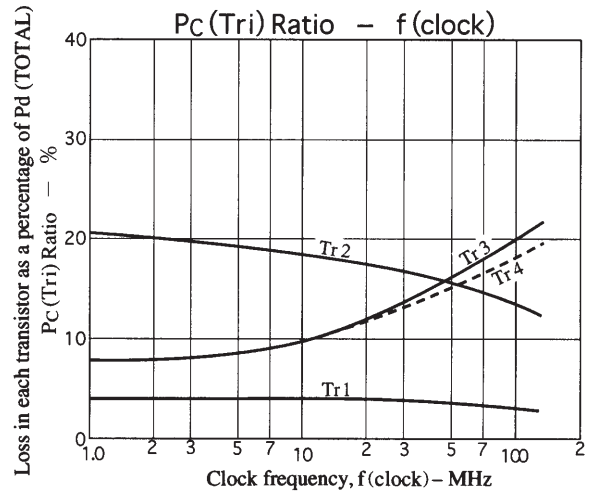
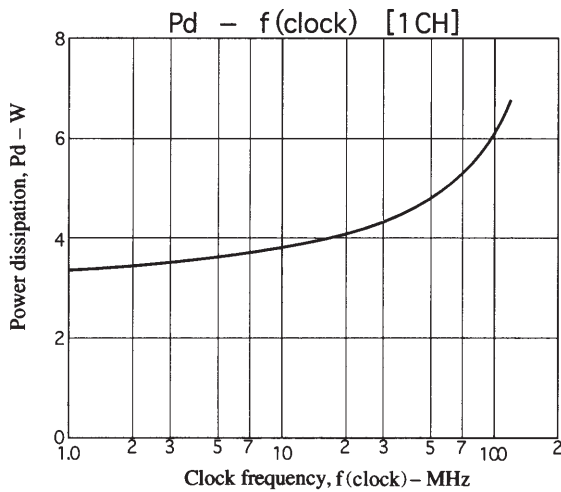
$$\Delta T_j = 1.5 \times 30 = 45 \text{ [}^\circ\text{C]}$$

Here,  $\Delta T_j < 50^\circ\text{C}$ , and we need only consider cases where  $T_c < 100^\circ\text{C}$ . Therefore, we must design a  $\theta_h$  for the heat sink such that the  $T_c < 100^\circ\text{C}$  condition holds when three channels are operating at maximum levels, i.e.,  $P_d(\text{TOTAL}) = P_d(\text{one channel}) \times 3$ .

$\Delta T_c$  will be  $100 - 60 = 40^\circ\text{C}$ , and therefore:

$$\theta_h = \Delta T_c \div P_d (\text{TOTAL}) = 40 \div (6.8 \times 3) = 2.0, \text{ i.e. } \theta_h = 2.0 \text{ }^\circ\text{C/W}$$

In actual practice, the ambient temperature and operating conditions will allow a heat sink smaller than that indicated by this calculation to be used. Therefore, design optimization taking the actual conditions and the above data into account is also required.



$V_{CC}$ (V)	$V_{BB}$ (V)	$V_{OUT}$ (V)	$V_O$ (center)
80	10	40	45

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