PRELIMINARY DATA SHEET

VPC 3205C,
VPC 3215C
Video Processor Family

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Video Processor Family

Release Note: Revision bars indicate significant changes to the previous edition.

1. Introduction

The VPC 32x5 is a high-quality, single-chip video front-end, which is targeted for 4:3 and 16:9, 50/60 and 100/120 Hz TV sets. It can be combined with other members of the DIGIT3000 IC family (such as CIP 3250A, DDP 3300A, TPU 3040) and/or it can be used with 3rd-party products.

The main features of the VPC 32x5 are

- all-digital video processing
- high-performance adaptive 4H comb filter Y/C separator with adjustable vertical peaking
- multi-standard color decoder PAL/NTSC/SECAM including all substandards
- 4 composite, 1 S-VHS input, 1 composite output
- integrated high-quality A/D converters and associated clamp and AGC circuits
- multi-standard sync processing
- linear horizontal scaling (0.25 ... 4), as well as non-linear horizontal scaling ‘panorama vision’
- PAL+ preprocessing (VPC 3215)
- line-locked clock, data and sync output (VPC 3215)
- display/deflection control (VPC 3205)
- submicron CMOS technology
- I^2C-Bus Interface
- one 20.25 MHz crystal, few external components
- 68-pin PLCC package

1.1. System Architecture

Fig. 1–1 shows the block diagram of the video processor.

1.2. Video Processor Family

The VPC video processor family supports 15/32 kHz systems and is available with different comb filter options. The 50 Hz/single scan versions provide controlling for the display and the vertical/east west deflection of DDP 3300A. The 100 Hz/double scan versions have a line-locked clock output interface and the PAL+ preprocessing option. Table 1–1 gives an overview of the VPC video processor family.

Table 1–1: VPC Processor Family

Features	50 Hz/ single scan	100 Hz/ double scan
4H comb filter	VPC 32**05C**	VPC 32**15C**
2H comb filter	VPC 32**00A**	VPC 32**10A**
no comb filter	VPC 32**01A**	VPC 32**11A**

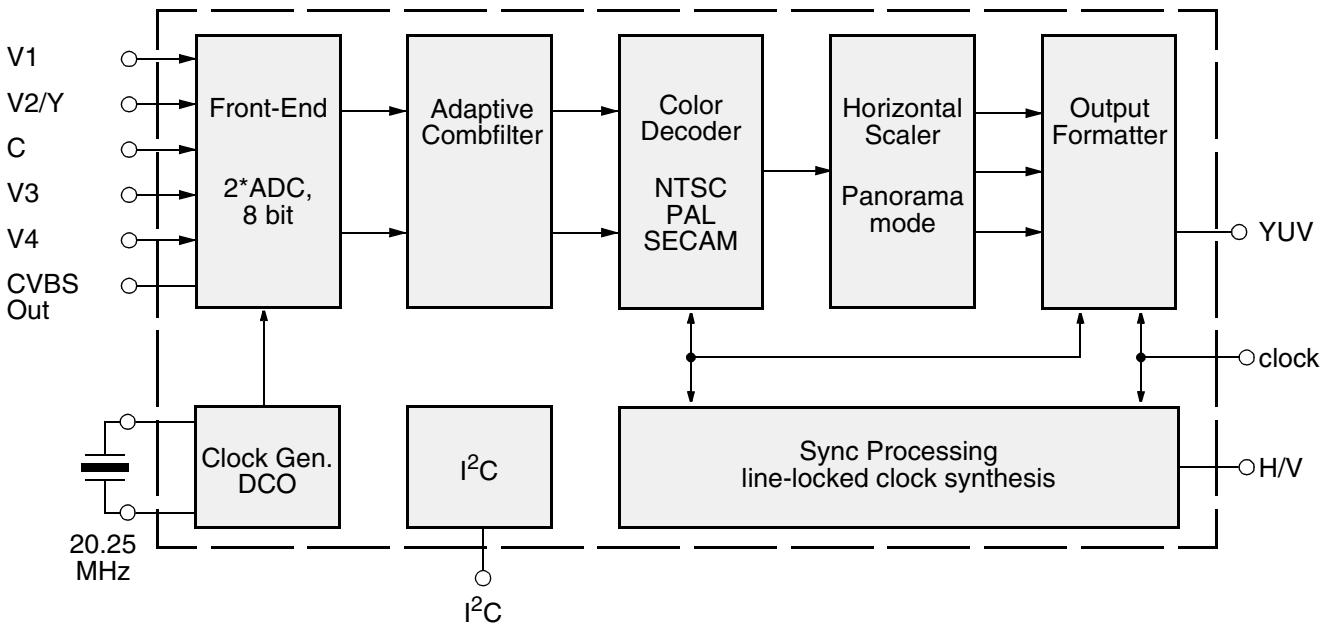


Fig. 1–1: VPC 32x5C block diagram

1.3. VPC Applications

Fig. 1–2 depicts several VPC applications. Since the VPC functions as a video front-end, it must be complemented with additional functionality to form a complete TV set.

The DDP 33x0 contains the video back-end with video postprocessing (contrast, peaking, DTI,...), H/V-deflection, RGB insertion (SCART, Text, PIP,...) and tube control (cutoff, white drive, beam current limiter). It generates a beam scan velocity modulation output from the digital YC_rC_b and RGB signals. Note that this signal is not generated from the external analog RGB inputs.

The CIP 3250A provides a high quality analog RGB interface with character insertion capability. This allows appropriate processing of external sources, such as MPEG2 set-top boxes in transparent (4:2:2) quality. Furthermore, it translates RGB/Fastblank signals to the common digital video bus and makes those signals available for 100 Hz upconversion or double scan processing. In some European countries (Italy), this feature is mandatory.

The IP indicates memory based image processing, such as scan rate conversion, vertical processing (Zoom), or PAL+ reconstruction.
Examples:

– Europe: 15 kHz/50 Hz → 32 kHz/100 Hz interlaced

– US: 15 kHz/60 Hz → 32 kHz/60 Hz non-interlaced

Note that the VPC supports memory based applications through line-locked clocks, syncs, and data. CIP may run either with the native DIGIT3000 clock but also with a line-locked clock system.

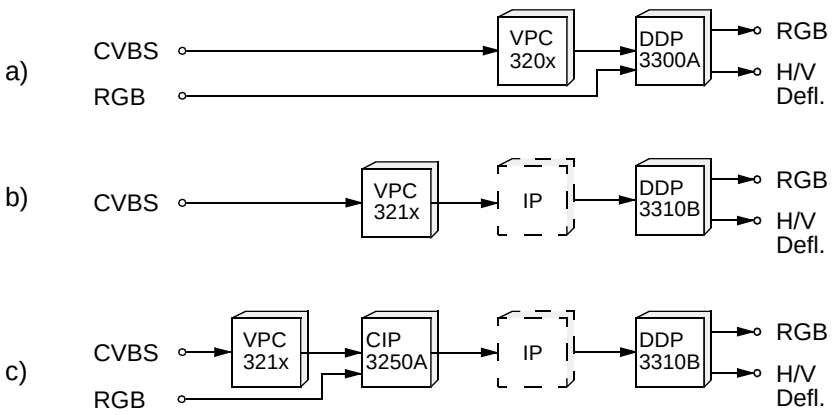


Fig. 1–2: VPC 32xx applications
a) 15 kHz application Europe
b) double scan application (US, Japan)
c) 100 Hz application (Europe) with RGB inputs

2. Functional Description

2.1. Analog Front-End

This block provides the analog interfaces to all video inputs and mainly carries out analog-to digital conversion for the following digital video processing. A block diagram is given in Fig. 2–1.

Most of the functional blocks in the front-end are digitally controlled (clamping, AGC, and clock-DCO). The control loops are closed by the Fast Processor (‘FP’) embedded in the decoder.

2.1.1. Input Selector

Up to five analog inputs can be connected. Four inputs are for input of composite video or S-VHS luma signal. These inputs are clamped to the sync back porch and are amplified by a variable gain amplifier. One input is for connection of S-VHS carrier-chrominance signal. This input is internally biased and has a fixed gain amplifier.

2.1.2. Clamping

The composite video input signals are AC coupled to the IC. The clamping voltage is stored on the coupling capacitors and is generated by digitally controlled current sources. The clamping level is the back porch of the video signal. S-VHS chroma is also AC coupled. The input pin is internally biased to the center of the ADC input range.

2.1.3. Automatic Gain Control

A digitally working automatic gain control adjusts the magnitude of the selected baseband by +6/–4.5 dB in 64 logarithmic steps to the optimal range of the ADC. The gain of the video input stage including the ADC is 213 steps/V with the AGC set to 0 dB.

2.1.4. Analog-to-Digital Converters

Two ADCs are provided to digitize the input signals. Each converter runs with 20.25 MHz and has 8 bit resolution. An integrated bandgap circuit generates the required reference voltages for the converters. The two ADCs are of a 2-stage subranging type.

2.1.5. Digitally Controlled Clock Oscillator

The clock generation is also a part of the analog front end. The crystal oscillator is controlled digitally by the control processor; the clock frequency can be adjusted within ±150 ppm.

2.1.6. Analog Video Output

The input signal of the Luma ADC is available at the analog video output pin. The signal at this pin must be buffered by a source follower. The output voltage is 2 V, thus the signal can be used to drive a 75 Ω line. The magnitude is adjusted with an AGC in 8 steps together with the main AGC.

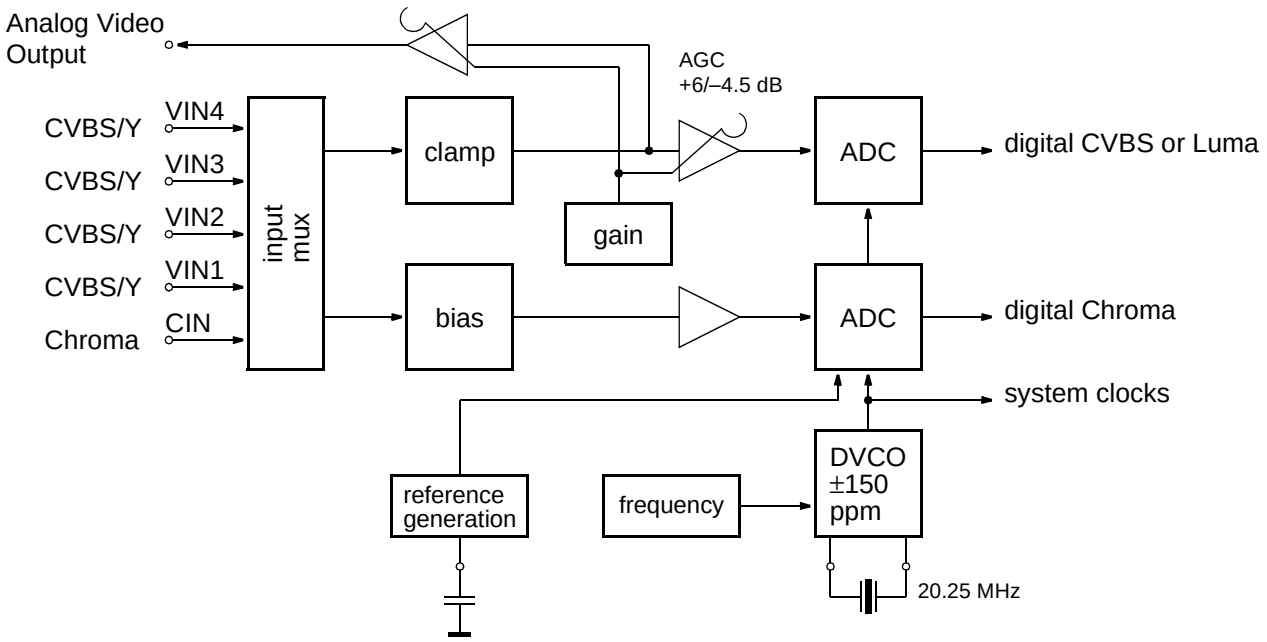


Fig. 2–1: Analog front-end

2.2. Adaptive Comb Filter

The 4H adaptive comb filter is used for high-quality luminance/chrominance separation for PAL or NTSC composite video signals. The comb filter improves the luminance resolution (bandwidth) and reduces interferences like cross-luminance and cross-color. The adaptive algorithm eliminates most of the mentioned errors without introducing new artifacts or noise.

A block diagram of the comb filter is shown in Fig. 2–2. The filter uses four line delays to process the information of three video lines. To have a fixed phase relationship of the color subcarrier in the three channels, the system clock (20.25 MHz) is fractionally locked to the color subcarrier. This allows the processing of all color standards and substandards using a single crystal frequency.

The CVBS signal in the three channels is filtered at the subcarrier frequency by a set of bandpass/notch filters. The output of the three channels is used by the adaption logic to select the weighting that is used to reconstruct the luminance/chrominance signal from the 4 bandpass/notch filter signals. By using soft mixing of the 4 signals switching artifacts of the adaption algorithm are completely suppressed.

The comb filter uses the middle line as reference, therefore, the comb filter delay is two lines. If the comb filter is switched off, the delay lines are used to pass the luma/chroma signals from the A/D converters to the luma/chroma outputs. Thus, the processing delay is always two lines.

In order to obtain the best-suited picture quality , the user has the possibility to influence the behaviour of the adaption algorithm going from moderate combing to strong combing. Therfore, the following three parameters may be adjusted:

– HDG (horizontal difference gain)
– VDG (vertical difference gain)
– DDR (diagonal dot reducer)

HDG typically defines the comb strength on horizontal edges. It determines the amount of the remaining cross-luminance and the sharpness on edges respectively. As HDG increases, the comb strength, e. g. cross luminance reduction and sharpness, increases.

VDG typically determines the comb filter behaviour on vertical edges. As VDG increases, the comb strength, e. g. the amount of hanging dots, decreases.

After selecting the combfilter performance in horizontal and vertical direction, the diagonal picture performance may further be optimized by adjusting DDR. As DDR increases, the dot crawl on diagonal colored edges is reduced.

To enhance the vertical resolution of the the picture, the VPC 32x5 provides a vertical peaking circuitry. The filter gain is adjustable between 0 – +6 dB and a coring filter suppresses small amplitudes to reduce noise artifacts. In relation to the comb filter, this vertical peaking widely contributes to an optimal two-dimensional resolution homogeneity.

2.3. Color Decoder

In this block, the standard luma/chroma separation and multi-standard color demodulation is carried out. The color demodulation uses an asynchronous clock, thus allowing a unified architecture for all color standards.

A block diagram of the color decoder is shown in Fig. 2–4. The luma as well as the chroma processing, is shown here. The color decoder also provides several special modes, e.g. wide band chroma format which is intended for S-VHS wide bandwidth chroma. Also, filter settings are available for processing a PAL+ helper signal.

If the adaptive comb filter is used for luma chroma separation, the color decoder uses the S-VHS mode processing. The output of the color decoder is YC_rC_b in a 4:2:2 format.

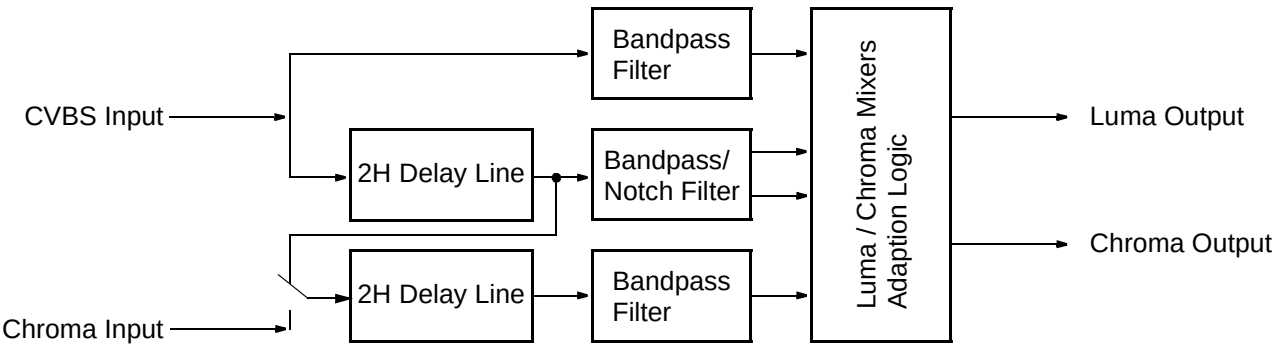


Fig. 2–2: Block diagram of the adaptive comb filter (PAL mode)

2.3.1. IF-Compensation

With off-air or mistuned reception, any attenuation at higher frequencies or asymmetry around the color subcarrier is compensated. Four different settings of the IF-compensation are possible (see Fig. 2–3):

– flat (no compensation)

– 6 dB/octave

– 12 dB/octave

– 10 dB/MHz

The last setting gives a very large boost to high frequencies. It is provided for SECAM signals that are decoded using a SAW filter specified originally for the PAL standard.

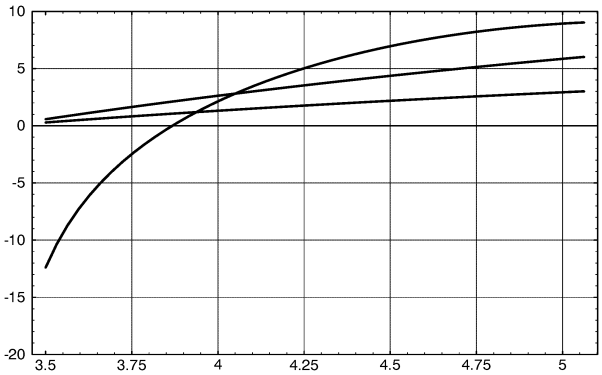


Fig. 2–3: Frequency response of chroma IF-compensation

2.3.2. Demodulator

The entire signal (which might still contain luma) is quadrature-mixed to the baseband. The mixing frequency is equal to the subcarrier for PAL and NTSC, thus achieving the chroma demodulation. For SECAM, the mixing frequency is 4.286 MHz giving the quadrature baseband components of the FM modulated chroma. After the mixer, a lowpass filter selects the chroma components; a downsampling stage converts the color difference signals to a multiplexed half rate data stream.

The subcarrier frequency in the demodulator is generated by direct digital synthesis; therefore, substandards such as PAL 3.58 or NTSC 4.43 can also be demodulated.

2.3.3. Chrominance Filter

The demodulation is followed by a lowpass filter for the color difference signals for PAL/NTSC. SECAM requires a modified lowpass function with bell-filter characteristic. At the output of the lowpass filter, all luma information is eliminated.

The lowpass filters are calculated in time multiplex for the two color signals. Three bandwidth settings (narrow, normal, broad) are available for each standard (see Fig. 2–5). For PAL/NTSC, a wide band chroma filter can be selected. This filter is intended for high bandwidth chroma signals, e.g. a nonstandard wide bandwidth S-VHS signal.

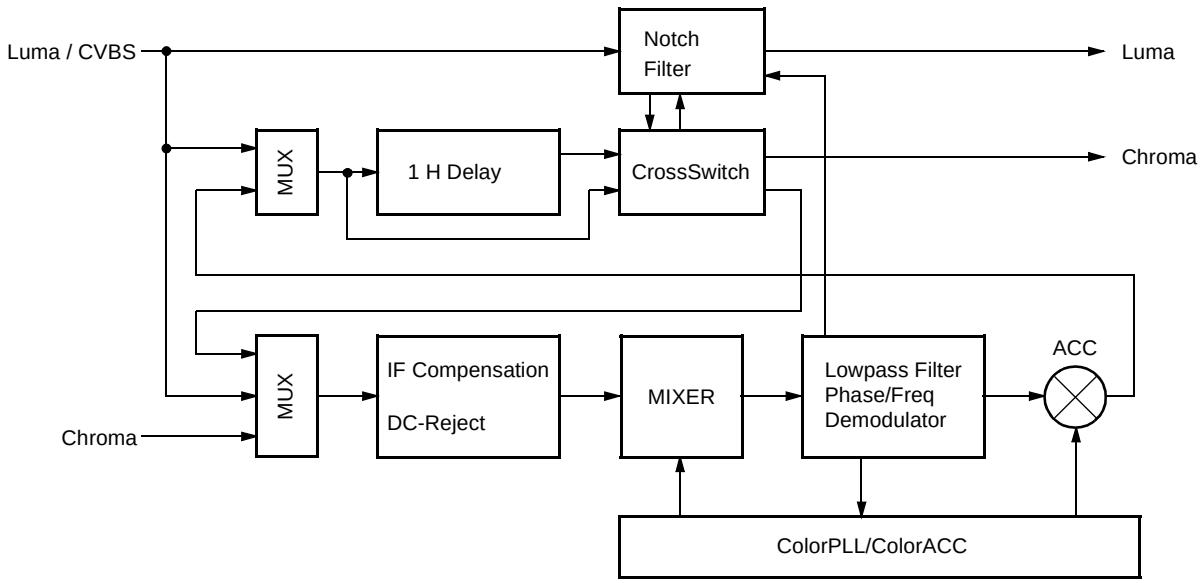


Fig. 2–4: Color decoder

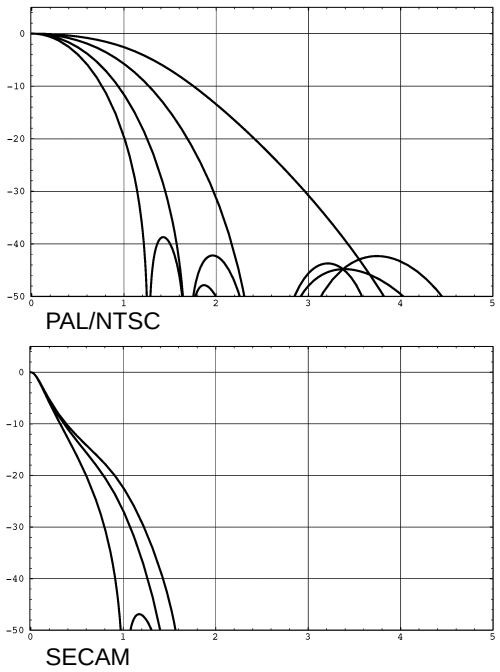


Fig. 2–5: Frequency response of chroma filters

2.3.4. Frequency Demodulator

The frequency demodulator for demodulating the SECAM signal is implemented as a CORDIC-structure. It calculates the phase and magnitude of the quadrature components by coordinate rotation.

The phase output of the CORDIC processor is differentiated to obtain the demodulated frequency. After the deemphasis filter, the Dr and Db signals are scaled to standard C_rC_b amplitudes and fed to the cross-over-switch.

2.3.5. Burst Detection

In the PAL/NTSC-system the burst is the reference for the color signal. The phase and magnitude outputs of the CORDIC are gated with the color key and used for controlling the phase-lock-loop (APC) of the demodulator and the automatic color control (ACC) in PAL/NTSC.

The ACC has a control range of +30 ... –6 dB.

For SECAM decoding, the frequency of the burst is measured. Thus, the current chroma carrier frequency can be identified and is used to control the SECAM processing. The burst measurements also control the color killer operation; they can be used for automatic standard detection as well.

2.3.6. Color Killer Operation

The color killer uses the burst-phase/burst-frequency measurement to identify a PAL/NTSC or SECAM color signal. For PAL/NTSC, the color is switched off (killed) as long as the color subcarrier PLL is not locked. For SECAM, the killer is controlled by the toggle of the burst frequency. The burst amplitude measurement is used to switch-off the color if the burst amplitude is below a programmable threshold. Thus, color will be killed for very noisy signals. The color amplitude killer has a programmable hysteresis.

2.3.7. PAL Compensation/1-H Comb Filter

The color decoder uses one fully integrated delay line. Only active video is stored.

The delay line application depends on the color standard:

– NTSC: 1-H comb filter **or** color compensation

– PAL: color compensation

– SECAM: crossover-switch

In the NTSC compensated mode, Fig. 2–6 c), the color signal is averaged for two adjacent lines. Thus, cross-color distortion and chroma noise is reduced. In the NTSC 1-H comb filter mode, Fig. 2–6 d), the delay line is in the composite signal path, thus allowing reduction of cross-color components, as well as cross-luminance. The loss of vertical resolution in the luminance channel is compensated by adding the vertical detail signal with removed color information. If the 4H adaptive comb filter is used, the 1-H NTSC comb filter has to be deselected.

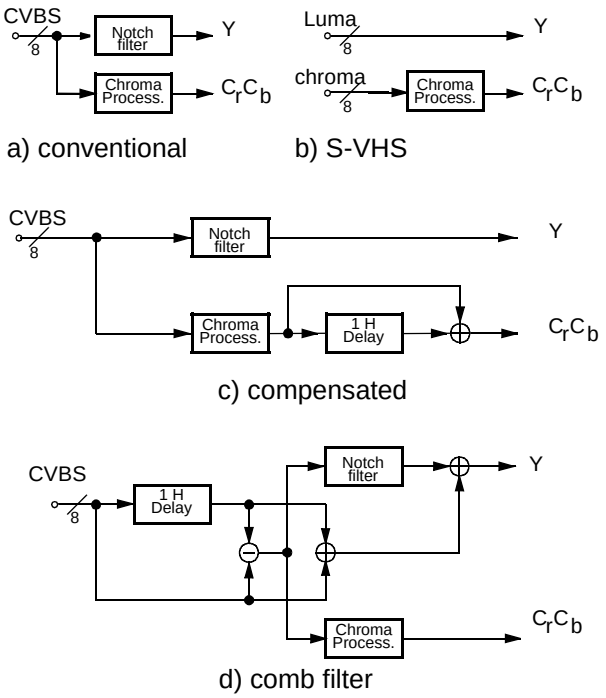


Fig. 2–6: NTSC color decoding options

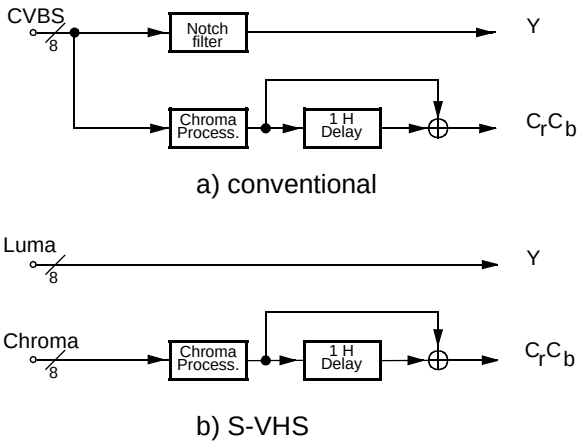


Fig. 2–7: PAL color decoding options

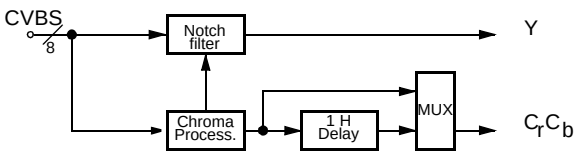


Fig. 2–8: SECAM color decoding

2.3.8. Luminance Notch Filter

If a composite video signal is applied, the color information is suppressed by a programmable notch filter. The position of the filter center frequency depends on the subcarrier frequency for PAL/NTSC. For SECAM, the notch is directly controlled by the chroma carrier frequency. This considerably reduces the cross-luminance. The frequency responses for all three systems are shown in Fig. 2–9.

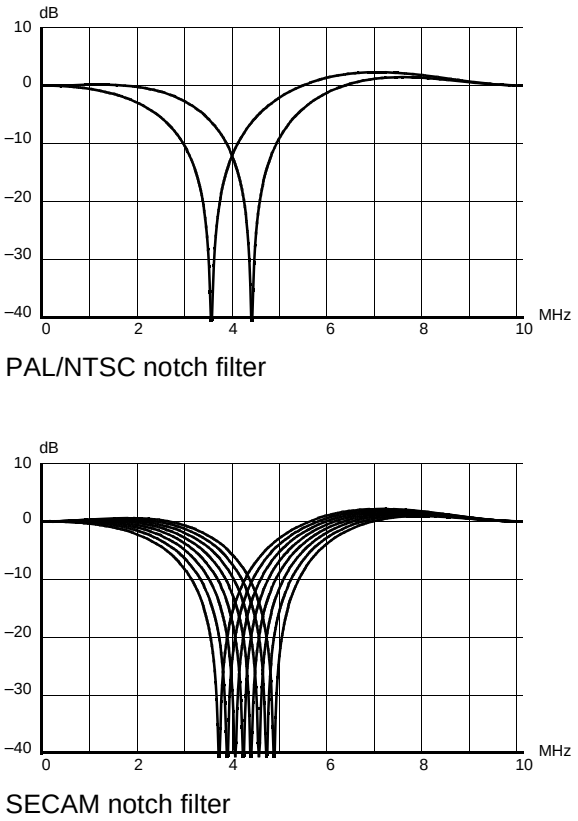


Fig. 2–9: Frequency responses of the luma notch filter for PAL, NTSC, SECAM

2.3.9. Skew Filtering

The system clock is free-running and not locked to the TV line frequency. Therefore, the ADC sampling pattern is not orthogonal. The decoded YC_rC_b signals are converted to an orthogonal sampling raster by the skew filters, which are part of the scaler block.

The skew filters are controlled by a skew parameter and allow the application of a group delay to the input signals without introducing waveform or frequency response distortion.

The amount of phase shift of this filter is controlled by the horizontal PLL1. The accuracy of the filters is 1/32 clocks for luminance and 1/4 clocks for chroma. Thus the 4:2:2 YC_rC_b data is in an orthogonal pixel format even in the case of nonstandard input signals such as VCR.

2.4. Horizontal Scaler

The 4:2:2 YCrCb signal from the color decoder is processed by the horizontal scaler. The scaler block allows a linear or nonlinear horizontal scaling of the input video signal in the range of 0.25 to 4. Nonlinear scaling, also called “panorama vision”, provides a geometrical distortion of the input picture. It is used to fit a picture with 4:3 format on a 16:9 screen by stretching the picture geometry at the borders. Also, the inverse effect can be produced by the scaler. A summary of scaler modes is given in Table 2–1.

The scaler contains a programmable decimation filter, a 1-line FIFO memory, and a programmable interpolation filter. The scaler input filter is also used for pixel skew correction, see 2.3.9. The decimator/interpolator structure allows optimal use of the FIFO memory. The controlling of the scaler is done by the internal Fast Processor.

Table 2–1: Scaler modes

Mode	Scale Factor	Description
Compression 4:3 → 16:9	0.75 linear	4:3 source displayed on a 16:9 tube, with side panels
Panorama 4:3 →16:9	non-linear compr	4:3 source displayed on a 16:9 tube, Borders distorted
Zoom 4:3 → 4:3	1.33 linear	Letterbox source (PAL+) displayed on a 4:3 tube, vertical overscan with cropping of side panels
Panorama 4:3 → 4:3	non-linear zoom	Letterbox source (PAL+) displayed on a 4:3 tube, vertical overscan, borders distorted, no cropping
20.25 → 13.5 MHz	0.66	sample rate conversion to line-locked clock

2.5. Blackline Detector

In case of a letterbox format input video, e.g. Cinemascope, PAL+ etc., black areas at the upper and lower part of the picture are visible. It is suitable to remove or reduce these areas by a vertical zoom and/or shift operation.

The VPC 32xx supports this feature by a letterbox detector. The circuitry detects black video lines by measuring the signal amplitude during active video. For every field the number of black lines at the upper and lower part of the picture are measured, compared to the previous measurement and the minima are stored in the I^2C-register BLKLIN. To adjust the picture amplitude, the external controller reads this register, calculates the vertical scaling coefficient and transfers the new settings, e.g. vertical sawtooth parameters, horizontal scaling coefficient etc., to the VPC.

Letterbox signals containing logos on the left or right side of the black areas are processed as black lines, while subtitles, inserted in the black areas, are processed as non-black lines. Therefore the subtitles are visible on the screen. To suppress the subtitles, the vertical zoom coefficient is calculated by selecting the larger number of black lines only. Dark video scenes with a low contrast level compared to the letterbox area are indicated by the BLKPIC bit.

2.6. Control and Data Output Signals

The VPC 32xx supports two output modes: In DIGIT3000 mode, the output interfaces run at the main system clock, in line-locked mode, the VPC generates an asynchronous line-locked clock that is used for the output interfaces.

2.6.1. Line-Locked Clock Generation

An on-chip rate multiplier will be used to synthesize any desired output clock frequency of 13.5/16/18 MHz. A double clock frequency output is available to support 100 Hz systems. The synthesizer is controlled by the embedded RISC controller, which also controls all front-end loops (clamp, AGC, PLL1, etc.). This allows the generation of a line-locked output clock regardless of the system clock (20.25 MHz) which is used for comb filter operation and color decoding. The control of scaling and output clock frequency is kept independent to allow aspect ratio conversion combined with sample rate conversion. The line-locked clock circuity generates control signals, e.g. horizontal/vertical sync, active video output, it is also the interface from the internal (20.25 MHz) clock to the external line-locked clock system.

If no line-locked clock is required, i.e. in the DIGIT3000 mode, the system runs at the 20.25 MHz main clock. The horizontal timing reference in this mode is provided by the front-sync signal. In this case, the line-locked clock block and all interfaces run from the 20.25 MHz main clock. The synchronization signals from the line-locked clock block are still available, but for every line the internal counters are reset with the main-sync signal. A double clock signal is not available in DIGIT3000 mode.

2.6.2. Sync Signals

The front end will provide a number of sync/control signals which are output with the output clock. The sync signals are generated in the line-locked clock block.

– Href : horizontal sync
– AVO: active video out (programmable)
– HC: horizontal clamp (programmable)
– Vref : vertical sync
– INTLC: interlace
– HELPER: PAL+ helper lines

All horizontal signals are not qualified with field information, i.e. the signals are present on all lines. The horizontal timing is shown in Fig. 2–10. Details of the horizontal/vertical timing are given in Fig. 2–14.

2.6.3. DIGIT3000 Output Format

The picture bus format between all DIGIT3000 ICs is 4:2:2 YCrCb with 20.25 MHz samples/s. Only active video is transferred, synchronized by the system main sync signal (MSY) which indicates the start of valid data for each scan line and which initializes the color multiplex. The video data is orthogonally sampled YCrCb, the output format is given in Table 2–2. The number of active samples per line is 1080 for all standards (525 and 625).

The output can be switched to 4:1:1 mode with the output format according to Table 2–3.

Via the MSY line, serial data is transferred which contains information about the main picture such as current line number, odd/even field etc.). It is generated by the deflection circuitry and represents the orthogonal timebase for the entire system.

Table 2–2: Orthogonal 4:2:2 output format

Luma	**Y_1**	**Y_2**	**Y_3**	**Y_4**
Chroma	**C_{b1}**	**C_{r1}**	**C_{b3}**	**C_{r3}**

2.6.4. Line-Locked 4:2:2 Output Format

In line-locked mode, the VPC 32xx will produce the industry standard pixel stream for YC_rC_b data. The difference to DIGIT3000 native mode is only the number of active samples, which of course, depends on the chosen scaling factor. Thus, Table 2–2 is valid for both 4:2:2 modes.

2.6.5. Line-Locked 4:1:1 Output Format

The orthogonal 4:1:1 output format is compatible to the industry standard. The YC_rC_b samples are skew-corrected and interpolated to an orthogonal sampling raster (see Table 2–3).

Table 2–3: 4:1:1 Orthogonal output format

Luma Chroma	**Y_1**	**Y_2**	**Y_3**	**Y_4**
C_3, C_7	C_{b1}^{7}	C_{b1}^{5}	C_{b1}^{3}	C_{b1}^{1}
C_2, C_6	C_{b1}^{6}	C_{b1}^{4}	C_{b1}^{2}	C_{b1}^{0}
C_1, C_5	C_{r1}^{7}	C_{r1}^{5}	C_{r1}^{3}	C_{r1}^{1}
C_0, C_4	C_{r1}^{6}	C_{r1}^{4}	C_{r1}^{2}	C_{r1}^{0}

note: $C^*_x{}^Y$ (x = pixel number and y = bit number)

2.6.6. Output Code Levels

Output Code Levels correspond to ITU-R code levels:
Y = 16...240
Black Level = 16
C_rC_b = 128±112
An overview over the output code levels is given in Table 2–4.

2.6.7. Output Signal Levels

All data and sync lines operate at TTL compliant levels. With an optional external 3.3 V supply for the output pins, reduced voltage swings can be obtained.

2.6.8. Test Pattern Generator

The YC_rC_b outputs can be switched to a test mode where YC_rC_b data are generated digitally in the VPC32xx. Test patterns include luma/chroma ramps, flat field, and a pseudo color bar.

2.6.9. Priority Bus Codec

The VPC data outputs are controlled by the priority bus interface. This interface allows a maximum of 8 signal sources to be connected on a common video YC_rC_b bus. The 3-bit priority bus signal controls the arbitration and source switching of the video sources on a pixel-by-pixel basis. The priority bus makes features possible, such as

– real time digital PIP insertion

– Teletext/Mixed-mode picture insertion.

In general, each source has its own YC_rC_b bus request. This bus request may either be software or hardware controlled, i.e. a fast blank signal. Data collision on the bus is avoided by a bus arbiter that provides the individual bus grant in accordance to the user defined source priority.

Each master sends a bus request using his individual priority ID onto the bus and immediately reads back the bus state. Only in case of a positive arbitration, e.g. the master reads back his own priority ID, the bus is granted to the master.

2.7. PAL+ Support

For PAL+, the VPC 321x provides basic helper preprocessing:

– A/D conversion (shared with the existing ADCs)

– mixing with subcarrier frequency

– lowpass filter 2.5 MHz

– gain control by chroma ACC

– delay compensation to composite video path

– helper window (line# identification)

– output at the luma output port

Helper signals are processed like the main video luma signals, i.e. they are subject to scaling, sample rate conversion and orthogonalization if activated. The adaptive comb filter processing is switched off for the helper lines.

It is expected that further helper processing (e.g. non-linear expansion, matched filter) is performed outside the VPC.

2.7.1. Output Signals for PAL+/Color+ Support

For a PAL+/Color+ signal, the 625 line PAL image contains a 16/9 core picture of 431 lines which is in standard PAL format. The upper and lower 72 lines contain the PAL+ helper signal, and line 23 contains signalling information for the PAL+ transmission.

For PAL+ mode, the Y signal of the core picture, which is during lines 60–274 and 372–586, is replaced by the orthogonal composite video input signal. In order to fit the signal to the 8-bit port width, the ADC signal amplitudes are used. During the helper window, which is in lines 24–59, 275–310, 336–371, 587–622, the demodulated helper is signal processed by the horizontal scaler and the output circuitry. It is available at the luma output port. The processing in the helper reference lines 23 and 623 is different for the wide screen signaling part and the black reference and helper burst signals. The code levels are given in detail in Table 2–4, the output signal for the helper reference line is shown in Fig. 2–11.

Table 2–4: Output signal code levels for PAL/PAL+ signal

Output Signal	**Luma Outputs Y[7:0]**			**Chroma Outputs C[7:0]**	
	Output Format	Black/Zero Level	Amplitude	Output Format	Amplitude
Standard YCrCb (100% Chroma	binary	16	224	offset binary	128±112
				signed	±112
CVBS, CrCb	binary	64	149 (luma)	offset binary	128±112
				signed	±112
Demodulated Helper	signed	0	±109	–	–
Helper WSS	binary	68	149 (WSS:106)	–	–
Helper black level, Ref. Burst	offset binary	128	19 (128–109)	–	–

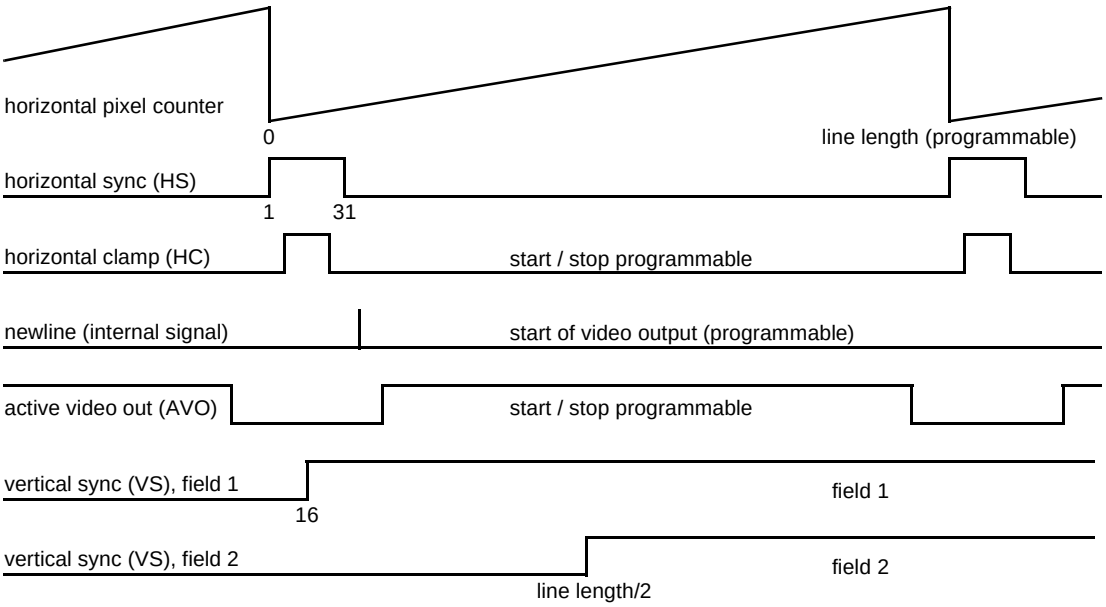


Fig. 2–10: Horizontal timing for line-locked mode

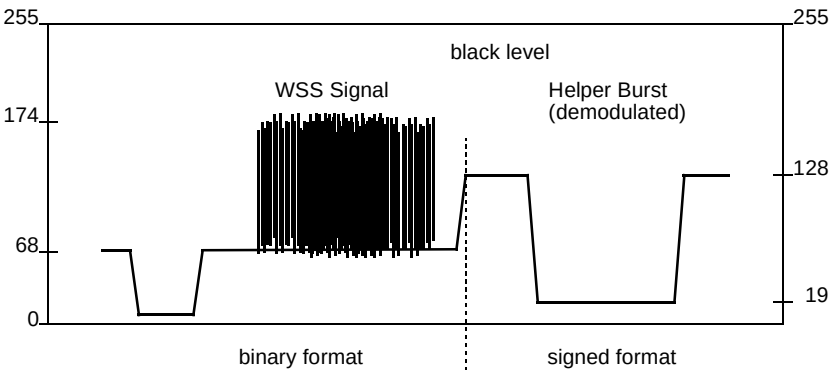


Fig. 2–11: PAL+ helper reference line output signal

2.8. Video Sync Processing

Fig. 2–12 shows a block diagram of the front-end sync processing. To extract the sync information from the video signal, a linear phase lowpass filter eliminates all noise and video contents above 1 MHz. The sync is separated by a slicer; the sync phase is measured. A variable window can be selected to improve the noise immunity of the slicer. The phase comparator measures the falling edge of sync, as well as the integrated sync pulse.

The sync phase error is filtered by a phase-locked loop that is computed by the FP. All timing in the front-end is derived from a counter that is part of this PLL, and it thus counts synchronously to the video signal.

A separate hardware block measures the signal back porch and also allows gathering the maximum/minimum of the video signal. This information is processed by the FP and used for gain control and clamping.

For vertical sync separation, the sliced video signal is integrated. The FP uses the integrator value to derive vertical sync and field information.

The information extracted by the video sync processing is multiplexed onto the hardware front sync signal (FSY) and is distributed to the rest of the video processing system. The format of the front sync signal is given in Fig. 2–13.

The data for the vertical deflection, the sawtooth, and the East-West correction signal is calculated by the VPC 32xx. The data is buffered in a FIFO and transferred to the back-end IC DDP 3300A by a single wire interface.

Frequency and phase characteristics of the analog video signal are derived from PLL1. The results are fed to the scaler unit for data interpolation and orthogonalization and to the clock synthesizer for line-locked clock generation. Horizontal and vertical syncs are latched with the line-locked clock.

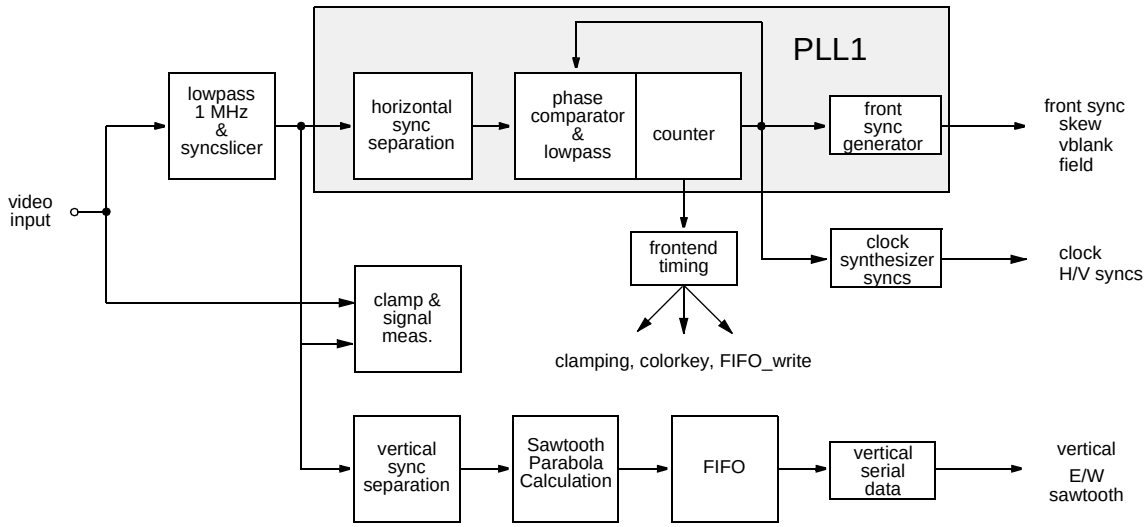


Fig. 2–12: Sync separation block diagram

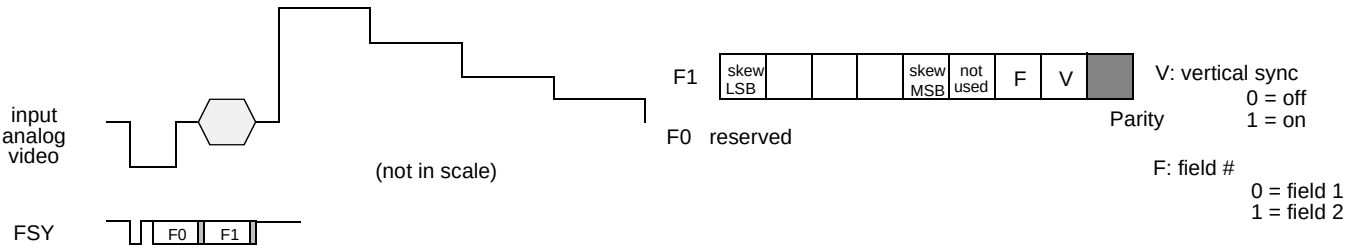
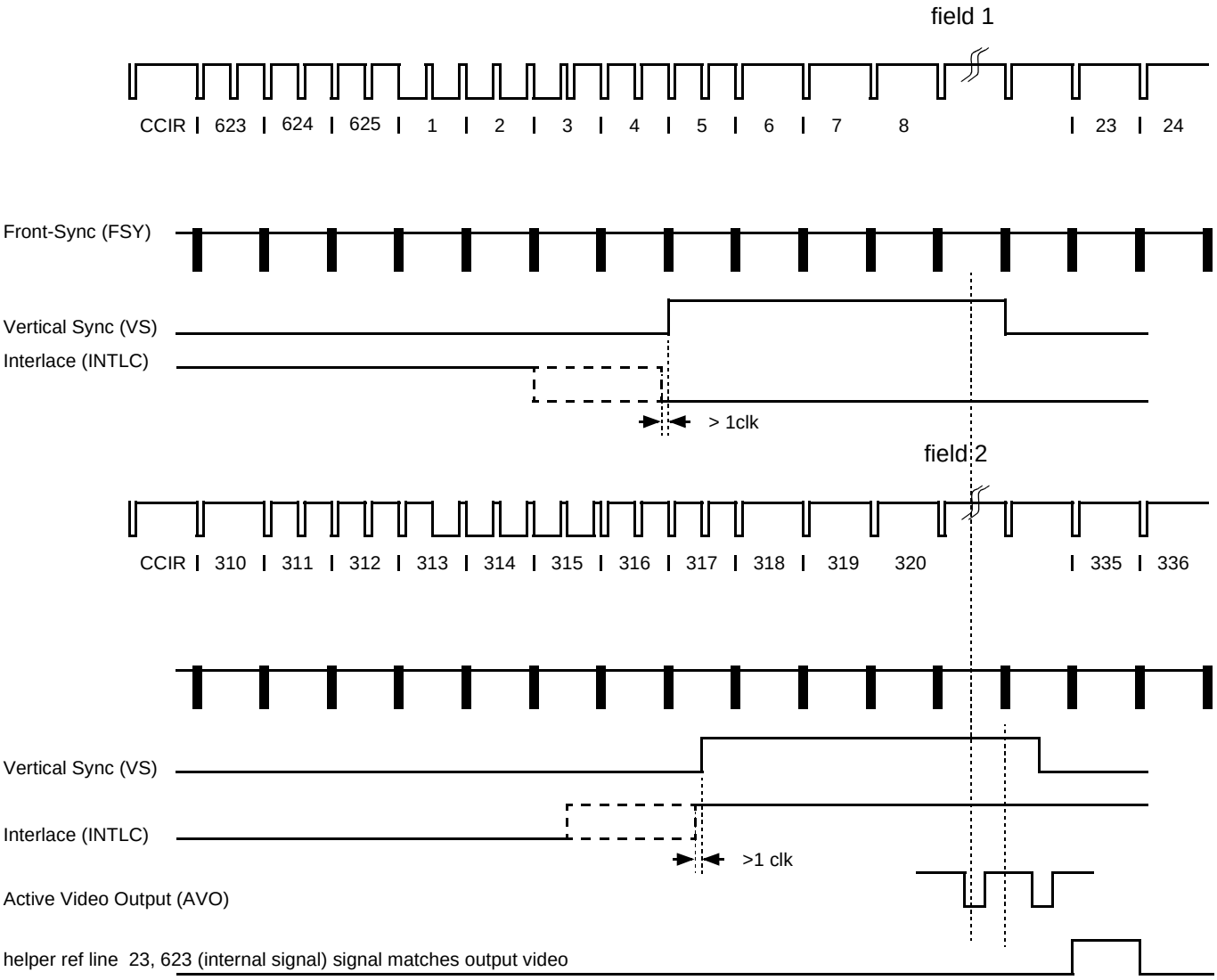


Fig. 2–13: Front sync format



The following signals are identical for field1 / field2

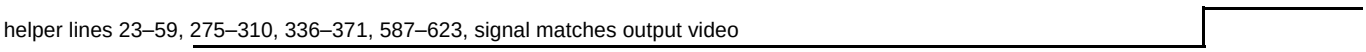


Fig. 2–14: Vertical timing of VPC 32x5 shown in reference to input video.
Video output signals are delayed by 3-h for comb filter version (VPC 32x5).

3. Serial Interface

3.1. I²C-Bus Interface

Communication between the VPC and the external controller is done via I²C-bus. The VPC has an I²C-bus slave interface and uses I²C clock synchronization to slow down the interface if required. The I²C-bus interface uses one level of subaddress: one I²C-bus address is used to address the IC and a subaddress selects one of the internal registers. The I²C-bus chip address is given below:

A6	A5	A4	A3	A2	A1	A0	R/W
1	0	0	0	1	1	1	1/0

The registers of the VPC have 8 or 16-bit data size; 16-bit registers are accessed by reading/writing two 8-bit data words.

Figure 3–1 shows I²C-bus protocols for read and write operations of the interface; the read operation requires an extra start condition and repetition of the chip address with read command set.

3.2. Control and Status Registers

Table 3–1 gives definitions of the VPC control and status registers. The number of bits indicated for each register in the table is the number of bits implemented in hardware, i.e. a 9-bit register must always be accessed using two data bytes but the 7 MSB will be ‘don’t care’ on write operations and ‘0’ on read operations. Write registers that can be read back are indicated in Table 3–1.

Functions implemented by software in the on-chip control microprocessor (FP) are explained in Table 3–2.

A hardware reset initializes all control registers to 0. The automatic chip initialization loads a selected set of registers with the default values given in Table 3–1.

The register modes given in Table 3–1 are

– w: write only register

– w/r: write/read data register

– r: read data from VPC

– v: register is latched with vertical sync

The mnemonics used in the Intermetall VPC demo software are given in the last column.

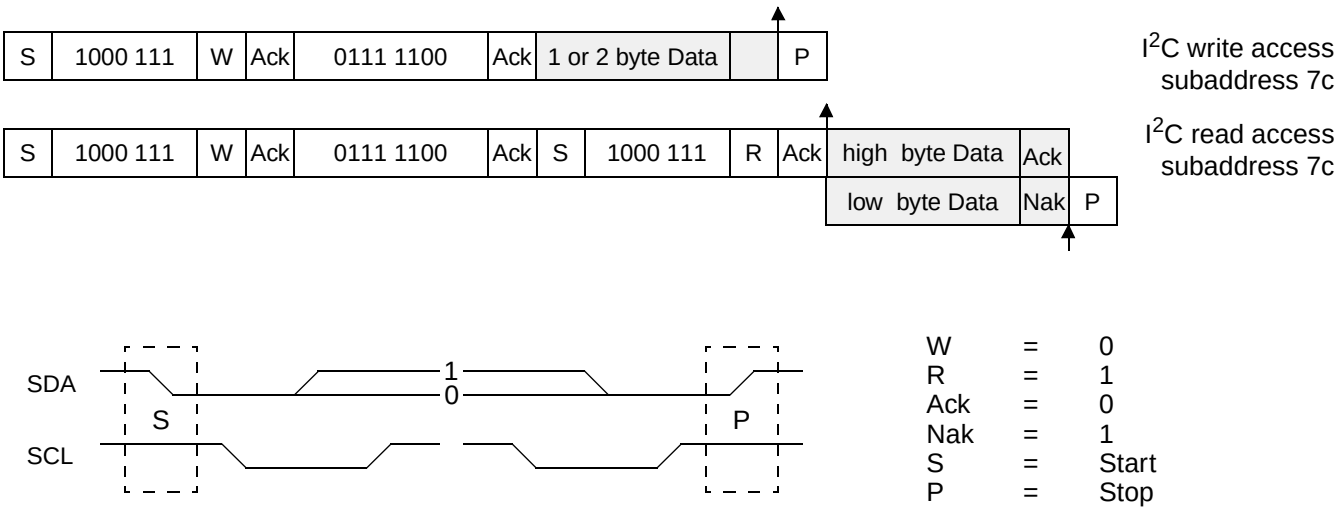


Fig. 3–1: I²C-bus protocols

Table 3–1: Control and status registers

I²C Sub-address	Number of bits	Mode	Function	Default	Name
			FP Interface		
h'35	8	r	FP status bit [0] write request bit [1] read request bit [2] busy	–	FPSTA
h'36	16	w	bit[8:0] 9-bit FP read address bit[11:9] reserved, set to zero	–	FPRD
h'37	16	w	bit[8:0] 9-bit FP write address bit[11:9] reserved, set to zero	–	FPWR
h'38	16	w/r	bit[11:0] FP data register, reading/writing to this register will autoincrement the FP read/ write address. Only 16 bit of data are transferred per I²C telegram.	–	FPDAT
			Black Line Detector		
h'12	16	w/r	read only register, do not write to this register! After reading, LOWLIN and UPLIN are reset to 127 to start a new measurement. bit[6:0] number of lower black lines bit[7] always 0 bit[14:8] number of upper black lines bit[15] 0/1 normal/black picture	–	BLKLIN LOWLIN UPLIN BLKPIC
			Pin Circuits		
h'1F	16	w/r	SYNC pins (HS, HC, AVO, HELP, INTLC, VS): bit[2:0] 0..7 output strength for SYNC Pins (7 = tristate, 6 = weak ... 0 = strong) bit[3] 0/1 pushpull/tristate for AVO Pin bit[4] 0/1 pushpull/tristate for other SYNC Pins bit[5] 0/1 synchronization/no synchronization with horizontal HS for signals VS and INTLC CLOCK pins (LLC1, LLC2): bit[6] 0/1 pushpull/tristate for LLC1 bit[7] 0/1 pushpull/tristate for LLC2 DATA pins (LB[7:0], CB[7:0]): bit[10:8] 0..7 output strength for DATA pins (7 = tristate, 6 = weak ... 0 = strong) bit[11] 0/1 **tristate**/pushpull for DATA pins bit[12] 0/1 half-cycle pull-up(DIGIT3000)/pushpull for LB, CB (LCC) bit[13] reserved (set to 0) bit[14:15] output strength for LLC1: (–2,–1,0,1)	0 0 0 0 0 0 0 0 0 0	TRPAD SNCSTR AVODIS SNCDIS VASYSEL LLC1DIS LLC2DIS DATSTR DATEN LCPUDIS LLC1STR

I²C Sub-address	Number of bits	Mode	Function	Default	Name
h'20	8	w/r	SYNC GENERATOR CONTROL:		SYNCMODE
			bit[1:0] 00 AVO and active Y/C data at same time	0	AVOPRE
			01 AVO precedes Y/C data one clock cycle		
			10 AVO precedes Y/C data two clock cycles		
			11 AVO precedes Y/C data three clock cycles		
			bit[2] 0/1 positive/negative polarity for HS signal	0	HSINV
			bit[3] 0/1 positive/negative polarity for HC signal	0	HCINV
			bit[4] 0/1 positive/negative polarity for AVO signal	0	AVOINV
			bit[5] 0/1 positive/negative polarity for VS signal	0	VSINV
			bit[6] 0/1 positive/negative polarity for HELP signal	0	HELPINV
			bit[7] 0/1 positive/negative polarity for INTLC signal	0	INTLCINV
h'30	8	w/r	V-SYNC DELAY CONTROL:		VSDEL
			bit[7:0] VS delay (8 LLC clock cycles per LSB)	0	VSDEL
Priority Bus					
h'23	8	w/r	priority bus overwrite register		
			bit [7:0] 8 bit mask, bit[x] = 1 : overwrite priority x	0	PRIOVR
h'24	8	w/r	priority bus ID register and control		PRIOMODE
			bit [2:0] 0..7 priority ID, 0 highest	0	PID
			bit [4:3] 0..3 pad driver strength, 0 (strong) to 3 (weak)	0	PRIOSTR
			bit [5] 0/1 output mode: DIGIT3000/LLC	0	OMODE
			bit [6] 0/1 source for prio request: AVO/active always	0	PIDSRC
			bit [7] 0/1 disable/enable priority interface, if disabled data pins are tristate !	0	PIDE
Sync Generator					
h'21	16	w/r	LINE LENGTH:		
			bit[10:0] LINE LENGTH register In LLC mode, this register defines the cycle of the sync counter which generates the SYNC pulses. In LLC mode, the synccounter counts from 0 to LINE LENGTH, so this register has to be set to "number of pixels per line –1". In DIGIT3000 mode, LINE LENGTH has to be set to 1295 for correct adjustment of vertical signals.	1295	LINLEN
			bit[15:11] reserved (set to 0)		
h'26	16	w/r	HC START:		
			bit[10:0] HC START defines the beginning of the HC signal in respect to the value of the sync counter.	50	HCSTRT
			bit[15:11] reserved (set to 0)		
h'27	16	w/r	HC STOP:		
			bit[10:0] HC STOP defines the end of the HC signal in respect to the value of the sync counter.	800	HCSTOP
			bit[15:11] reserved (set to 0)		

I²C Sub-address	Number of bits	Mode	Function	Default	Name
h'28	16	w/r	AVO START: bit[10:0] AVO START defines the beginning of the AVO signal in respect to the value of the sync counter. bit[11] reserved (set to 0) bit[12] 0/1 vertical window disable/enable bit[13] 0/1 vertical window 312/262 lines bit[15:14] –2..1 vertical window interlace offset	60	AVSTRT VERWIN
h'29	16	w/r	AVO STOP: bit[10:0] AVO STOP defines the end of the AVO signal in respect to the value of the sync counter. bit[15:11] reserved for test picture generation (set to 0 in normal operation) bit[11] 0/1 disable/enable test pattern generator bit[13:12] luma output mode: 00 Y = ramp (240 ... 17) 01 Y = 16 10 Y = 90 11 Y = 240 bit[14] 0/1 chroma output: 422/411 mode bit[15] 0/1 chroma output: pseudo color bar/zero if LMODE = 0	0 0 0 0 0	AVSTOP COLBAREN LMODE M411 CMODE
h'22	16	w/r	NEWLINE: bit[10:0] NEWLINE defines the readout start of the next line inrespect to the value of the sync counter. The value of this register must be greater than 31 for correct operation and should be identical to AVOSTART (recommended). In case of 1H-bypass mode for scaler block, NEWLINE has no function. bit[12:11] reserved (set to 0) bit[13] vertical free run mode enabled, the vertical frequency is selected via VERWIN (h'28) bit[15:14] reserved (set to 0)	50 0	NEWLIN FLW

Table 3–2: Control Registers of the Fast Processor

– default values are initialized at reset
– * indicates: register is initialized according to the current standard when SDT register is changed.

FP Sub-address	Function	Default	Name
	Standard Selection		
h'20	Standard select:		SDT
	bit[2:0] standard	0	
	0 PAL B,G,H,I (50 Hz) 4.433618		PAL
	1 NTSC M (60 Hz) 3.579545		NTSC
	2 SECAM (50 Hz) 4.286		SECAM
	3 NTSC44 (60 Hz) 4.433618		NTSC44
	4 PAL M (60 Hz) 3.575611		PALM
	5 PAL N (50 Hz) 3.582056		PALN
	6 PAL 60 (60 Hz) 4.433618		PAL60
	7 NTSC COMB (60 Hz) 3.579545		NTSCC
	bit[3] 0/1 MOD standard modifier PAL modified to simple PAL NTSC modified to compensated NTSC SECAM modified to monochrome 625 NTSCC modified to monochrome 525	0	SDTMOD
	bit[4] 0/1 PAL+ mode off/on	0	PALPLUS
	bit[5] 0/1 4-H COMB mode	0	COMB
	bit[6] 0/1 S-VHS mode: The S-VHS/COMB bits allow the following modes: 00 composite input signal 01 comb filter active 10 S-VHS input signal 11 CVBS mode (composite input signal, no luma notch)	0	SVHS
	Option bits allow to suppress parts of the initialization; this can be used for color standard search: bit[7] no hpll setup bit[8] no vertical setup bit[9] no acc setup bit[10] 4-H comb filter setup only	0	SDTOPT
	bit[11] status bit, normally write 0. After the FP has switched to a new standard, this bit is set to 1 to indicate operation complete. Standard is automatically initialized when the insel register is written.		

FP Sub-address	Function	Default	Name
h'21	Input select: writing to this register will also initialize the standard		INSEL
	bit[1:0] luma selector	0	VIS
	00 VIN3		
	01 VIN2		
	10 VIN1		
	11 VIN4		
	bit[2] chroma selector	1	CIS
	0/1 VIN1/CIN		
	bit[4:3] IF compensation	0	IFC
	00 off		
	01 6 dB/Okt		
	10 12 dB/Okt		
	11 10 dB/MHz only for SECAM		
	bit[6:5] chroma bandwidth selector	2	CBW
	00 narrow		
	01 normal		
	10 broad		
	11 wide		
	bit[7] 0/1 adaptive/fixed SECAM notch filter	0	FNTCH
	bit[8] 0/1 enable luma lowpass filter	0	LOWP
	bit[10:9] hpll speed	3	HPLLMD
	00 no change		
	01 terrestrial		
	10 vcr		
	11 mixed		
	bit[11] status bit, write 0, this bit is set to 1 to indicate operation complete.		
h'22	picture start position: This register sets the start point of active video and can be used e.g. for panning. The setting is updated when 'sdt' register is updated or when the scaler mode register 'scmode' is written.	0	SFIF
h'23	luma/chroma delay adjust. The setting is updated when 'sdt' register is updated. bit[5:0] reserved, set to zero bit[11:6] luma delay in clocks, allowed range is +1 ... –7	0	LDLY
h'29	helper delay register (PAL+ mode only) bit[11:0] delay adjust for helper lines adjustable from –96...96, 1 step corresponds to 1/32 clock	0	HLP_DLY
h'2f	VGA mode select, pull-in range is limited to 2%		VGA_C
	bit[1:0] 0 31.5 kHz		
	1 35.2 kHz	0	VGAMODE
	2/3 37.9 kHz		
	is set to 0 by FP if VGA = 0		
	bit[10] 0/1 disable/enable VGA mode		
	bit[11] status bit, write 0, this bit is set to 1 to indicate operation complete.	0	VGA

FP Sub-address	Function	Default	Name
	Comb Filter		
h'28	comb filter control register bit[1:0] notch filter select 00 flat frequency characteristic 01 min. peaked 10 med. peaked 11 max. peaked bit[3:2] diagonal dot reduction 00 min. reduction ... 11 max. reduction bit[4:5] horizontal difference gain 00 min. gain ... 11 max. gain bit[7:6] vertical difference gain 00 max. gain ... 11 min. gain bit[11:8] vertical peaking gain 0 no vertical peaking... 15 max. vertical peaking	h'e7 3 1 2 3 0	COMB_UC NOSEL DDR HDG VDG VPK
h'55	comb filter test register bit[1:0] reserved, set ot 0 bit[2] 0/1 disable/enable vertical peaking DC rejection filter bit[3] 0/1 disable/enable vertical peaking coring bit[11:4] reserved, set to 0	 0 0	CMB_TST DCR COR
	Color Processing		
h'34	ACC multiplier value for PAL+ Helper Signal b[10:0] eeemmmmmmmm m * 2^{-e}	1280	ACCH
h'36	ACC PAL+ Helper gain adjust, gain is referenced to PAL burst, allowed values from 256..1023 a value of zero allows manual adjust of Helper amplitude via ACCh	787	HLPGAIN
h'39	amplitude killer level (0:killer disabled)	25	KILVL
h'3a	amplitude killer hysteresis	5	KILHY
h'16c	automatic helper disable for nonstandard signals bit[11:0] 0 automatic function disabled bit[1:0] 01 enable bit[11:2] 1..50 number of fields to switch on helper signal	0	HLPDIS
h'dc	NTSC tint angle, ±512 = ±π/4	0	TINT
	Horizontal PLL		
h'aa h'ab h'ac	h-pll gain setting, these registers are used to set the h-pll speed, pll speed selection is done via the input selection register		
	DVCO		
h'f8	crystal oscillator center frequency adjust, –2048 ... 2047	–720	DVCO
h'f9	crystal oscillator center frequency adjustment value for line-lock mode, true adjust value is DVCO – ADJUST. For factory crystal alignment, using standard video signal: disable autolock mode, set DVCO = 0, set lock mode, read crystal offset from ADJUST register and use negative value for initial center frequency adjustment via DVCO.	read only	ADJUST

FP Sub-address	Function	Default	Name
h'f7	crystal oscillator line-locked mode, lock command/status write: 100 enable lock 0 disable lock read: 0 unlocked >2047 locked	0	XLCK
h'b5	crystal oscillator line-locked mode, autolock feature. If autolock is enabled, crystal oscillator locking is started automatically. bit[11:0] threshold, 0:autolock off	400	AUTOLCK
	FP Status Register		
h'12	general purpose control bits bit[2:0] reserved, do not change bit[3] vertical standard force bit[8:4] reserved, do not change bit[9] disable flywheel interlace bit[11:10] reserved, do not change to enable vertical free run mode set vfrc to 1 and dflw to 0	 0 1	 VFRC DFLW
h'13	standard recognition status bit[0] 1 vertical lock bit[1] 1 horizontally locked bit[2] 1 no signal detected bit[3] 1 color amplitude killer active bit[4] 1 disable amplitude killer bit[5] 1 color ident killer active bit[6] 1 disable ident killer bit[7] 1 interlace detected bit[8] 1 no vertical sync detection bit[9] 1 spurious vertical sync detection bit[12:10] reserved	–	ASR
h'14	input noise level, available only for VPC 3215C	read only	NOISE
h'cb	number of lines per field, P/S: 312, N: 262	read only	NLPF
h'15	vertical field counter, incremented per field	read only	VCNT
h'74	measured sync amplitude value, nominal: 768 (PAL), 732 (NTSC)	read only	SAMPL
h'31	measured burst amplitude	read only	BAMPL
h'f0	firmware version number bit[7:0] internal revision number bit[11:8] firmware release	read only	–
h'f1	hardware version number bit[5:0] internal hardware revision number bit[11:6] hardware id, VPC 32x5C = 01	read only	–

FP Sub-address	Function	Default	Name
	Scaler Control Register		
h'40	scaler mode register bit[1:0] scaler mode 0 linear scaling mode 1 nonlinear scaling mode, 'panorama' 2 nonlinear scaling mode, 'waterglass' 3 reserved bit[2] reserved, set to 0 bit[3] color mode select 0/1 4:2:2 mode / 4:1:1 mode bit[4] scaler bypass bit[5] reserved, set to 0 bit[6] luma output format 0 ITU-R luma output format (16–240) 1 CVBS output format bit[7] chroma output format 0/1 ITU-R (offset binary) / signed bit[10:8] reserved, set to 0 bit[11] 0 scaler update command, when the registers are updated the bit is set to 1	0	SCMODE PANO S411 BYE YOF COF
h'41	luma offset register bit[6:0] luma offset 0..127 ITU-R output format: 57 CVBS output format: 4 this register is updated when the scaler mode register is written	57	YOFFS
h'42	active video length for 1H-FIFO bit[11:0] length in pixels D3000 mode (1296/h)1080 LLC mode (864/h)720 this register is updated when the scaler mode register is written	1080	FFLIM
h'43	scaler1 coefficient: This scaler compresses the signal. For compression by a factor c, the value c*1024 is required. bit[11:0] allowed values from 1024... 4095 This register is updated when the scaler mode register is written.	1024	SCINC1
h'44	scaler2 coefficient: This scaler expands the signal. For expansion by a factor c, the value 1/c*1024 is required. bit[11:0] allowed values from 256..1024 This register is updated when the scaler mode register is written.	1024	SCINC2
h'45	scaler1/2 nonlinear scaling coefficient This register is updated when the scaler mode register is written.	0	SCINC
h'47 – h'4b	scaler1 window controls, see table 5 12-bit registers for control of the nonlinear scaling This register is updated when the scaler mode register is written.	0	SCW1_0 – 4
h'4c – h'50	scaler2 window controls, see table 5 12-bit registers for control of the nonlinear scaling This register is updated when the scaler mode register is written.	0	SCW2_0 – 4

FP Sub-address	Function	Default	Name
	LLC Control Register		
h'60	horizontal offset bit[11:0] offset between FSY and HS	0	LLC_OFFSET
h'65	vertical freeze start freeze llc pll for llc_start < line number < llc_stop bit[11:0] allowed values from –156...+156	–10	LLC_START
h'66	vertical freeze stop freeze llc pll for llc_start < line number < llc_stop bit[11:0] allowed values from –156...+156	4	LLC_STOP
h'69 h'6a	20 bit llc clock center frequency 13.5 MHz 174763 = h'02AAAB 16 MHz –135927 = h'FDED08 18 MHz 174763 = h'02AAAB	42 = h'02A 2731 = h'AAB	LLC_CLOCKH LLC_CLOCKL
h'61	pll frequency limiter, 8% 13.5 MHz 54 16 MHz 48 18 MHz 54	54	LLC_DFLIMIT
h'6d	llc clock generator control word bit[4:0] hardware register shadow llc_clkc = 5→13.5 MHz llc_clkc = 3→16 MHz llc_clkc = 3→18 MHz bit[10:5] reserved bit[11] 0/1 enable/disable llc pll	2053	LLC_CLKC

Table 3–3: Control Registers of the Fast Processor that are used for the control of DDP 3300A

– this function is only available in the 50 Hz version (VPC 320x)
– default values are initialized at reset
– * indicates: register is initialized according to the current standard when SDT register is changed

FP Sub-address	Function	Default	Name
	FP Display Control Register		
h'130	White Drive Red (0...1023)	700	WDR [1)]
h'131	White Drive Green (0...1023)	700	WDG [1)]
h'132	White Drive Blue (0...1023)	700	WDB [1)]
h'139	Internal Brightness, Picture (0 ..511), the center value is 256, the range allows for both increase and reduction of brightness.	256	IBR
h'13c	Internal Brightness, measurement (0...511), the center value is 256, the brightness for measurement can be set to measure at higher cutoff current. The measurement brightness is independent of the drive values.	256	IBRM
h'13a	Analog Brightness for external RGB (0...511), the center value is 256, the range allows for both increase and reduction of brightness.	256	ABR
h'13b	Analog Contrast for external RGB (0...511)	350	ACT
[1)] The white drive values will become active only after writing the blue value WDB, latching of new values is indicated by setting the MSB of WDB.			
	FP Display Control Register, BCL		
h'144	BCL threshold current, 0...2047 (max ADC output ~1152)	1000	BCLTHR
h'142	BCL time constant 0...15 →13 ... 1700 msec	15	BCLTM
h'143	BCL loop gain. 0..15	0	BCLG
h'145	BCL minimum contrast 0 ...1023	307	BCLMIN
h'105	Test register for BCL/EHT comp. function, register value: 0 normal operation 1 stop ADC offset compensation x>1 use x in place of input from Measurement ADC	0	BCLTST
	FP Display Control Register, Deflection		
h'103	interlace offset, –2048 ...2047 This value is added to the SAWTOOTH output during one field.	0	INTLC
h'102	discharge sample count for deflection retrace, SAWTOOTH DAC output impedance is reduced for DSCC lines after vertical retrace.	7	DSCC
h'11f	vertical discharge value, SAWTOOTH output value during discharge operation, typically same as A0 init value for sawtooth.	–1365	DSCV
h'10b	EHT (electronic high tension) compensation coefficient, 0...511	0	EHT
h'10a	EHT time constant. 0 ..15 → 3.2 ...410 msec	15	EHTTM

Control registers, continued

FP Sub-address	Function	Default	Name
FP Display Control Register			
FP Display Control Register, Vertical Sawtooth			
h’110	DC offset of SAWTOOTH output This offset is independent of EHT compensation.	0	OFS
h’11b	accu0 init value	–1365	A0
h’11c	accu1 init value	900	A1
h’11d	accu2 init value	0	A2
h’11e	accu3 init value	0	A3
FP Display Control Register, East-West Parabola			
h’12b	accu0 init value	–1121	A0
h’12c	accu1 init value	219	A1
h’12d	accu2 init value	479	A2
h’12e	accu3 init value	–1416	A3
h’12f	accu4 init value	1052	A4

3.2.1. Calculation of Vertical and East-West Deflection Coefficients

In Table 3–4 the formula for the calculation of the deflection initialization parameters from the polynominal coefficients a,b,c,d,e is given for the vertical and East-West deflection. Let the polynomial be

$$P = a + b(x - 0.5) + c(x - 0.5)^2 + d(x - 0.5)^3 + e(x - 0.5)^4$$

The initialization values for the accumulators a0..a3 for vertical deflection and a0..a4 for East-West deflection are 12-bit values. The coefficients that should be used to calculate the initialization values for different field frequencies are given below, the values must be scaled by 128, i.e. the value for a0 of the 50 Hz vertical deflection is

$$a0 = (a \cdot 128 - b \cdot 1365.3 + c \cdot 682.7 - d \cdot 682.7) \div 128$$

3.2.2. Scaler Adjustment

In case of linear scaling, most of the scaler registers need not be set. Only the scaler mode, active video length, and the fixed scaler increments (scinc1/scinc2) must be written.

The adjustment of the scaler for nonlinear scaling modes should use the parameters given in table 3–5. An example for ‘panorama vision’ mode with 13.5 MHz line-locked clock is depicted in Fig. 3–2. The figure shows the scaling of the input signal and the variation of the scaling factor during the active video line. The scaling factor starts below 1, i.e. for the borders the video data is expanded by scaler 2. The scaling factor becomes one and compression scaling is done by scaler 1. When the picture center is reached, the scaling factor is held constant. At the second border the scaler increment is inverted and the scaling factor changes back symmetrically. The picture indicates the function of the scaler increments and the scaler window parameters. The correct adjustment requires that pixel counts for the respective windows are always in number of output samples of scaler 1 or 2.

Table 3–4: Tables for the Calculation of Initialization values for Vertical Sawtooth and East-West Parabola

Vertical Deflection 50 Hz				
	a	**b**	**c**	**d**
a0	128	–1365.3	+682.7	–682.7
a1		899.6	–904.3	+1363.4
a2			296.4	–898.4
a3				585.9

Vertical Deflection 60 Hz				
	a	**b**	**c**	**d**
a0	128	–1365.3	+682.7	–682.7
a1		1083.5	–1090.2	+1645.5
a2			429.9	–1305.8
a3				1023.5

East-West Deflection 50 Hz					
	a	**b**	**c**	**d**	**e**
a0	128	–341.3	1365.3	–85.3	341.3
a1		111.9	–899.6	84.8	–454.5
a2			586.8	–111.1	898.3
a3				72.1	–1171.7
a4					756.5

East-West Deflection 60 Hz					
	a	**b**	**c**	**d**	**e**
a0	128	–341.3	1365.3	–85.3	341.3
a1		134.6	–1083.5	102.2	–548.4
a2			849.3	–161.2	1305.5
a3				125.6	–2046.6
a4					1584.8

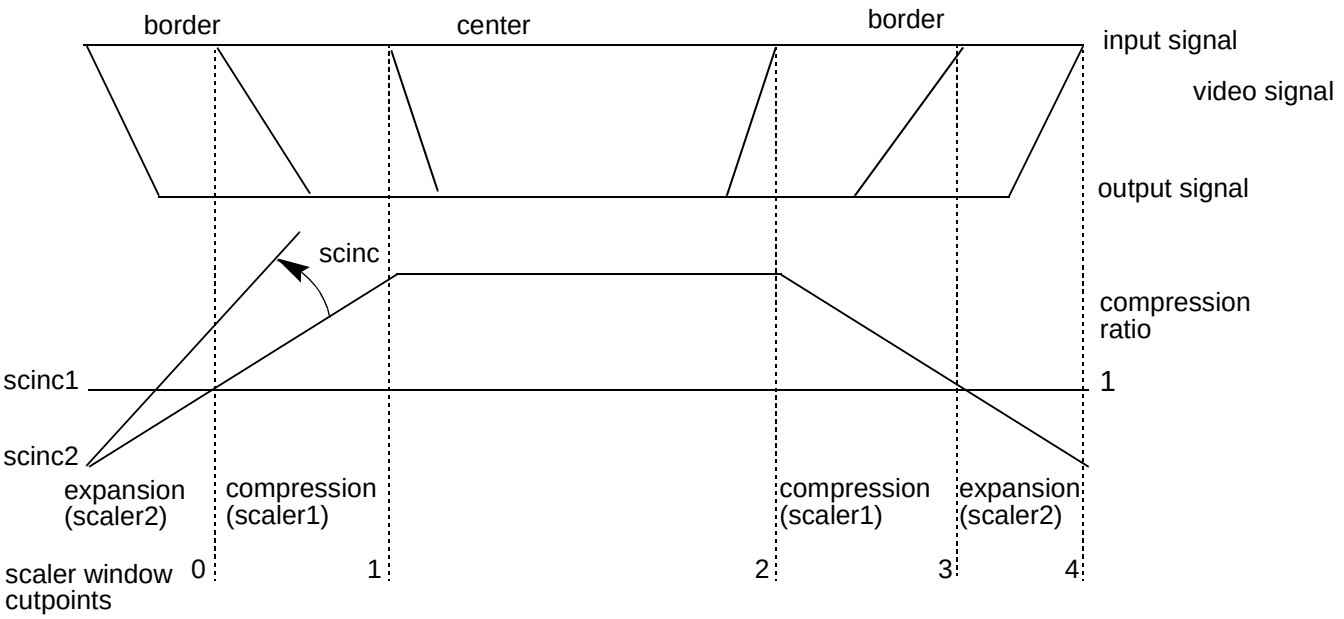


Fig. 3–2: Scaler operation for ‘panorama’ mode at 13.5 MHz

Table 3–5: Set-up values for nonlinear scaler modes

Mode	DIGIT3000 (20.25 MHz)				LLC (13.5 MHz)			
	‘waterglass’ border 35%		‘panorama’ border 30%		‘waterglass’ border 35%		‘panorama’ border 30%	
Register	center 3/4	center 5/6	center 4/3	center 6/5	center 3/4	center 5/6	center 4/3	center 6/5
scinc1	1643	1427	1024	1024	2464	2125	1024	1024
scinc2	1024	1024	376	611	1024	1024	573	914
scinc	90	56	85	56	202	124	190	126
fflim	945	985	921	983	719	719	681	715
scw1 – 0	110	115	83	94	104	111	29	13
scw1 – 1	156	166	147	153	104	111	115	117
scw1 – 2	317	327	314	339	256	249	226	241
scw1 – 3	363	378	378	398	256	249	312	345
scw1 – 4	473	493	461	492	360	360	341	358
scw2 – 0	110	115	122	118	104	111	38	14
scw2 – 1	156	166	186	177	104	111	124	118
scw2 – 2	384	374	354	363	256	249	236	242
scw2 – 3	430	425	418	422	256	249	322	346
scw2 – 4	540	540	540	540	360	360	360	360

4. Specifications

4.1. Outline Dimensions

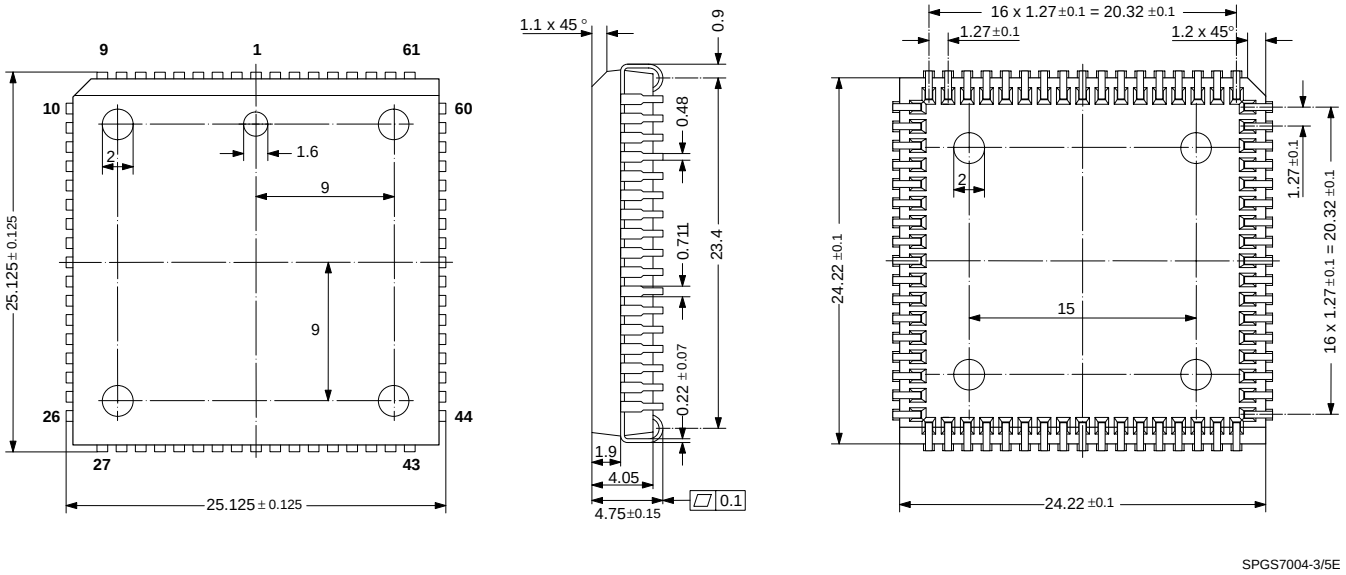


Fig. 4–1: 68-Pin Plastic Leaded Chip Carrier Package **(PLCC68)**
Weight approximately 4.8 g
Dimensions in mm

4.2. Pin Connections and Short Descriptions

NC = not connected
LV = if not used, leave vacant
X = obligatory; connect as described in circuit diagram

Pin No. PLCC 68-pin	Pin Name	Type	Connection (if not used)	Short Description
1	GND_F	SUPPLY	X	Ground, Analog Front-End
2	GND_F	SUPPLY	X	Ground, Analog Front-End
3	CLK5	OUT	LV	CCU 5 MHz Clock Output
4	V_{STBY}	SUPPLY	X	Standby Supply Voltage
5	XTAL2	OUT	X	Analog Crystal Output
6	XTAL1	IN	X	Analog Crystal Input
7	GND_F	SUPPLY	X	Ground, Analog Front-End
9	GND_P	SUPPLY	X	Ground, Output Pad Circuitry
10	INTLC	OUT	LV	Interlace Output
12	VS	OUT	LV	Vertical Sync Pulse
13	FSY	OUT	LV	Front Sync Pulse
14	MSY/HS	IN/OUT	LV	Main Sync/Horizontal Sync Pulse
15	HELPER	OUT	LV	Helper Line Output

Pin No. PLCC 68-pin	Pin Name	Type	Connection (if not used)	Short Description
16	HC	IN/OUT	LV	Horizontal Clamp Pulse
17	AVO	OUT	LV	Active Video Output
18	LLC2	OUT	LV	Double Output Clock
19	LLC1	IN/OUT	LV	Output Clock
20	Y7	OUT	GND_P	Picture Bus Luma (MSB)
21	Y6	OUT	GND_P	Picture Bus Luma
22	Y5	OUT	GND_P	Picture Bus Luma
23	Y4	OUT	GND_P	Picture Bus Luma
24	Y3	OUT	GND_P	Picture Bus Luma
25	Y2	OUT	GND_P	Picture Bus Luma
26	GND_P		X	Ground, Output Pad Circuitry
28	Y1	OUT	GND_P	Picture Bus Luma
29	Y0	OUT	GND_P	Picture Bus Luma (LSB)
30	CLK20	IN/OUT	LV	Main Clock Output 20.25 MHz
31	V_{SUPD}	SUPPLY	X	Supply Voltage, Digital Circuitry
34	GND_D	SUPPLY	X	Ground, Digital Circuitry
35	GND_P	SUPPLY	X	Ground, Output Pad Circuitry
36	V_{SUPP}	SUPPLY	X	Supply Voltage, Output Pad Supply
38	C7	OUT	GND_P	Picture Bus Chroma (MSB)
39	C6	OUT	GND_P	Picture Bus Chroma
40	C5	OUT	GND_P	Picture Bus Chroma
41	C4	OUT	GND_P	Picture Bus Chroma
42	C3	OUT	GND_P	Picture Bus Chroma
43	C2	OUT	GND_P	Picture Bus Chroma
46	C1	OUT	GND_P	Picture Bus Chroma
47	C0	OUT	GND_P	Picture Bus Chroma (LSB)
48	PR0	IN/OUT	LV	Picture Bus Priority (LSB)
49	PR1	IN/OUT	LV	Picture Bus Priority
50	PR2	IN/OUT	LV	Picture Bus Priority (MSB)
51	GND_P	SUPPLY	X	Ground, Output Pad Circuitry
52	VGAV	IN	GND_P	VGAV Input

Pin No. PLCC 68-pin	Pin Name	Type	Connection (if not used)	Short Description
53	FPDAT	IN/OUT	LV	Front-End/Back-End Data
54	RESQ	IN	X	Reset Input, Active Low
55	SDA	IN/OUT	X	I^2C Bus Data
56	SCL	IN/OUT	X	I^2C Bus Clock
57	TEST	IN	GND_D	Test Pin, connect to GND_D
58	VIN4	IN	VRT	Video 4 Analog Input
59	GND_F	SUPPLY	X	Ground, Analog Front-End
60	VIN3	IN	VRT	Video 3 Analog Input
61	VIN2	IN	VRT	Video 2 Analog Input
62	VIN1	IN	VRT*	Video 1 Analog Input
63	CIN	IN	LV*	Chroma/Video 4 Analog Input
64	VOUT	OUT	LV	Analog Video Output
65	ASGF		X	Analog Shield GND_F
66	V_{SUPF}	SUPPLY	X	Supply Voltage, Analog Front-End
67	ISGND	SUPPLY	X	Signal Ground for Analog Input, connect to GND_F
68	VRT	OUTPUT	X	Reference Voltage Top, Analog
8, 11 27, 32 33, 37 44, 45	NC	–	LV OR GND_D	Not connected

*) chroma selector must be set to 1 (CIN chroma select)

4.3. Pin Descriptions (pin numbers for PLCC68 package)

Pin 1 – Ground, Analog Front-End GND_F

Pin 2 – Ground, Analog Front-End GND_F

Pin 3 – CCU 5 MHz Clock Output CLK5 (Fig. 4–11)
This pin provides a clock frequency for the TV microcontroller, e.g. a CCU 3000 controller. It is also used by the DDP 3300A display controller as a standby clock.

Pin 4 – Standby Supply Voltage V_{STDBY}
In standby mode, only the clock oscillator is active, GND_F should be ground reference. Please activate RESQ before powering-up other supplies

Pins 6 and 5 – XTAL1 Crystal Input and XTAL2 Crystal Output (Fig. 4–8)
These pins are connected to an 20.25 MHz crystal oscillator which is digitally tuned by integrated shunt capacitances. The CLK20 and CLK5 clock signals are derived from this oscillator. An external clock can be fed into XTAL1. In this case, clock frequency adjustment must be switched off.

Pin 7 – Ground, Analog Front-End GND_F

Pin 9 – Ground, Output Pad Circuitry GND_P

Pin 10 – Interlace Output, INTLC (Fig. 4–4)
This pin supplies the interlace information, 0 indicates first field, 1 indicates second field.

Pin 12 – Vertical Sync Pulse, VS (Fig. 4–4)
This pin supplies the vertical sync signal.

Pin 13 – Front Sync Pulse, FSY (Fig. 4–4)
This pin supplies the front sync information.

Pin 14 – Main Sync/Horizontal Sync Pulse MSY/HS (Fig. 4–4)
This pin supplies the horizontal sync pulse information in line-locked mode. In DIGIT3000 mode, this pin is the main sync input.

Pin 15 – Helper Line Output, Helper (Fig. 4–4)
This signal indicates a helper line in PAL+ mode.

Pin 16 – Horizontal Clamp Pulse, HC (Fig. 4–4)
This signal can be used to clamp an external video signal, that is synchronous to the input signal. The timing is programmable.

Pin 17 – Active Video Output, AVO (Fig. 4–4)
This pin indicates the active video output data. The signal is clocked with the LLC1 clock.

Pin 18 – Double Output Clock, LLC2 (Fig. 4–6)

Pin 19 – Output Clock, LLC1 (Fig. 4–6)
This is the clock reference for the luma, chroma, and status outputs.

Pin 26 – Ground, Output Pad Circuitry GND_P

Pins 20 to 25,28,29 – Luma Outputs Y0 – Y7 (Fig. 4–4)
These output pins carry the digital luminance data. The data are clocked with the LLC1 clock.

Pin 30 – Main Clock Output CLK20 (Fig. 4–5)
This is the 20.25 MHz main clock output.

Pin 31 – Supply Voltage, Digital Circuitry V_{SUPD}

Pin 34 – Ground, Digital Circuitry GND_D

Pin 35 – Ground, Output Pad Circuitry GND_P

Pin 36 – Supply Voltage, Output Pad Supply V_{SUPP}

Pins 38 to 43,46,47 – Chroma Outputs C0–C7 (Fig. 4–4)
These outputs carry the digital CrCb chrominance data. The data are clocked with the LL1 clock. The data are sampled at half the clock rate and multiplexed. The CrCb multiplex is reset for each TV line.

Pins 48 to 50 – Picture Bus Priority PR0–PR2 (Fig. 4–6)
The Picture Bus Priority lines carry the digital priority selection signals. The priority interface allows digital switching of up to 8 sources to the back-end processor. Switching for different sources is prioritized and can be on a per pixel basis.

Pin 51 – Ground, Output Pad Circuitry GND_P

Pin 52 – VGAV-Input. (Fig. 4–3)
This pin is connected to the vertical sync signal of a VGA signal.

Pin 53 – Front-End/Back-End Data FPDAT (Fig. 4–6)
This pin interfaces to the DDP 3300A back-end processor. The information for the deflection drives and for the white drive control, i.e. the beam current limiter, is transmitted by this pin.

Pin 54 – Reset Input RESQ (Fig. 4–3)
A low level on this pin resets the VPC 32xx.

Pin 55 – I^2C Bus Data SDA (Fig. 4–13)
This pin connects to the I^2C bus data line.

Pin 56 – I^2C Bus Clock SCL (Fig. 4–3)
This pin connects to the I^2C bus clock line.

Pin 57 – Test Input TEST (Fig. 4–3)
This pin enables factory test modes. For normal operation, it must be connected to ground.

Pin 59 – Ground, Analog Front-End GND_F

Pins 62,61,60,58 – Video Input 1–4 (Fig. 4–12)
These are the analog video inputs. A CVBS or S-VHS luma signal is converted using the luma (Video 1) AD converter. The VIN1 input can also be switched to the chroma (Video 2) ADC. The input signal must be AC-coupled.

Pin 63 – Chroma Input CIN (Fig. 4–10)
This pin is connected to the S-VHS chroma signal. A resistive divider is used to bias the input signal to the middle of the converter input range. CIN can only be connected to the chroma (Video 2) A/D converter. The signal must be AC-coupled.

Pin 64 – Analog Video Output, VOUT (Fig. 4–7)
The analog video signal that is selected for the main (luma, CVBS) ADC is output at this pin. An emitter follower is required at this pin.

Pin 65 – Ground, Analog Shield Front-End GND_F

Pin 66 – Supply Voltage, Analog Front-End V_{SUPF} (Fig. 4–9)

Pin 67 – Signal GND for Analog Input ISGND (Fig. 4–11) This is the high quality ground reference for the video input signals.

Pin 68 – Reference Voltage Top VRT (Fig. 4–9)
Via this pin, the reference voltage for the A/D converters is decoupled. The pin is connected with 10 µF/47 nF to the Signal Ground Pin.

4.4. Pin Configuration

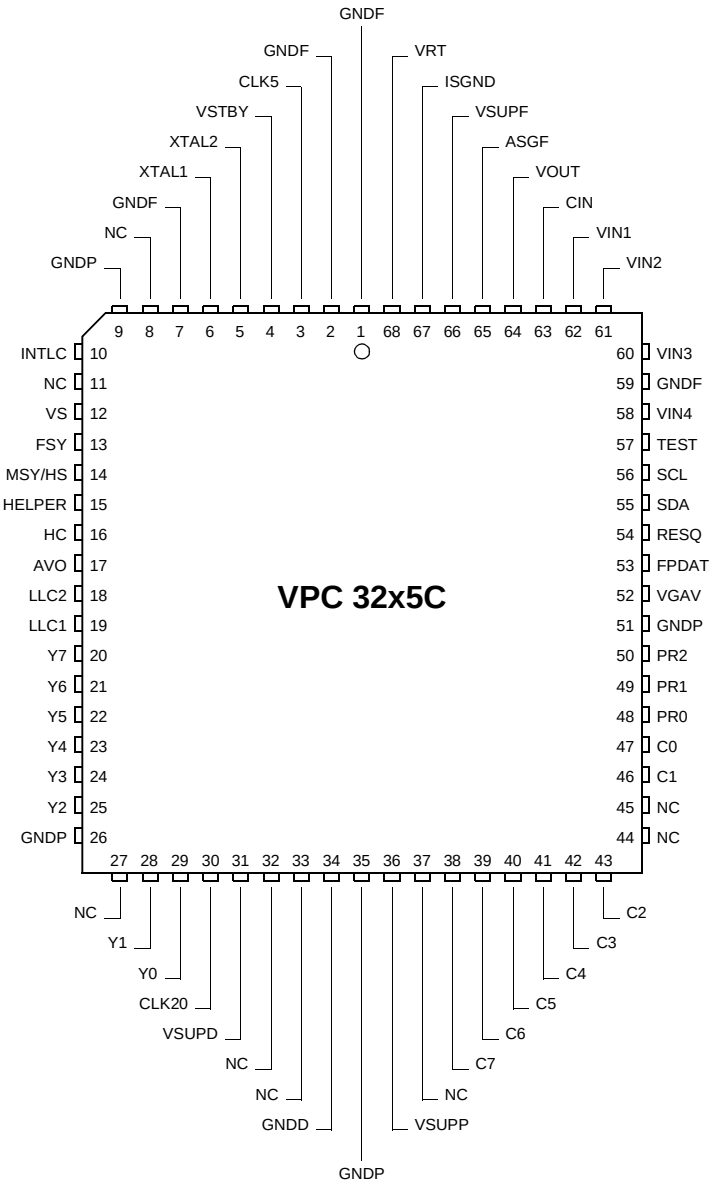


Fig. 4–2: 68-pin PLCC package

4.5. Pin Circuits

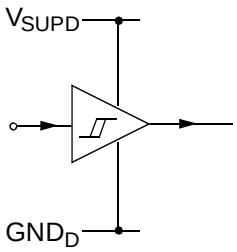


Fig. 4–3: Input pins RESQ, TEST, VGAV

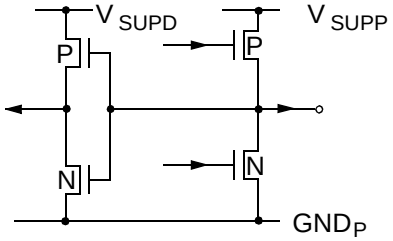


Fig. 4–4: Output pins C0–C7, Y0–Y7, FSY, HC, AVO, HELPER, VS, INTLC, HS, LLC1, LLC2

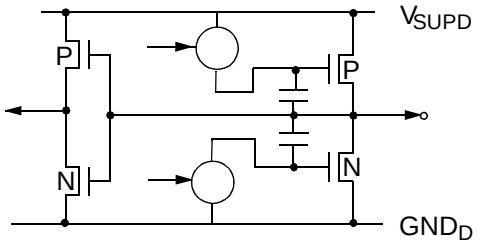


Fig. 4–5: Output pin CLK20

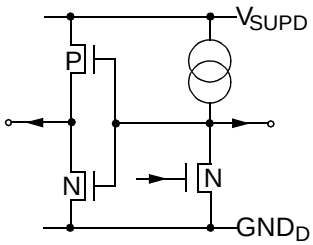


Fig. 4–6: Input/Output pins PR0–PR2, FPDAT

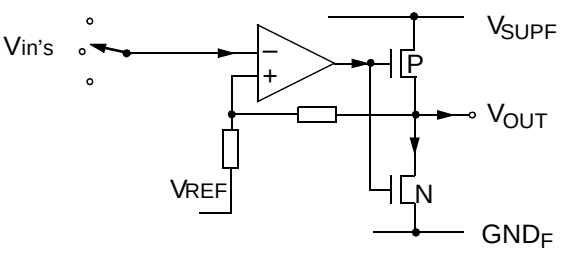


Fig. 4–7: Output pin VOUT

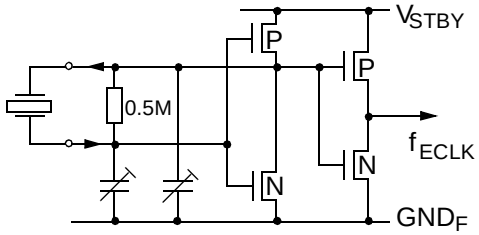


Fig. 4–8: Input/Output Pins XTAL1, XTAL2

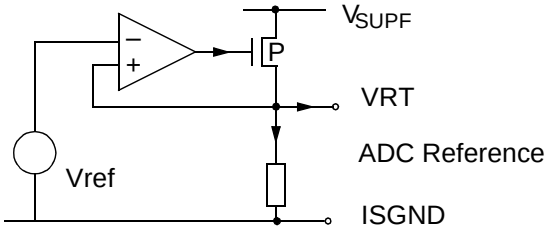


Fig. 4–9: Pins VRT, ISGND

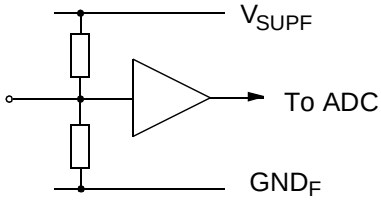


Fig. 4–10: Chroma input CIN

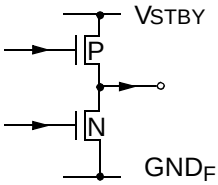


Fig. 4–11: Output pin CLK5

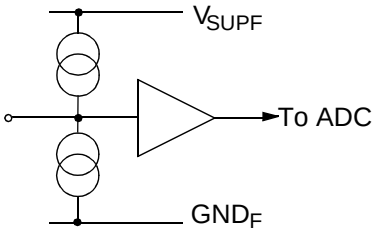


Fig. 4–12: Input pins VIN1–VIN4

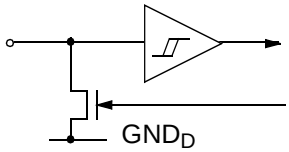


Fig. 4–13: Pins SDA, SCL

4.6. Electrical Characteristics

4.6.1. Absolute Maximum Ratings

Symbol	Parameter	Pin No.	Min.	Max.	Unit
T_A	Ambient Operating Temperature	–	0	65	°C
T_S	Storage Temperature	–	–40	125	°C
V_{SUP}	Supply Voltage, all Supply Inputs	–	–0.3	6	V
V_I	Input Voltage, all Inputs	–	–0.3	V_{SUP}+0.3	V
V_O	Output Voltage, all Outputs	–	–0.3	V_{SUP}+0.3	V

Stresses beyond those listed in the “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only. Functional operation of the device at these or any other conditions beyond those indicated in the “Recommended Operating Conditions/Characteristics” of this specification is not implied. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.

4.6.2. Recommended Operating Conditions

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit
T_A	Ambient Operating Temperature	–	0	–	65	°C
V_{SUP}	Supply Voltages, all Supply Pins	–	4.75	5.0	5.25	V
V_{SUPP}	Supply Volt., Output Pad Supply	VSUPP	3.15	–	5.25	V
f_{XTAL}	Clock Frequency	XTAL1/2	–	20.25	–	MHz

4.6.3. Recommended Crystal Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit
T_A	Operating Ambient Temperature	0	–	65	°C
f_P	Parallel Resonance Frequency with Load Capacitance **C_L = 13 pF**	–	20.250000	–	MHz
$\Delta f_P/f_P$	Accuracy of Adjustment	–	–	±20	ppm
$\Delta f_P/f_P$	Frequency Temperature Drift	–	–	±30	ppm
R_R	Series Resistance	–	–	25	Ω
C_0	Shunt Capacitance	3	–	7	pF
C_1	Motional Capacitance	20	–	30	fF
Load Capacitance Recommendation					
C_{Lext}	External Load Capacitance [1] from pins to Ground (pin names: Xtal1 Xtal2)	–	3.3	–	pF
DCO Characteristics [2,3]					
$C_{ICLoadmin}$	Effective Load Capacitance @ min. DCO–Position, Code 0, package: 68PLCC	3	4.3	5.5	pF
$C_{ICLoadrng}$	Effective Load Capacitance Range, DCO Codes from 0..255	11	12.7	15	pF

[1] Remarks on defining the External Load Capacitance:

External capacitors at each crystal pin to ground are required. They are necessary to tune the effective load capacitance of the PCBs to the required load capacitance C_L of the crystal. The higher the capacitors, the lower the clock frequency results. The nominal free running frequency should match f_p MHz. Due to different layouts of customer PCBs the matching capacitor size should be determined in the application. The suggested value is a figure based on experience with various PCB layouts. Tuning condition: Code DVCO Register=–720

[2] Remarks on Pulling Range of DCO:

The pulling range of the DCO is a function of the used crystal and effective load capacitance of the IC (C_{ICLoad} +$C_{LoadBoard}$). The resulting frequency f_L with an effective load capacitance of $C_{Leff} = C_{ICLoad} + C_{LoadBoard}$ is:

$$f_L = f_P * \frac{1 + 0.5 * [\, C_1 / (C_0 + C_L)\,]}{1 + 0.5 * [\, C_1 / (C_0 + C_{Leff})\,]}$$

[3] Remarks on DCO codes

The DCO hardware register has 8 bits, the fp control register uses a range of –2048...2047

4.6.4. Characteristics

at T_A = 0 to 65 °C, $V_{SUPD/F}$ = 4.75 to 5.25 V, V_{SUPP} = 3.15 to 3.5V f = 20.25 MHz for min./max. values
at T_C = 60 °C, $V_{SUPD/F}$ = 5 V, Vsupp = 3.15V f = 20.25 MHz for typical values

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit
P_{TOT}	Total Power Dissipation	–	–	1.15	1.5	W
I_{VSUPA}	Current Consumption	V_{SUPF}	–	40	–	mA
I_{VSUPD}	Current Consumption	V_{SUPD}	–	160	–	mA
I_{VSUPP}	Current Consumption	V_{SUPP}	–	40	–	mA
I_{VSTDBY}	Current Consumption	V_{STDBY}	–	1	–	mA
IL	Input / Output Leakage Current	All I/O Pins	–1	–	1	µA

4.6.4.1. Characteristics, 5 MHz Clock Output

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
V_{OL}	Output Low Voltage	CLK5	–	–	0.4	V	I_{OL} = 0.4 mA
V_{OH}	Output High Voltage		4.0	–	V– STDBY	V	$-I_{OL}$ = 0.9 mA
t_{OT}	Output Transition Time		–	50	–	ns	C_{LOAD} = 30 pF

4.6.4.2. Characteristics, 20 MHz Clock Input/Output, External Clock Input (XTAL1)

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
V_{DCAV}	DC Average	CLK20	$V_{SUP}/2$ – 0.3	$V_{SUP}/2$	$V_{SUP}/2$ + 0.3	V	C_{LOAD} = 30 pF
V_{PP}	V_{OUT} Peak to Peak		1.3	1.6	–	V	C_{LOAD} = 30 pF
t_{OT}	Output Transition Time		–	–	18	ns	C_{LOAD} = 30 pF
V_{IT}	Input Trigger Level		2.1	2.5	2.9	V	only for test purposes
V_I	Clock Input Voltage	XTAL1	1.3	–	–	V_{PP}	capacitive coupling used, XTAL2 open

4.6.4.3. Characteristics, Reset Input, Test Input

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
V_{IL}	Input Low Voltage	RESQ TEST	–	–	1.5	V	
V_{IH}	Input High Voltage		3.0	–	–	V	

4.6.4.4. Characteristics, Priority, FPDAT Input/Output

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
V_{OL}	Output Low Voltage	PR[2:0] FPDAT	–	–	0.5	V	I_{OL} = 14.4 mA, strength 0 I_{OL} = 10.8 mA, strength 1 I_{OL} = 7.2 mA, strength 2 I_{OL} = 3.6 mA, strength 3 note: FPDAT strength = 2
V_{OH}	Output High Voltage		1.8	2.0	2.5	V	$-I_{OL}$ = 10 µA C_{LOAD} = 70 pF
t_{OH}	Output Hold Time		6	–	–	ns	
t_{ODL}	Output Delay Time		–	–	35	ns	C_{LOAD} = 70 pF I_L = 14.4 mA strength = 3
I_{PL}	Output Pull-up Current	PR[2:0] FPDAT	1.2	1.5	1.5	mA	V_{OL} = 0 V
V_{IL}	Input Low Voltage		–	–	0.8	V	
V_{IH}	Input High Voltage		1.5	–	–	V	
t_{IS}	Input Setup Time		7	–	–	ns	
t_{IH}	Input Hold Time		5	–	–	ns	

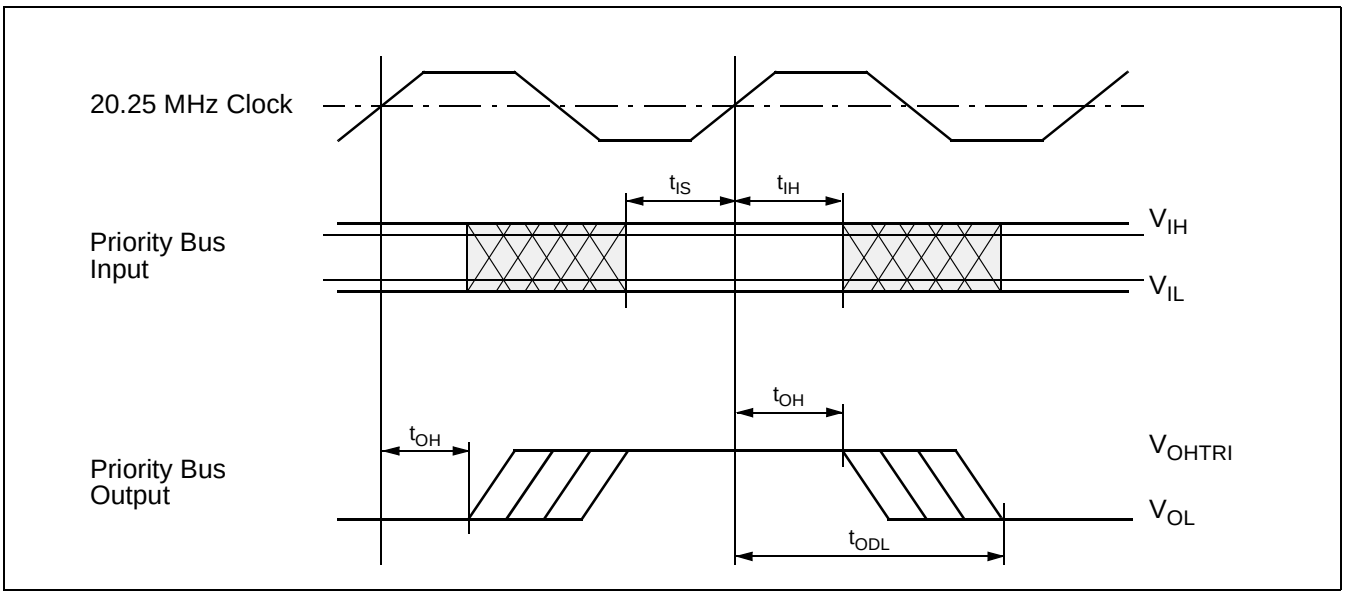


Fig. 4–14: Priority, FPDAT input/output

4.6.4.5. Characteristics, VGAV Input

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
V_{IL}	Input Low Voltage	VGAV	–	–	0.8	V	
V_{IH}	Input High Voltage		2.0	–	–	V	

4.6.4.6. Characteristics, I²C Bus Interface

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
V_{IL}	Input Low Voltage	SDA, SCL	–	–	1.5	V	
V_{IH}	Input High Voltage		3.0	–	–	V	
V_{OL}	Output Low Voltage		–	–	0.4 0.6	V V	I_I = 3 mA I_I = 6 mA
V_{IH}	Input Capacitance		–	–	5	pF	
t_F	Signal Fall Time		–	–	300	ns	C_L = 400 pF
t_R	Signal Rise Time		–	–	300	ns	C_L = 400 pF
f_{SCL}	Clock Frequency	SCL	0	–	400	kHz	
t_{LOW}	Low Period of SCL		1.3	–	–	µs	
t_{HIGH}	High Period of SCL		0.6	–	–	µs	
$t_{SU\ Data}$	Data Set Up Time to SCL high	SDA	100	–	–	ns	
$t_{HD\ Data}$	DATA Hold Time to SCL low		0	–	0.9	µs	

4.6.4.7. Characteristics, Analog Video Inputs

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
V_{VIN}	Analog Input Voltage	VIN1, VIN2 VIN3, VIN4 CIN	0	–	3.5	V	
C_{CP}	Input Coupling Capacitor Video Inputs	VIN1, VIN2 VIN3, VIN4	–	680	–	nF	
C_{CP}	Input Coupling Capacitor Chroma Input	CIN	–	1	–	nF	

4.6.4.8. Characteristics, Analog Front-End and ADCs

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
V_{VRT}	Reference Voltage Top	VRT	2.5	2.6	2.8	V	10 µF/10 nF, 1 GΩ Probe
Luma – Path							
R_{VIN}	Input Resistance	VIN1 VIN2 VIN3 VIN4	1	–	–	MΩ	Code Clamp–DAC=0
C_{VIN}	Input Capacitance		–	5	–	pF	
V_{VIN}	Full Scale Input Voltage	VIN1 VIN2 VIN3 VIN4	1.8	2.0	2.2	V_{PP}	min. AGC Gain
V_{VIN}	Full Scale Input Voltage		0.5	0.6	0.7	V_{PP}	max. AGC Gain
AGC	AGC step width		–	0.166	–	dB	6-Bit Resolution= 64 Steps f_{sig}=1MHz, – 2 dBr of max. AGC–Gain
DNL_{AGC}	AGC Differential Non-Linearity		–	–	±0.5	LSB	

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
V_{VINCL}	Input Clamping Level, CVBS	VIN1 VIN2 VIN3 VIN4	–	1.0	–	V	Binary Level = 64 LSB min. AGC Gain
Q_{CL}	Clamping DAC Resolution		–16		15	steps	5 Bit – I–DAC, bipolar V_{VIN}=1.5 V
$I_{CL–LSB}$	Input Clamping Current per step		0.7	1.0	1.3	µA	
DNL_{ICL}	Clamping DAC Differential Non-Linearity		–	–	±0.5	LSB	
Chroma – Path							
R_{CIN}	Input Resistance SVHS Chroma	CIN VIN1	1.4	2.0	2.6	kΩ	
V_{CIN}	Full Scale Input Voltage, Chroma		1.08	1.2	1.32	V_{PP}	
V_{CINDC}	Input Bias Level, SVHS Chroma		–	1.5	–	V	
	Binary Code for Open Chroma Input		–	128	–	–	
Dynamic Characteristics for all Video-Paths (Luma + Chroma)							
BW	Bandwith	VIN1 VIN2 VIN3 VIN4	8	10	–	MHz	–2 dBr input signal level
XTALK	Crosstalk, any Two Video Inputs		–	–56	–	dB	1 MHz, –2 dBr signal level
THD	Total Harmonic Distortion		–	50	–	dB	1 MHz, 5 harmonics, –2 dBr signal level
SINAD	Signal to Noise and Distortion Ratio		–	45	–	dB	1 MHz, all outputs, –2 dBr signal level
INL	Integral Non-Linearity		–	–	±1	LSB	Code Density, DC-ramp
DNL	Differential Non-Linearity		–	–	±0.8	LSB	
DG	Differential Gain		–	–	±3	%	–12 dBr, 4.4 MHz signal on DC-ramp
DP	Differential Phase		–	–	1.5	deg	
Analog Video Output							
V_{OUT}	Output Voltage	Out: VOUT In: VIN1 VIN2 VIN3 VIN4	1.7	2.0	2.3	V_{PP}	V_{IN} = 1 V_{PP}, AGC= 0 dB
AGC_{VOUT}	AGC step width, VOUT		–	1.333	–	dB	3 Bit Resolution=7 Steps 3 MSB's of main AGC
DNL_{AGC}	AGC Differential Non-Linearity		–	–	±0.5	LSB	
V_{OUTDC}	DC-level		–	1	–	V	clamped to Back porch
BW	V_{OUT} Bandwidth		8	10	–	MHz	Input: –2 dBr of main ADC range, C_L≤10 pF
THD	V_{OUT} Total Harmonic Distortion		–	–	–40	dB	Input: –2 dBr of main ADC range, C_L≤10 pF 1 MHz, 5 Harmonics
C_{LVOUT}	Load Capacitance	VOUT	–	–	10	pF	
I_{LVOUT}	Output Current		–	–	±0.1	mA	

4.6.4.9. Characteristics, Output Pin Specification

Output Specification for SYNC, CONTROL, and DATA Pins:
Y[7:0], C[7:0], AVO, HS, HC, HELPER, INTLC, VS, FSY

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
V_{OL}	Output Low Voltage	–	–	–	0.4	V	see table below
V_{OH}	Output High Voltage	–	2.4	–	–	V	see table below
t_{OH}	Output Hold Time	–	6	–	–	ns	
t_{OD}	Output Delay Time	–	–	–	35	ns	NOTE 1

NOTE 1: C_{LOAD} depends on the selected driver strength which is I^2C-programmable.

Table 4–1: Driver strength

Strength	V_{SUPP} = 5 V Load	V_{SUPP} = 3.3 V Load
000	< 100 pF	< 50 pF
001	< 55 pF	< 28 pF
010	< 37 pF	< 20 pF
011	< 28 pF	< 14 pF
100	< 23 pF	< 12 pF
101	< 18 pF	< 10 pF
110	< 14 pF	< 8 pF
111	pins tristate	

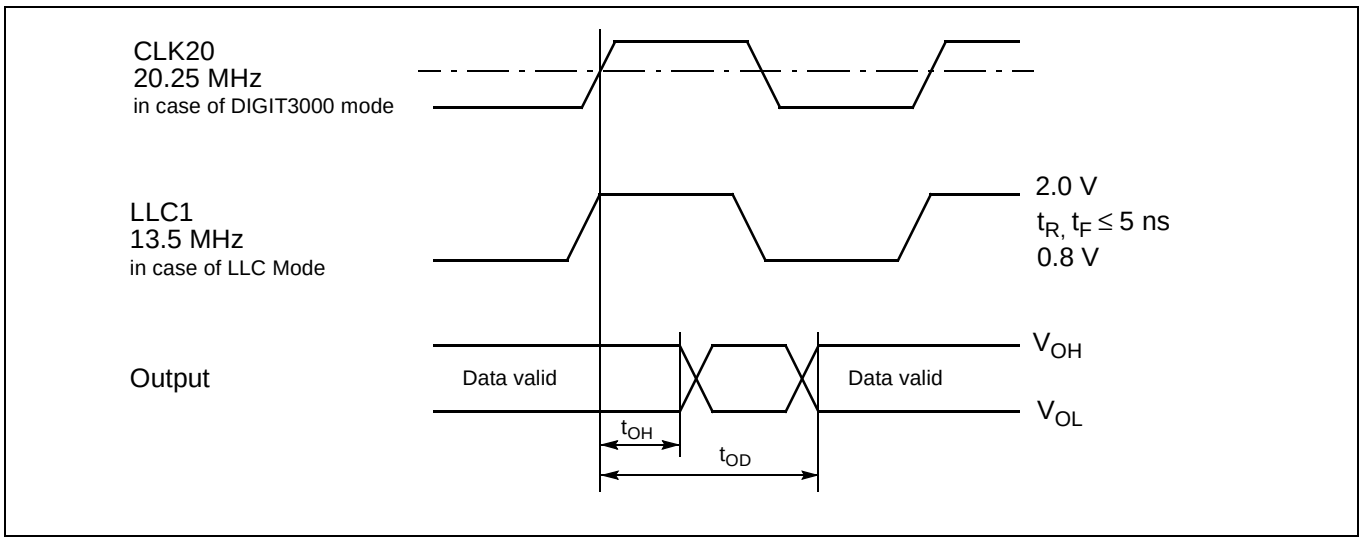


Fig. 4–15: Sync, control, and data outputs

4.6.4.10. Characteristics, Input Pin Specification

Input Specification for SYNC, CONTROL, and DATA Pin: MSY (DIGIT3000 mode only)

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
V_{IL}	Input Low Voltage	–	–	–	0.8	V	
V_{IH}	Input High Voltage	–	1.5	–	–	V	
t_{IS}	Input Setup Time	–	7	–	–	ns	
t_{IH}	Input Hold Time	–	5	–	–	ns	

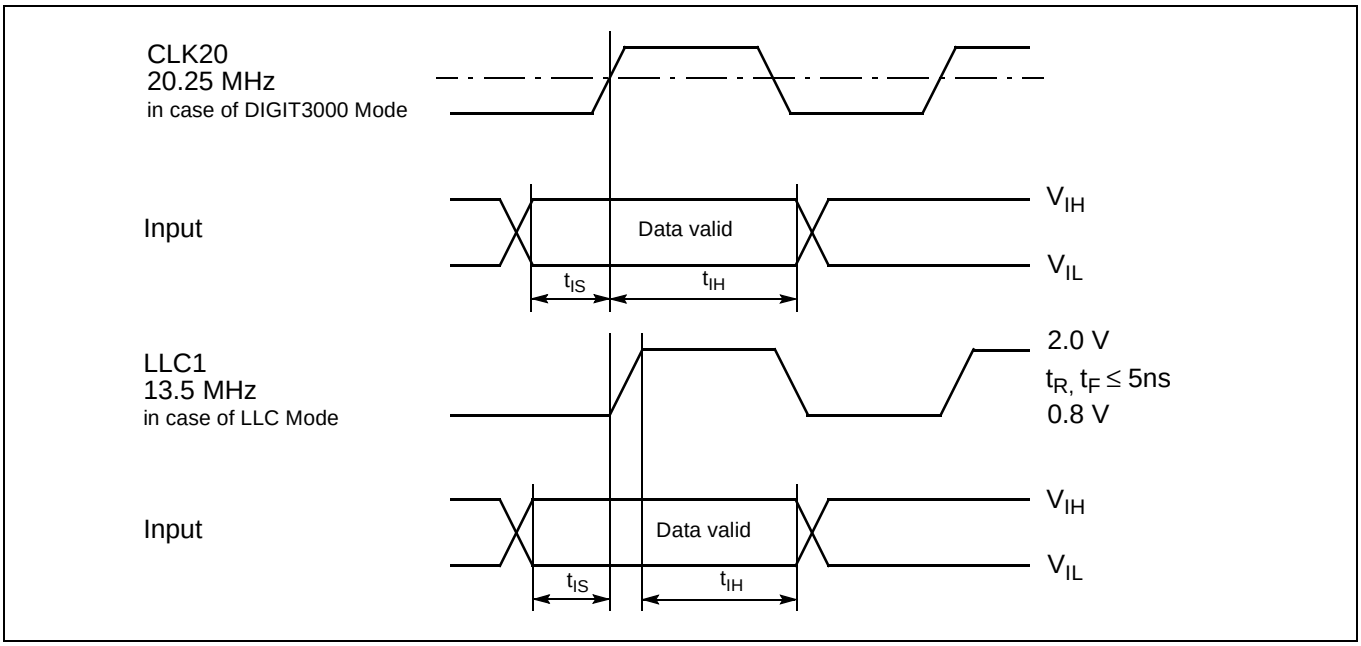


Fig. 4–16: Sync, control, and data inputs

4.6.4.11. Characteristics, Clock Output Specification

Line-Locked Clock Pins: LLC1, LLC2

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
CL	Load capacitance	–	–	–	50	pF	
13.5 MHz Line Locked Clock							
$1/T_{13}$	LLC1 Clock Frequency	–	12.5	–	14.5	MHz	
t_{WL13}	LLC1 Clock Low Time	–	26	–	–	ns	C_L = 30 pF
t_{WH13}	LLC1 Clock High Time	–	26	–	–	ns	C_L = 30 pF
$1/T_{27}$	LLC2 Clock Frequency	–	25	–	29	MHz	
t_{WL27}	LLC2 Clock Low Time	–	10	–	–	ns	C_L = 30 pF
t_{WH27}	LLC2 Clock High Time	–	10	–	–	ns	C_L = 30 pF
16 MHz Line Locked Clock							
$1/T_{13}$	LLC1 Clock Frequency	–	14.8	–	17.2	MHz	
18 MHz Line Locked Clock							
$1/T_{13}$	LLC1 Clock Frequency	–	16.6	–	19.4	MHz	
common timings – all modes							
t_{SK}	Clock Skew	–	0	–	4	ns	
t_R, t_F	Clock Rise/Fall Time	–	–	–	5	ns	C_L = 30 pF
V_{IL}	Input Low Voltage	–	–	–	0.8	V	
V_{IH}	Input High Voltage	–	2.0	–	–	V	
V_{OL}	Output Low Voltage	–	–	–	0.4	V	I_L = 2 mA
V_{OH}	Output High Voltage	–	2.4	–	–	V	I_H = –2 mA

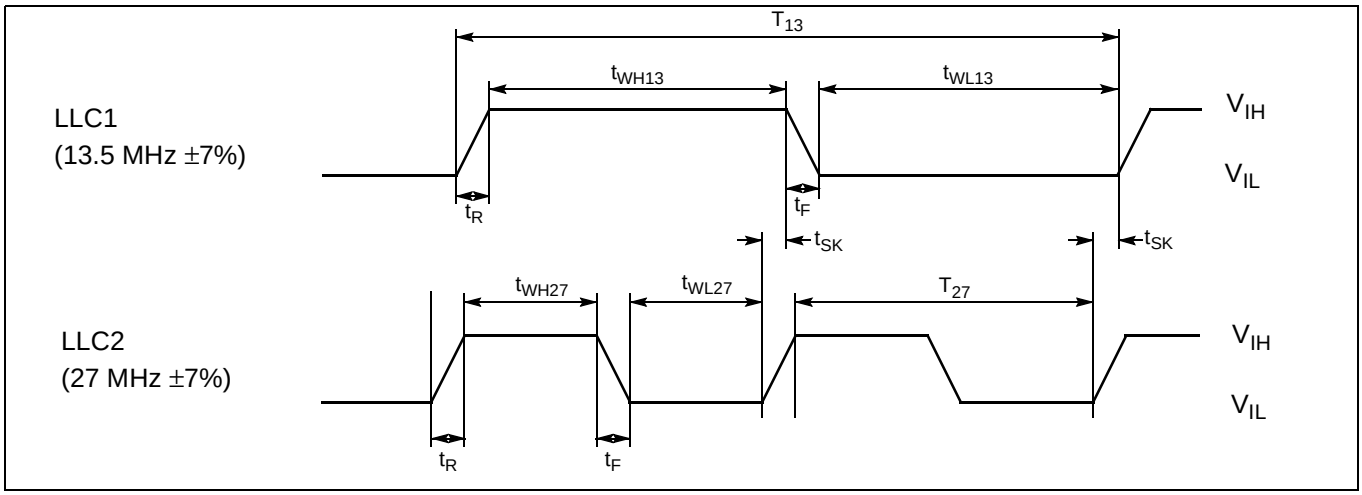
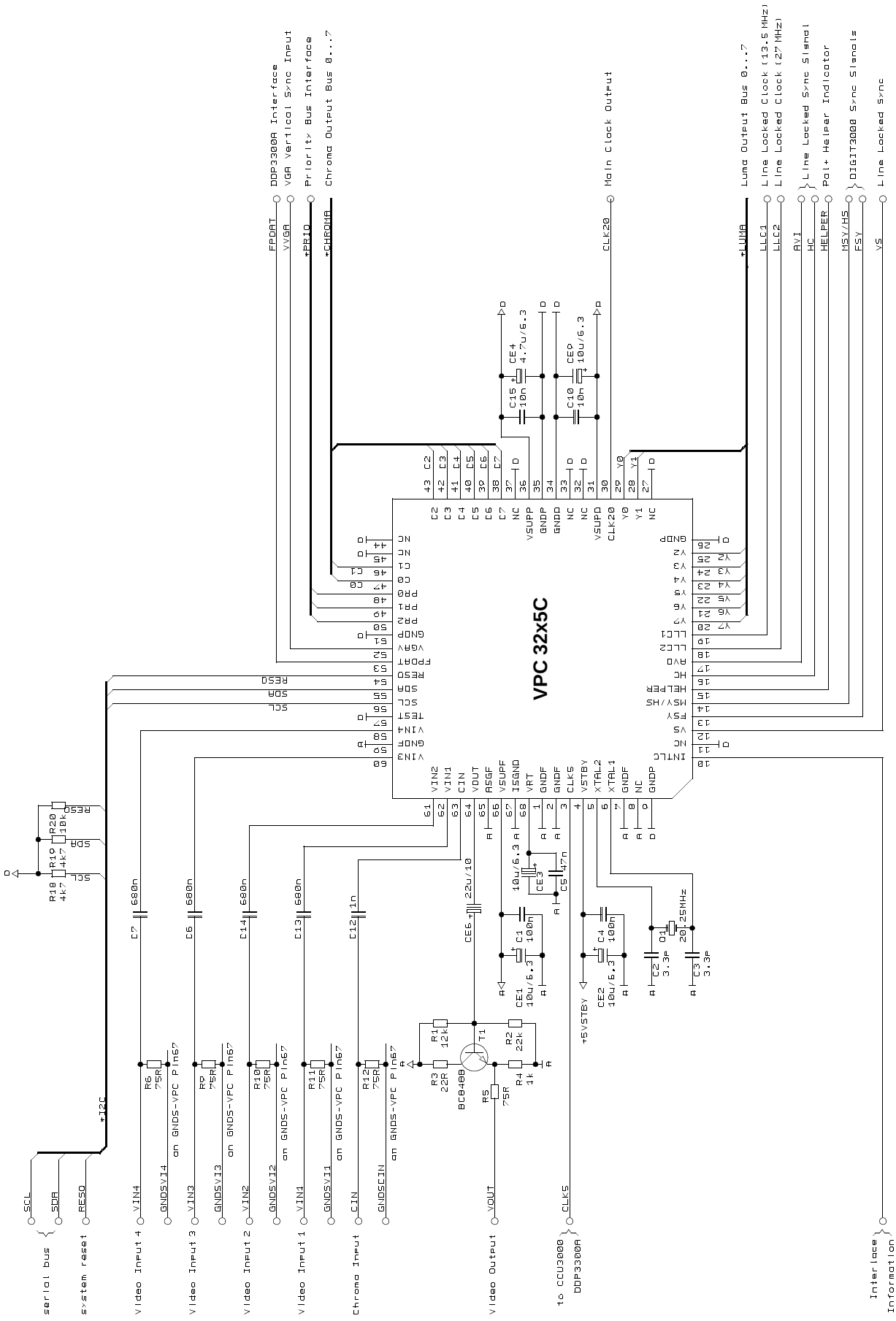


Fig. 4–17: Line-locked clock output pins

5. Application Circuit



5.1. VGA mode with VPC3215C

In 100 Hz TV applications it can be desirable to display a VGA-signal on the TV. In this case a VGA-graphic card delivers the H, V and RGB signals. These signals can be feed "directly" to the backend signal processing. The VPC can generate a stable line locked clock for the 100 Hz system in relation to the VGA sync signals.

While the V-sync is connected to the VGAV pin directly, the H-sync has to be pulse-shaped and amplitude adjusted until it is connected to one of the video input pins of the VPC. The recommended circuitry to filter the H sync is given in the figure below.

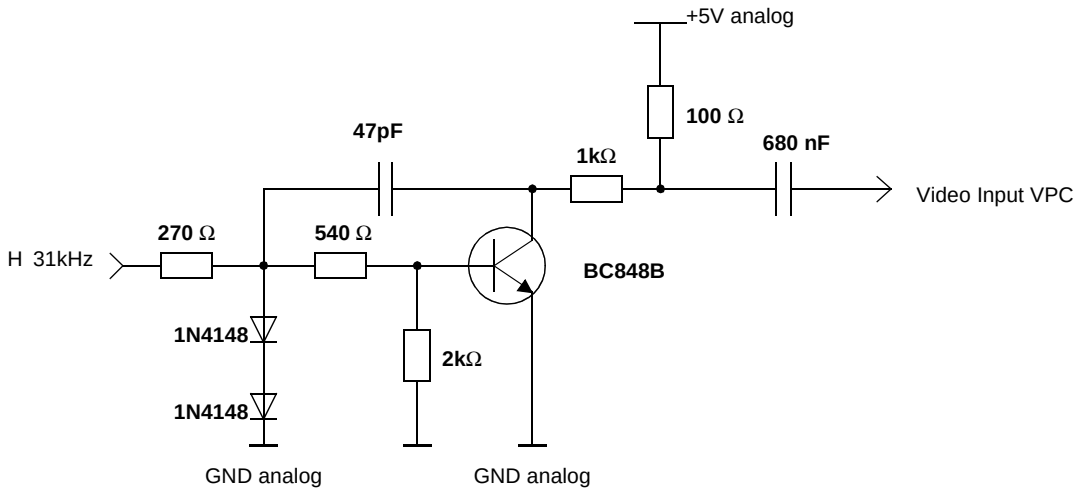


Fig. 5–1: Application circuit for horizontal VGA-input

6. Data Sheet History

1. Preliminary data sheet: “VPC 3205C, VPC 3215C Video Processor Family, Aug. 15, 1997 6251-457-1PD. First release of the preliminary data sheet.

2. Preliminary data sheet: “VPC 3205C, VPC 3215C Video Processor Family, Oct. 19, 1998, 6251-457-2PD. Second release of the preliminary data sheet. Major changes:

– Fig. 4–1: Outline Dimensions for PLCC68 changed.

– Additional information contained in Supplement No.3 / 6251-457-3PDS, Edition May 25 1998 has been included.

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