Ordering number : EN5429A

Wideband Output Module (Video Pack)

VP301

Ultrahigh Resolution CRT Display Video Output Amplifier

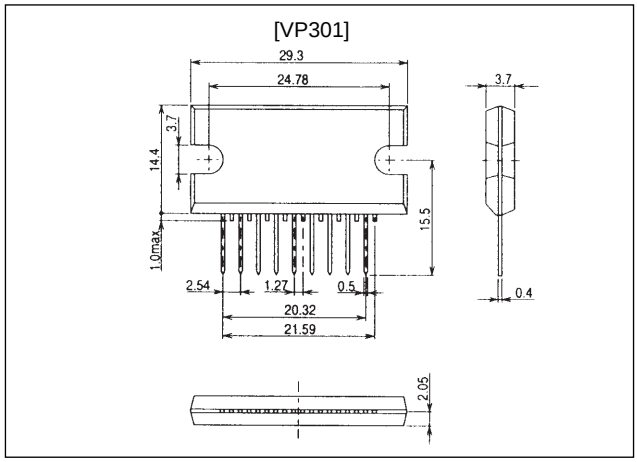
Features

- Ultrahigh frequency, wide bandwidth video output f (–3 dB) = 145 MHz, V_O = 40 to 50 Vp-p
- Molded construction (9 pins)
- Optimal for monitors that require an f_H greater than 90 kHz

Package Dimensions

unit: mm

2136



Specifications

Absolute Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{CC} max		90	V
	V_{BB} max		15	V
Allowable power dissipation	Pd max	Ideal heat sink at Ta = 25°C	25	W
Junction temperature	Tj max		150	°C
Case temperature	Tc		100	°C
Storage temperature	Tstg		–20 to +110	°C

Operating Conditions at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Recommended supply voltage I	V_{CC}		70	V
	V_{BB}		10	V
Recommended supply voltage II	V_{CC}		80	V
	V_{BB}		10	V

Electrical Characteristics at Ta = 25°C

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Frequency band I (–3 dB)	fc	V_{CC} = 70 V, V_{BB} = 10 V, C_L = 5 pF, V_{IN} (DC) = 3.0 V, V_{OUT} (p-p) = 40 V		145		MHz
Frequency band II (–3 dB)	fc	V_{CC} = 80 V, V_{BB} = 10 V, C_L = 5 pF, V_{IN} (DC) = 3.3 V, V_{OUT} (p-p) = 50 V		140		MHz
Impulse response characteristics	t_r	V_{CC} = 80 V, V_{BB} = 10 V, C_L = 5 pF, V_{IN} (DC) = 3.3 V, V_{OUT} (p-p) = 40 V		3.0		ns
	t_f			2.4		ns
Voltage gain	G_V (DC)		13	15	17	double
Current drain I	I_{CC} (1)	V_{CC} = 70 V, V_{BB} = 10 V, V_{IN} (DC) = 2.7 V, f = 10 MHz clock, C_L = 5 pF, V_{OUT} (p-p) = 40 V		65		mA
	I_{CC} (2)	V_{CC} = 70 V, V_{BB} = 10 V, V_{IN} (DC) = 2.7 V, f = 150 MHz clock, C_L = 5 pF, V_{OUT} (p-p) = 40 V		95		mA
Current drain II	I_{CC} (1)	V_{CC} = 80 V, V_{BB} = 10 V, V_{IN} (DC) = 3.0 V, f = 10 MHz clock, C_L = 5 pF, V_{OUT} (p-p) = 50 V		76		mA
	I_{CC} (2)	V_{CC} = 80 V, V_{BB} = 10 V, V_{IN} (DC) = 3.0 V, f = 150 MHz clock, C_L = 5 pF, V_{OUT} (p-p) = 50 V		105		mA

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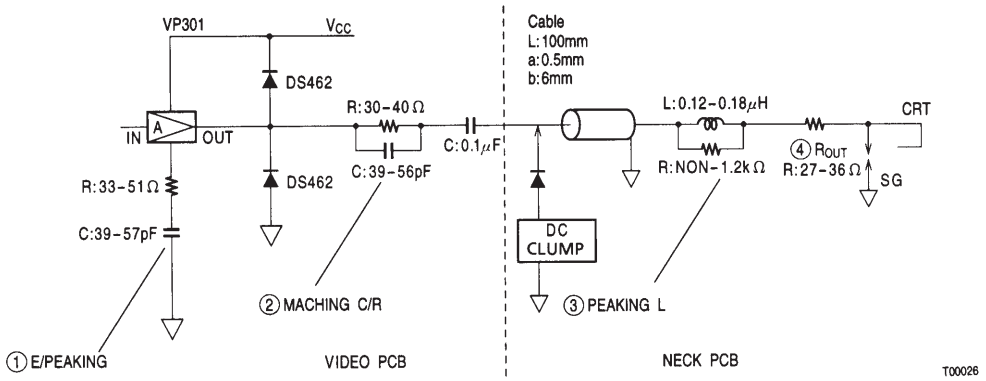
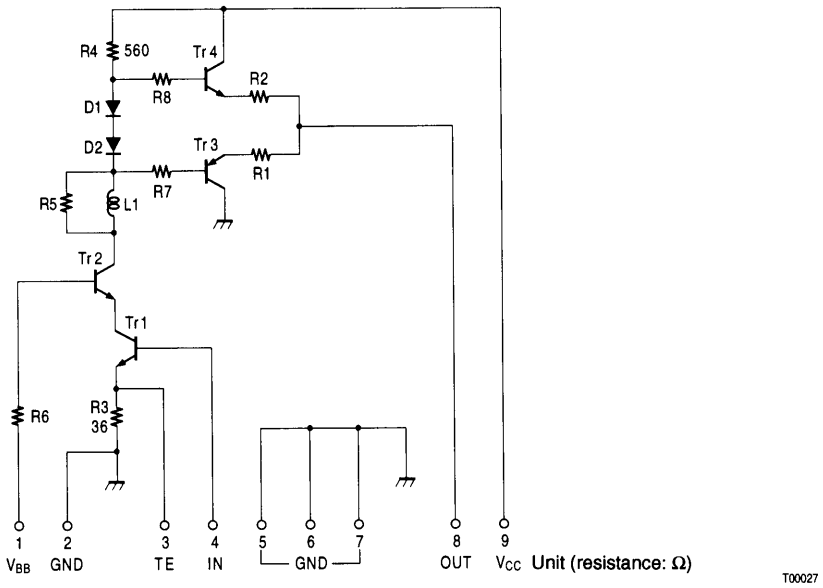
IC Peripheral Circuit (output block) Application Example



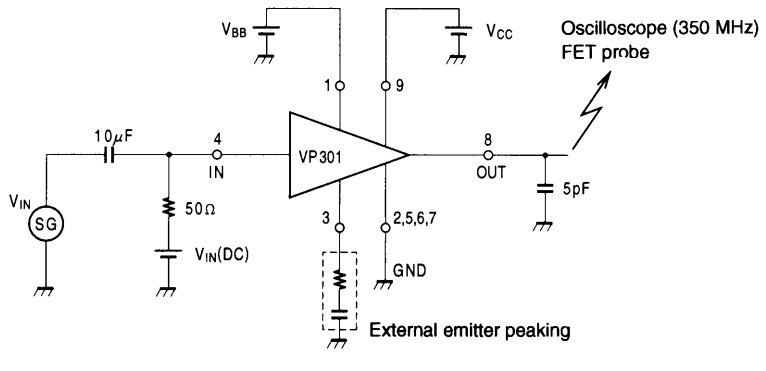
② Matching RC circuit ·····This RC circuit matches the video pack output to the transmission system. It is not required if the total output capacitance Co(total) is no more than 15 pF.

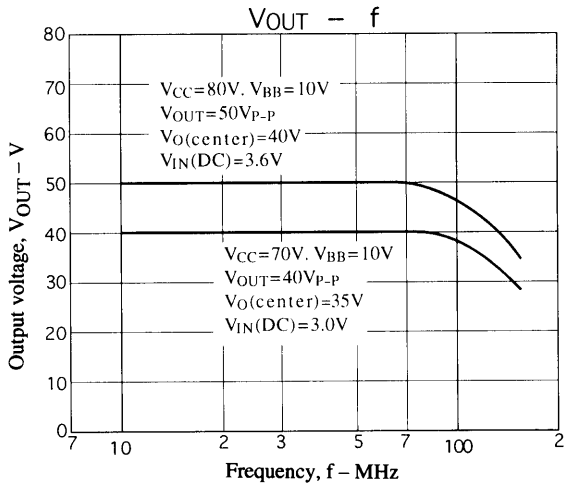
④ R_{OUT}·····Determine the value of this resistor based on the discharge test withstand capacity and the required frequency bandwidth.

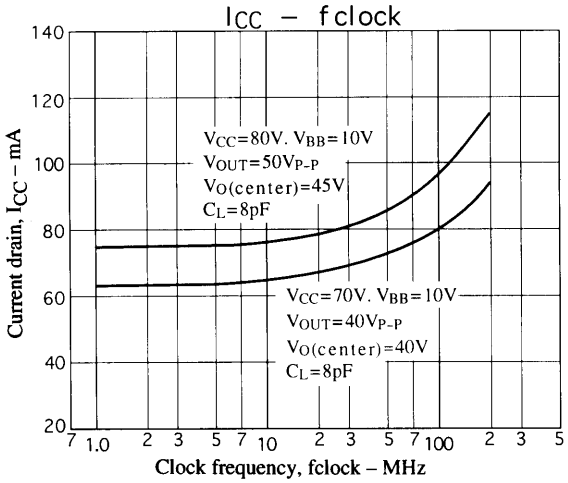
Internal Equivalent Circuit

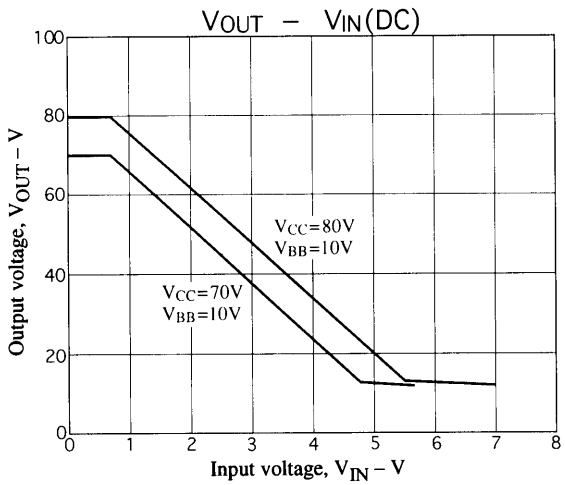


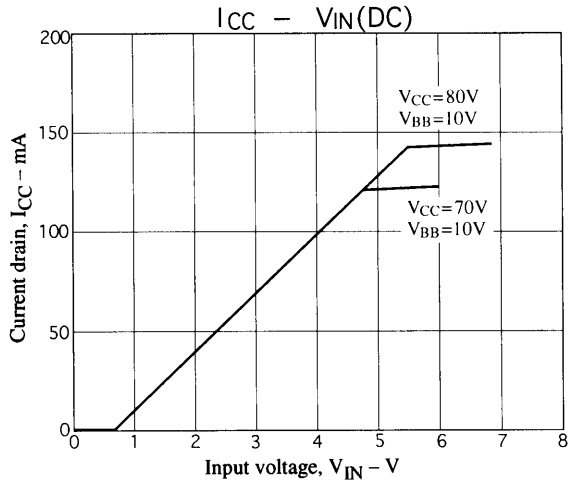
VP301 Test Circuit

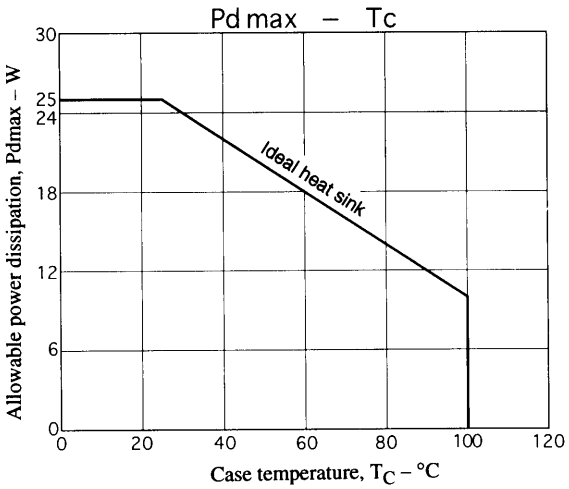



VOUT – f
VCC=80V. VBB=10V
VOUT=50VP-P
VO(center)=40V
VIN(DC)=3.6V
VCC=70V. VBB=10V
VOUT=40VP-P
VO(center)=35V
VIN(DC)=3.0V
Output voltage, VOUT – V
Frequency, f – MHz


ICC – fclock
VCC=80V. VBB=10V
VOUT=50VP-P
VO(center)=45V
CL=8pF
VCC=70V. VBB=10V
VOUT=40VP-P
VO(center)=40V
CL=8pF
Current drain, ICC – mA
Clock frequency, fclock – MHz


VOUT – VIN(DC)
VCC=80V
VBB=10V
VCC=70V
VBB=10V
Output voltage, VOUT – V
Input voltage, VIN – V


ICC – VIN(DC)
VCC=80V
VBB=10V
VCC=70V
VBB=10V
Current drain, ICC – mA
Input voltage, VIN – V


Pd max – Tc
Ideal heat sink
Allowable power dissipation, Pdmax – W
Case temperature, TC – °C

Surge Protection

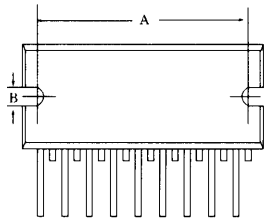
Surge protection is required when this device is connected to a CRT. This product requires the same protection as earlier products.

A. Termination spark gap
B. Surge suppression resistor
C. Surge suppression diode (Installed in the vicinity of the IC output pin.)

Caution: The value of surge suppression resistors must be determined taking both the stipulated discharge test and the required frequency bandwidth into account.

Notes on Mounting

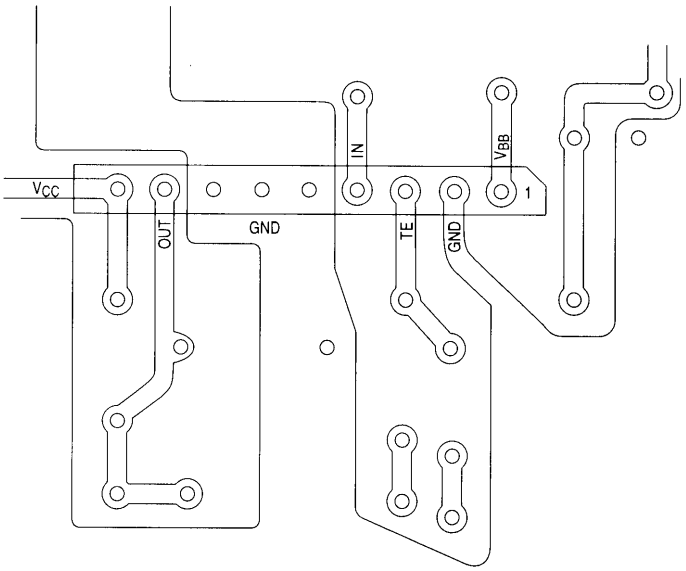
- Heat sink mounting
  Since the specified heat sink is required to operate a mounted video pack, we recommend the following mounting technique. (See the thermal design item for details on the required heat sink.) In particular, since the package used for this product is even more compact than that used in the earlier VPA series, the following points require special care. (These are recommendations.)
  1. A tightening torque of between 39 and 58 N·cm is recommended. Note that 49 N·cm is the standard torque.
  2. The bolt hole spacing in the heat sink should match that of the IC. In particular, the bolt hole spacing should be made as close as possible, within the range that mounting is possible, to the dimensions A and B in the package dimensions drawing, as shown below.



  3. Use either the truss screws (truss bolts) or binding screws (binding bolts) stipulated in the JIS standards as the mounting bolts. Also, use washers to protect the IC case.
  4. Foreign matter, such as machining chips, must not be left trapped between the IC case and the heat sink. If grease is applied to the junction surface, be sure to apply the grease evenly.
  5. Solder the IC leads to the printed circuit board after mounting the heat sink to the IC.

Note: The heat sink is absolutely required to operate this video pack. Never, in any situation, apply power to a video pack as an independent device. The video pack may be destroyed.

- Peripheral wiring and ground leading
- Inputs and outputs must be laid out as direct lines and must not cross.
- If a double-sided printed circuit board is used, the output pattern must not be laid out on the other side of the printed circuit board from the ground pattern, since this would increase the output capacitance.



IC Peripheral Pin Layout (Top view)

Thermal Design
During operation, the transistor junction temperature must remain under 150°C, the maximum junction temperature (Tjmax) for the VP301. The following section presents thermal design data and a thermal design example for the VP301.

Thermal Design for the VP301

The heat generated by the transistors in a video pack varies with the frequency, and also varies between the transistors in the video pack themselves. Here, thermal design consists of selecting a heat sink such that transistor junction temperatures in the worst case do not exceed 150°C.
Taking the upper limit of the operating frequency, 150 MHz (clock) as a representative usage of the VP301, we consider thermal design at this frequency. From Figure 1 we can see that transistor 3 (Tr3 in the SEPP stage) generates the largest amount of heat, and that the loss (heat generation) in this transistor is about 22% of the total loss. The chip temperature of each transistor is determined using the following formula.

$Tj\ (Tri) = \theta j\text{-}c\ (Tri) \times P_C\ (Tri) + \Delta Tc + Ta\ [°C]$ .....Formula (1)

θj-c(Tri): Thermal resistance of an individual transistor*
Pc(Tri): Loss for an individual transistor
ΔTc: Case temperature rise
Ta: Ambient temperature (chassis internal temperature)

* For the VP301, θj-c (Tr1) = 40°C/W, θj-c (Tr2 to Tr4) = 25°C/W .....(a)

Sample Calculation

Thermal resistance, θh, for a heat sink for use at V_{CC} = 80 V, V_{BB} = 10 V, V_O = 50 Vp-p, $_{f = 150\ MHz}$ (clock) at temperatures up to 60°C.
Considering figures 1 and 2, we focus on transistor 3 and determine the temperature.
The loss in transistor 3, PC(Tr3), can be estimated using the value of Pd(total) from Figure 2 to be:

$P_C\ (Tr3) = Pd\ (total)_{\ f = 150\ MHz} \times P_C ratio\ (Tr3) = 8.3 \times 0.22$ .....Formula (2)
≈ 1.83 [W]

From formula (1) and (a) the temperature rise for the transistor, ΔTj(Tr3) can be calculated to be:

$\Delta Tj\ (Tr3) = \theta j\text{-}c\ (Tr3) \times P_C\ (Tr3) = 25 \times 1.83$ .....Formula (3)
$= 45.75$ [°C]

Since Tc(max) = 100°C and Tj(max) = 150°C = ΔTj + Tc(max),
it suffices to determine a thermal resistance for the heat sink so that Tc(max) does not exceed 100°C.
Assuming operation at an ambient temperature of Ta = 60°C, the allowable case temperature rise will be: ΔTc = 100 – 60 = 40°C. Therefore,

$\therefore \theta h = \Delta Tc \div Pd\ (total)_{\ f = 150\ MHz} = 40 \div 8.3$ .....Formula (4)
And this is: = 4.8[°C/W]

Note: The above calculation assumes 100% operation at the clock frequency. However, since CRT operation also includes blanking periods, clock operation can be expected to be about 80% of the time. Since video packs are operated at close to the cutoff state during blanking periods, the loss during this period can be assumed to be zero, and the total loss, Pd(total), will be:

$Pd\ (total)_{\ f = 150\ MHz} = Pd\ (total)_{\ f = 150\ MHz} \times 0.8 = 8.3 \times 0.8$
$= 6.64$ [W]

Thus the heat sink can be made smaller than the one calculated above. We recommend performing a full thermal designs based on the actual operating conditions.

Figure 1 Pc(ratio) – f clock

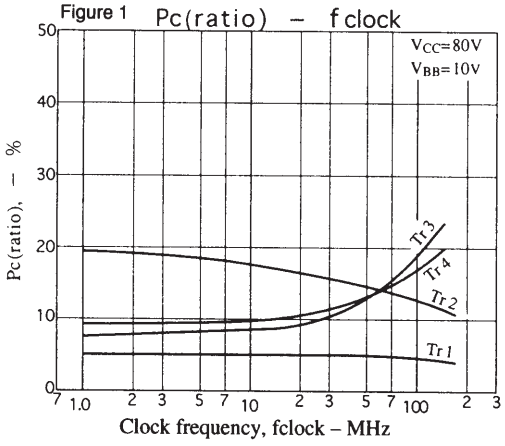


Figure 2 Pd – f clock