

Features:

- 155.52 MHz SAW-based LVPECL output
- RoHS Compliant
- Low Profile Surface Mount Package
- Excellent solder reflow performance
- PCB Substrate for excellent TCE match
- Non-peaking Attenuation Response

Description and applications:

Surface mount 15.9 mm SQ frequency translator operating at a 3.3V supply with complementary LVPECL outputs for use in telecom & datacom

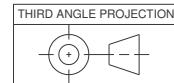
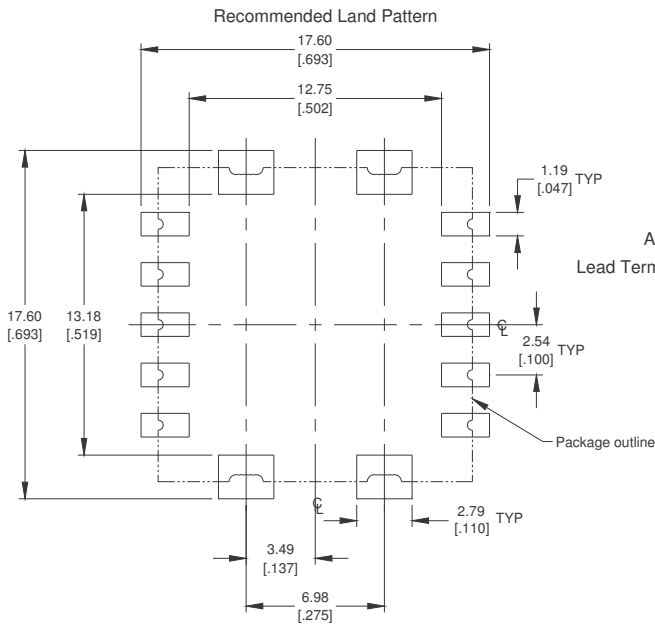
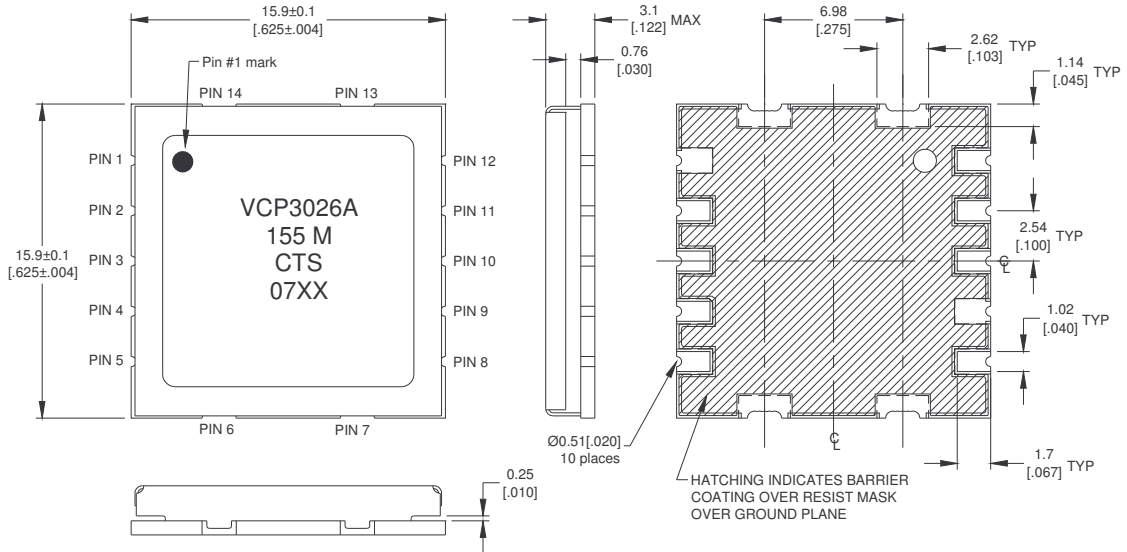
- See WWW.CTSCORP.COM for product patent status.



Electrical Specifications:

VCP3026A	Specification									
Input frequency	38.88 MHz									
Output frequency	155.52 MHz									
Supply Voltage ($\pm 5\%$)	3.3V									
PECL input	400 mV min. peak-to-peak									
PECL output	<table border="1"> <thead> <tr> <th></th> <th>Min.</th> <th>Max.</th> </tr> </thead> <tbody> <tr> <td>Logic "0"</td> <td>1.49V</td> <td>1.68V</td> </tr> <tr> <td>Logic "1"</td> <td>2.28V</td> <td>2.42V</td> </tr> </tbody> </table>		Min.	Max.	Logic "0"	1.49V	1.68V	Logic "1"	2.28V	2.42V
	Min.	Max.								
Logic "0"	1.49V	1.68V								
Logic "1"	2.28V	2.42V								
Output Duty Cycle	45/55% max									
Current Drain	95 mA max.									
Operating Temperature	-40 to 85°C									
Input frequency tracking capability	+/- 32 ppm minimum									
Peaking	< 0.1 dB									
Jitter attenuation	<ul style="list-style-type: none"> > -0.5 dB @ 100 Hz offset > -27 dB @ 1 kHz offset 									
RMS phase jitter generation (12 kHz to 50 MHz)	<ul style="list-style-type: none"> < 1 psec max. < .5 psec typical 									

Mechanical Dimensions (mm):
15.9mm x 15.9mm x 3.1mm (max.):



All dimensions are in MM [Inches].
 All dimensions are nominal unless otherwise specified.
 Lead Termination Finish: Gold Flash, <10 micro inch, over Ni plated Cu.

PIN OUT

Pin	Symbol	Function
1	LD	Lock detect Logic "1" indicates a locked condition (CMOS level $\geq V_{dd}-0.04$) Logic "0" indicates that no input signal is present or the input signal has moved out of the lock range (CMOS Level $\leq 0.4V$)
2	IN	Input frequency
3	/IN	NC: not connected internally
4	GND	Ground
5	E/D	Enable/ disable Logic "0" = output disabled (CMOS Level $\leq 0.4V$) Logic "1" = output enabled (CMOS Level $\geq V_{dd}-0.4 V$)
6	Gnd	Ground
7	Gnd	Ground
8	/OUT	Complementary output
9	OUT	Output
10	Vcc	Power supply voltage
11	N/C	No connection
12	Gnd	Ground
13	Gnd	Ground
14	Gnd	Ground

Solder Reflow Conditions

Device is capable of withstanding reflow of 260 degrees C for 10 seconds maximum.

Moisture Sensitivity: **MSL 1**

RoHS: **This device is fully compliant to RoHS Directive 2002/95/EC.**