

Features

- **Low-power consumption**
 - Active: 25mA at 70ns
 - Stand-by: 10 μ A (CMOS input/output)
2 μ A CMOS input/output, L version
- **Single + 1.8 to 2.2V Power Supply**
- **Equal access and cycle time**
- **70/85/100/150 ns access time**
- **Easy memory expansion with $\overline{CE1}$, CE2 and \overline{OE} inputs**
- **1.0V data retention mode**
- **TTL compatible, Tri-state input/output**
- **Automatic power-down when deselected**
- **Package available: 32-TSOP1 / STSOP**

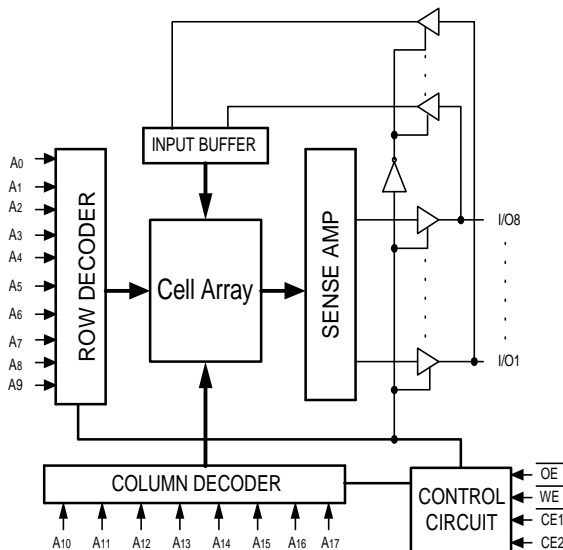
Functional Description

The V62C1802048L is a low power CMOS Static RAM organized as 262,144 words by 8 bits. Easy memory expansion is provided by an active LOW $\overline{CE1}$, an active HIGH CE2, an active LOW \overline{OE} , and Tri-state I/O's. This device has an automatic power-down mode feature when deselected.

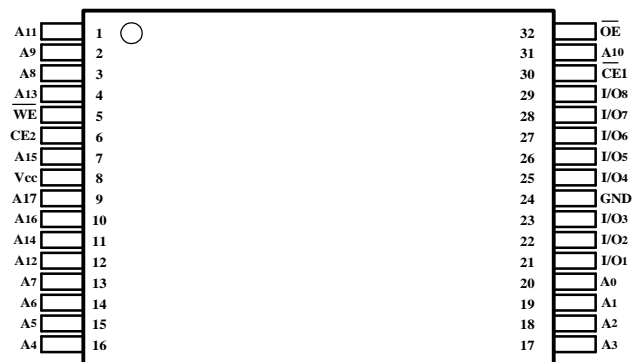
Writing to the device is accomplished by taking Chip Enable 1 ($\overline{CE1}$) with Write Enable (\overline{WE}) LOW, and Chip Enable 2 (CE2) HIGH. Reading from the device is performed by taking Chip Enable 1 ($\overline{CE1}$) with Output Enable (\overline{OE}) LOW while Write Enable (\overline{WE}) and Chip Enable 2 (CE2) is HIGH. The I/O pins are placed in a high-impedance state when the device is deselected: the outputs are disabled during a write cycle.

The V62C1802048LL comes with a 1V data retention feature and Lower Standby Power. The V62C1802048L is available in a 32-pin 8 x 13.4 & 8 x 20 mm TSOP1 / STSOP packages.

Logic Block Diagram



32-Pin TSOP1 / STSOP



Absolute Maximum Ratings *

| Parameter | Symbol | Minimum | Maximum | Unit |
|------------------------------------|----------------|---------|---------|------|
| Voltage on Any Pin Relative to Gnd | Vt | -0.5 | 4.6 | V |
| Power Dissipation | P _T | – | 1.0 | W |
| Storage Temperature (Plastic) | Tstg | -55 | +150 | °C |
| Temperature Under Bias | Tbias | -40 | +85 | °C |

* **Note:** Stresses greater than those listed above Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any conditions outside those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Truth Table

| CE1 | CE2 | WE | OE | Data | Mode |
|-----|-----|----|----|----------|------------------------|
| H | X | X | X | High-Z | Standby |
| X | L | X | X | High-Z | Standby |
| L | H | H | L | Data Out | Active, Read |
| L | H | H | H | High-Z | Active, Output Disable |
| L | H | L | X | Data In | Active, Write |

* **Key:** X = Don't Care, L = Low, H = High

Recommended Operating Conditions (T_A = 0°C to +70°C / -40°C to 85°C)**

| Parameter | Symbol | Min | Typ | Max | Unit |
|----------------|-----------------|-------|-----|-----------------------|------|
| Supply Voltage | V _{CC} | 1.8 | 2.0 | 2.2 | V |
| | Gnd | 0.0 | 0.0 | 0.0 | V |
| Input Voltage | V _{IH} | 1.6 | - | V _{CC} + 0.2 | V |
| | V _{IL} | -0.5* | - | 0.4 | V |

* V_{IL} min = -1.0V for pulse width less than t_{RC}/2.

** For Industrial Temperature.

DC Operating Characteristics ($V_{CC} = 1.8$ to $2.2V$, $Gnd = 0V$, $T_A = 0^{\circ}C$ to $+70^{\circ}C$ / $-40^{\circ}C$ to $85^{\circ}C$)

| Parameter | Sym | Test Conditions | -70 | | -85 | | -100 | | -150 | | Unit |
|---|------------|--|-----|-----|-----|-----|------|-----|------|-----|---------|
| | | | Min | Max | Min | Max | Min | Max | Min | Max | |
| Input Leakage Current | $ I_{LI} $ | $V_{CC} = Max,$ $V_{in} = Gnd$ to V_{CC} | - | 1 | - | 1 | - | 1 | - | 1 | μA |
| Output Leakage Current | $ I_{LO} $ | $\overline{CE1} = V_{IH}$ or $CE2 = V_{IL}$ $V_{CC} = Max, V_{OUT} = Gnd$ to V_{CC} | - | 1 | - | 1 | - | 1 | - | 1 | μA |
| Operating Power Supply Current | I_{CC} | $\overline{CE1} = V_{IL}, CE2 = V_{IH}$ $V_{IN} = V_{IH}$ or $V_{IL}, I_{OUT} = 0mA$ | - | 3 | - | 3 | - | 3 | - | 3 | mA |
| Average Operating Current | I_{CC1} | $\overline{CE1} = V_{IL}, CE2 = V_{IH}$ $I_{OUT} = 0mA,$ Min Cycle, 100% Duty | - | 20 | - | 20 | - | 15 | - | 15 | mA |
| | I_{CC2} | $\overline{CE1} = 0.2V,$ $CE2 = V_{CC} - 0.2V$ $I_{OUT} = 0mA,$ Cycle Time=1 μs , 100% Duty | - | 3 | - | 3 | - | 3 | - | 3 | mA |
| Standby Power Supply Current (TTL Level) | I_{SB} | $\overline{CE1} = V_{IH}$ or $CE2 = V_{IL}$ | - | 0.3 | - | 0.3 | - | 0.3 | - | 0.3 | mA |
| Standby Power Supply Current (CMOS Level) | I_{SB1} | $\overline{CE1} \geq V_{CC} - 0.2V$ or $CE2 \leq 0.2V, f = 0$ $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$ | - | 10 | - | 10 | - | 10 | - | 10 | μA |
| | | L | - | 2 | - | 2 | - | 2 | - | 2 | μA |
| Output Low Voltage | V_{OL} | $I_{OL} = 2 mA$ | - | 0.4 | - | 0.4 | - | 0.4 | - | 0.4 | V |
| Output High Voltage | V_{OH} | $I_{OH} = -1 mA$ | 1.6 | - | 1.6 | - | 1.6 | - | 1.6 | - | V |

Capacitance ($f = 1MHz, T_A = 25^{\circ}C$)

| Parameter* | Symbol | Test Condition | Max | Unit |
|-------------------|-----------|-------------------------|-----|------|
| Input Capacitance | C_{in} | $V_{in} = 0V$ | 7 | pF |
| I/O Capacitance | $C_{I/O}$ | $V_{in} = V_{out} = 0V$ | 8 | pF |

* This parameter is guaranteed by device characterization and is not production tested.

AC Test Conditions

Input Pulse Level 0.4V to 1.6V
 Input Rise and Fall Time 5ns
 Input and Output Timing
 Reference Level 50% of input level
 $(V_{IL} + V_{IH})/2$

Output Load Condition

70ns/85 ns $C_L = 30pf + 1TTL$ Load
 Load 100ns/150 ns $C_L = 100pf + 1TTL$ Load

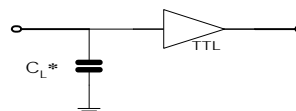


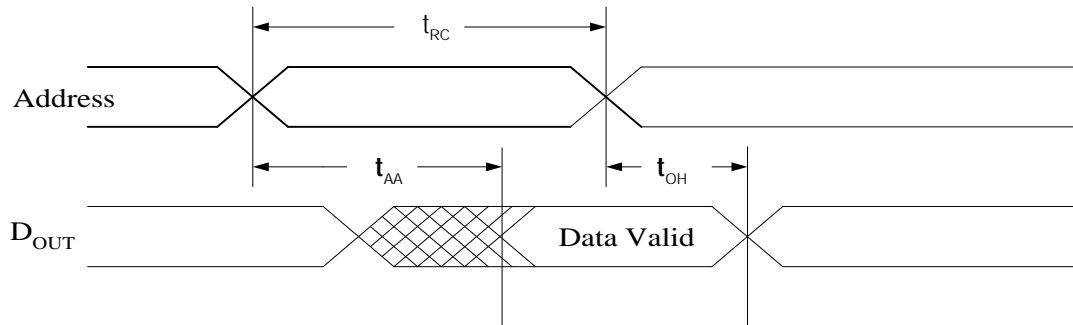
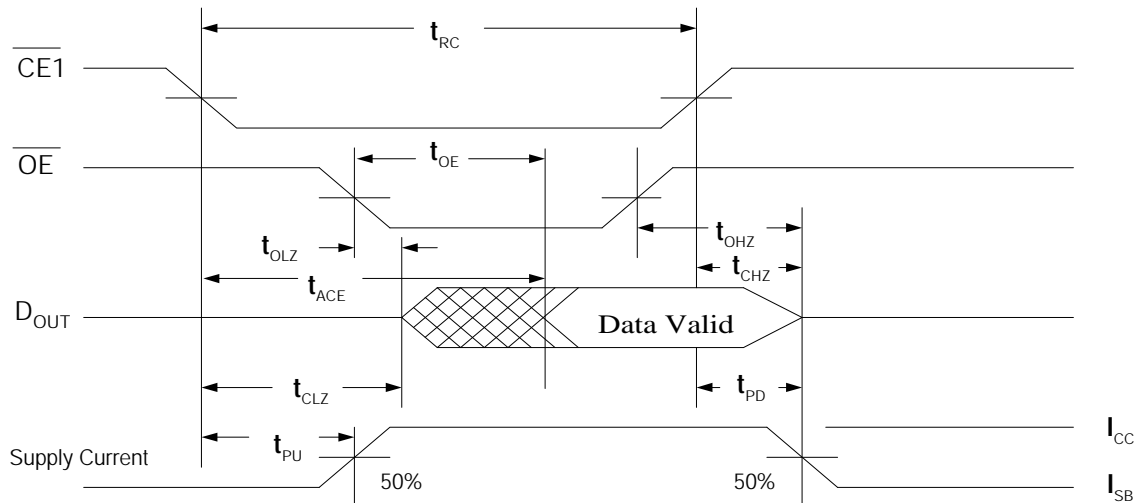
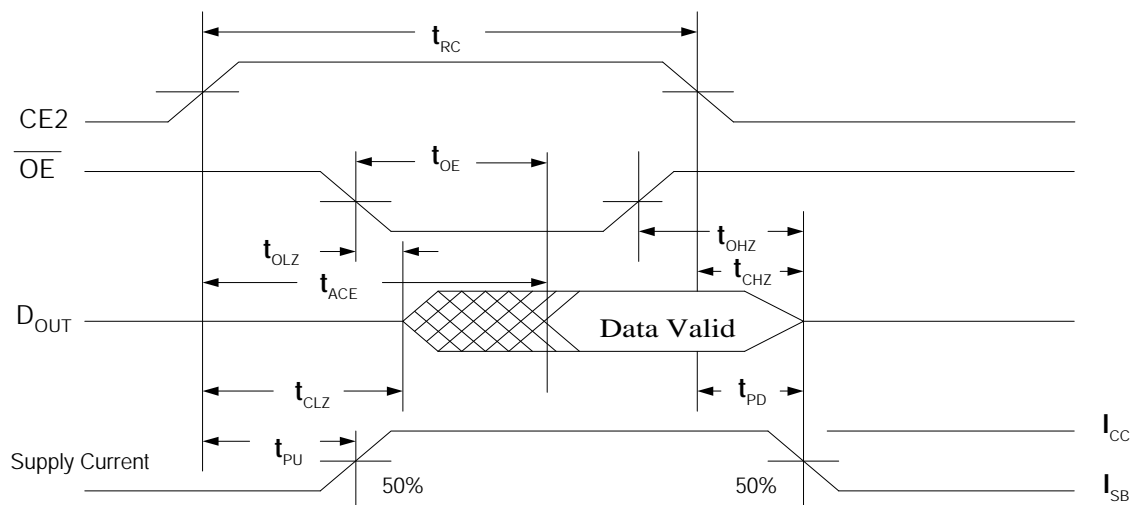
Figure A. * Including Scope and Jig Capacitance

Read Cycle ^(3,9) ($V_{cc} = 1.8$ to $2.2V$, $Gnd = 0V$, $T_A = 0^{\circ}C$ to $+70^{\circ}C$ / $-40^{\circ}C$ to $+85^{\circ}C$)

| Parameter | Symbol | -70 | | -85 | | -100 | | -150 | | Unit | Note |
|------------------------------------|-----------|-----|-----|-----|-----|------|-----|------|-----|------|------|
| | | Min | Max | Min | Max | Min | Max | Min | Max | | |
| Read Cycle Time | t_{RC} | 70 | - | 85 | - | 100 | - | 150 | - | ns | |
| Address Access Time | t_{AA} | - | 70 | - | 85 | - | 100 | - | 150 | ns | |
| Chip Enable Access Time | t_{ACE} | - | 70 | - | 85 | - | 100 | - | 150 | ns | |
| Output Enable Access Time | t_{OE} | - | 40 | - | 40 | - | 50 | - | 70 | ns | |
| Output Hold from Address Change | t_{OH} | 10 | - | 10 | - | 10 | - | 10 | - | ns | |
| Chip Enable to Output in Low-Z | t_{CLZ} | 10 | - | 10 | - | 10 | - | 10 | - | ns | 4,5 |
| Chip Disable to Output in High-Z | t_{CHZ} | - | 30 | - | 35 | - | 40 | - | 50 | ns | 4,5 |
| Output Enable to Output in Low-Z | t_{OLZ} | 5 | - | 5 | - | 5 | - | 5 | - | ns | 4,5 |
| Output Disable to Output in High-Z | t_{OHZ} | - | 25 | - | 30 | - | 35 | - | 40 | ns | 4,5 |
| Power-Up Time | t_{PU} | 0 | - | 0 | - | 0 | - | 0 | - | ns | 5 |
| Power-Down Time | t_{PD} | - | 70 | - | 85 | - | 100 | - | 150 | ns | 5 |

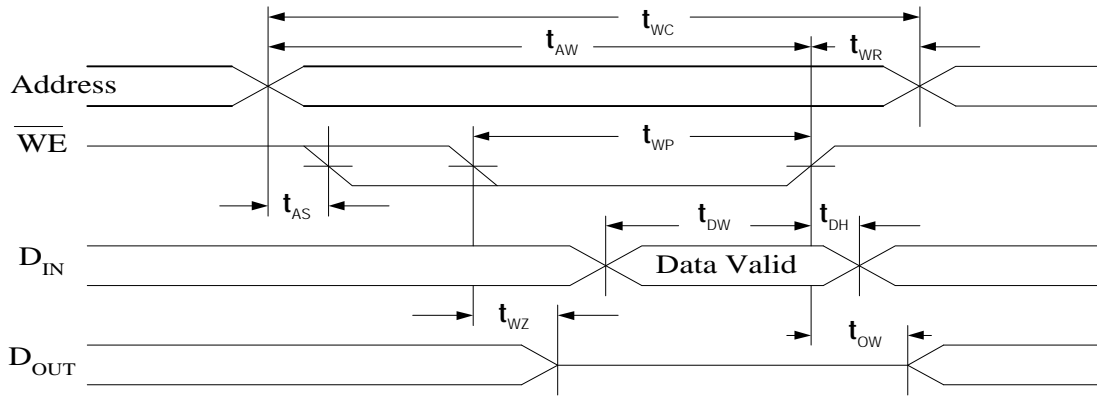
Write Cycle ^(3,11) ($V_{cc} = 1.8$ to $2.2V$, $Gnd = 0V$, $T_A = 0^{\circ}C$ to $+70^{\circ}C$ / $-40^{\circ}C$ to $+85^{\circ}C$)

| Parameter | Symbol | -70 | | -85 | | -100 | | -150 | | Unit | Note |
|----------------------------------|----------|-----|-----|-----|-----|------|-----|------|-----|------|------|
| | | Min | Max | Min | Max | Min | Max | Min | Max | | |
| Write Cycle Time | t_{WC} | 70 | - | 85 | - | 100 | - | 150 | - | ns | |
| Chip Enable to Write End | t_{CW} | 60 | - | 70 | - | 80 | - | 120 | - | ns | |
| Address Setup to Write End | t_{AW} | 60 | - | 70 | - | 80 | - | 120 | - | ns | |
| Address Setup Time | t_{AS} | 0 | - | 0 | - | 0 | - | 0 | - | ns | |
| Write Pulse Width | t_{WP} | 50 | - | 60 | - | 70 | - | 100 | - | ns | |
| Write Recovering Time | t_{WR} | 0 | - | 0 | - | 0 | - | 0 | - | ns | |
| Data Valid to Write End | t_{DW} | 30 | - | 35 | - | 40 | - | 60 | - | ns | |
| Data Hold Time | t_{DH} | 0 | - | 0 | - | 0 | - | 0 | - | ns | |
| Write Enable to Output in High-Z | t_{WZ} | - | 30 | - | 35 | - | 40 | - | 50 | ns | 4,5 |
| Output Active from Write End | t_{OW} | 5 | - | 5 | - | 5 | - | 5 | - | ns | 4,5 |

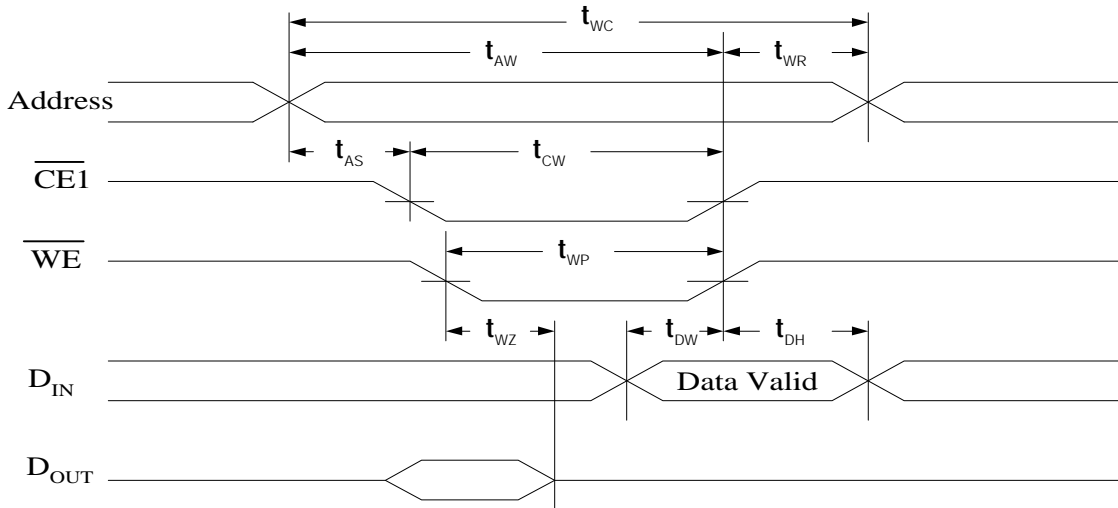
Timing Waveform of Read Cycle 1 ^(3,6,7,9) (Address Controlled)

Timing Waveform of Read Cycle 2 ^(5,6,8,9) ($\overline{CE1}$ Controlled)

Timing Waveform of Read Cycle 3 ^(3,6,8,9) (CE2 Controlled)




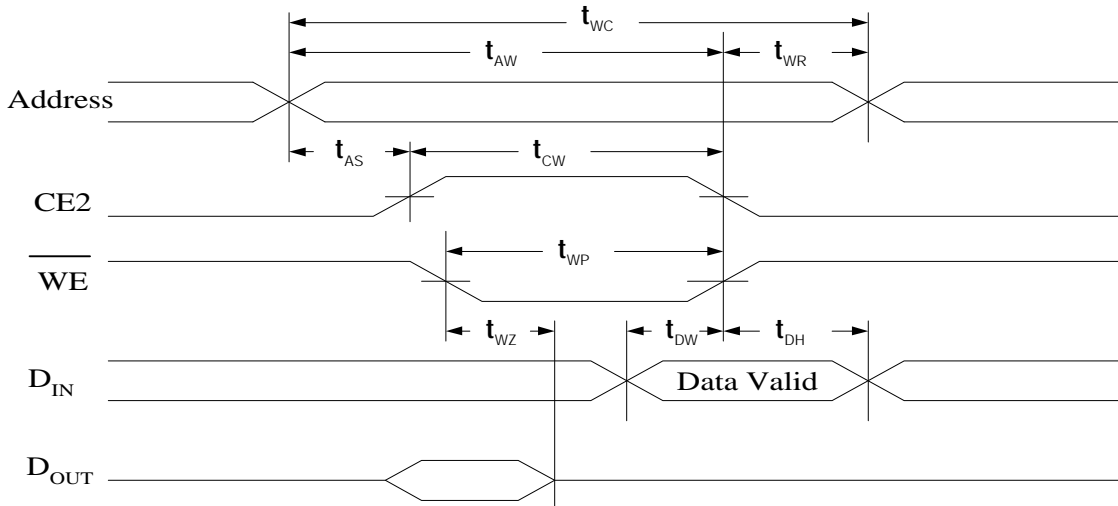
Timing Waveform of Write Cycle 1 ^(10,11) (\overline{WE} Controlled)



Timing Waveform of Write Cycle 2 ^(10,11) ($\overline{CE1}$ Controlled)

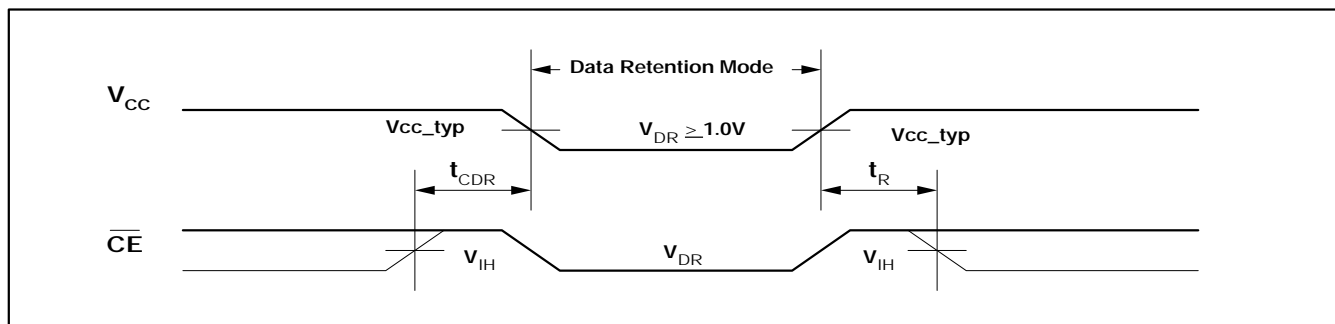


Timing Waveform of Write Cycle 3 ^(10,11) (CE2 Controlled)



Data Retention Characteristics (L Version Only)⁽¹⁾

| Parameter | Symbol | Test Condition | Min | Max | Unit |
|--|-------------------|---|-----------------|-----|------|
| V _{CC} for Data Retention | V _{DR} | $\overline{CE}_1 \geq V_{CC} - 0.2V$ or | 1.0 | - | V |
| Data Retention Current | I _{CCDR} | $CE_2 \leq +0.2V$ | | 1 | μA |
| Chip Deselect to Data Retention Time | t _{CDR} | $V_{IN} \geq V_{CC} - 0.2V$ or | 0 | - | ns |
| Operation Recovery Time ⁽²⁾ | t _R | $V_{IN} \leq 0.2V$ | t _{RC} | - | ns |

Data Retention Waveform (L Version Only) (T_A = 0⁰C to +70⁰C / -40⁰C to +85⁰C)

Notes

1. L-version includes this feature.
2. This Parameter is samples and not 100% tested.
3. For test conditions, see *AC Test Condition*, Figure A.
4. This parameter is tested with CL = 5pF as shown in Figure B. Transition is measured ± 500mV from steady-state voltage.
5. This parameter is guaranteed, but is not tested.
6. \overline{WE} is HIGH for read cycle.
7. $\overline{CE1}$ and \overline{OE} are LOW and CE2 is HIGH for read cycle.
8. Address valid prior to or coincident with $\overline{CE1}$ transition LOW or CE2 transition HIGH.
9. All read cycle timings are referenced from the last valid address to the first transition address.
10. $\overline{CE1}$ or \overline{WE} must be HIGH or CE2 must be LOW during address transition.
11. All write cycle timings are referenced from the last valid address to the first transition address.

Ordering Information

| Device Type* | Speed | Package |
|---------------------|--------------|--------------------------------|
| V62C1802048L-70V | 70 ns | 8x13.4 mm 32-pin Plastic STSOP |
| V62C1802048L-85V | 85 ns | |
| V62C1802048L-100V | 100 ns | |
| V62C1802048L-150V | 150 ns | |
| V62C1802048LL-70V | 70 ns | |
| V62C1802048LL-85V | 85 ns | |
| V62C1802048LL-100V | 100 ns | |
| V62C1802048LL-150V | 150 ns | |
| V62C1802048L-70T | 70 ns | 8 x 20 mm 32-pin Plastic TSOP1 |
| V62C1802048L-85T | 85 ns | |
| V62C1802048L-100T | 100 ns | |
| V62C1802048L-150T | 150 ns | |
| V62C1802048LL-70T | 70 ns | |
| V62C1802048LL-85T | 85 ns | |
| V62C1802048LL-100T | 100 ns | |
| V62C1802048LL-150T | 150 ns | |

* For Industrial Temperature tested devices, an "I" designator will be added to the end of the Device number.

U.S.A.

3910 NORTH FIRST STREET
SAN JOSE, CA 95134
PHONE: 408-433-6000
FAX: 408-433-0952

TAIWAN

7F, NO. 102
MIN-CHUAN E. ROAD, SEC. 3
TAIPEI
PHONE: 886-2-2545-1213
FAX: 886-2-2545-1209

SINGAPORE

10 ANSON ROAD #23-13
INTERNATIONAL PLAZA
SINGAPORE 079903
PHONE: 65-3231801
FAX: 65-3237013

UK & IRELAND

SUITE 50, GROVEWOOD
BUSINESS CENTRE
STRATHCLYDE BUSINESS
PARK
BELLSHILL, LANARKSHIRE,
SCOTLAND, ML4 3NQ
PHONE: 44-1698-748515
FAX: 44-1698-748516

NO 19 LI HSIN ROAD
SCIENCE BASED IND. PARK
HSIN CHU, TAIWAN, R.O.C.
PHONE: 886-3-579-5888
FAX: 886-3-566-5888

JAPAN

ONZE 1852 BUILDING 6F
2-14-6 SHINTOMI, CHUO-KU
TOKYO 104-0041
PHONE: 03-3537-1400
FAX: 03-3537-1402

**GERMANY
(CONTINENTAL
EUROPE & ISRAEL)**

BENZSTRASSE 32
71083 HERRENBERG
GERMANY
PHONE: +49 7032 2796-0
FAX: +49 7032 2796 22

U.S. SALES OFFICES**NORTHWESTERN**

3910 NORTH FIRST STREET
SAN JOSE, CA 95134
PHONE: 408-433-6000
FAX: 408-433-0952

SOUTHWESTERN

302 N. EL CAMINO REAL #200
SAN CLEMENTE, CA 92672
PHONE: 949-361-7873
FAX: 949-361-7807

**CENTRAL,
NORTHEASTERN &
SOUTHEASTERN**

604 FIELDWOOD CIRCLE
RICHARDSON, TX 75081
PHONE: 214-826-6176
FAX: 214-828-9754

The information in this document is subject to change without notice.

MOSEL VITELIC makes no commitment to update or keep current the information contained in this document. No part of this document may be copied or reproduced in any form or by any means without the prior written consent of MOSEL-VITELIC.

MOSEL VITELIC subjects its products to normal quality control sampling techniques which are intended to provide an assurance of high quality products suitable for usual commercial applications. MOSEL VITELIC does not do testing appropriate to provide 100% product quality assurance and does not assume any liability for consequential or incidental arising from any use of its products. If such products are to be used in applications in which personal injury might occur from failure, purchaser must do its own quality assurance testing appropriate to such applications.