V61C5181024
128K X 8 HIGH SPEED STATIC RAM

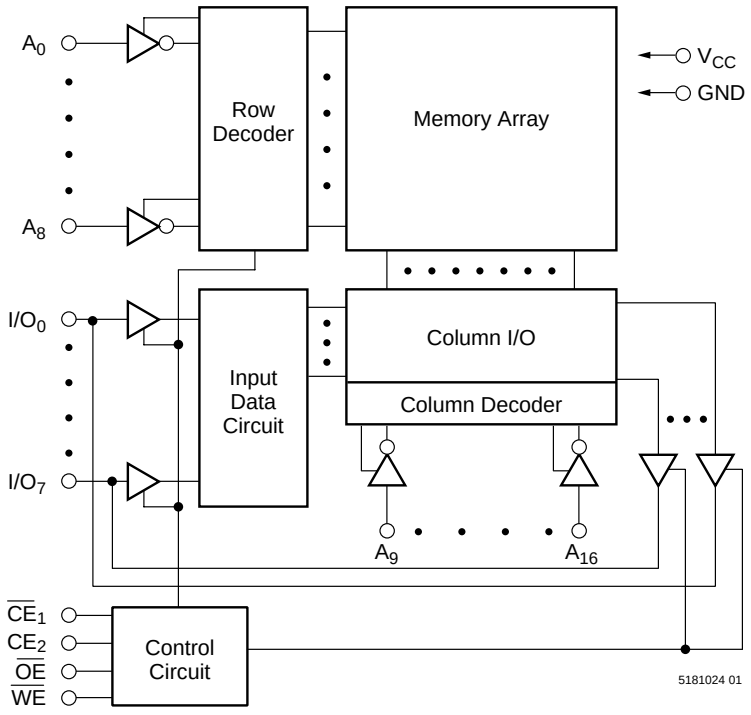
Features

- High-speed: 10, 12, 15 ns
- Fully static operation
- All inputs and outputs directly TTL compatible
- Three state outputs
- Low data retention current (V_{CC} = 2V)
- Single 5V ± 10% Power Supply
- Low CMOS Standby current of 5 mA max
- Packages
  - 32-pin TSOP
  - 32-pin 300 mil SOJ

Description

The V61C5181024 is a 1,048,576-bit static random-access memory organized as 131,072 words by 8 bits. Inputs and three-state outputs are TTL compatible and allow for direct interfacing with common system bus structures. The V61C5181024 is available in 32-pin SOJ, PDIP and TSOP.

Functional Block Diagram



Device Usage Chart

Operating Temperature Range	Package Outline		Access Time (ns)			Temperature Mark
	T	R	10	12	15	
0°C to 70°C	•	•	•	•	•	Blank

Pin Descriptions

A_0–A_{16} Address Inputs
These 17 address inputs select one of the 128K x 8 bit segments in the RAM.

$\overline{CE}_1$, CE_2 Chip Enable Inputs
$\overline{CE}_1$ is active LOW and CE_2 is active HIGH. Both chip enables must be active to read from or write to the device. If either chip enable is not active, the device is deselected and is in a standby power mode. The I/O pins will be in the high-impedance state when deselected.

$\overline{OE}$ Output Enable Input
The Output Enable input is active LOW. When $\overline{OE}$ is LOW with $\overline{CE}$ LOW and $\overline{WE}$ HIGH, data of the selected memory location will be available on the I/O pins. When $\overline{OE}$ is HIGH, the I/O pins will be in the high impedance state.

$\overline{WE}$ Write Enable Input
An active LOW input, $\overline{WE}$ input controls read and write operations. When $\overline{CE}$ and $\overline{WE}$ inputs are both LOW, the data present on the I/O pins will be written into the selected memory location.

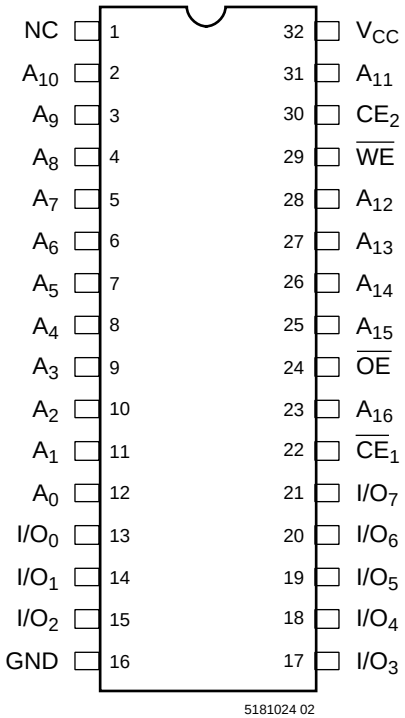
I/O_0–I/O_7 Data Input and Data Output Ports
These 8 bidirectional ports are used to read data from and write data into the RAM.

V_{CC} Power Supply

GND Ground

Pin Configurations (Top View)

32-Pin SOJ



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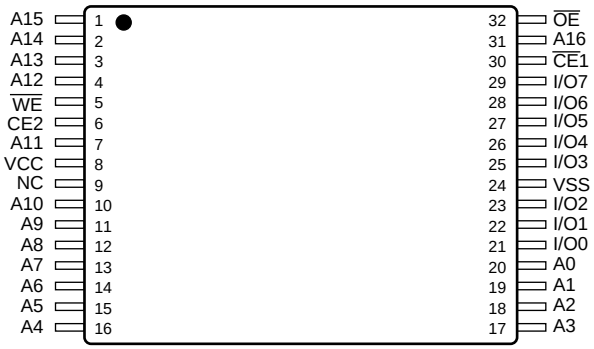
32-Pin TSOP-I (Standard)



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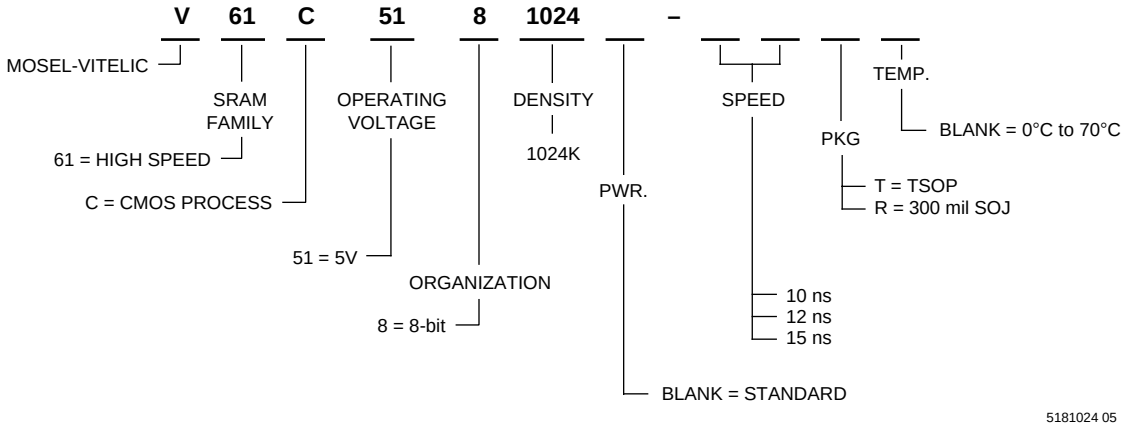
Ordering Information



Absolute Maximum Ratings (1)

Symbol	Parameter	Commercial	Units
V_{CC}	Supply Voltage	-0.5 to +7	V
V_N	Input Voltage	-0.5 to +7	V
V_{DQ}	Input/Output Voltage Applied	V_{CC} + 0.5	V
T_{BIAS}	Temperature Under Bias	-10 to +125	°C
T_{STG}	Storage Temperature	-65 to +150	°C

NOTE:
1. Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Capacitance*

T_A = 25°C, f = 1.0MHz

Symbol	Parameter	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	pF
C_{OUT}	Output Capacitance	$V_{I/O}$ = 0V	8	pF

NOTE:
1. This parameter is guaranteed by design and not tested.

Truth Table

Mode	$\overline{CE}_1$	CE_2	$\overline{OE}$	$\overline{WE}$	I/O Operation
Standby	H	X	X	X	High Z
Standby	X	L	X	X	High Z
Output Disable	L	H	H	H	High Z
Read	L	H	L	H	D_{OUT}
Write	L	H	X	L	D_{IN}

NOTE:
X = Don’t Care, L = LOW, H = HIGH

DC Electrical Characteristics (over all temperature ranges, V_{CC} = 5V ± 10%)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V_{IL}	Input LOW Voltage(1,2)		-0.5	—	0.8	V
V_{IH}	Input HIGH Voltage(1)		2.2	—	6	V
I_{IL}	Input Leakage Current	V_{CC} = Max, V_{IN} = 0V to V_{CC}	-5	—	5	µA
I_{OL}	Output Leakage Current	V_{CC} = Max, $\overline{CE}_1$ = V_{IH}, V_{OUT} = 0V to V_{CC}	-5	—	5	µA
V_{OL}	Output LOW Voltage	V_{CC} = Min, I_{OL} = 2.1mA	—	—	0.4	V
V_{OH}	Output HIGH Voltage	V_{CC} = Min, I_{OH} = -1mA	2.4	—	—	V

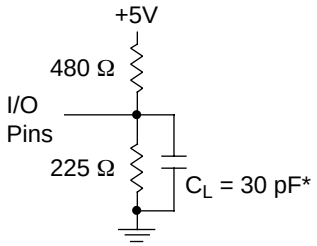
Symbol	Parameter	Com.(4)	Ind.(4)	Units
I_{CC1}	Average Operating Current, $\overline{CE}_1$ = V_{IL}, CE_2 = V_{IH}, Output Open, V_{CC} = Max., f = f_{MAX}(3)	130	140	mA
I_{SB}	TTL Standby Current $\overline{CE}_1 \geq V_{IH}$, $CE_2 \leq V_{IL}$, V_{CC} = Max.	35	40	mA
I_{SB1}	CMOS Standby Current, $\overline{CE}_1 \geq V_{CC} - 0.2V$, $CE_2 \leq 0.2V$, $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$, V_{CC} = Max.	5	6	mA

NOTES:
1. These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.
2. V_{IL} (Min.) = -3.0V for pulse width < 20ns.
3. $f_{MAX} = 1/t_{RC}$.
4. Maximum values.

AC Test Conditions

Input Pulse Levels	0 to 3V
Input Rise and Fall Times	3 ns
Timing Reference Levels	1.5V
Output Load	see below

AC Test Loads and Waveforms



* Includes scope and jig capacitance

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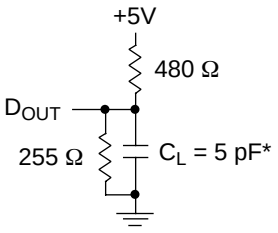
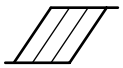
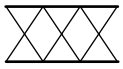
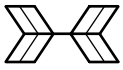


for t_{CLZ}, t_{CHZ}, t_{OLZ}, t_{WZ}, t_{OW}, and t_{OHZ}

5181024 06B

Key to Switching Waveforms

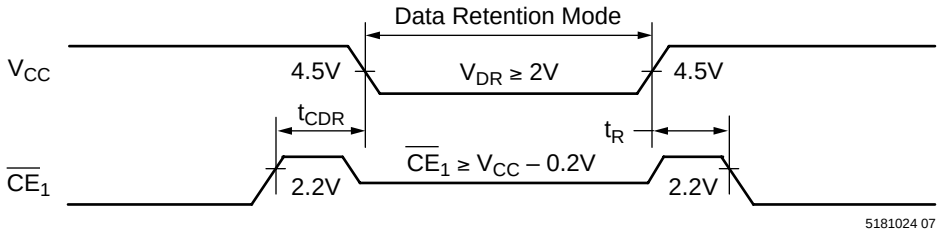
WAVEFORM	INPUTS	OUTPUTS
———	MUST BE STEADY	WILL BE STEADY
———		
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
	DON'T CARE: ANY CHANGE PERMITTED	CHANGING: STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

Data Retention Characteristics

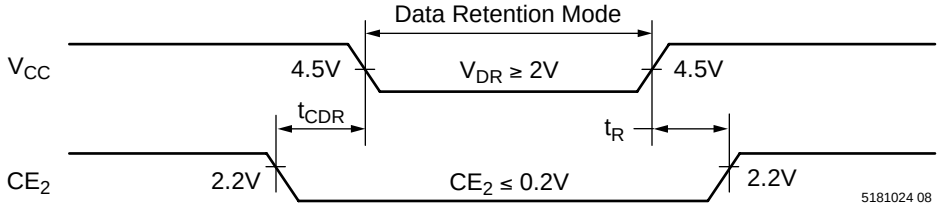
Symbol	Parameter	Min.	Typ.(2)	Max.	Units
V_{DR}	V_{CC} for Data Retention $\overline{CE}_1 \geq V_{CC} - 0.2V$, $CE_2 \leq 0.2V$, $V_{IN} \geq V_{CC} - 0.2V$, or $V_{IN} \leq 0.2V$	2.0	—	5.5	V
I_{CCDR}	Data Retention Current $\overline{CE}_1 \geq V_{DR} - 0.2V$, $CE_2 \leq 0.2V$, $V_{IN} \geq V_{CC} - 0.2V$, or $V_{IN} \leq 0.2V$	—	—	150	µA
t_{CDR}	Chip Deselect to Data Retention Time	0	—	—	ns
t_R	Operation Recovery Time (see Retention Waveform)	t_{RC}(1)	—	—	ns

NOTES:
1. t_{RC} = Read Cycle Time
2. T_A = +25°C.

Low V_{CC} Data Retention Waveform (1) ($\overline{CE}_1$ Controlled)



Low V_{CC} Data Retention Waveform (2) (CE_2 Controlled)



AC Electrical Characteristics

(over all temperature ranges)

Read Cycle

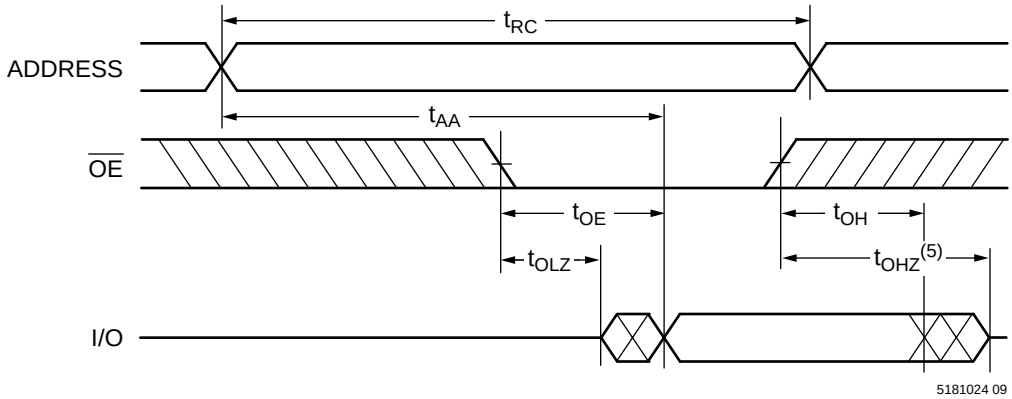
Parameter Name	Parameter	-10		-12		-15		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{RC}	Read Cycle Time	10	—	12	—	15	—	ns
t_{AA}	Address Access Time	—	10	—	12	—	15	ns
t_{ACS1}	Chip Enable Access Time	—	10	—	12	—	15	ns
t_{ACS2}	Chip Enable Access Time	—	10	—	12	—	15	ns
t_{OE}	Output Enable to Output Valid	—	6	—	6	—	7	ns
t_{CLZ1}	Chip Enable to Output in Low Z	3	—	3	—	3	—	ns
t_{CLZ2}	Chip Enable to Output in Low Z	3	—	3	—	3	—	ns
t_{OLZ}	Output Enable to Output in Low Z	0	—	0	—	0	—	ns
t_{CHZ}	Chip Disable to Output in High Z	0	3	0	3	0	4	ns
t_{OHZ}	Output Disable to Output in High Z	0	3	0	3	0	4	ns
t_{OH}	Output Hold from Address Change	3	—	3	—	3	—	ns

Write Cycle

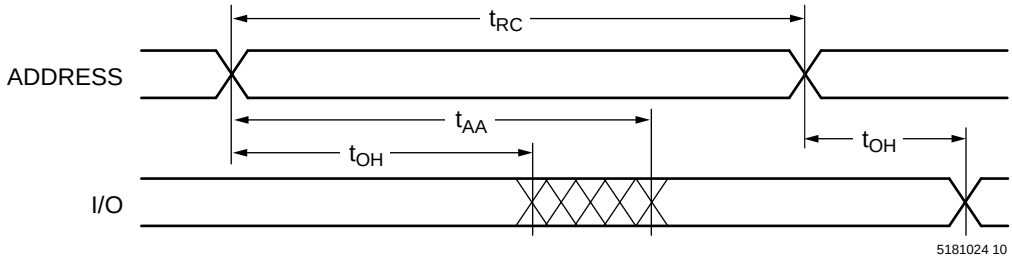
Parameter Name	Parameter	-10		-12		-15		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{WC}	Write Cycle Time	10	—	12	—	15	—	ns
t_{CW1}	Chip Enable to End of Write	8	—	10	—	13	—	ns
t_{CW2}	Chip Enable to End of Write	8	—	10	—	13	—	ns
t_{AS}	Address Setup Time	0	—	0	—	0	—	ns
t_{AW}	Address Valid to End of Write	8	—	10	—	13	—	ns
t_{WP}	Write Pulse Width	8	—	9	—	11	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	ns
t_{WHZ}	Write to Output High-Z	0	5	0	5	0	5	ns
t_{WLZ}	Write to Output Low Z	3	—	3	—	5	—	ns
t_{DW}	Data Setup to End of Write	5	—	6	—	8	—	ns
t_{DH}	Data Hold from End of Write	0	—	0	—	0	—	ns

Switching Waveforms (Read Cycle)

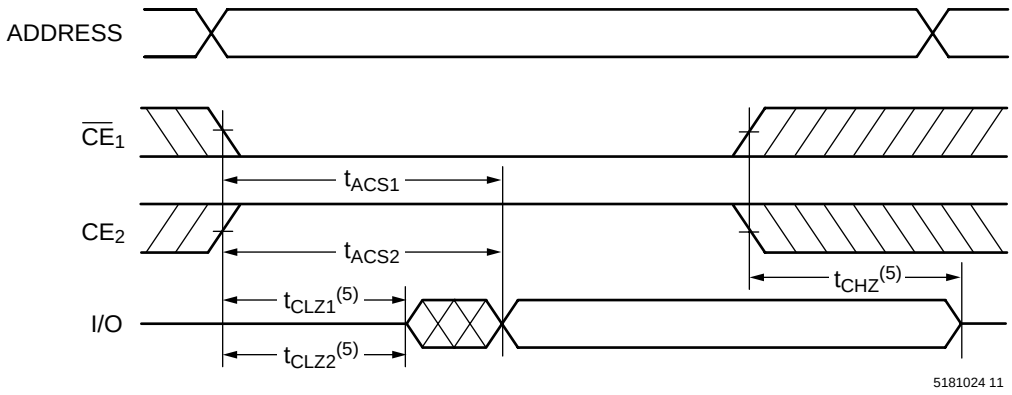
Read Cycle 1(1, 2)



Read Cycle 2(1, 2, 4)



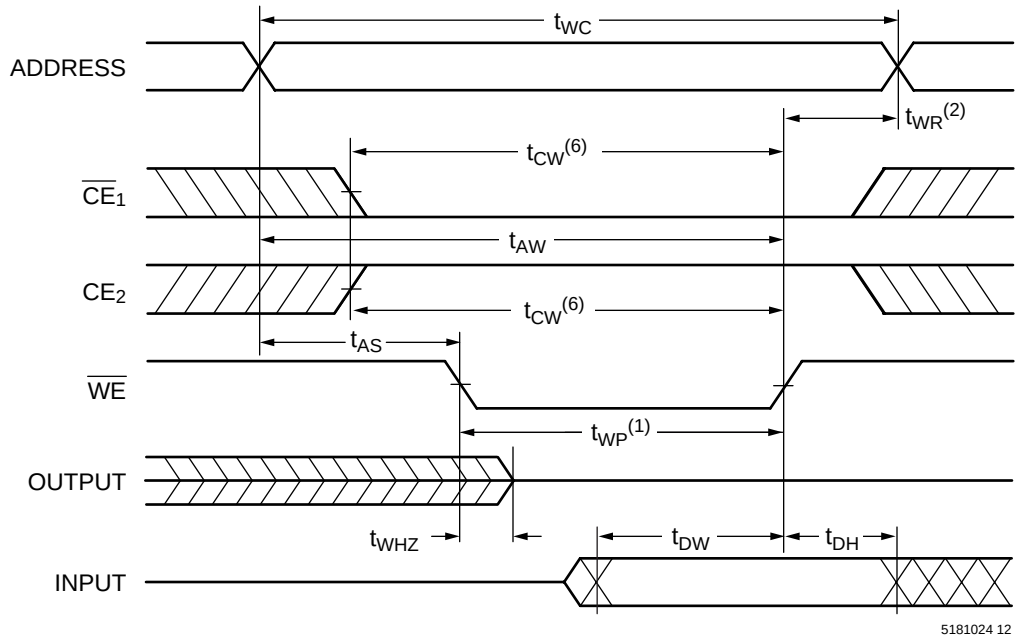
Read Cycle 3(1, 3, 4)



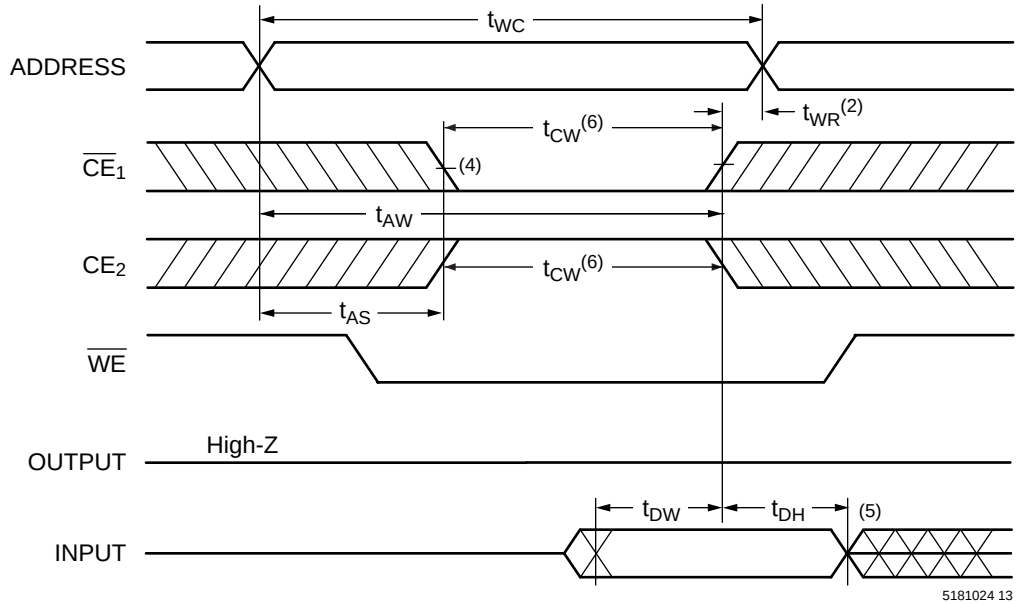
NOTES:
1. $\overline{WE}$ = V_{IH}.
2. $\overline{CE}_1$ = V_{IL} and CE_2 = V_{IH}.
3. Address valid prior to or coincident with $\overline{CE}_1$ transition LOW and/or CE_2 transition HIGH.
4. $\overline{OE}$ = V_{IL}.
5. Transition is measured ±500mV from steady state with C_L = 5pF. This parameter is guaranteed and not 100% tested.

Switching Waveforms (Write Cycle)

Write Cycle 1 ($\overline{WE}$ Controlled)[4]



Write Cycle 2 (CE Controlled)[4]



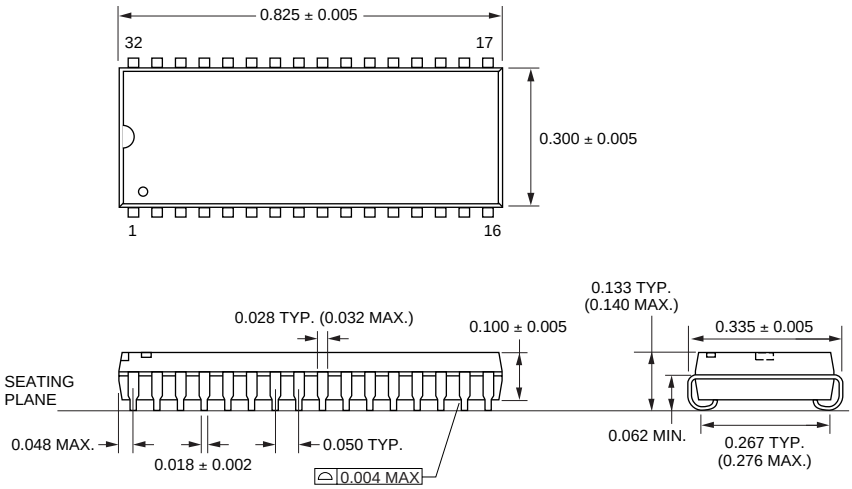
NOTES:

1. The internal write time of the memory is defined by the overlap of $\overline{CE}_1$ and CE_2 active and $\overline{WE}$ low. All signals must be active to initiate and any one signal can terminate a write by going inactive. The data input setup and hold timing should be referenced to the second transition edge of the signal that terminates the write.
2. t_{WR} is measured from the earlier of $\overline{CE}_1$ or $\overline{WE}$ going high, or CE_2 going LOW at the end of the write cycle.
3. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
4. $\overline{OE}$ = V_{IL} or V_{IH}. However it is recommended to keep $\overline{OE}$ at V_{IH} during write cycle to avoid bus contention.
5. If $\overline{CE}_1$ is LOW and CE_2 is HIGH during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.
6. t_{CW} is measured from $\overline{CE}_1$ going low or CE_2 going HIGH to the end of write.

Package Diagrams

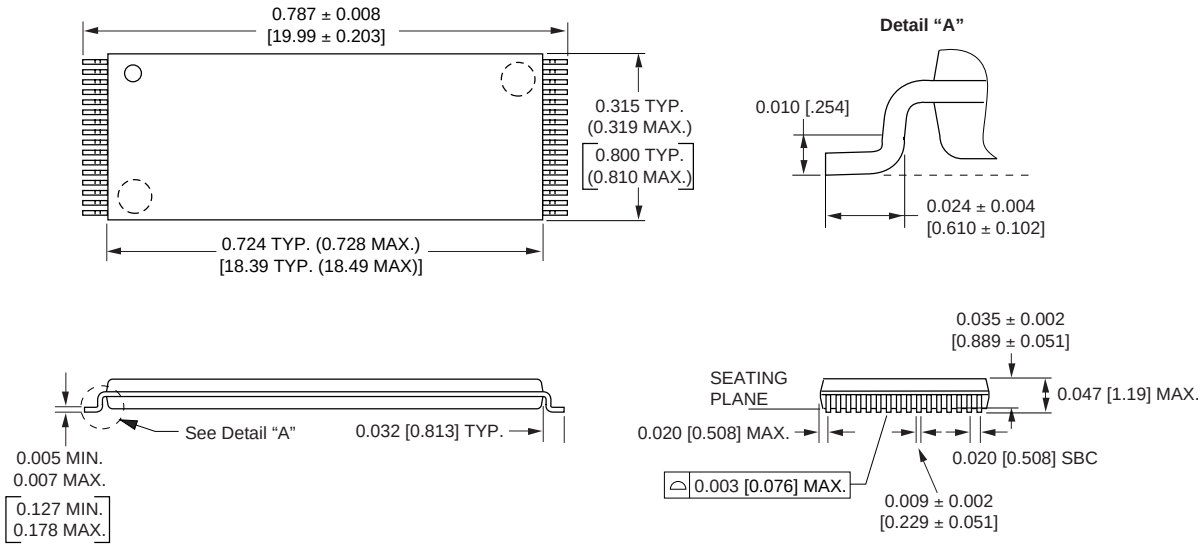
32-Pin 300 mil SOJ

Units in inches



32-Pin TSOP-I

Units in inches [mm]



Notes

Notes

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