UTRON Technology Inc.

UT87C301

Universal Digital TV Encoder

UT87C301

Preliminary Rev1.0
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Features

- Universal digital interface accepts YUV, YCrCb (CCIR656) or RGB video data in non interlaced format. Fully DVO Compliant.
- Supports underscan/overscan operations for various graphics display resolutions.
- Flicker removal with up to 7-line of filtering.
- Enhanced dot crawl control and area reduction.
- Fully programmable through I^2C port or compatible Serial Port.
- Supports all NTSC and PAL TV formats.
- Provides Composite, S-Video and SCART outputs.
- Auto-detection & Hot-plug detection of TV presence.
- Programmable contrast enhancement.
- Programmable Sharpness/black level control.
- Composite quality enhanced by Notch & chroma filtering.
- Dynamic Start and Stop video Stream.
- Support for low voltage interface to VGA controller.
- Programmable power management, low power consumption.
- 10-bit video DAC outputs.
- Anti-Copy Protection / MacroVision.
- Complete Windows , LINUX driver and DOS BIOS software.
- IA-TV Friendly (UT87C301) software.(*)
- Offered in 44-pin TQFP or LQFP or PQFP

(*) Patent pending

General Description

UTRON's UT87C301 is a Digital Video Stream to TV encoder. It provides a DVO compliant solution for TV output and a universal digital input port in order to accept video pixel stream in either RGB or YUV/YCbCr format and converts this directly into multiple TV formats. The goal of UT87C301 is to be able to use TV as a display device, together with, or instead of a CRT or flat panel for Information Appliances.

It provides excellent quality video output in resolutions including 640x480, 720x480 and 800x600. UT87C301 has an optional flicker filter, built-in Luminance notch filter for reduced cross color distortion, color low-pass filters for reduced cross luminance distortion, high accuracy low-jitter phase locked loop, horizontal & vertical scaling, simultaneous display of composite and S-video out to 10-bit DAC interface, and SCART output. All features are software programmable through a I^2C port.

Application

-TV centric display Information Appliance (IA)
-Interactive TV Box (ITV)
-Computer to TV (PC2TV)
-Personal Video Recoder (PVR)
-Digital Entertainment Box (DEB)

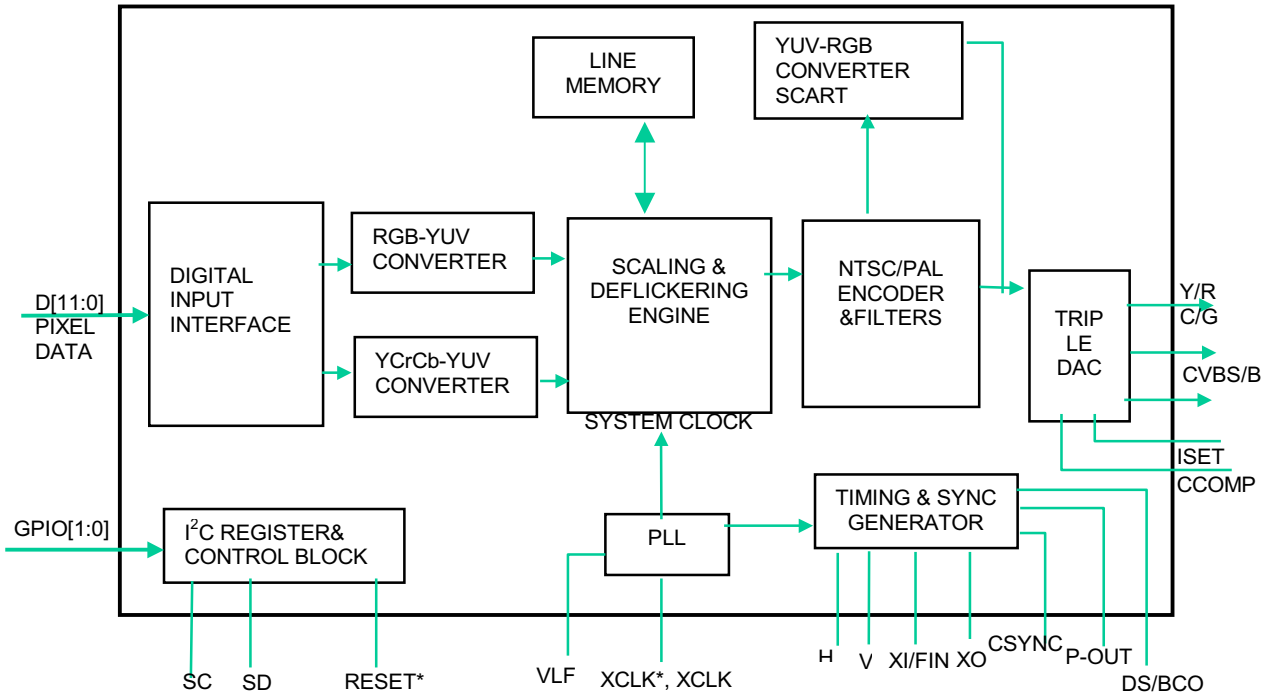

Figure 1-1. Function Block Diagram

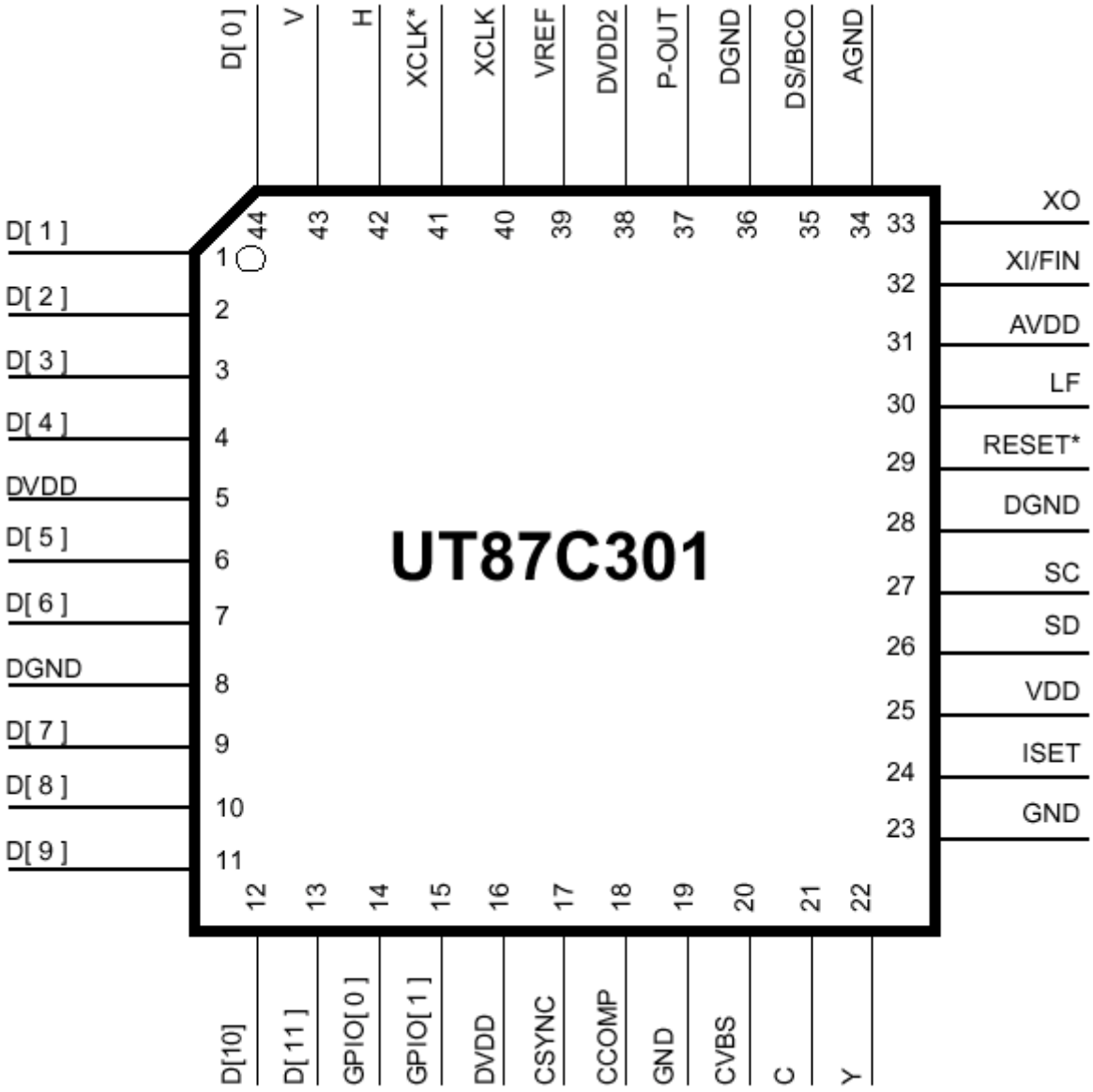

Figure 1-2. 44-Pin TQFP/PQFP/LQFP

Pin Descriptions

Table 1-1. Pin Descriptions

44-Pin TQFP	Type	Symbol	Description
39	Analog	VREF	**Reference Voltage Input** The VREF pin inputs a reference voltage of DVDD2/2. The signal is derived externally through a resistor divider and decoupling capacitor, and will be used as a reference level for data and sync inputs.
40	In	XCLK	**External Clock Input** This input along with XCLK* will form a differential clock input . For applications where a differential clock is not available, the XCLK* pin should be connected to the VREF pin.
41	In	XCLK*	**External Clock Input*** See XCLK description
42	In/Out	H	**Horizontal Sync Input/Output** When the SYO bit is low, this pin accepts a horizontal sync input . The level is 0 to DVDD2, with VREF as the threshold level. When the SYO bit is high, the device will output a horizontal sync pulse. The output is driven from the DVDD supply.
43	In/Out	V	**Vertical Sync Input/Output** When the SYO bit is low, this pin accepts a vertical sync input. The level is 0 to DVDD2 with VREF as the threshold level. When the SYO bit is high, the device will out put a vertical sync pulse. The output is driven from the DVDD supply.
44.1-4, 6-7,9-13	In	D[0]-D[11]	**Data [0] through Data [11] Inputs** These pins accept 12 data inputs from the graphics controller. The level is 0 to DVDD2, with VREF as the threshold level.
14-15	In/Out	GPIO[0] GPIO[1]	**General Purpose Input/ Output [0-1] and Internal pull-Down** These pins provide general purpose I/O's controlled via the IIC or Serial Data/Clock bus, GPIO[1] can be driven out or read back controlled by registers 1Bh and 1Ch, bits [7], it has the internal pull-down or external pull-up to determine IIC address. GPIO[0] can be driven out or read back controlled by registers 1Bh and 1Ch, bits [6], it is used to determine external crystal whether is NTSC(14.3181Mhz) or PAL(17.322Mhz).
17	Out	CSYNC	**Composite Sync Output** A 75 Ohm termination resistor with short traces should be att ached between CSYNC and ground for optimum performance. In SCART mode, this pin outputs the composite sync signal.
18	Analog	CCOMP	**Capacitor Compensation**

44-Pin TQFP	Type	Symbol	Description
			A 0.1 uf capacitor connected to digital VDD, it is used inside the DAC.
20	Analog	CVBS/B	**Composite Video Output/Blue Output** A 75 Ohm termination resistor with short traces should be attached between CVBS and ground for optimum performance. In normal operating modes other than SCART, this pin outputs the composite video signal. In SCART mode, this pin outputs the blue signal.
21	Analog	C/G	**Chroma Output/Green Output** A 75 Ohm termination resistor with short traces should be attached between C and ground for optimum performance. In normal operating modes other than SCART, this pin outputs the chroma video signal. In SCART mode, this pin outputs the green signal.
22	Analog	Y/R	**Luma Output / Red Output** A 75 Ohm termination resistor with short traces should be attached between Y and ground for optimum performance. In normal operating modes other than SCART, this pin outputs the luma video signal. In SCART mode, this pin outputs the red signal.
24	In	ISET	**Current Set Resistor Input** This pin sets the DAC current. A 33 ohm resistor should be connected between this pin and GND using short and wide traces.
26	In/Out	SD	**Serial Data Input/Output** This pin functions as the serial data pin of the I^2C interface port, and uses the DVDD supply. (see the I^2C Port Operation section for details)
27	In	SC	**Serial Clock Input** This pin functions as the serial clock pin of the I^2C interface port, and uses the DVDD supply. (see the I^2C Port Operation section for details)
29	In	RESET*	**Reset* Input** When this pin is low, the UT87C301 is held in the power-on reset condition. When this pin is high, the device operates normally and reset is controlled through the I^2C register.
30	Analog	LF	**Loop Filter** PLL external loop filter.
32	In	XI/FIN	**Crystal Input/External Reference Input** A parallel resonance 14.31818MHz(NTSC) +20ppm or 17.322Mhz(PAL) +20ppm crystal should be attached between this pin and XO. However, an external CMOS clock can be attached to XI/FIN.
33	Out	XO	**Crystal Output** A parallel resonance 14.31818MHz(NTSC) +20ppm or 17.322Mhz(PAL) +20ppm crystal should be attached between this pin and XI/FIN. However, if an external CMOS clock is attached to XI/FIN, XO should not be connected.

44-Pin TQFP	Type	Symbol	Description
35	In/Out	DS/BCO	**Data start (input)/Buffered Clock (output)** In normal operating modes, when configured as an input, the rising edge of this signal identifies the first active pixel of data for each active line. The level is 0 to DVDD2, with VREF as the threshold level. When configured as an output this pin provides a buffered clock output, driven by the DVDD supply. The output clock can be selected using the BCO register (17th) (see Reg-isters and Programing).
37	Out	P-Out	**Pixel Clock Output** This pin provides a pixel clock signal to the VGA controller (adjustable as 1X, 2X) and is driven from the DVDD2 supply. This clock will only be provided in master clock modes, and will be tri-stated otherwise, (see the section on Digital Video Interface and Registers and Programming for more details). The capacitive loading on this pin should be kept to a minimum.
5,16	Power	DVDD	**Digital Supply Voltage**
8,28,36	Power	DGND	**Digital Ground**
19,23	Power	GND	**DAC**
25	Power	VDD	**DAC Supply Voltage**
31	Power	AVDD	**PLL Supply Voltage**
34	Power	AGND	**PLL Ground**
38	Power	DVDD2	**I/O SUPPLY VOLTAGE**

Digital Video Interface

The UT87C301 digital video interface provides a flexible digital interface between a Video/Graphics controller or Micro Controller and the TV encoder IC forming the ideal quality/cost configuration for performing the TV-output function. This digital interface consists of up to 12 data signals and 4 control signals, all of which are subject to programmable control through the UT87C301 register set. This interface can be configured as 8 or 12-bit inputs operating in multiplexed mode. It will also accept either YCrCb or RGB (15, 16 or 24-bit color depth) data formats and will accept non-interlaced data formats. A summary of the input data format modes is as follows:

Table 1-2. Input Data Formats

Bus Width	Transfer Mode	Color Space and Depth	Format Reference
8-bit	2X-multiplexed	RGB 15-bit	5-5-5 over two bytes
8-bit	2X-multiplexed	RGB 16-bit	5-6-5 over two bytes
8-bit	2X-multiplexed	YCrCb (24-bit)	Cb,Y0,Cr,Y1,(CCIR656 style)
12-bit	2X-multiplexed	RGB 24	8-8-8 over two words - 'C' version
12-bit	2X-multiplexed	RGB 24	8-8-8 over two words -' I' version

The clock and timing signals used to latch and process the incoming pixel data is dependent upon the clock mode. The UT87C301 can operate in either master (the UT87C301 generates a pixel frequency which is either returned as a phase-aligned pixel clock or used directly to latch data), or slave mode (the graphics chip generates the pixel clock). The pixel clock frequency will change depending upon the active image size (e.g., 640x480 or 800x600), the desired output format (NTSC or PAL), and the amount of scaling desired. The pixel clock may be requested to be 1X or 2X the pixel data rate (subject to a 100MHz frequency limitation). In the case of a 1X pixel clock the UT87C301 will automatically use both clock edges, if a multiplexed data format is selected.

Sync Signals: Horizontal and vertical sync signals will normally be supplied by the VGA controller, but may be selected to be generated by the UT87C301. The period of the horizontal sync should be equal to the duration of the pixel clock, times the first value of the *(Total Pixels/line x Total Lines/Fram*e) column of **Table 1-11** (Display Mode Register 00H description). The leading edge of the horizontal sync is used to determine the start of each line. The Vertical sync signal must be able to be set to the second value in the *(Total Pixels/Line x Total Lines/Fram*e) column of **Table 1-11** .

Master Clock Mode: The UT87C301 generates a clock signal (output at theP-OUT pin) which will be used by the VGA controller as a frequency reference. The VGA controller will then generate a clock signal which will be input via the XCLK input. This incoming signal will be used to latch (and de-multiplex, if required) incoming data. The XCLK input clock rate must match the input data rate, and the P-OUT clock can be requested to be 1X or 2X the pixel data rate. As an alternative, the P-OUT clock signal can also be used as the input clock signal (connected directly to the XCLK input) to latch the incoming data. If this mode is used, the incoming data must meet setup and hold times with respect to the XCLK input (with the only internal adjustment being XCLK polarity).

Slave Clock Mode: The VGA controller will generate a clock which will be input to the XCLK pin (no clock signal will be output on the P-OUT pin). This signal must match the input data rate, must occur at 1X or 2X the pixel data rate, and will be used to latch (and de-multiplex if required) incoming data. Also, the graphics IC transmits back to the TV encoder the horizontal and vertical timing signals, and pixel data, each of which must meet the specified setup and hold times with respect to the pixel clock.

Pixel Data: Active pixel data will be expected after a programmable number pixels times the multiplex rate after the leading edge of Horizontal Sync. In other words, specifying the horizontal back porch value (as a pixel count), plus horizontal sync width, will determine when the chip will begin to sample pixels.

Input Data Formats

The XCLK and XCLK* signals are used to latch data from the graphics chip. Data can be latched coincident with the rising edge of XCLK, falling edge of XCLK, or both edges, depending upon register settings of XCM and MCP. The input data format is shown in **Figure 1-3**. The Pixel Data bus represents an 8 or 12-bit multiplexed data stream, which contains either RGB or YCrCb formatted data. In IDF settings of 4, 5, 7, 8 and 9, the input data rate is 2X pixel clock, and each pair of Pn values (e.g., P0a and P0b) will contain a complete pixel, encoded as shown in the tables below. When the input is YCrCb, the color-difference data will be transmitted at half the data rate of the luminance data, with the sequence

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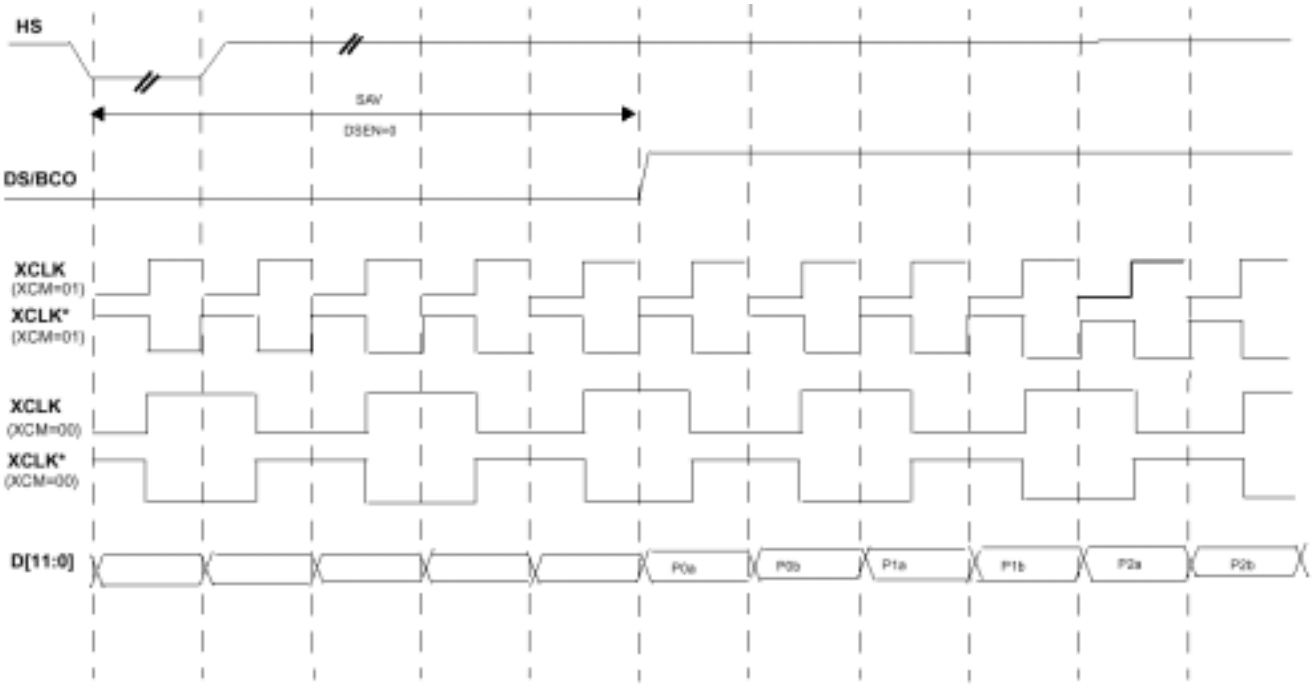
being set as Cb0, Y0, Cr0, Y1 where Cb0,Y0,Cr0 refers to co-sited luminance and color-difference samples --- and the following Y1 byte refers to the next luminance sample, per CCIR656 standards. However, the clock frequency is dependent upon the current mode, not 27MHz, as specified in CCIR656.



When DSEN = 1(Bit 4 of register 1CH), SAV should be set to 11d

Figure 1-3. Non-multiplexed Data Transfers

Table 1-3. RGB 8-bit Multiplexed Mode

IDF# Format		7 RGB 5- 6-5				8 RGB 5 -5-5			
Pixel#		P0a	P0b	P1a	P1b	P0a	P0b	P1a	P1b
Bus Data	D[7]	G0[2]	R0[4]	G1[2]	R1[4]	G0[2]	x	G1[2]	x
	D[6]	G0[1]	R0[3]	G1[1]	R1[3]	G0[1]	R0[4]	G1[1]	R1[4]
	D[5]	G0[0]	R0[2]	G1[0]	R1[2]	G0[0]	R0[3]	G1[0]	R1[3]
	D[4]	B0[4]	R0[1]	B1[4]	R1[1]	B0[4]	R0[2]	B1[4]	R1[2]
	D[3]	B0[3]	R0[0]	B1[3]	R1[0]	B0[3]	R0[1]	B1[3]	R1[1]
	D[2]	B0[2]	G0[5]	B1[2]	G1[5]	B0[2]	R0[0]	B1[2]	R1[0]
	D[1]	B0[1]	G0[4]	B1[1]	G1[4]	B0[1]	G0[4]	B1[1]	G1[4]
	D[0]	B0[0]	G0[3]	B1[0]	G1[3]	B0[0]	G0[3]	B1[0]	G1[3]

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Table 1-4. RGB 12-bit Multiplexed Mode

IDF# Format		4 12-bit RGB (12-12)				5 12-bit RGB (12-12)			
Pixel#		P0a	P0b	P1a	P1b	P0a	P0b	P1a	P1b
Bus Data	D[11]	G0[3]	R0[7]	G1[3]	R1[7]	G0[4]	R0[7]	G1[4]	R1[7]
	D[10]	G0[2]	R0[6]	G1[2]	R1[6]	G0[3]	R0[6]	G1[3]	R1[6]
	D[9]	G0[1]	R0[5]	G1[1]	R1[5]	G0[2]	R0[5]	G1[2]	R1[5]
	D[8]	G0[0]	R0[4]	G1[0]	R1[4]	B0[7]	R0[4]	B1[7]	R1[4]
	D[7]	B0[7]	R0[3]	B1[7]	R1[3]	B0[6]	R0[3]	B1[6]	R1[3]
	D[6]	B0[6]	R0[2]	B1[6]	R1[2]	B0[5]	G0[7]	B1[7]	G1[7]
	D[5]	B0[5]	R0[1]	B1[5]	R1[1]	B0[4]	G0[6]	B1[4]	G1[6]
	D[4]	B0[4]	R0[0]	B1[4]	R1[0]	B0[3]	G0[5]	B1[3]	G1[5]
	D[3]	B0[3]	G0[7]	B1[3]	G1[7]	G0[0]	R0[2]	G1[0]	R1[2]
	D[2]	B0[2]	G0[6]	B1[2]	G1[6]	B0[2]	R0[1]	B1[2]	R1[1]
	D[1]	B0[1]	G0[5]	B1[1]	G1[5]	B0[1]	R0[0]	B1[1]	R1[0]
	D[0]	B0[0]	G0[4]	B1[0]	G1[4]	B0[0]	G0[1]	B1[0]	G1[1]

Table 1-5. YCrCb Multiplexed Mode

IDF# Format		9 YCrCb 8-bit							
Pixel#		P0a	P0b	P1a	P1b	P2a	P2b	P3a	P3b
Bus Data	D[7]	Cb0[7]	Y0[7]	Cr0[7]	Y1[7]	Cb2[7]	Y2[7]	Cr2[7]	Y3[7]
	D[6]	Cb0[6]	Y0[6]	Cr0[6]	Y1[6]	Cb2[6]	Y2[6]	Cr2[6]	Y3[6]
	D[5]	Cb0[5]	Y0[5]	Cr0[5]	Y1[5]	Cb2[5]	Y2[5]	Cr2[5]	Y3[5]
	D[4]	Cb0[4]	Y0[4]	Cr0[4]	Y1[4]	Cb2[4]	Y2[4]	Cr2[4]	Y3[4]
	D[3]	Cb0[3]	Y0[3]	Cr0[3]	Y1[3]	Cb2[3]	Y2[3]	Cr2[3]	Y3[3]
	D[2]	Cb0[2]	Y0[2]	Cr0[2]	Y1[2]	Cb2[2]	Y2[2]	Cr2[2]	Y3[2]
	D[1]	Cb0[1]	Y0[1]	Cr0[1]	Y1[1]	Cb2[1]	Y2[1]	Cr2[1]	Y3[1]
	D[0]	Cb0[0]	Y0[0]	Cr0[0]	Y1[0]	Cb2[0]	Y2[0]	Cr2[0]	Y3[0]

Table 1-6. Absolute Maximum Ratings

Symbol	Description	Min	Typ	Max	Units
	VDD relative to GND	-0.5		4.0	V
	Input voltage of all digital pins [1]	GND-0.5		VDD+0.5	V
T_{SC}	Analog output short circuit duration		Indefinite		Sec
T_{AMB}	Ambient operating temperature	-55		85	℃
T_{STOR}	Storage temperature	-65		150	℃
T_J	Junction temperature			150	℃
T_{VPS}	Vapor phase soldering (one minute)			220	℃

Notes:
- Stresses greater than those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions above those indicated under the normal operating condition of this specification is not recommended. Exposure to absolute maximum rating conditions for extended periods my affect reliability.
- The device is fabricated using high-performance CMOS technology. It should be handled as an ESD sensitive device. Volt-age on any signal pin that exceeds the power supply voltages by more than + 0. 5V can induce destructive latch.

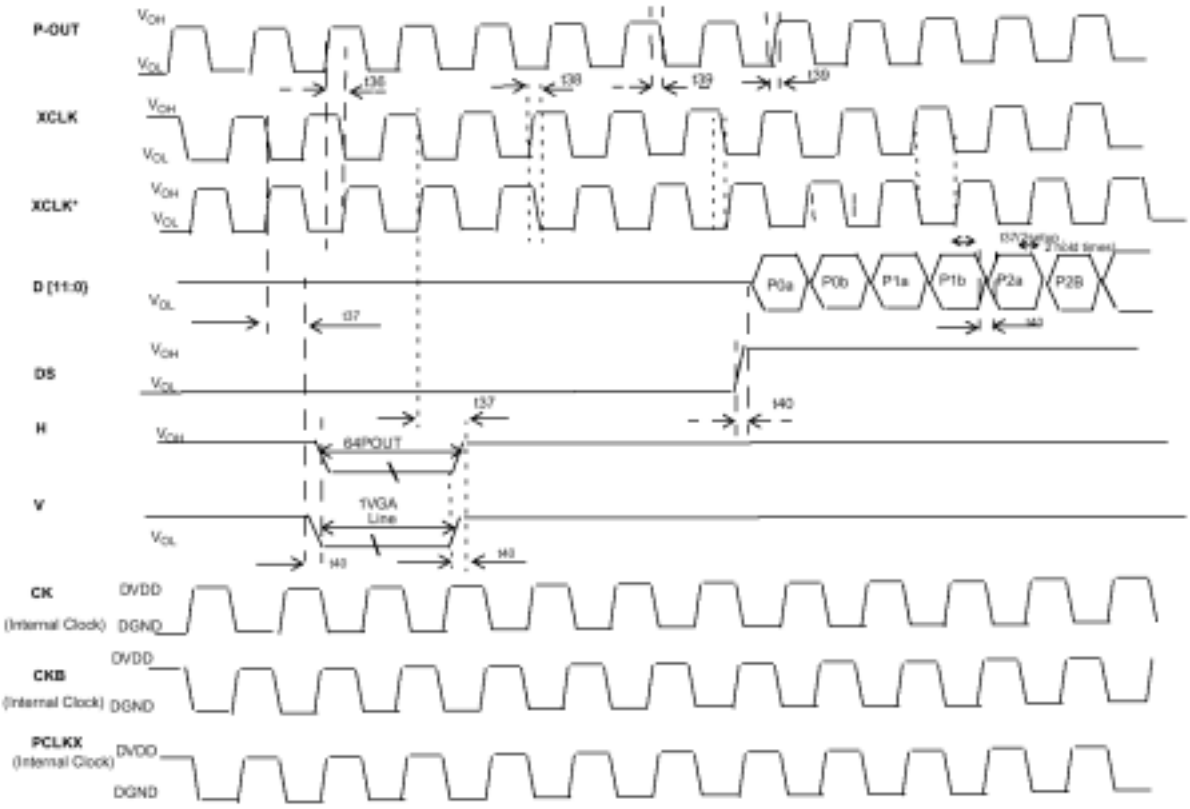
Table 1-7. Recommended Operating Conditions

Symbol	Description	Min	Typ	Max	Units
VDD	DAC power supply voltage	3.1		3.6	V
AVDD	Analog supply voltage	3.1		3.6	
DVDD	Digital supply voltage	3.1	3.3	3.6	
DVDD2	Digital supply voltage (P-OUT) VGA controller interface = 1.1V	1.0	1.1	1.3	
DVDD2	Digital supply voltage (P-OUT) VGA controller interface = 1.8V	1.7	1.8	1.9	V
DVDD2	Digital supply voltage (P-OUT) VGA controller interface = 3.3V	3.1	3.3	3.6	V
R_L	Output load to DAC outputs		37.5		Ohm

Table 1-8. Electrical Characteristics (Operating Conditions: T_A = 0℃ -70℃, VDD = 3.3V+ 5%)

	Video D/A resolution		10		Bits
	Full scale output current		33.89		mA
	Video level error			10	%
	VDD & AVDD (3.3 V) current (simultaneous S-Video& composite outputs)		130		mA
	DVDD (3. 3V) current		47		mA
	DVDD2 (1. 8V) current (15pF load)		3		mA

Timing Information



Symbol	Parameter	Min	Max	Unit
V_{OH}	Output High level of interface signals	DVDD2 - 0.2	DVDD2 + 0.2	V
V_{OL}	Output Low level of interface signals	-0.2	0. 2	V
t36	P-OUT = VREF to XCLK = XCLK* Delay	2	9	nS
t37	XCLK = XCLK* to D [11: 0], H, V & D S = VREF Setup and Hold	3		nS
t38	XCLK = XCLK* rise/fall time w/15pF load			nS
t39	P-OUT rise/fall time w/ 15pF load			nS
t40	D[11:0], H, V & DW rise/ fall time w /15pF load			nS
DVDD2	Digital I/O Supply Voltage	1.1	3. 6	V

Table 1-9. Digital Inputs/Outputs

Symbol	Description	Test Condition	Min	Typ	Max	Unit
V_{SDOL}	SD Output Low Voltage	IOL = 2.0 mA			0. 4	V
V_{IICIH}	SD Input High Voltage		3.4		VDD + 0.5	V
V_{IICIL}	SD Input Low Voltage		GND-0.5		1. 4	V
V_{DATAIH}	D[0-11] Input High Voltage		2.5		DVDD+0. 5	V
V_{DATAIL}	D[0-11] Input Low Voltage		GND-0.5		0. 8	V
$V_{P\text{-}OUT\ OH}$	P-OUT Output High Voltage	IOL = - 400 uA	2.8			V
$V_{P\ -OUTO\ L}$	P-OUT Output Low Voltage	IOL = 3.2 mA			0. 2	V

NOTE:

V_{IIC} -refers to I^2C pins SD and SC.
V_{DATA} - refers to all digital pixel and clock inputs.
V_{SD} - refers to I^2C pin SD as an output.
$V_{P\text{-}OUT}$ - refers to pixel data output Time -Graphics.

ORDERING INFORMATION

PART NO.	PACKAGE
UT87C301XC	44PIN TQFP
UT87C301TC	44PIN LQFP
UT87C301QC	44PIN PQFP

REVISION HISTORY

REVISION	DESCRIPTION	DATE
1.0	Original	APR.26.2001