FEATURES

- Access time : 70/100ns(max)
- CMOS Low operating power
  Operating : 30/20mA (Icc max)
  Standby : 20μA (TYP.) L-version
  2μA (TYP.) LL-version
- Single 2.3V~2.7V power supply
- Operating Temperature:
  Industrial : -40℃~85℃
- All inputs and outputs TTL compatible
- Fully static operation
- Three state outputs
- Data retention voltage : 1.5V (min)
- Package : 32-pin 8mm×20mm TSOP-I
  32-pin 8mm×13.4mm STSOP

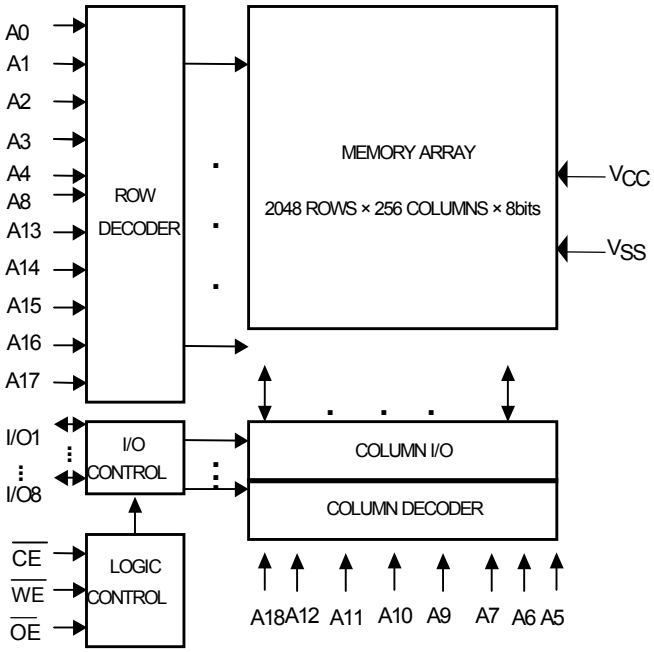
GENERAL DESCRIPTION

The UT62V5128(I) is a 4,194,304-bit high speed CMOS static random access memory organized as 524,288 words by 8 bits. It is fabricated using high performance, high reliability CMOS technology.

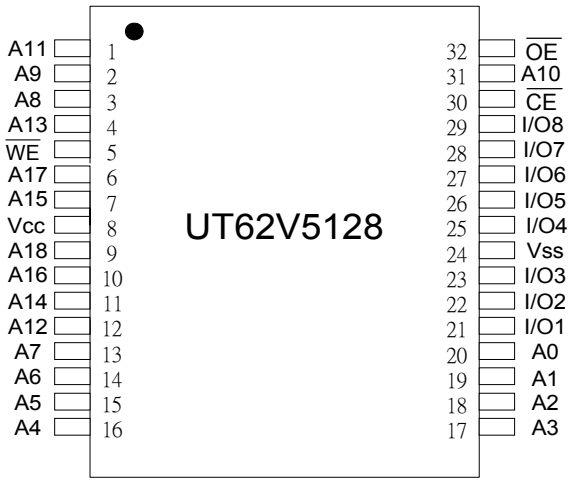
The UT62V5128(I) is designed for high speed system applications. It is particularly well suited for battery back-up nonvolatile memory applications.

The UT62V5128(I) operates from a single 2.3V~2.7V power supply and all inputs and outputs are fully TTL compatible.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



TSOP-1 / STSOP

PIN DESCRIPTION

SYMBOL	DESCRIPTION
A0 - A18	Address Inputs
I/O1 - I/O8	Data Inputs/Outputs
$\overline{CE}$	Chip Enable Input
$\overline{WE}$	Write Enable Input
$\overline{OE}$	Output Enable Input
Vcc	Power Supply
Vss	Ground
NC	No Connection

TRUTH TABLE

MODE	$\overline{WE}$	$\overline{CE}$	$\overline{OE}$	I/O OPERATION	SUPPLY CURRENT
Standby	X	H	X	High – Z	I_{SB}, I_{SB1}
Output Disable	H	L	H	High – Z	I_{CC},I_{CC1},I_{CC2}
Read	H	L	L	D_{OUT}	I_{CC},I_{CC1},I_{CC2}
Write	L	L	X	D_{IN}	I_{CC},I_{CC1},I_{CC2}

Note: H = V_{IH}, L=V_{IL}, X = Don't care.

ABSOLUTE MAXIMUM RATINGS*

PARAMETER		SYMBOL	RATING	UNIT
Terminal Voltage with Respect to V_{SS}		V_{TERM}	-0.5 to 3.6	V
Operating Temperature	Industrial	T_A	-20 to 85	℃
Storage Temperature		T_{STG}	-65 to 150	℃
Power Dissipation		P_D	1	W
DC Output Current		I_{OUT}	50	mA
Soldering Temperature (under 10 secs)		Tsolder	260	℃

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect device reliability.

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 2.3V~2.7V, TA =-40℃ to 85℃(I))

PARAMETER	SYMBOL	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
Power Voltage	Vcc			2.3	2.5	2.7	V
Input High Voltage	V_{IH}			2.0	-	Vcc+0.3	V
Input Low Voltage	V_{IL}			- 0.2	-	0.6	V
Input Leakage Current	I_{LI}	V_{SS} ≦V_{IN} ≦V_{CC}		- 1	-	1	µA
Output Leakage Current	I_{LO}	V_{SS} ≦$V_{I/O}$ ≦V_{CC}, Output Disabled		- 1	-	1	µA
Output High Voltage	V_{OH}	I_{OH}= -0.5mA		2.0	-	-	V
Output Low Voltage	V_{OL}	I_{OL}= 0.5mA		-	-	0.4	V
Operating Power Supply Current	I_{CC}	Cycle time=Min.100% duty,	70	-	20	30	mA
		$\overline{CE}$ = V_{IL}, $I_{I/O}$ =0mA ,	100	-	15	20	mA
	Icc1	Cycle time = 1µs,100% duty, $\overline{CE}$ ≦0.2,$I_{I/O=}$0mA, other pins at 0.2V or Vcc-0.2V,		-	3	4	mA
	Icc2	Cycle time =500ns,100% duty, $\overline{CE}$ ≦0.2,$I_{I/O=}$0mA other pins at 0.2V or Vcc-0.2V,		-	6	8	mA
Standby Current(TTL)	I_{SB1}	$\overline{CE}$ =V_{IH}		-	0.3	0.5	mA
Standby Current(CMOS)	I_{SB1}	$\overline{CE}$ ≧V_{CC}-0.2V	-L	-	20	80	µA
		other pins at 0.2V or Vcc-0.2V,	-LL	-	2	15	µA

CAPACITANCE (TA=25℃, f=1.0MHz)

PARAMETER	SYMBOL	MIN.	MAX	UNIT
Input Capacitance	C_{IN}	-	6	pF
Input/Output Capacitance	$C_{I/O}$	-	8	pF

Note : These parameters are guaranteed by device characterization, but not production tested.

AC TEST CONDITIONS

Input Pulse Levels	0V to 2.2V
Input Rise and Fall Times	5ns
Input and Output Timing Reference Levels	1.2V
Output Load	C_L = 30pF, I_{OH}/I_{OL} = -0.5mA/0.5mA

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 2.3V~2.7V , TA = -40℃ to 85℃(I))

(1) READ CYCLE

PARAMETER	SYMBOL	UT62V5128(I)-70		UT62V5128(I)-100		UNIT
		MIN.	MAX.	MIN.	MAX.	
Read Cycle Time	t_{RC}	70	-	100	-	ns
Address Access Time	t_{AA}	-	70	-	100	ns
Chip Enable Access Time	t_{ACE}	-	70	-	100	ns
Output Enable Access Time	t_{OE}	-	35	-	50	ns
Chip Enable to Output in Low Z	t_{CLZ*}	10	-	10	-	ns
Output Enable to Output in Low Z	t_{OLZ*}	5	-	5	-	ns
Chip Disable to Output in High Z	t_{CHZ*}	-	25	-	30	ns
Output Disable to Output in High Z	t_{OHZ*}	-	25	-	35	ns
Output Hold from Address Change	t_{OH}	5	-	5	-	ns

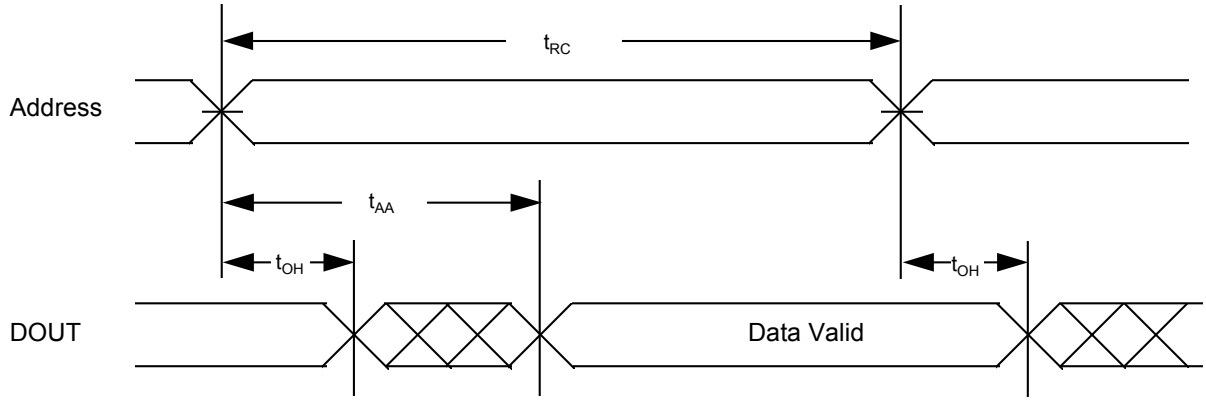
(2) WRITE CYCLE

PARAMETER	SYMBOL	UT62V5128(I)-70		UT62V5128(I)-100		UNIT
		MIN.	MAX.	MIN.	MAX.	
Write Cycle Time	t_{WC}	70	-	100	-	ns
Address Valid to End of Write	t_{AW}	60	-	80	-	ns
Chip Enable to End of Write	t_{CW}	60	-	80	-	ns
Address Set-up Time	t_{AS}	0	-	0	-	ns
Write Pulse Width	t_{WP}	55	-	70	-	ns
Write Recovery Time	t_{WR}	0	-	0	-	ns
Data to Write Time Overlap	t_{DW}	30	-	40	-	ns
Data Hold from End of Write Time	t_{DH}	0	-	0	-	ns
Output Active from End of Write	t_{OW*}	5	-	5	-	ns
Write to Output in High Z	t_{WHZ*}	-	30	-	40	ns

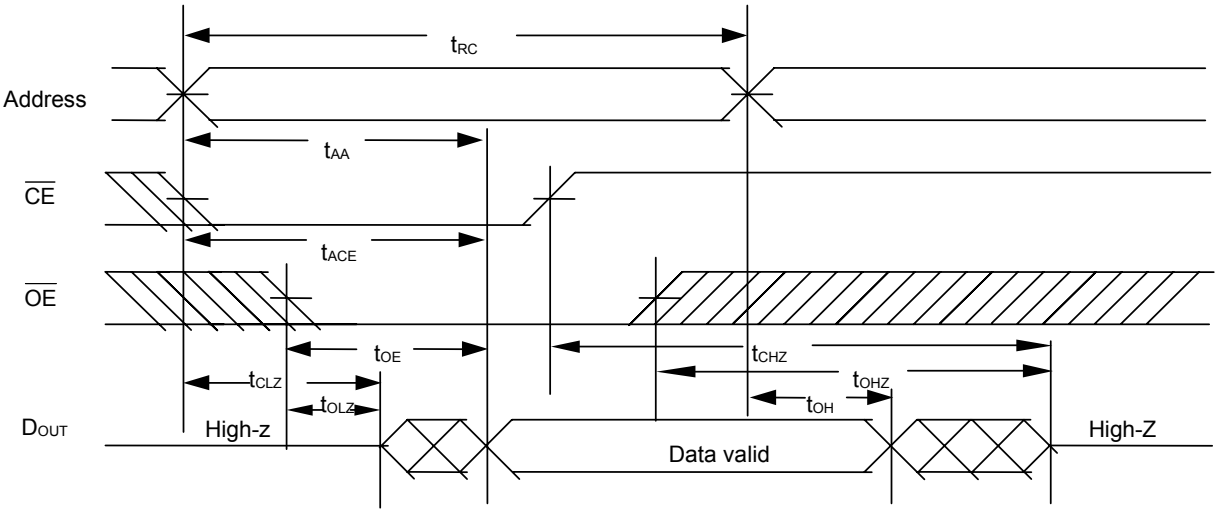
*These parameters are guaranteed by device characterization, but not production tested.

TIMING WAVEFORMS

READ CYCLE 1 (Address Controlled) (1,2,4)



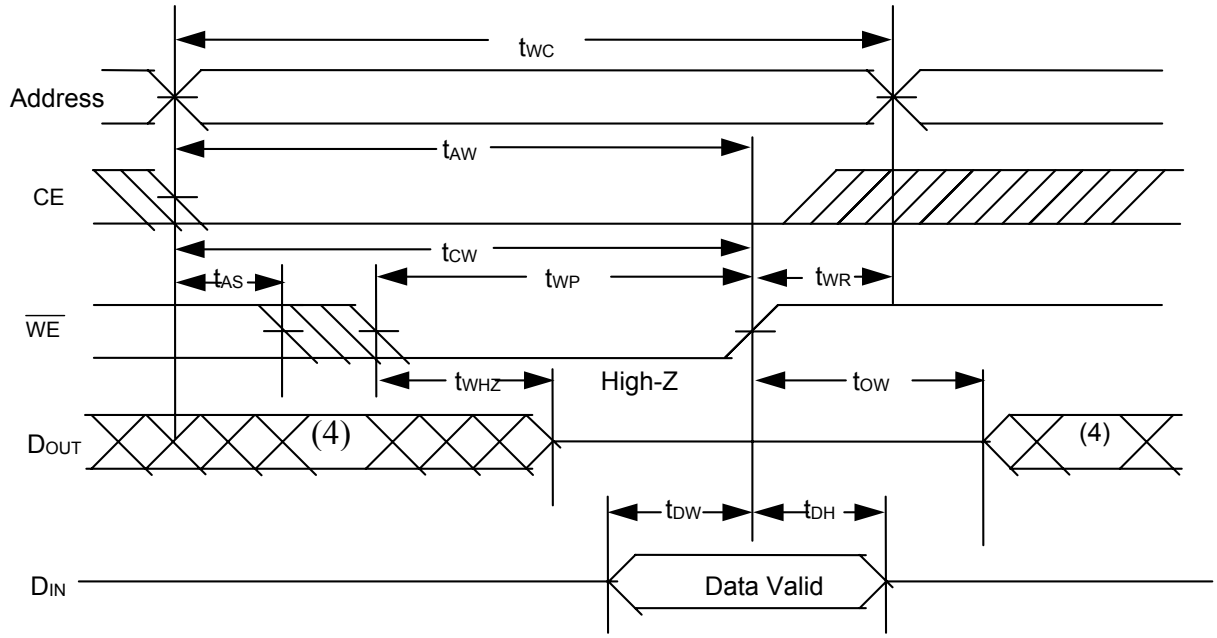
READ CYCLE 2 ($\overline{CE}$ and $\overline{OE}$ Controlled) (1,3,5,6)



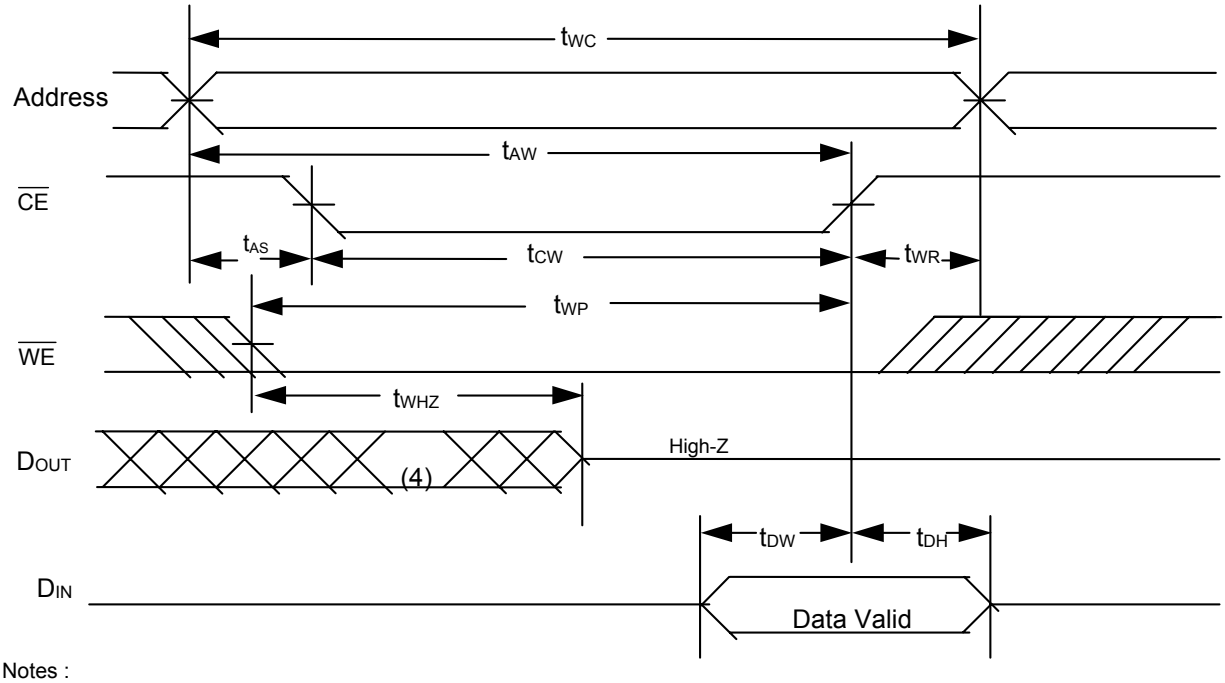
Notes :

1. $\overline{WE}$ is HIGH for read cycle.
2. Device is continuously selected $\overline{CE}$ =V_{IL}.
3. Address must be valid prior to or coincident with $\overline{CE}$ transition; otherwise t_{AA} is the limiting parameter.
4. $\overline{OE}$ is LOW.
5. t_{CLZ}, t_{OLZ}, t_{CHZ} and t_{OHZ} are specified with C_L = 5pF. Transition is measured ± 500mV from steady state.
6. At any given temperature and voltage condition, t_{CHZ} is less than t_{CLZ}, t_{OHZ} is less than t_{OLZ}.

WRITE CYCLE 1 ($\overline{WE}$ Controlled) (1,2,3,5)



WRITE CYCLE 2 ($\overline{CE}$ Controlled) (1,2,5)



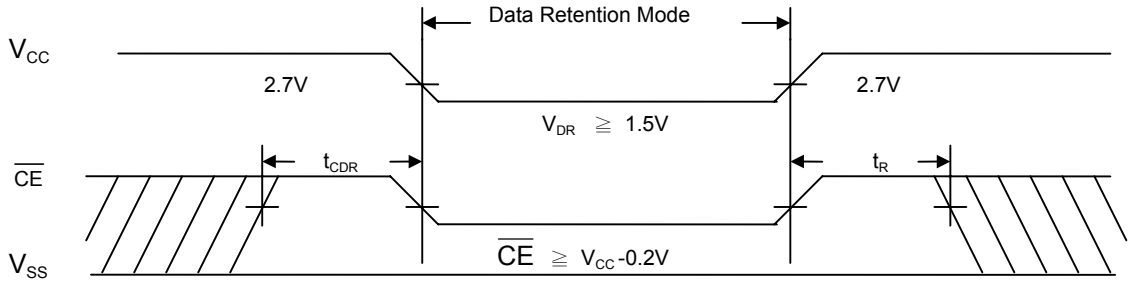
Notes :

1. $\overline{WE}$ or $\overline{CE}$ must be HIGH during all address transitions.
2. A write occurs during the overlap of a low $\overline{CE}$ and a low $\overline{WE}$.
3. During a $\overline{WE}$ controlled with write cycle with $\overline{OE}$ LOW, t_{WP} must be greater than $t_{WHZ}+t_{DW}$ to allow the drivers to turn off and data to be placed on the bus.
4. During this period, I/O pins are in the output state, and input singals must not be applied.
5. If the $\overline{CE}$ LOW transition occurs simultaneously with or after $\overline{WE}$ LOW transition, the outputs remain in a high impedance state.
6. 6. t_{OW} and t_{WHZ} are specified with C_L = 5pF. Transition is measured ± 500mV from steady state.

DATA RETENTION CHARACTERISTICS (TA = -40℃ to 85℃(I))

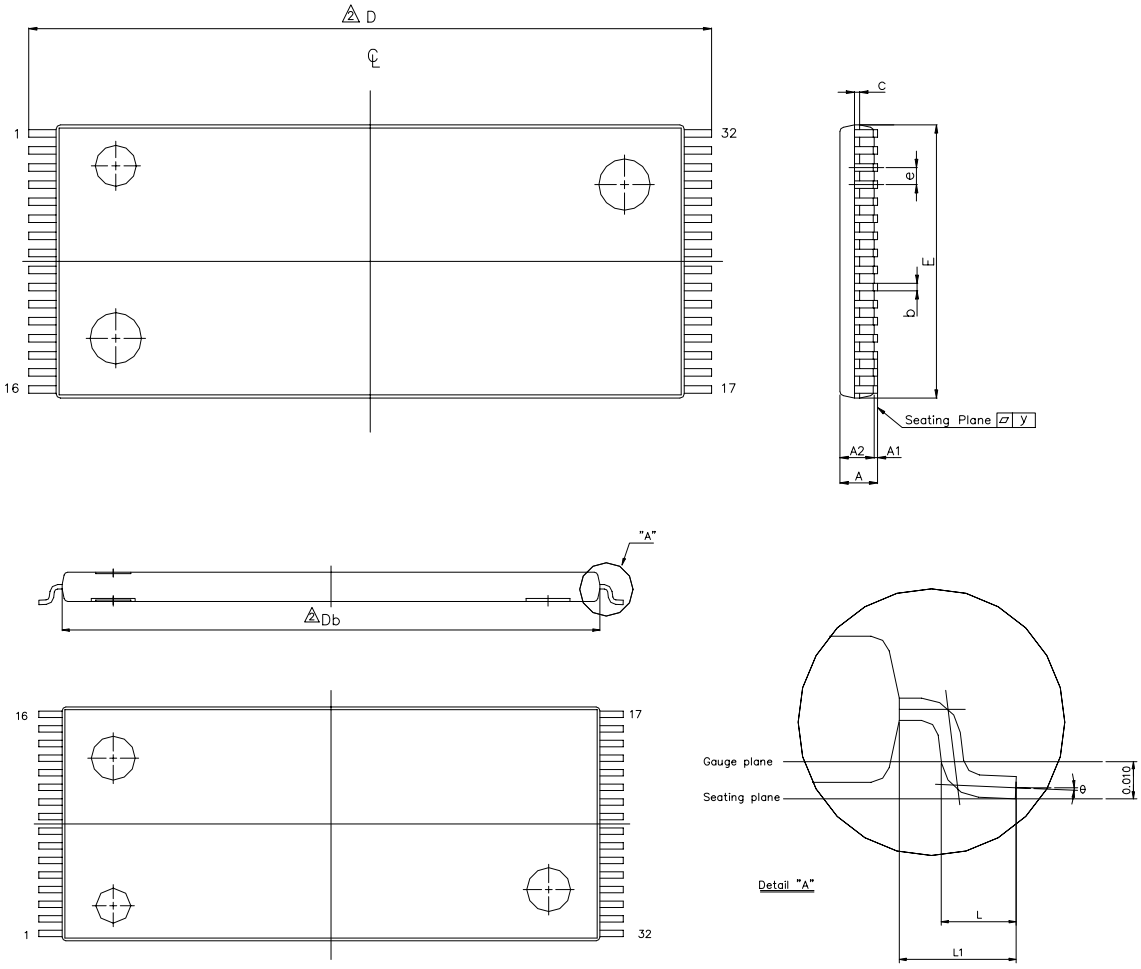
PARAMETER	SYMBOL	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
Vcc for Data Retention	V_{DR}	$\overline{CE} \geqq V_{CC}$-0.2V		1.5	-	-	V
Data Retention Current	I_{DR}	Vcc=1.5V	- L	-	1	50	µA
		$\overline{CE} \geqq V_{CC}$-0.2V	- LL	-	0.5	15	µA
Chip Disable to Data Retention Time	t_{CDR}	See Data Retention Waveforms (below)		0	-	-	ms
Recovery Time	t_R			5	-	-	ms

DATA RETENTION WAVEFORM



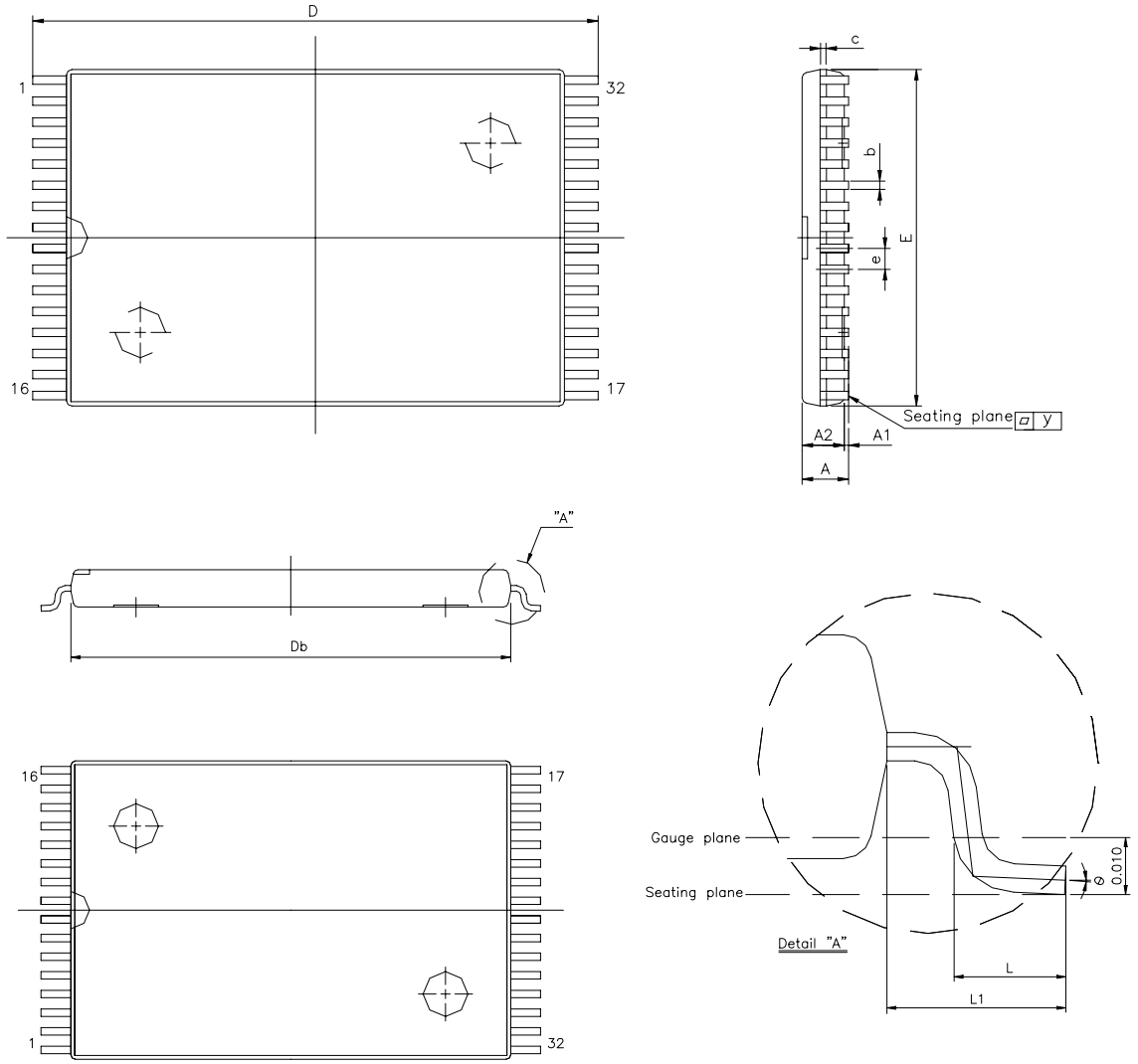
PACKAGE OUTLINE DIMENSION

32 pin 8mm × 20mm TSOP-I PACKAGE OUTLINE DIMENSION



SYMBOL \ UNIT	INCH(BASE)	MM(REF)
A	0.047 (MAX)	1.20 (MAX)
A1	0.004 ± 0.002	0.10 ± 0.05
A2	0.039 ± 0.002	1.00 ± 0.05
b	0.008 + 0.002	0.20 + 0.05
c	0.005 (TYP)	0.127 (TYP)
D	0.724 ± 0.004	18.40 ± 0.10
E	0.315 ± 0.004	8.00 ± 0.10
e	0.020 (TYP)	0.50 (TYP)
HD	0.787 ± 0.008	20.00 ± 0.20
L	0.0197 ± 0.004	0.50 ± 0.10
L1	0.0315 ± 0.004	0.08 ± 0.10
y	0.003 (MAX)	0.076 (MAX)
θ	0°～5°	0°～5°

32 pin STSOP PACKAGE OUTLINE DIMENSION



Note：
1.E dimension is not including end flash.
2.The total of both sides' end flash Is not above 0.3mm.

SYMBOL \ UNIT	MM(REF)	INCH(BASE)
A	1.20(Max.)	0.047(Max).
A1	0.1060.05	0.00460.002
A2	1.0060.05	0.03960.002
b	020(typ.)	0.006(typ.)
c	0.15(typ.)	0.006(typ.)
D	13.4060.20	0.52660.006
Db	11.8060.10	0.46560.004
E	8.00060.10	0.31560.004
e	0.50(typ.)	0.020(typ.)
L	0.5060.10	0.02060.004
L1	0.8060.10	0.031560.004
y	0.08(Max.)	0.003(Max.)
e	08~58	08~58

ORDERING INFORMATION

INDUSTRIAL TEMPERATURE

PART NO.	ACCESS TIME (ns)	STANDBY CURRENT (µA) TYP.	PACKAGE
UT62V5128LC-70LI	70	20	32 PIN TSOP- I
UT62V5128LC-70LLI	70	2	32 PIN TSOP- I
UT62V5128LC-100LI	100	20	32 PIN TSOP- I
UT62V5128LC-100LLI	100	2	32 PIN TSOP- I
UT62V5128LS-70LI	70	20	36 PIN STSOP
UT62V5128LS-70LLI	70	2	36 PIN STSOP
UT62V5128LS-100LI	100	20	36 PIN STSOP
UT62V5128LS-100LLI	100	2	36 PIN STSOP

REVISION HISTORY

REVISION	DESCRIPTION	DATE
Preliminary Rev. 0.1	Original.	Mar, 2001
Rev. 1.0	1. The symbols CE# and OE# and WE# are revised as. $\overline{CE}$ and $\overline{OE}$ and $\overline{WE}$. 2. Separate Industrial and Consumer SPEC.	Aug 7,2001