FEATURES

- Fast access time :
  55ns(max.) for Vcc=2.7V~3.6V
  70ns(max.) for Vcc=2.5V~3.6V
- CMOS Low operating power
  Operating : 40/25mA (Icc max.)
  Standby : T_A=0℃~50℃
  20 uA(max.) L -version
  3 uA(max.) LL-version
- Single 2.5V~3.6V power supply
- Operating temperature:
  Industrial : -40℃~85℃
- All inputs and outputs TTL compatible
- Fully static operation
- Three state outputs
- Data retention voltage: 1.5V (min)
- Package : 32-pin 8mm x 20mm TSOP-Ⅰ
  32-pin 8mm x 13.4mm STSOP
  36-pin 6mm × 8mm TFBGA

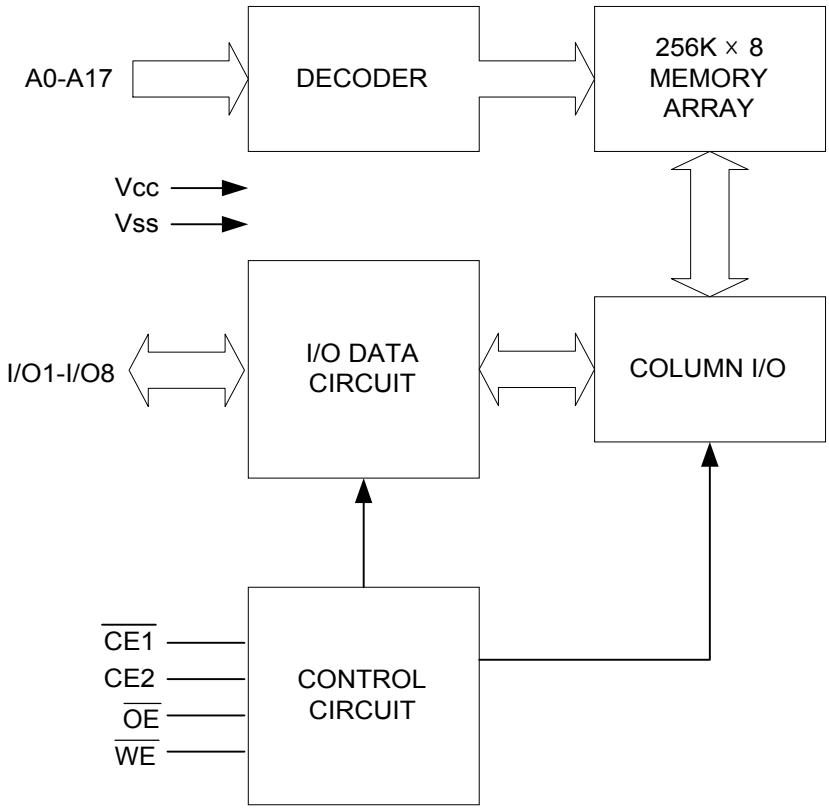
GENERAL DESCRIPTION

The UT62L2568 is a 2,097,152-bit low power CMOS static random access memory organized as 262,144 words by 8 bits. It is fabricated using high performance, high reliability CMOS technology.

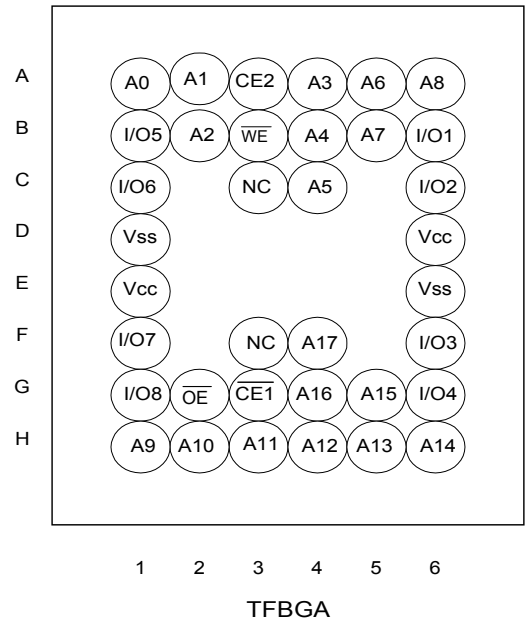
The UT62L2568 is designed for very low power system applications. It is particularly well suited for battery back-up nonvolatile memory applications.

It operates from a wide range of 2.5V~ 3.6V supply voltage. Easy memory expansion is provided by using two chip enable input ($\overline{CE1}$,CE2). And all inputs and three-state outputs are fully TTL compatible.

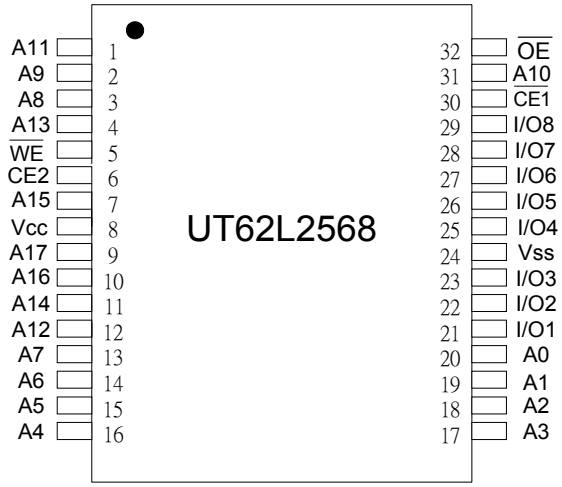
FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



TFBGA



TSOP-1 / STSOP

PIN DESCRIPTION

SYMBOL	DESCRIPTION
A0 - A17	Address Inputs
I/O1 - I/O8	Data Inputs/Outputs
$\overline{CE1}$,CE2	Chip Enable Inputs
$\overline{WE}$	Write Enable Input
$\overline{OE}$	Output Enable Input
V_{CC}	Power Supply
V_{SS}	Ground
NC	No Connection

TRUTH TABLE

MODE	$\overline{CE1}$	CE2	$\overline{OE}$	$\overline{WE}$	I/O OPERATION	SUPPLY CURRENT
Standby	H	X	X	X	High - Z	I_{SB},I_{SB1} , I_{SB2}
	X	L	X	X	High -Z	I_{SB},I_{SB1} , I_{SB2}
Output Disable	L	H	H	H	High - Z	I_{CC} , Icc1 , Icc2
Read	L	H	L	H	D_{OUT}	$I_{CC,}$ Icc1 , Icc2
Write	L	H	X	L	D_{IN}	$I_{CC,}$ Icc1 , Icc2

Note: H = V_{IH}, L=V_{IL}, X = Don't care.

ABSOLUTE MAXIMUM RATINGS*

PARAMETER	SYMBOL	RATING	UNIT
Terminal Voltage with Respect to V_{SS}	V_{TERM}	-0.5 to Vcc+0.3V	V
Operating Temperature Industrial	T_A	-40 to 85	℃
Storage Temperature	T_{STG}	-65 to 150	℃
Power Dissipation	P_D	1	W
DC Output Current	I_{OUT}	50	mA
Soldering Temperature (under 10 secs)	Tsolder	260	℃

*Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect device reliability.

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 2.5V~3.6V, T_A = -40℃ to 85℃)

PARAMETER	SYMBOL	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
Power Voltage	Vcc			2.5	3.0	3.6	V
Input High Voltage	V_{IH}			2.2	-	Vcc+0.3	V
Input Low Voltage	V_{IL}			- 0.3	-	0.6	V
Input Leakage Current	I_{LI}	V_{SS} ≦V_{IN} ≦V_{CC}		- 1	-	1	µA
Output Leakage Current	I_{LO}	V_{SS} ≦$V_{I/O}$ ≦$V_{CC,}$ Output Disabled		- 1	-	1	µA
Output High Voltage	V_{OH}	I_{OH}= - 1mA		2.2	-	-	V
Output Low Voltage	V_{OL}	I_{OL}= 2.1mA		-	-	0.4	V
Operating Current	I_{CC}	Cycle time=Min.100% duty, $\overline{CE1}$ =V_{IL}, CE2 = V_{IH}, $I_{I/O}$ =0mA	55	-	25	40	mA
			70	-	15	25	mA
	Icc_1	Cycle time = 1µs,100% duty, $\overline{CE1}$ ≦0.2V,CE2≧V_{CC}-0.2V, $I_{I/O=}$0mA, other pins at 0.2V or Vcc-0.2V,		-	4	5	mA
	Icc_2	Cycle time =500ns,100% duty, $\overline{CE1}$ ≦0.2V,CE2≧V_{CC}-0.2V, $I_{I/O=}$0mA, other pins at 0.2V or Vcc-0.2V,		-	8	10	mA
Standby Current (TTL)	I_{SB}	$\overline{CE1}$ =V_{IH} or CE2 = V_{IL}		-	0.3	0.5	mA
Standby Current (CMOS)	I_{SB1}	$\overline{CE1}$ ≧V_{CC}-0.2V or CE2≦0.2V, other pins at 0.2V or Vcc-0.2V, T_A=0℃~50℃	-L	-	-	20	µA
			-LL	-	-	3	µA
	I_{SB2}	$\overline{CE1}$ ≧V_{CC}-0.2V or CE2≦0.2V, other pins at 0.2V or Vcc-0.2V, T_A= - 40℃~85℃	-L	-	-	80	µA
			-LL	-	-	10	µA

CAPACITANCE (T_A=25℃, f=1.0MHz)

PARAMETER	SYMBOL	MIN.	MAX	UNIT
Input Capacitance	C_{IN}	-	6	pF
Input/Output Capacitance	$C_{I/O}$	-	8	pF

Note : These parameters are guaranteed by device characterization, but not production tested.

AC TEST CONDITIONS

Input Pulse Levels	0V to 3V
Input Rise and Fall Times	5ns
Input and Output Timing Reference Levels	1.5V
Output Load	C_L = 30pF+1TTL, I_{OH}= -1mA, I_{OL}= 2.1mA

AC ELECTRICAL CHARACTERISTICS (T_A = - 40℃ to 85℃)

(1) READ CYCLE

PARAMETER	SYMBOL	UT62L2568-55 V_{CC} = 2.7V~3.6V		UT62L2568-70 V_{CC} = 2.5V~3.6V		UNIT
		MIN.	MAX.	MIN.	MAX.	
Read Cycle Time	t_{RC}	55	-	70	-	ns
Address Access Time	t_{AA}	-	55	-	70	ns
Chip Enable Access Time	t_{ACE1}, t_{ACE2}	-	55	-	70	ns
Output Enable Access Time	t_{OE}	-	30	-	35	ns
Chip Enable to Output in Low Z	t_{CLZ1*}, t_{CLZ2*}	10	-	10	-	ns
Output Enable to Output in Low Z	t_{OLZ*}	5	-	5	-	ns
Chip Disable to Output in High Z	t_{CHZ1*}, t_{CHZ2*}	-	20	-	25	ns
Output Disable to Output in High Z	t_{OHZ*}	-	20	-	25	ns
Output Hold from Address Change	t_{OH}	10	-	10	-	ns

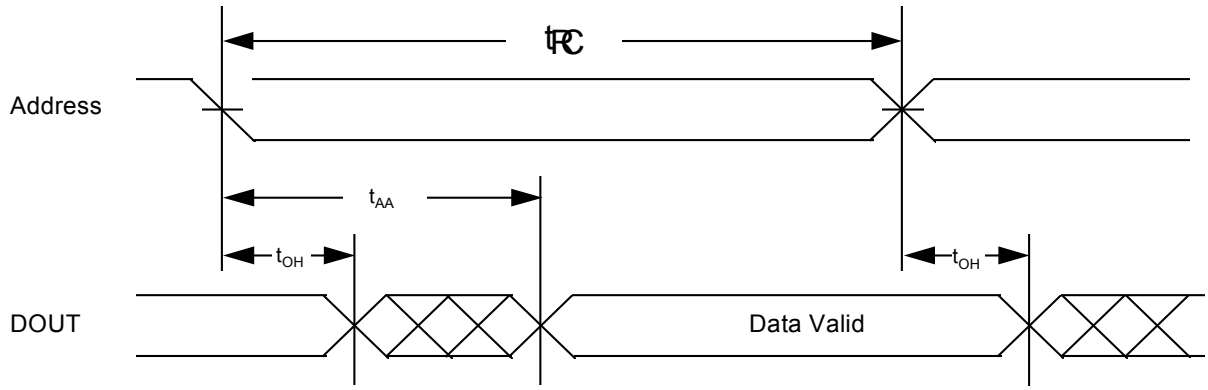
(2) WRITE CYCLE

PARAMETER	SYMBOL	UT62L2568-55 V_{CC} = 2.7V~3.6V		UT62L2568-70 V_{CC} = 2.5V~3.6V		UNIT
		MIN.	MAX.	MIN.	MAX.	
Write Cycle Time	t_{WC}	55	-	70	-	ns
Address Valid to End of Write	t_{AW}	50	-	60	-	ns
Chip Enable to End of Write	t_{CW1}, t_{CW2}	50	-	60	-	ns
Address Set-up Time	t_{AS}	0	-	0	-	ns
Write Pulse Width	t_{WP}	45	-	55	-	ns
Write Recovery Time	t_{WR}	0	-	0	-	ns
Data to Write Time Overlap	t_{DW}	25	-	30	-	ns
Data Hold from End of Write Time	t_{DH}	0	-	0	-	ns
Output Active from End of Write	t_{OW*}	5	-	5	-	ns
Write to Output in High Z	t_{WHZ*}	-	30	-	30	ns

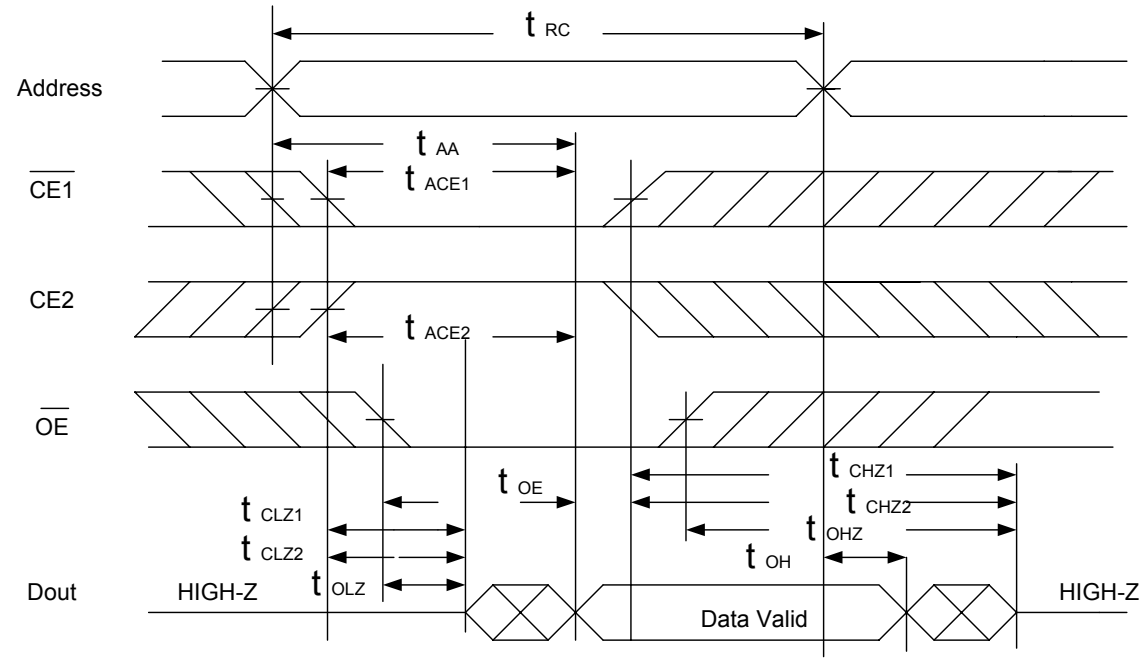
*These parameters are guaranteed by device characterization, but not production tested.

TIMING WAVEFORMS

READ CYCLE 1 (Address Controlled) (1,2,4)



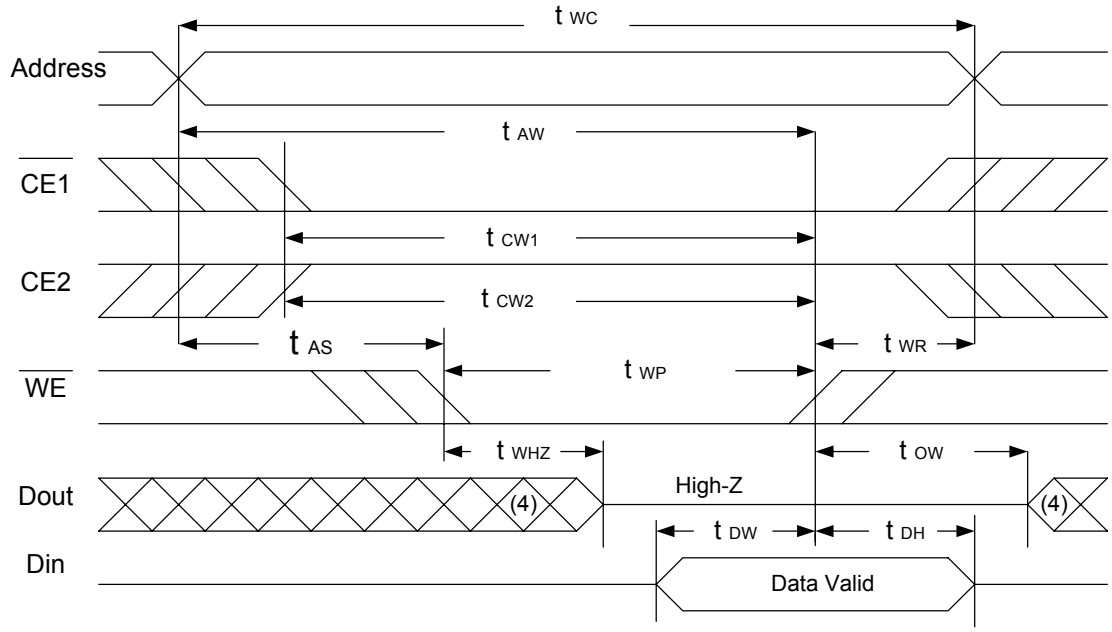
READ CYCLE 2 ($\overline{CE1}$, CE2 and $\overline{OE}$ Controlled) (1,3,5,6)



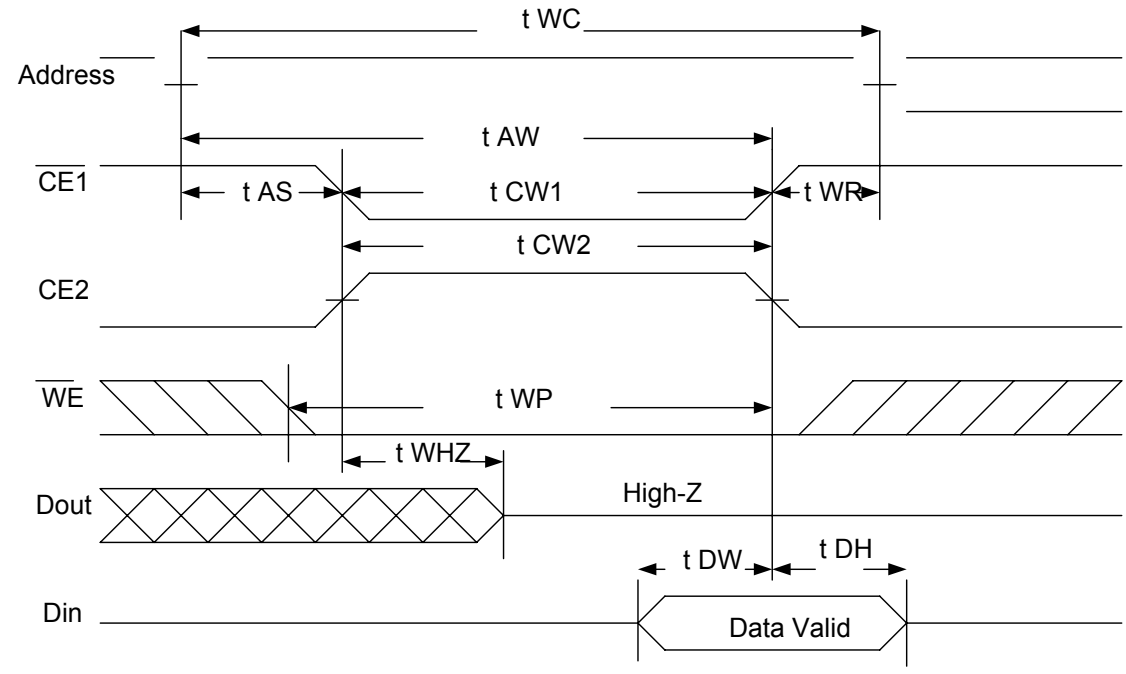
Notes :

1. $\overline{WE}$ is HIGH for a read cycle.
2. Device is continuously selected $\overline{OE}$, $\overline{CE1}$ =V_{IL} and CE2=V_{IH}.
3. Address must be valid prior to or coincident with $\overline{CE1}$ low and CE2 high transition; otherwise t_{AA} is the limiting parameter.
4. $\overline{OE}$ is low.
5. t_{CLZ1}, t_{CLZ2}, t_{OLZ}, t_{CHZ1}, t_{CHZ2} and t_{OHZ} are specified with C_L=5pF. Transition is measured ±500mV from steady state.
6. At any given temperature and voltage condition, t_{CHZ1} is less than t_{CLZ1}, t_{CHZ2} is less than t_{CLZ2}, t_{OHZ} is less than t_{OLZ}.

WRITE CYCLE 1 ($\overline{WE}$ Controlled) (1,2,3,5)



WRITE CYCLE 2 ($\overline{CE1}$ and CE2 Controlled) (1,2,5)



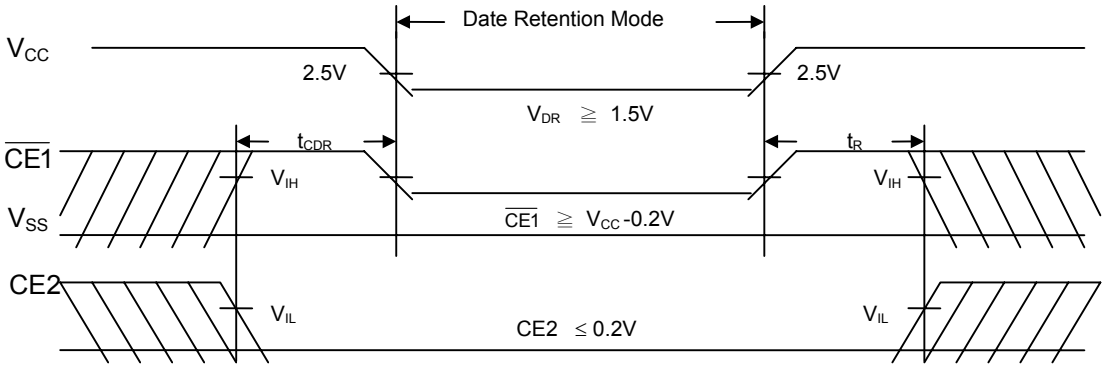
Notes :

1. $\overline{WE}$ or $\overline{CE1}$ must be HIGH or CE2 must be LOW during all address transitions.
2. A write occurs during the overlap of a low $\overline{CE1}$, a high CE2 and a low $\overline{WE}$.
3. During a $\overline{WE}$ controlled with write cycle with $\overline{OE}$ LOW, t_{WP} must be greater than $t_{WHZ}+t_{DW}$ to allow the I/O drivers to turn off and data to be placed on the bus.
4. During this period, I/O pins are in the output state, and input signals must not be applied.
4. If the $\overline{CE1}$ LOW transition occurs simultaneously with or after $\overline{WE}$ LOW transition, the outputs remain in a high Impedance state.
6. t_{OW} and t_{WHZ} are specified with C_L=5pF. Transition is measured ±500mV from steady state.

DATA RETENTION CHARACTERISTICS (T_A = - 40℃ to 85℃)

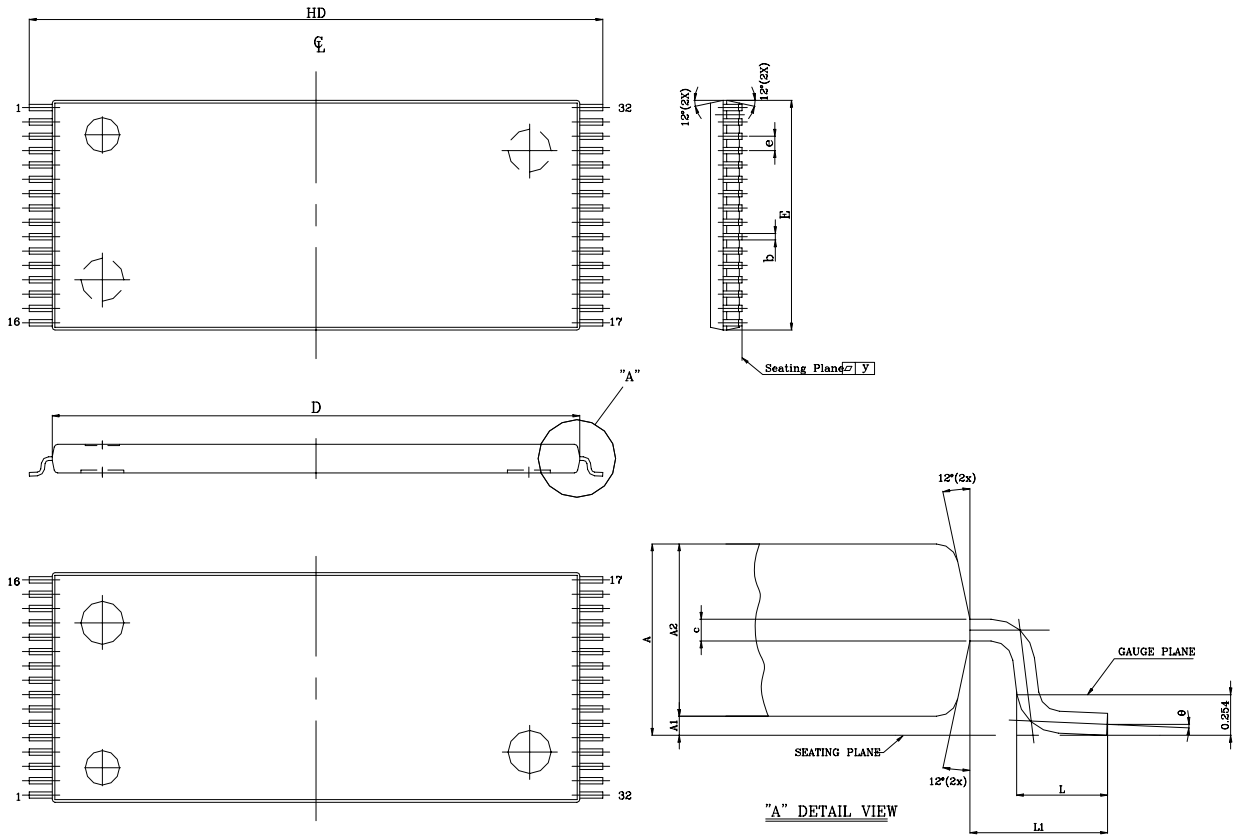
PARAMETER	SYMBOL	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
Vcc for Data Retention	V_{DR}	$\overline{CE} \geqq V_{CC}$-0.2V		1.5	-	3.6	V
Data Retention Current	I_{DR}	Vcc=1.5V	- L	-		80	µA
		$\overline{CE} \geqq V_{CC}$-0.2V	- LL	-		25	µA
Chip Disable to Data Retention Time	t_{CDR}	See Data Retention Waveforms (below)		0	-	-	ms
Recovery Time	t_R			5	-	-	ms

DATA RETENTION WAVEFORM



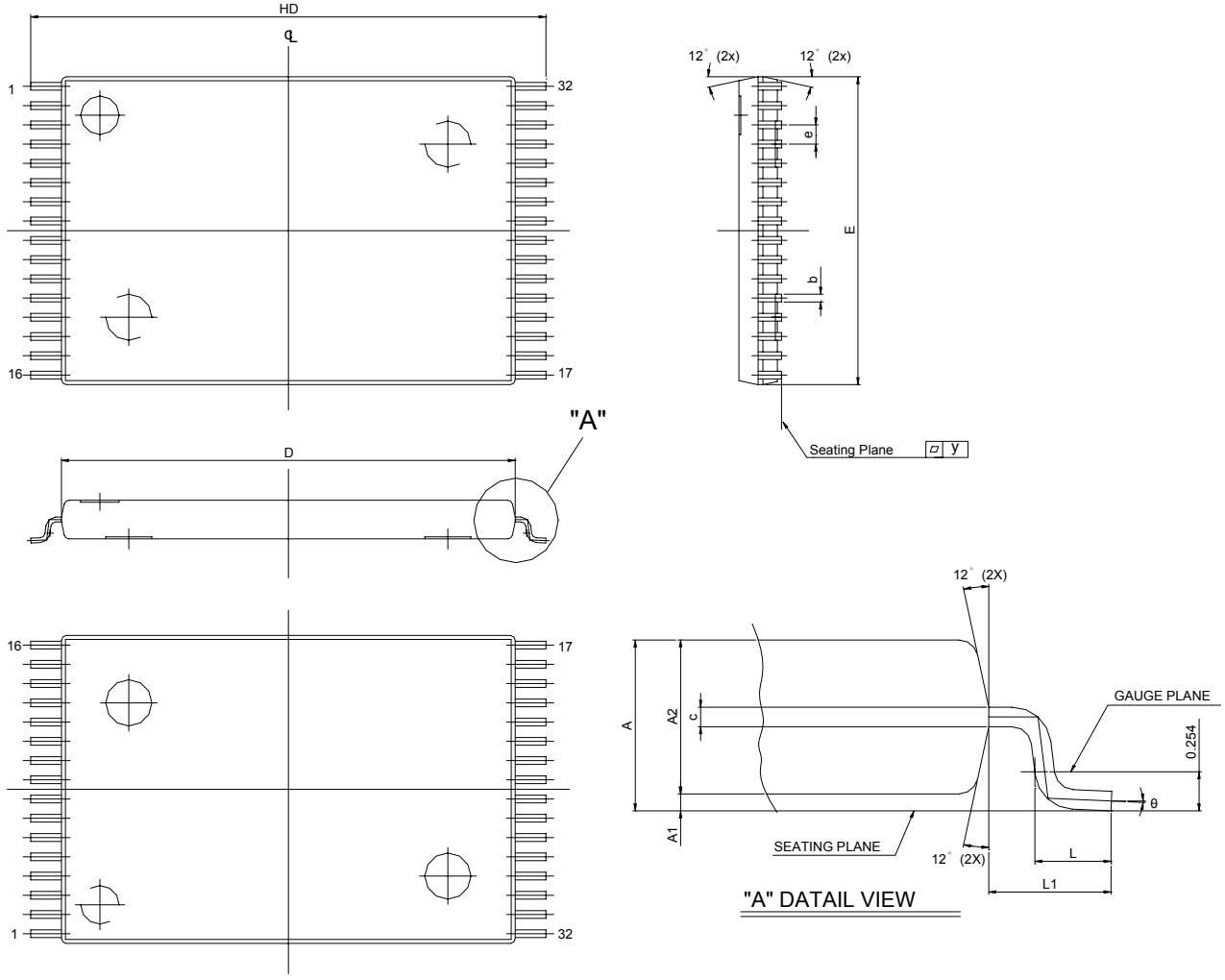
PACKAGE OUTLINE DIMENSION

32 pin 8mm x 20mm TSOP-I Package Outline Dimension



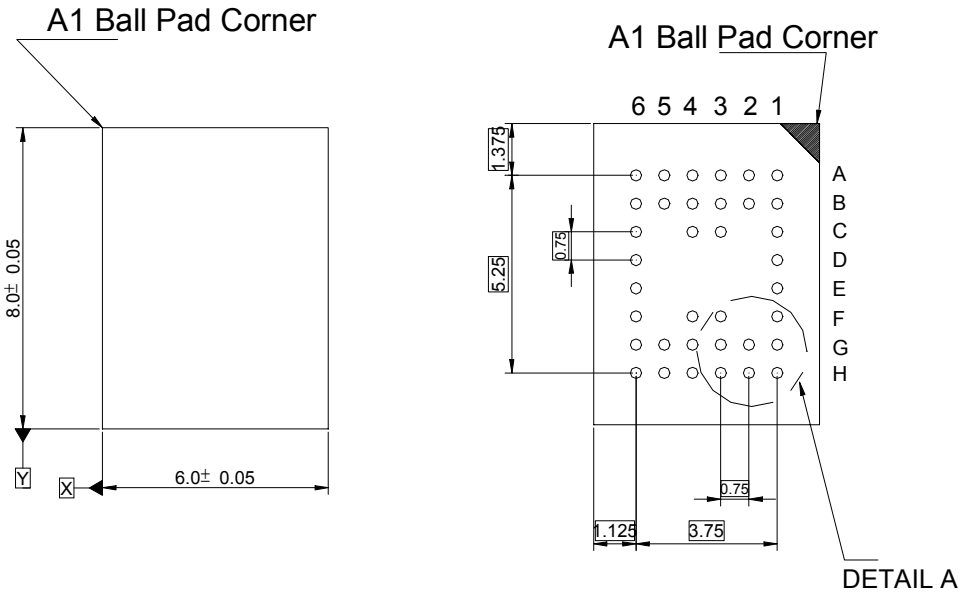
SYMBOL \ UNIT	INCH(BASE)	MM(REF)
A	0.047 (MAX)	1.20 (MAX)
A1	0.004 ±0.002	0.10 ±0.05
A2	0.039 ±0.002	1.00 ±0.05
b	0.008 + 0.002 - 0.001	0.20 + 0.05 -0.03
c	0.005 (TYP)	0.127 (TYP)
D	0.724 ±0.004	18.40 ±0.10
E	0.315 ±0.004	8.00 ±0.10
e	0.020 (TYP)	0.50 (TYP)
HD	0.787 ±0.008	20.00 ±0.20
L	0.0197 ±0.004	0.50 ±0.10
L1	0.0315 ±0.004	0.08 ±0.10
y	0.003 (MAX)	0.076 (MAX)
θ	0°～5°	0°～5°

32 pin 8mm x 13.4mm STSOP Package Outline Dimension



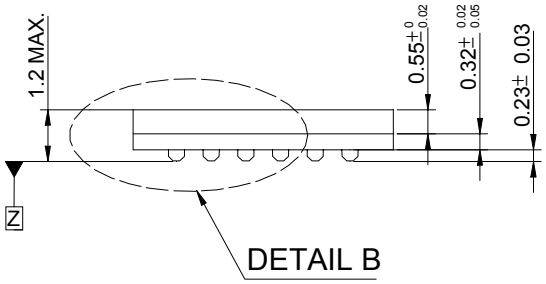
SYMBOL \ UNIT	INCH(BASE)	MM(REF)
A	0.049 (MAX)	1.25 (MAX)
A1	0.005 ±0.002	0.130 ±0.05
A2	0.039 ±0.002	1.00 ±0.05
b	0.008 ±0.01	0.20±0.025
c	0.005 (TYP)	0.127 (TYP)
D	0.465 ±0.004	11.80 ±0.10
E	0.315 ±0.004	8.00 ±0.10
e	0.020 (TYP)	0.50 (TYP)
HD	0.528±0.008	13.40 ±0.20.
L	0.0197 ±0.004	0.50 ±0.10
L1	0.0315 ±0.004	0.8 ±0.10
y	0.003 (MAX)	0.076 (MAX)
Θ	0°～5°	0°～5°

36 pin 6mm×8mm TFBGA Package Outline Dimension

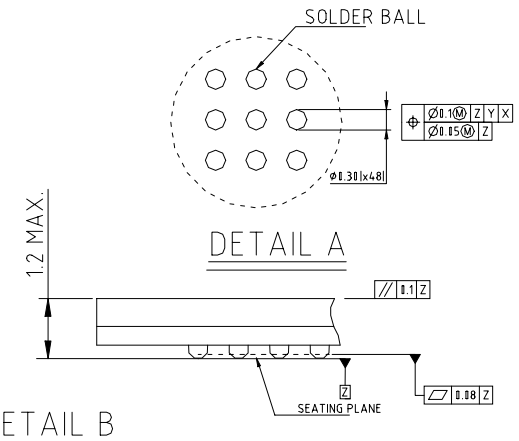


TOP VIEW (DIE VIEW)

BOTTOM VIEW (BALL SIDE)



SIDE VIEW



ORDERING INFORMATION

INDUSTRIAL TEMPERATURE

PART NO.	ACCESS TIME (ns)	STANDBY CURRENT (μA) max. T_A = 0℃ ~ 50℃	PACKAGE
UT62L2568LC-55LI	55	20	32 PIN TSOP-Ⅰ
UT62L2568LC-55LLI	55	3	32 PIN TSOP-Ⅰ
UT62L2568LC-70LI	70	20	32 PIN TSOP-Ⅰ
UT62L2568LC-70LLI	70	3	32 PIN TSOP-Ⅰ
UT62L2568LS-55LI	55	20	32 PIN STSOP
UT62L2568LS-55LLI	55	3	32 PIN STSOP
UT62L2568LS-70LI	70	20	32 PIN STSOP
UT62L2568LS-70LLI	70	3	32 PIN STSOP
UT62L2568BS-55LI	55	20	36 PIN TFBGA
UT62L2568BS-55LLI	55	3	36 PIN TFBGA
UT62L2568BS-70LI	70	20	36 PIN TFBGA
UT62L2568BS-70LLI	70	3	36 PIN TFBGA

REVISION HISTORY

REVISION	DESCRIPTION	DATE
Preliminary Rev. 0.1	Original.	Nov 28, 2001