



**FEATURES**

- Fast access time : 55/70/100 ns
- CMOS Low operating power  
Operating current: 45/35/25mA (I<sub>cc</sub> max)  
Standby current: 20 uA(TYP.) L-version  
3 uA(TYP.) LL-version
- Single 2.7V~3.6V power supply
- Operating temperature:  
Commercial : 0°C~70°C  
Extended : -20°C~80°C
- All inputs and outputs TTL compatible
- Fully static operation
- Three state outputs
- Data retention voltage: 1.5V (min)
- Data byte control :  $\overline{LB}$  (I/O1~I/O8)  
 $\overline{UB}$  (I/O9~I/O16)
- Package : 44-pin 400mil TSOP II  
48-pin 6mm × 8mm TFBGA

**GENERAL DESCRIPTION**

The UT62L25616 is a 4,194,304-bit low power CMOS static random access memory organized as 262,144 words by 16 bits.

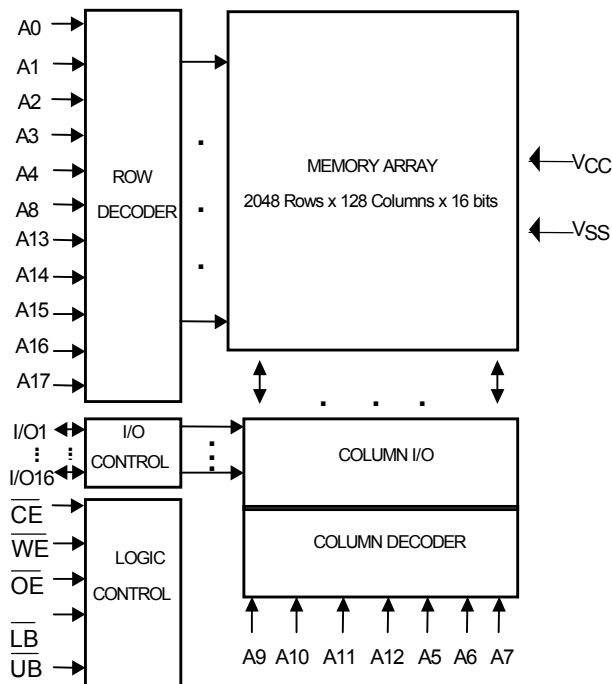
The UT62L25616 operates from a single 2.7V ~ 3.6V power supply and all inputs and outputs are fully TTL compatible.

The UT62L25616 is designed for low power system applications. It is particularly suited for use in high-density high-speed system applications.

**PIN DESCRIPTION**

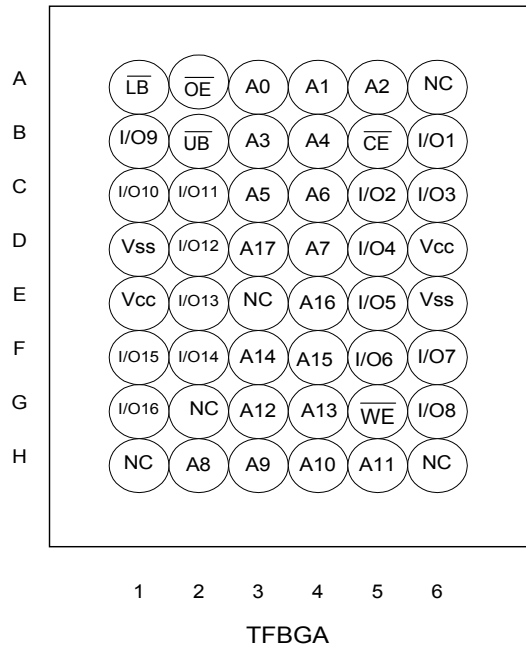
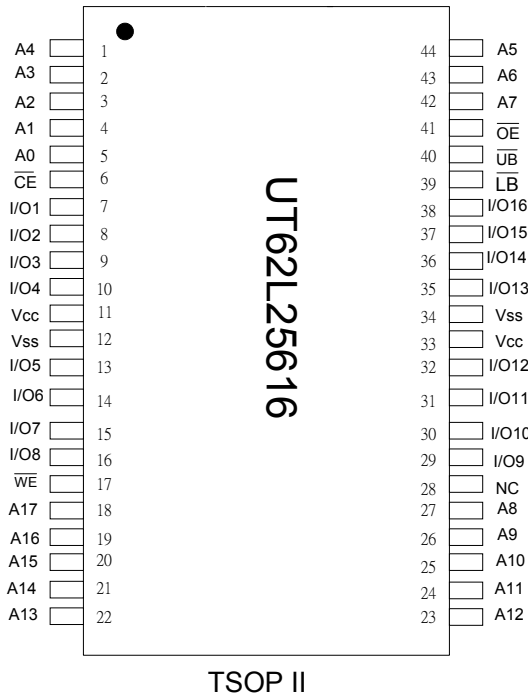
SYMBOL	DESCRIPTION
A0 - A17	Address Inputs
I/O1 - I/O16	Data Inputs/Outputs
$\overline{CE}$	Chip Enable Input
$\overline{WE}$	Write Enable Input
$\overline{OE}$	Output Enable Input
$\overline{LB}$	Lower-Byte Control
$\overline{UB}$	High-Byte Control
V <sub>CC</sub>	Power Supply
V <sub>SS</sub>	Ground
NC	No Connection

**FUNCTIONAL BLOCK DIAGRAM**





**PIN CONFIGURATION**



**TRUTH TABLE**

MODE	CE	OE	WE	LB	UB	I/O OPERATION		SUPPLY CURRENT
						I/O1-I/O8	I/O9-I/O16	
Standby	H	X	X	X	X	High - Z	High - Z	$I_{SB}, I_{SB1}$
	X	X	X	H	H	High - Z	High - Z	$I_{SB}, I_{SB1}$
Output Disable	L	H	H	L	X	High - Z	High - Z	$I_{CC}, I_{CC1}, I_{CC2}$
	L	H	H	X	L	High - Z	High - Z	$I_{CC}, I_{CC1}, I_{CC2}$
Read	L	L	H	L	H	$D_{OUT}$	High - Z	$I_{CC}, I_{CC1}, I_{CC2}$
	L	L	H	H	L	High - Z	$D_{OUT}$	$I_{CC}, I_{CC1}, I_{CC2}$
	L	L	H	L	L	$D_{OUT}$	$D_{OUT}$	$I_{CC}, I_{CC1}, I_{CC2}$
Write	L	X	L	L	H	$D_{IN}$	High - Z	$I_{CC}, I_{CC1}, I_{CC2}$
	L	X	L	H	L	High - Z	$D_{IN}$	$I_{CC}, I_{CC1}, I_{CC2}$
	L	X	L	L	L	$D_{IN}$	$D_{IN}$	$I_{CC}, I_{CC1}, I_{CC2}$

Note: H =  $V_{IH}$ , L =  $V_{IL}$ , X = Don't care.

**ABSOLUTE MAXIMUM RATINGS\***

PARAMETER	SYMBOL	RATING	UNIT
Terminal Voltage with Respect to $V_{SS}$	$V_{TERM}$	-0.5 to 4.6	V
Operating Temperature	Commercial	$T_A$	0 to 70
	Extended	$T_A$	-20 to 80
Storage Temperature	$T_{STG}$	-65 to +150	°C
Power Dissipation	$P_D$	1	W
DC Output Current	$I_{OUT}$	50	mA
Soldering Temperature (under 10 secs)	$T_{solder}$	260	°C

\*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect device reliability.

**DC ELECTRICAL CHARACTERISTICS** ( $V_{CC} = 2.7V \sim 3.6V$ ,  $T_A = 0^\circ C$  to  $70^\circ C$  /  $-20^\circ C$  to  $80^\circ C$ (E))

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT	
Power Voltage	$V_{CC}$		2.7	3.0	3.6	V	
Input High Voltage	$V_{IH}$		2.0	-	$V_{CC}+0.3$	V	
Input Low Voltage	$V_{IL}$		-0.2	-	0.6	V	
Input Leakage Current	$I_{LI}$	$V_{SS} \leq V_{IN} \leq V_{CC}$	-1	-	1	$\mu A$	
Output Leakage Current	$I_{LO}$	$V_{SS} \leq V_{IO} \leq V_{CC}$ ; Output Disabled	-1	-	1	$\mu A$	
Output High Voltage	$V_{OH}$	$I_{OH} = -1mA$	2.2	-	-	V	
Output Low Voltage	$V_{OL}$	$I_{OL} = 2.1mA$	-	-	0.4	V	
Operating Power Supply Current	$I_{CC}$	Cycle time=min, 100%duty, I/O=0mA, $\overline{CE} = V_{IL}$ ;	55	-	30	45	mA
			70	-	25	35	mA
			100	-	20	25	mA
Average Operation Current	icc1	Cycle time=1 $\mu s$ , 100%duty, I/O=0mA, $\overline{CE} \leq 0.2V$ , other pins at 0.2V or $V_{CC}-0.2V$ ,	-	4	5	mA	
	icc2	Cycle time=500ns, 100%duty, I/O=0mA, $\overline{CE} \leq 0.2V$ , other pins at 0.2V or $V_{CC}-0.2V$ ,	-	8	10	mA	
Standby Current (TTL)	$I_{SB}$	$\overline{CE} = V_{IH}$ , other pins = $V_{IL}$ or $V_{IH}$ ,	-	0.3	0.5	mA	
Standby Current (CMOS)	$I_{SB1}$	$\overline{CE} = V_{CC}-0.2V$ , other pins at 0.2V or $V_{CC}-0.2V$ ,	-L	-	20	80	$\mu A$
			-LL	-	3	25	$\mu A$

**CAPACITANCE** (TA=25°C, f=1.0MHz)

PARAMETER	SYMBOL	MIN.	MAX	UNIT
Input Capacitance	C <sub>IN</sub>	-	6	pF
Input/Output Capacitance	C <sub>I/O</sub>	-	8	pF

Note : These parameters are guaranteed by device characterization, but not production tested.

**AC TEST CONDITIONS**

Input Pulse Levels	0V to 3.0V
Input Rise and Fall Times	5ns
Input and Output Timing Reference Levels	1.5V
Output Load	C <sub>L</sub> = 30pF, I <sub>OH</sub> /I <sub>OL</sub> = -1mA / 2.1mA

**AC ELECTRICAL CHARACTERISTICS** (VCC = 2.7V~3.6V, TA = 0°C to 70°C / -20°C to 80°C (E))**(1) READ CYCLE**

PARAMETER	SYMBOL	UT62L25616-55		UT62L25616-70		UT62L25616-100		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Read Cycle Time	t <sub>RC</sub>	55	-	70	-	100	-	ns
Address Access Time	t <sub>AA</sub>	-	55	-	70	-	100	ns
Chip Enable Access Time	t <sub>ACE</sub>	-	55	-	70	-	100	ns
Output Enable Access Time	t <sub>OE</sub>	-	30	-	35	-	50	ns
Chip Enable to Output in Low Z	t <sub>CLZ*</sub>	10	-	10	-	10	-	ns
Output Enable to Output in Low Z	t <sub>OLZ*</sub>	5	-	5	-	5	-	ns
Chip Disable to Output in High Z	t <sub>CHZ*</sub>	-	20	-	25	-	30	ns
Output Disable to Output in High Z	t <sub>OHZ*</sub>	-	20	-	25	-	30	ns
Output Hold from Address Change	t <sub>OH</sub>	5	-	5	-	5	-	ns
$\overline{LB}, \overline{UB}$ Access Time	t <sub>BA</sub>	-	55	-	70	-	100	ns
$\overline{LB}, \overline{UB}$ to High-Z Output	t <sub>HZB</sub>	-	25	-	30	-	40	ns
$\overline{LB}, \overline{UB}$ to Low-Z Output	t <sub>LZB</sub>	0	-	0	-	0	-	ns

**(2) WRITE CYCLE**

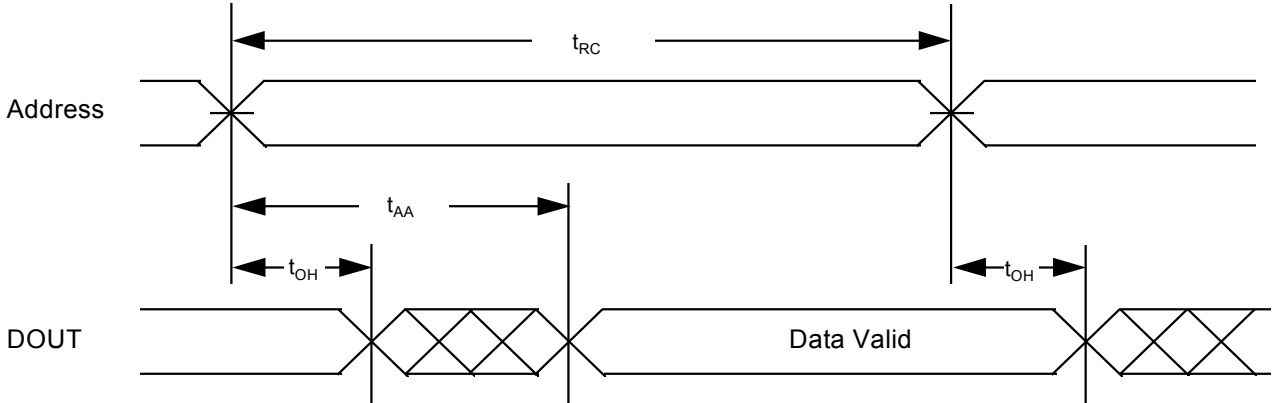
PARAMETER	SYMBOL	UT62L25616-55		UT62L25616-70		UT62L25616-100		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Write Cycle Time	t <sub>WC</sub>	55	-	70	-	100	-	ns
Address Valid to End of Write	t <sub>AW</sub>	50	-	60	-	80	-	ns
Chip Enable to End of Write	t <sub>CW</sub>	50	-	60	-	80	-	ns
Address Set-up Time	t <sub>AS</sub>	0	-	0	-	0	-	ns
Write Pulse Width	t <sub>WP</sub>	45	-	55	-	70	-	ns
Write Recovery Time	t <sub>WR</sub>	0	-	0	-	0	-	ns
Data to Write Time Overlap	t <sub>DW</sub>	25	-	30	-	40	-	ns
Data Hold from End of Write Time	t <sub>DH</sub>	0	-	0	-	0	-	ns
Output Active from End of Write	t <sub>OW*</sub>	5	-	5	-	5	-	ns
Write to Output in High Z	t <sub>WHZ*</sub>	-	30	-	30	-	40	ns
$\overline{LB}, \overline{UB}$ Valid to End of Write	t <sub>BW</sub>	45	-	60	-	80	-	ns

\*These parameters are guaranteed by device characterization, but not production tested.

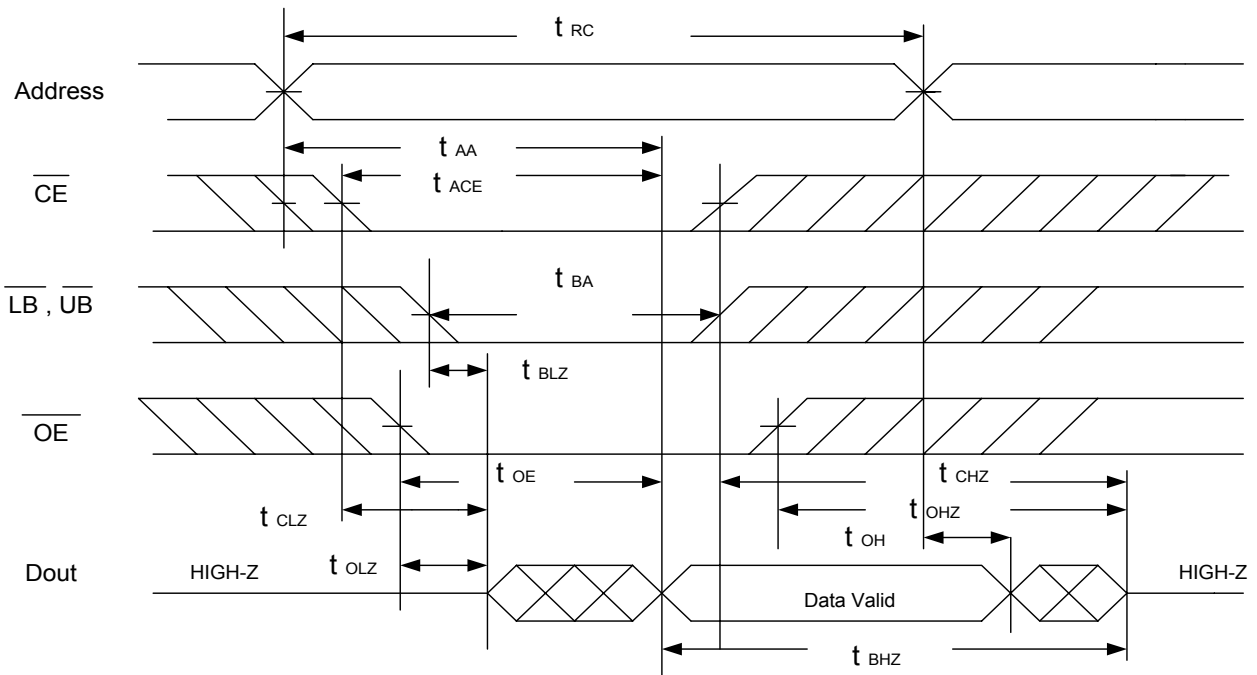


TIMING WAVEFORMS

READ CYCLE 1 (Address Controlled) (1,2,4)



READ CYCLE 2 ( $\overline{CE}$  and  $\overline{OE}$  Controlled) (1,3,5,6)

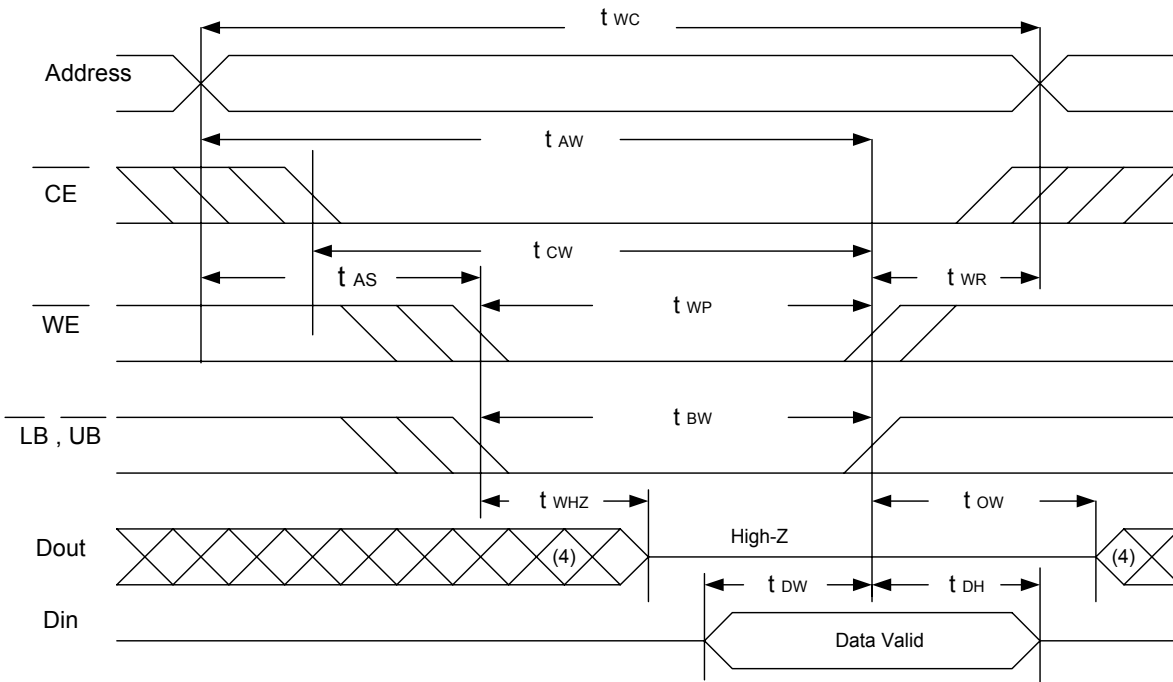


Notes :

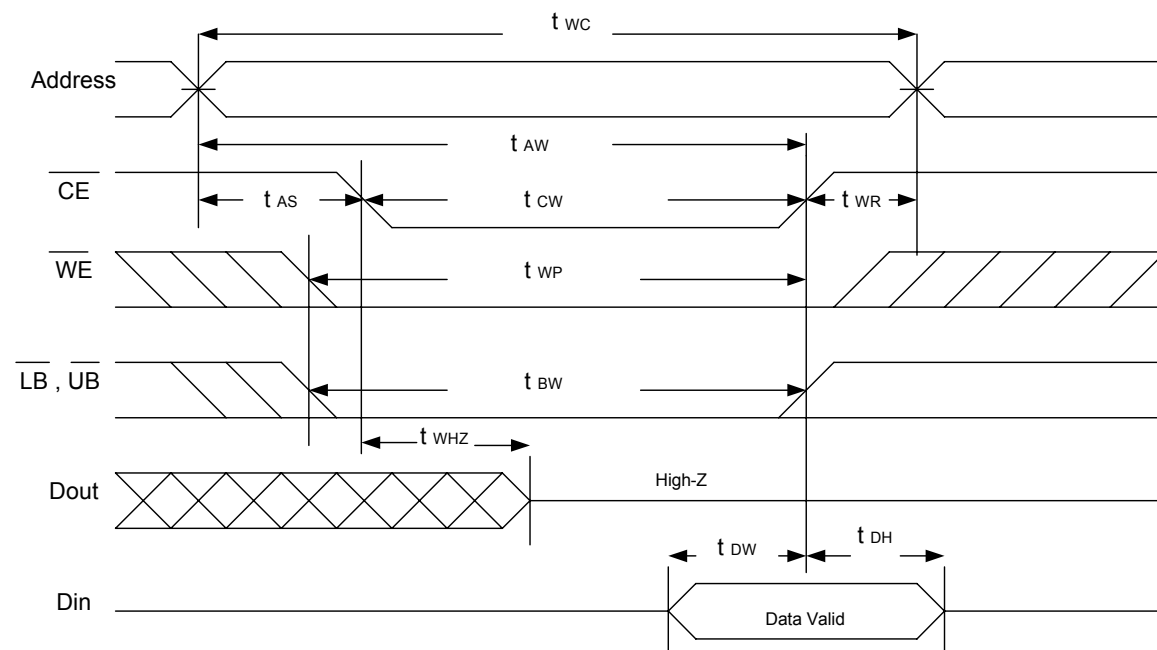
1.  $\overline{WE}$  is HIGH for read cycle.
2. Device is continuously selected  $\overline{CE} = V_{IL}$ .
3. Address must be valid prior to or coincident with  $\overline{CE}$  transition; otherwise  $t_{AA}$  is the limiting parameter.
4.  $\overline{OE}$  is LOW.
5.  $t_{CLZ}$ ,  $t_{OLZ}$ ,  $t_{CHZ}$  and  $t_{OHZ}$  are specified with  $C_L = 5pF$ . Transition is measured  $\pm 500mV$  from steady state.
6. At any given temperature and voltage condition,  $t_{CHZ}$  is less than  $t_{CLZ}$ ,  $t_{OHZ}$  is less than  $t_{OLZ}$ .



WRITE CYCLE 1 ( $\overline{WE}$  Controlled) (1,2,3,5)



WRITE CYCLE 2 ( $\overline{CE}$  Controlled) (1,2,5)



Notes :

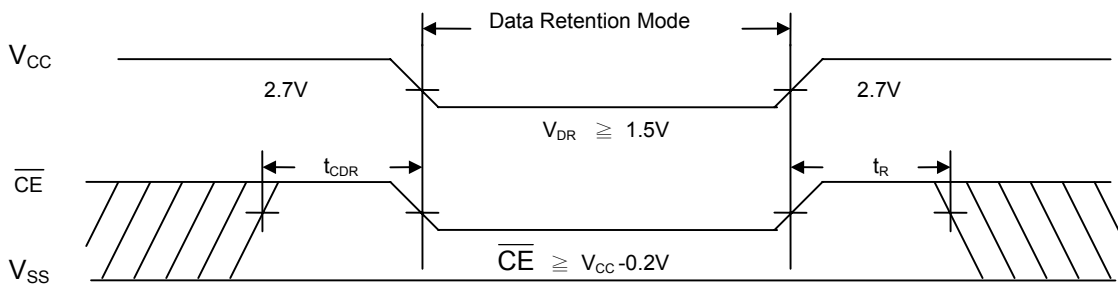
1.  $\overline{WE}$  or  $\overline{CE}$  must be HIGH during all address transitions.
2. A write occurs during the overlap of a low  $\overline{CE}$  and a low  $\overline{WE}$ .
3. During a  $\overline{WE}$  controlled with write cycle with  $\overline{OE}$  LOW,  $t_{wp}$  must be greater than  $t_{whz}+t_{dw}$  to allow the drivers to turn off and data to be placed on the bus.
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the  $\overline{CE}$  LOW transition occurs simultaneously with or after  $\overline{WE}$  LOW transition, the outputs remain in a high impedance state.
6.  $t_{ow}$  and  $t_{whz}$  are specified with  $C_L = 5pF$ . Transition is measured  $\pm 500mV$  from steady state.



DATA RETENTION CHARACTERISTICS (TA = 0°C to 70°C / -20°C to 80°C(E))

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
V <sub>CC</sub> for Data Retention	V <sub>DR</sub>	$\overline{CE} \geq V_{CC}-0.2V$	1.5	-	3.6	V
Data Retention Current	I <sub>DR</sub>	V <sub>CC</sub> =1.5V	- L	1	50	μA
		$\overline{CE} \geq V_{CC}-0.2V$	- LL	0.5	20	μA
Chip Disable to Data Retention Time	t <sub>CDR</sub>	See Data Retention Waveforms (below)	0	-	-	ms
Recovery Time	t <sub>R</sub>		5	-	-	ms

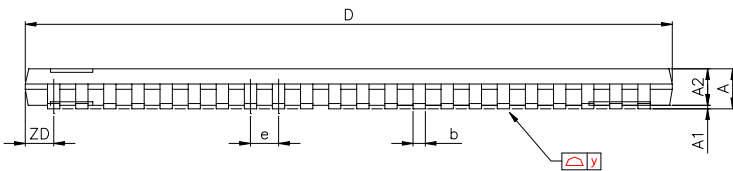
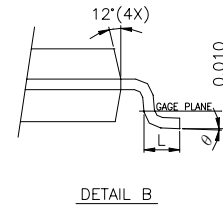
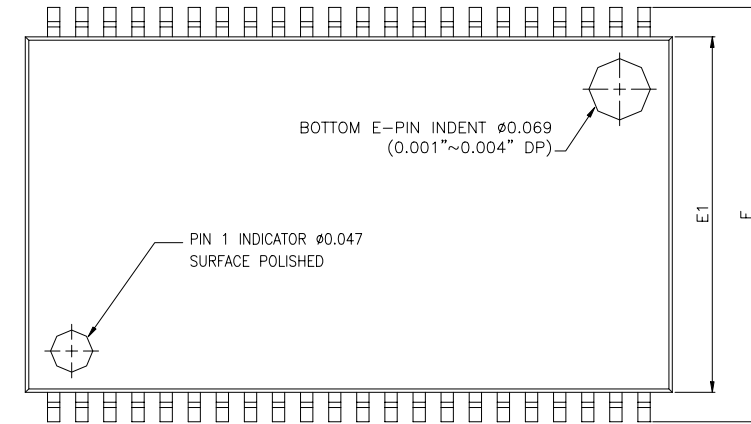
DATA RETENTION WAVEFORM





PACKAGE OUTLINE DIMENSION

44pin 400mil TSOP-II Package Outline Dimension



SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHS		
	MIN	NOM	MAX.	MIN.	NOM.	MAX.
A	1.00	-	1.20	0.039	-	0.047
A1	0.05	-	0.15	0.002	-	0.006
A2	0.95	1.00	1.05	0.037	0.039	0.041
b	0.30	0.35	0.45	0.012	0.014	0.018
c	0.12	-	0.21	0.0047	-	0.083
D	18.313	18.415	18.517	0.721	0.725	0.728
E	11.854	11.836	11.838	0.460	0.466	0.470
E1	10.058	10.180	10.282	0.398	0.400	0.404
e	-	0.800	-	-	0.0315	-
L	0.40	0.50	0.60	0.0157	0.020	0.0236
2D	-	0.805	-	-	0.0317	-
y	0.00	-	0.076	0.000	-	0.003
$\theta$	0°	-	5°	0°	-	5°





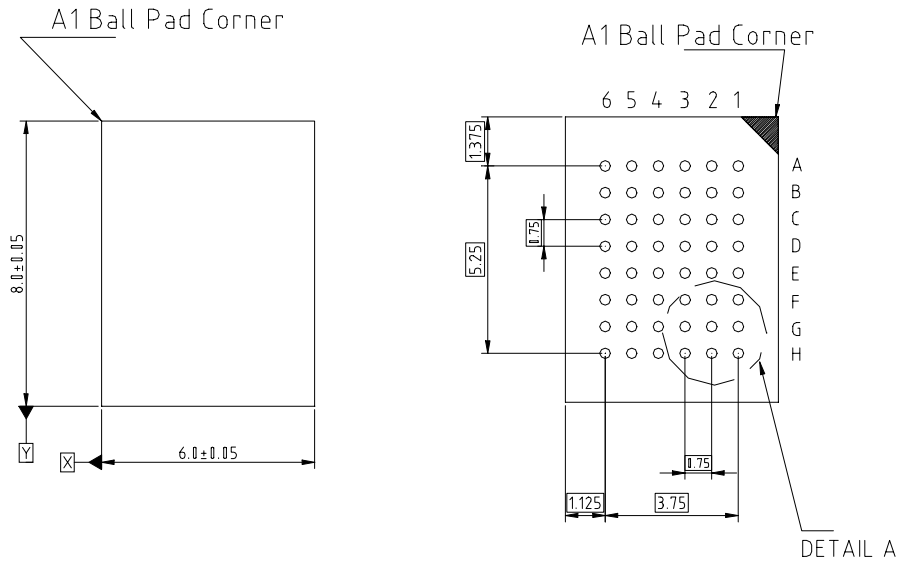
Rev. 1.1

UTRON

UT62L25616

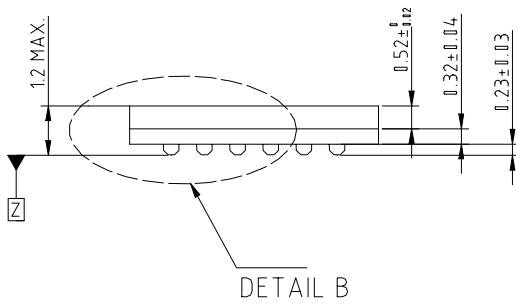
256K X 16 BIT LOW POWER CMOS SRAM

**48-pin 6mm×8mm TFBGA Outline Dimension**

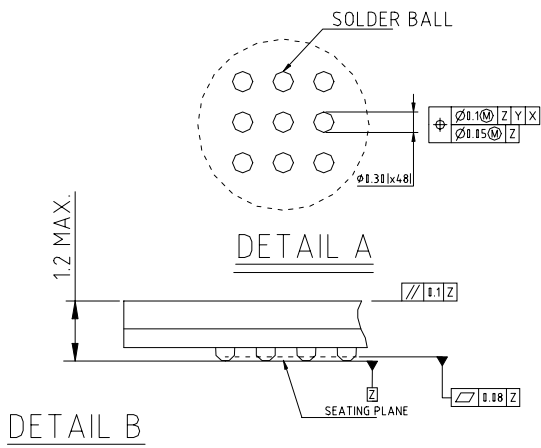


TOP VIEW | DIE VIEW |

BOTTOM VIEW | BALL SIDE |



SIDE VIEW



DETAIL B



**ORDERING INFORMATION**

**COMMERCIAL TEMPERATURE**

PART NO.	ACCESS TIME (ns)	STANDBY CURRENT (μA) TYP.	PACKAGE
UT62L25616MC-55L	55	20	44 PIN TSOP- II
UT62L25616MC-55LL	55	3	44 PIN TSOP- II
UT62L25616MC-70L	70	20	44 PIN TSOP- II
UT62L25616MC-70LL	70	3	44 PIN TSOP- II
UT62L25616BS-55L	55	20	48 PIN TFBGA
UT62L25616BS-55LL	55	3	48 PIN TFBGA
UT62L25616BS-70L	70	20	48 PIN TFBGA
UT62L25616BS-70LL	70	3	48 PIN TFBGA

**EXTENDED TEMPERATURE**

PART NO.	ACCESS TIME (ns)	STANDBY CURRENT (μA) TYP.	PACKAGE
UT62L25616MC-55LE	55	20	44 PIN TSOP- II
UT62L25616MC-55LLE	55	3	44 PIN TSOP- II
UT62L25616MC-70LE	70	20	44 PIN TSOP- II
UT62L25616MC-70LLE	70	3	44 PIN TSOP- II
UT62L25616BS-55LE	55	20	48 PIN TFBGA
UT62L25616BS-55LLE	55	3	48 PIN TFBGA
UT62L25616BS-70LE	70	20	48 PIN TFBGA
UT62L25616BS-70LLE	70	3	48 PIN TFBGA



**REVISION HISTORY**

REVISION	DESCRIPTION	DATE
Preliminary Rev. 0.5	Original.	Mar, 2001
Rev. 1.0	1. The symbols CE# and OE# and WE# are revised as $\overline{CE}$ and $\overline{OE}$ and $\overline{WE}$ . 2. Separate Industrial and Consumer SPEC. 3. Add access time 55ns range. 4. The power supply is revised: 3.3V⇒3.6V	Jul 4,2001
Rev. 1.1	1. Revised PIN CONFIGURATION : Rev 1.0 : No A17 pin→typing error Rev 1.1 : add A17 pin.	Oct 18,2001



Rev. 1.1

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UT62L25616

256K X 16 BIT LOW POWER CMOS SRAM

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