



FEATURES

- Access time : 55/70ns (max.)
- Low power consumption :
 Operating : 30/20 mA (typical)
 Standby : 10µA (max) L-version $T_A = 50^\circ\text{C}$
 3µA (max) LL-version $T_A = 50^\circ\text{C}$
- Power supply range : 2.5V ~ 3.6V
- All inputs and outputs TTL compatible
- Fully static operation
- Data retention voltage : 2V (min.)
- Operation Temperature
 Industrial : $-40^\circ\text{C} \sim +85^\circ\text{C}$
- Package : 32-pin 450mil SOP
 32-pin 8x20mm TSOP-1
 32-pin 8x13.4mm STSOP
 36-pin 6x8mm TFBGA

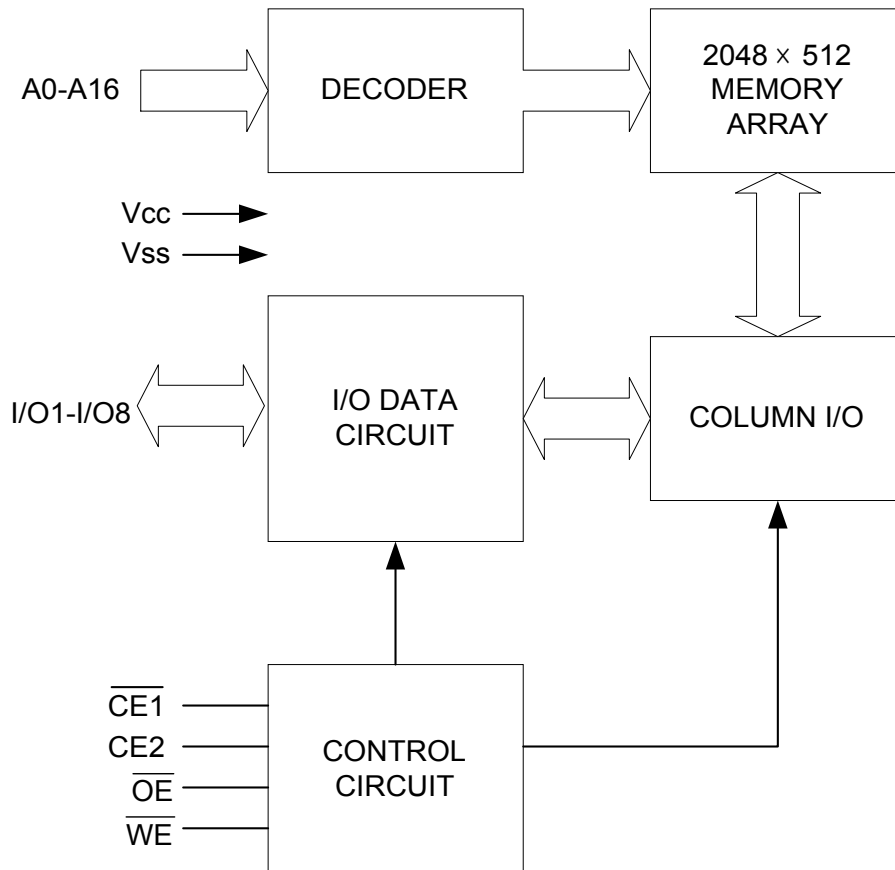
GENERAL DESCRIPTION

The UT62L1024 is a 1,048,576-bit low power CMOS static random access memory organized as 131,072 words by 8 bits. It is fabricated using high performance, high reliability CMOS technology.

Easy memory expansion is provided by using two chip enable input ($\overline{\text{CE1}}$,CE2) and supports industrial operating temperature range.

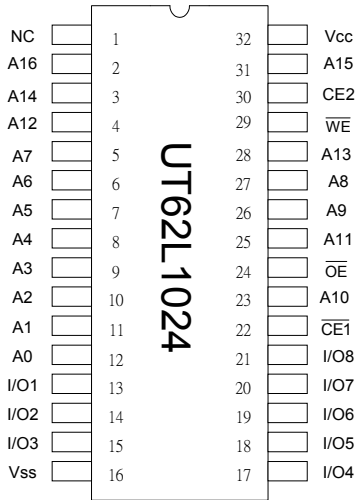
The UT62L1024 operates from a wide range 2.5V~3.6V power supply and all inputs and outputs are fully TTL compatible.

FUNCTIONAL BLOCK DIAGRAM

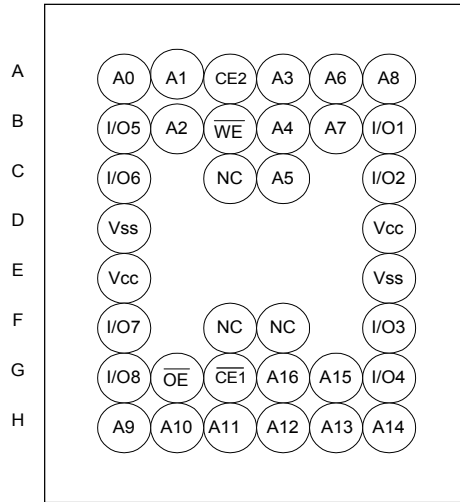




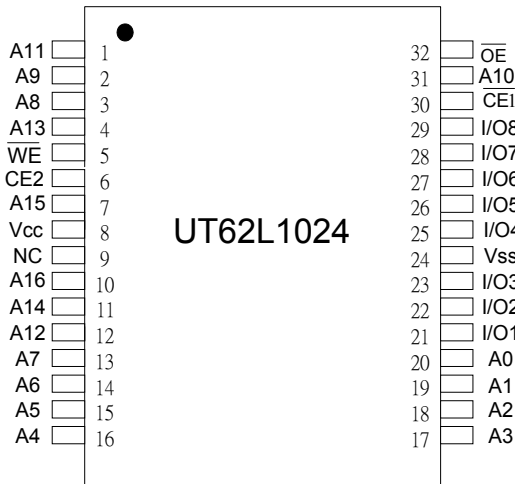
PIN CONFIGURATION



SOP



TFBGA



TSOP-1/STSOP

PIN DESCRIPTION

SYMBOL	DESCRIPTION
A0 - A16	Address Inputs
I/O1 - I/O8	Data Inputs/Outputs
CE1, CE2	Chip enable 1,2 Inputs
WE	Write Enable Input
OE	Output Enable Input
V _{CC}	Power Supply
V _{SS}	Ground
NC	No Connection



ABSOLUTE MAXIMUM RATINGS*

PARAMETER	SYMBOL	RATING	UNIT
Terminal Voltage with Respect to Vss	V_{TERM}	-0.5 to $V_{CC}+0.5$	V
Operating Temperature Industrial	T_A	-40 to +85	°C
Storage Temperature	T_{STG}	-65 to +150	°C
Power Dissipation	P_D	1	W
DC Output Current	I_{OUT}	50	mA
Soldering Temperature (under 10 sec)	T_{solder}	260	°C

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect device reliability.

TRUTH TABLE

MODE	$\overline{CE1}$	CE2	\overline{OE}	\overline{WE}	I/O OPERATION	SUPPLY CURRENT
Standby	H	X	X	X	High - Z	I_{SB}, I_{SB1}
Standby	X	L	X	X	High - Z	I_{SB}, I_{SB1}
Output Disable	L	H	H	H	High - Z	I_{CC}, I_{CC1}
Read	L	H	L	H	D_{OUT}	I_{CC}, I_{CC1}
Write	L	H	X	L	D_{IN}	I_{CC}, I_{CC1}

Note: H = V_{IH} , L = V_{IL} , X = Don't care.

**DC ELECTRICAL CHARACTERISTICS** ($V_{CC} = 2.5V \sim 3.6V$, $T_A = -40^{\circ}C \sim +85^{\circ}C$)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT		
Input High Voltage	V_{IH}		2.0	-	$V_{CC}+0.5$	V		
Input Low Voltage	V_{IL}		-0.5	-	0.6	V		
Input Leakage Current	I_{IL}	$V_{SS} \leq V_{IN} \leq V_{CC}$	-1	-	1	μA		
Output Leakage Current	I_{OL}	$V_{SS} \leq V_{IO} \leq V_{CC}$ $\overline{CE1} = V_{IH}$ or $CE2 = V_{IL}$ or $\overline{OE} = V_{IH}$ or $\overline{WE} = V_{IL}$	-1	-	1	μA		
Output High Voltage	V_{OH}	$I_{OH} = -1mA$	2.0	-	-	V		
Output Low Voltage	V_{OL}	$I_{OL} = 2.1mA$	-	-	0.4	V		
Average Operating Power Supply Current	I_{CC}	Cycle time = Min., 100% Duty, $\overline{CE1} = V_{IL}$, $CE2 = V_{IH}$, $I_{IO} = 0mA$	55	-	30	40	mA	
			70	-	20	30	mA	
	I_{CC1}	Cycle time = $1\mu s$, 100% Duty, $\overline{CE1} \leq 0.2V$, $CE2 \geq V_{CC}-0.2V$, $I_{IO} = 0mA$	-	-	5	mA		
Standby Power Supply Current	I_{SB}	$\overline{CE1} = V_{IH}$ or $CE2 = V_{IL}$	-	-	1.0	mA		
	I_{SB1}	$\overline{CE1} \geq V_{CC}-0.2V$ or $CE2 \leq 0.2V$	-L	$T_A = -40^{\circ}C \sim +85^{\circ}C$	-	-	50	μA
			-	$T_A = +50^{\circ}C$	-	-	10	μA
			-	$T_A = -40^{\circ}C \sim +85^{\circ}C$	-	-	10	μA
		LL	$T_A = +50^{\circ}C$	-	-	3	μA	

CAPACITANCE ($T_A = 25^{\circ}C$, $f = 1.0MHz$)

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
Input Capacitance	C_{IN}	-	6	pF
Input/Output Capacitance	$C_{I/O}$	-	8	pF

Note : These parameters are guaranteed by device characterization, but not production tested.

AC TEST CONDITIONS

Input Pulse Levels	0.4V to 2.2V
Input Rise and Fall Times	5ns
Input and Output Timing Reference Levels	1.5V
Output Load	$C_L = 30pF$, $I_{OH}/I_{OL} = -1mA/2.1mA$

**AC ELECTRICAL CHARACTERISTICS** ($V_{CC} = 2.5V \sim 3.6V$, $T_A = -40^{\circ}C \sim +85^{\circ}C$)**(1) READ CYCLE**

PARAMETER	SYMBOL	UT62L1024-55		UT62L1024-70		UNIT
		MIN.	MAX.	MIN.	MAX.	
Read Cycle Time	t_{RC}	55	-	70	-	ns
Address Access Time	t_{AA}	-	55	-	70	ns
Chip Enable Access Time	t_{ACE1}, t_{ACE2}	-	55	-	70	ns
Output Enable Access Time	t_{OE}	-	30	-	35	ns
Chip Enable to Output in Low-Z	t_{CLZ1}^*, t_{CLZ2}^*	10	-	10	-	ns
Output Enable to Output in Low-Z	t_{OLZ}^*	5	-	5	-	ns
Chip Disable to Output in High-Z	t_{CHZ1}^*, t_{CHZ2}^*	-	30	-	35	ns
Output Disable to Output in High-Z	t_{OHZ}^*	-	30	-	35	ns
Output Hold from Address Change	t_{OH}	5	-	5	-	ns

(2) WRITE CYCLE

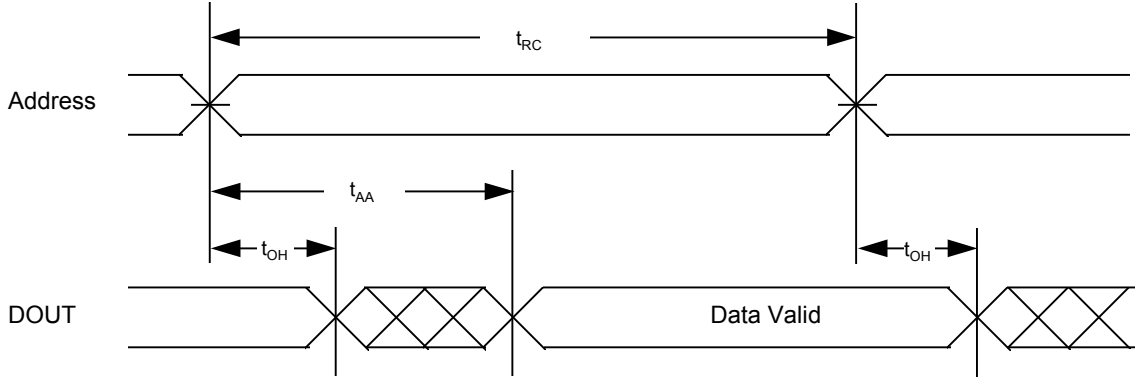
PARAMETER	SYMBOL	UT62L1024-55		UT62L1024-70		UNIT
		MIN.	MAX.	MIN.	MAX.	
Write Cycle Time	t_{WC}	55	-	70	-	ns
Address Valid to End of Write	t_{AW}	50	-	60	-	ns
Chip Enable to End of Write	t_{CW1}, t_{CW2}	50	-	60	-	ns
Address Set-up Time	t_{AS}	0	-	0	-	ns
Write Pulse Width	t_{WP}	40	-	45	-	ns
Write Recovery Time	t_{WR}	0	-	0	-	ns
Data to Write Time Overlap	t_{DW}	25	-	30	-	ns
Data Hold from End of Write-Time	t_{DH}	0	-	0	-	ns
Output Active from End of Write	t_{OW}^*	5	-	5	-	ns
Write to Output in High-Z	t_{WHZ}^*	-	20	-	25	ns

*These parameters are guaranteed by device characterization, but not production tested.

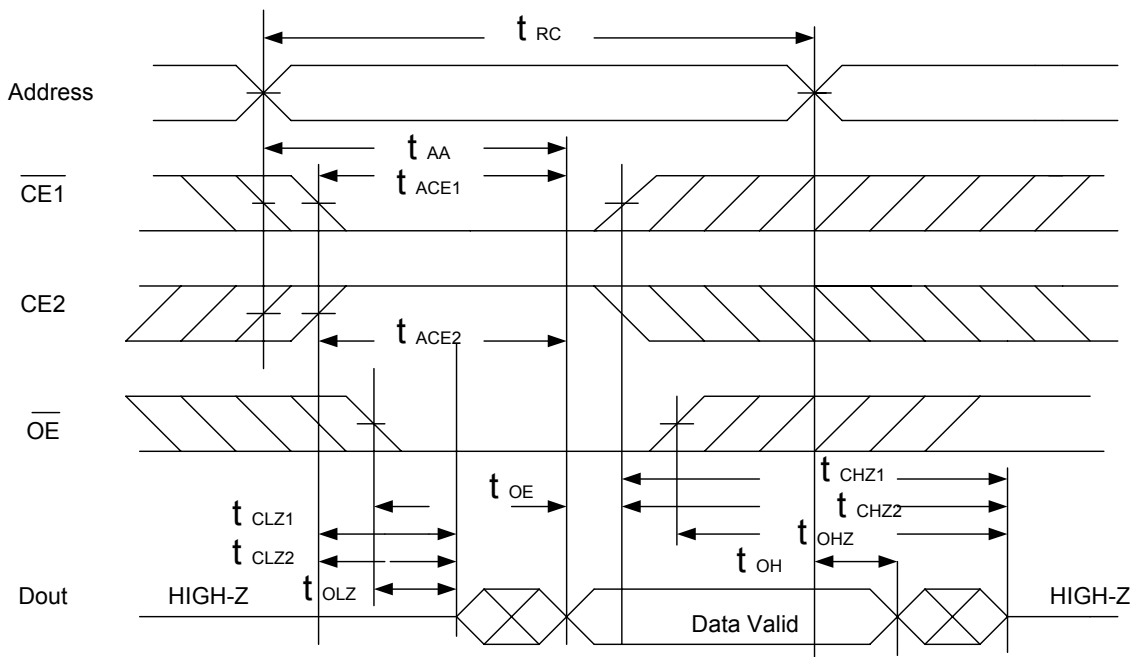


TIMING WAVEFORMS

READ CYCLE 1 (Address Controlled) (1,2,4)



READ CYCLE 2 ($\overline{CE1}$, CE2 and \overline{OE} Controlled) (1,3,5,6)

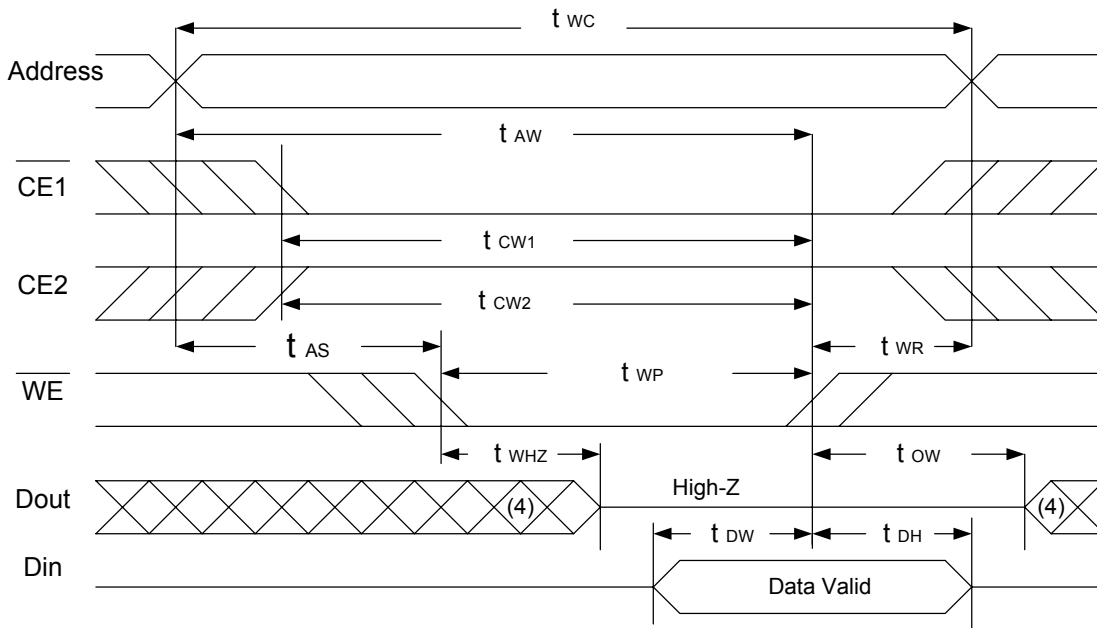


Notes :

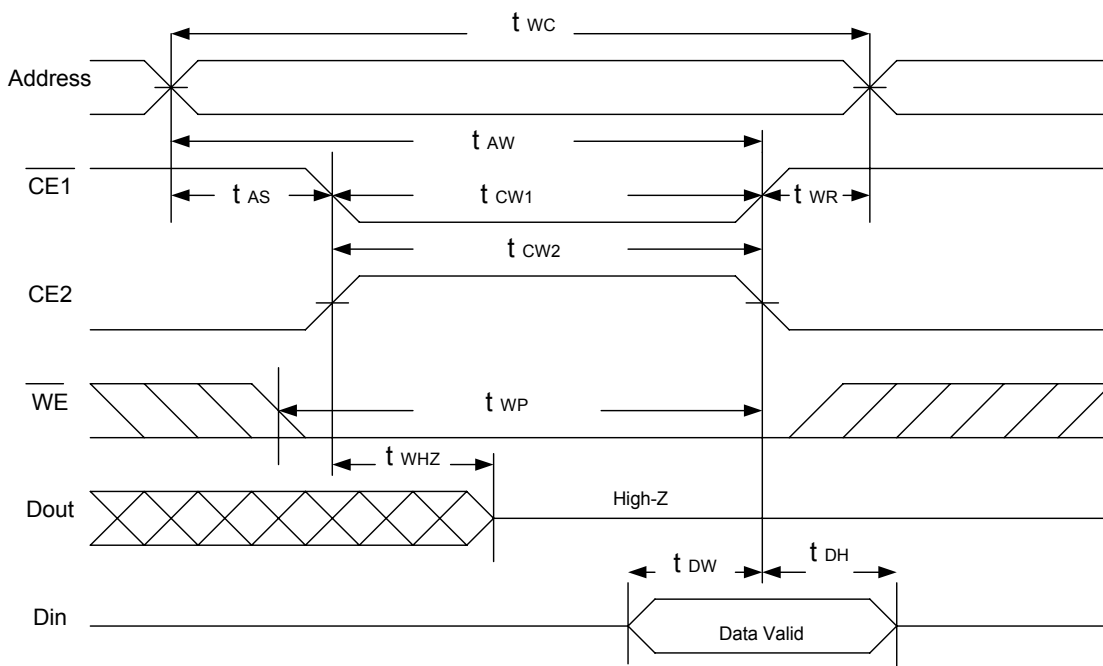
1. \overline{WE} is HIGH for a read cycle.
2. Device is continuously selected \overline{OE} , $\overline{CE1}=V_{IL}$ and $CE2=V_{IH}$.
3. Address must be valid prior to or coincident with $\overline{CE1}$ LOW and CE2 high transition; otherwise t_{AA} is the limiting parameter.
4. \overline{OE} is low.
5. t_{CLZ1} , t_{CLZ2} , t_{OLZ} , t_{CHZ1} , t_{CHZ2} and t_{OHZ} are specified with $C_L=5pF$. Transition is measured $\pm 500mV$ from steady state.
6. At any given temperature and voltage condition, t_{CHZ1} is less than t_{CLZ1} , t_{CHZ2} is less than t_{CLZ2} , t_{OHZ} is less than t_{OLZ} .



WRITE CYCLE 1 (\overline{WE} Controlled) (1,2,3,5)



WRITE CYCLE 2 ($\overline{CE1}$ and CE2 Controlled) (1,2,5)



Notes :

1. \overline{WE} or $\overline{CE1}$ must be HIGH or CE2 must be LOW during all address transitions.
2. A write occurs during the overlap of a low $\overline{CE1}$, a high CE2 and a low \overline{WE} .
3. During a \overline{WE} controlled with write cycle with \overline{OE} LOW, t_{wp} must be greater than $t_{whz}+t_{dw}$ to allow the I/O drivers to turn off and data to be placed on the bus.
4. During this period, I/O pins are in the output state, and input signals must not be applied.
4. If the $\overline{CE1}$ LOW transition occurs simultaneously with or after \overline{WE} LOW transition, the outputs remain in a high Impedance state.
6. t_{ow} and t_{whz} are specified with $C_L=5pF$. Transition is measured $\pm 500mV$ from steady state.



DATA RETENTION CHARACTERISTICS ($T_A = -40^{\circ}\text{C} \sim +85^{\circ}\text{C}$)

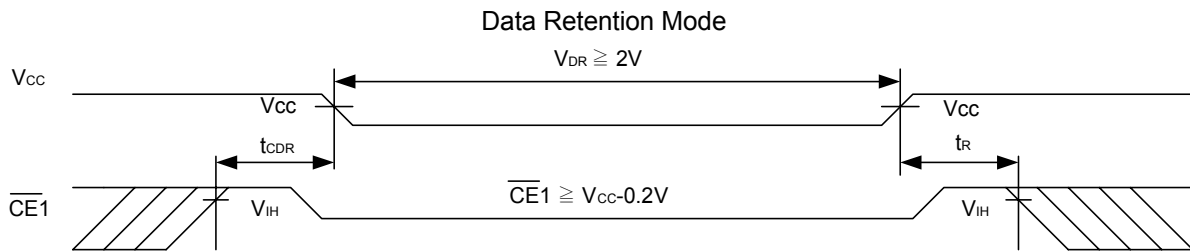
PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT	
Vcc for Data Retention	V_{DR}	$\overline{CE1} \geq V_{CC}-0.2\text{V}$ or $CE2 \leq 0.2\text{V}$	2.0	-	3.3	V	
Data Retention Current	I_{DR}	$V_{CC}=2\text{V}$ $\overline{CE1} \geq V_{CC}-0.2\text{V}$ or $CE2 \leq 0.2\text{V}$	- L	-	5	50 10*	μA
			- LL	-	1.5	15 2*	μA
Chip Disable to Data Retention Time	t_{CDR}	See Data Retention Waveforms (below)	0	-	-	ns	
Recovery Time	t_R		t_{RC}^*	-	-	ns	

t_{RC}^* = Read Cycle Time

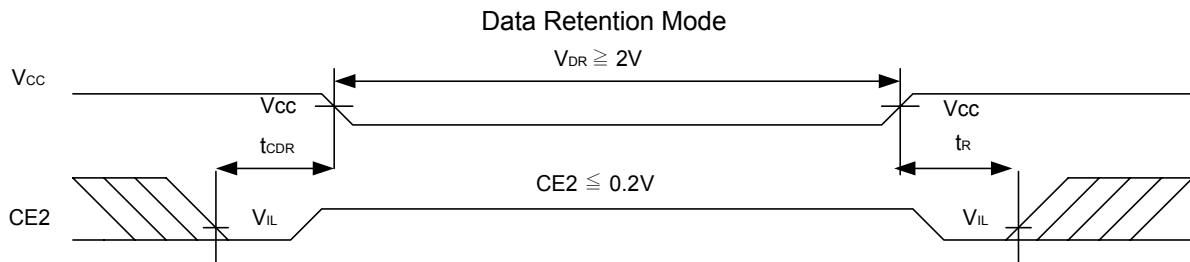
*Those parameters are for reference only under 50°C

DATA RETENTION WAVEFORM

Low Vcc Data Retention Waveform (1) ($\overline{CE1}$ controlled)



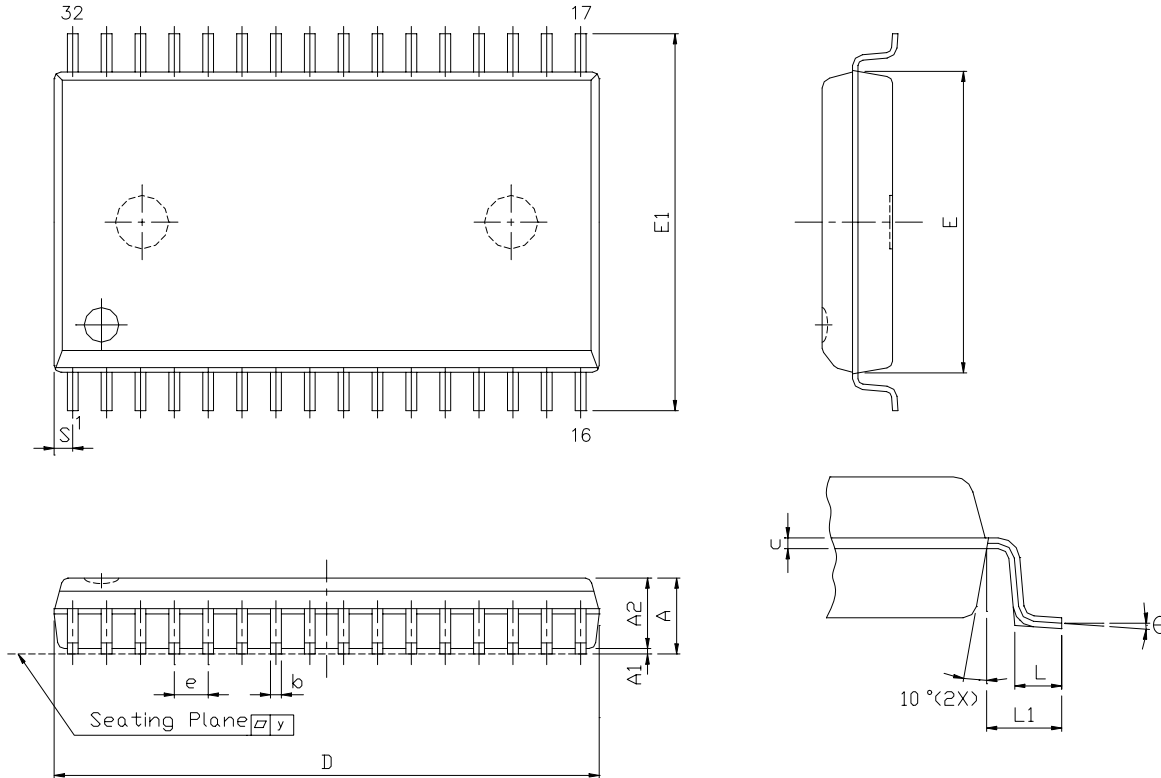
Low Vcc Data Retention Waveform (2) (CE2 controlled)





PACKAGE OUTLINE DIMENSION

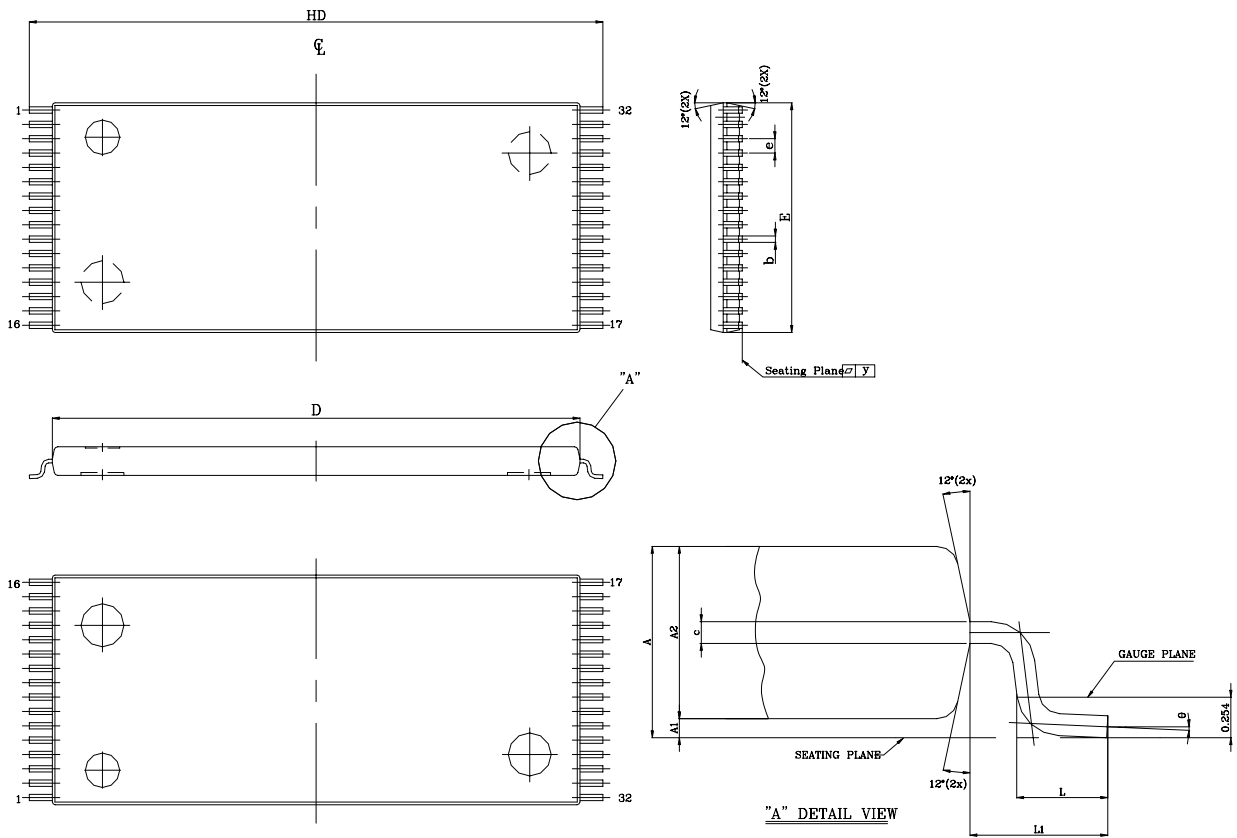
32 pin 450mil SOP Package Outline Dimension



SYMBOL \ UNIT	INCH(REF)	MM(BASE)
A	0.118 (MAX)	2.997 (MAX)
A1	0.004(MIN)	0.102(MIN)
A2	0.111(MAX)	2.82(MAX)
b	0.016(TYP)	0.406(TYP)
c	0.008(TYP)	0.203(TYP)
D	0.817(MAX)	20.75(MAX)
E	0.445 ± 0.005	11.303 ± 0.127
E1	0.555 ± 0.012	14.097 ± 0.305
e	0.050(TYP)	1.270(TYP)
L	0.0347 ± 0.008	0.881 ± 0.203
L1	0.055 ± 0.008	1.397 ± 0.203
S	0.026(MAX)	0.660 (MAX)
y	0.004(MAX)	0.101(MAX)
Θ	$0^\circ - 10^\circ$	$0^\circ - 10^\circ$



32 pin TSOP-I Package Outline Dimension

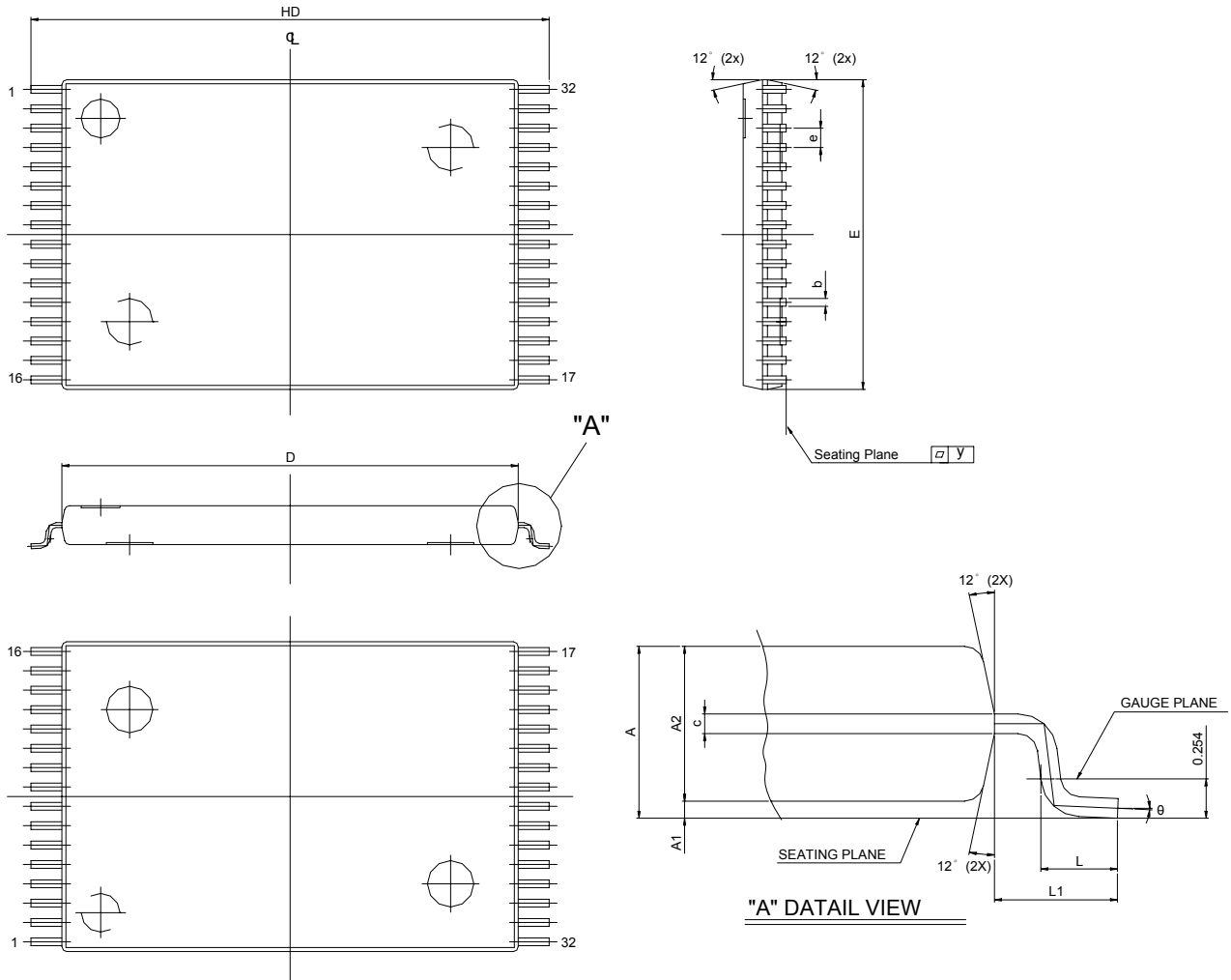


SYMBOL \ UNIT	INCH(BASE)	MM(REF)
A	0.047 (MAX)	1.20 (MAX)
A1	0.004 ± 0.002	0.10 ± 0.05
A2	0.039 ± 0.002	1.00 ± 0.05
b	0.008 + 0.002 - 0.001	0.20 + 0.05 - 0.03
c	0.005 (TYP)	0.127 (TYP)
D	0.724 ± 0.004	18.40 ± 0.10
E	0.315 ± 0.004	8.00 ± 0.10
e	0.020 (TYP)	0.50 (TYP)
HD	0.787 ± 0.008	20.00 ± 0.20
L	0.0197 ± 0.004	0.50 ± 0.10
L1	0.0315 ± 0.004	0.8 ± 0.10
y	0.003 (MAX)	0.076 (MAX)
θ	0° ~ 5°	0° ~ 5°





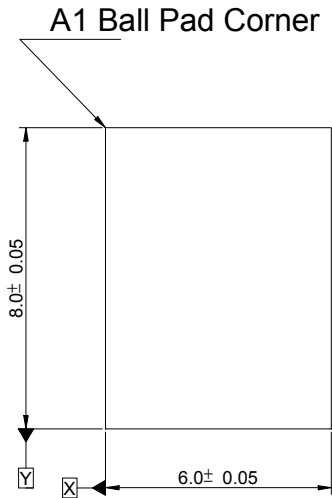
32 pin 8mm x 13.4mm STSOP Package Outline Dimension



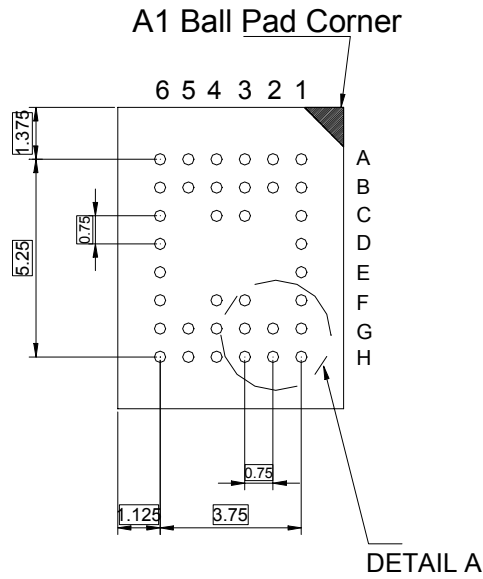
SYMBOL \ UNIT	INCH(BASE)	MM(REF)
A	0.049 (MAX)	1.25 (MAX)
A1	0.005 ± 0.002	0.130 ± 0.05
A2	0.039 ± 0.002	1.00 ± 0.05
b	0.008 ± 0.001	0.200 ± 0.025
c	0.005 (TYP)	0.127 (TYP)
D	0.465 ± 0.004	11.80 ± 0.10
E	0.315 ± 0.004	8.00 ± 0.10
e	0.020 (TYP)	0.50 (TYP)
HD	0.528 ± 0.008	13.40 ± 0.20.
L	0.0197 ± 0.004	0.50 ± 0.10
L1	0.0315 ± 0.004	0.8 ± 0.10
y	0.003 (MAX)	0.076 (MAX)
θ	0°~5°	0°~5°



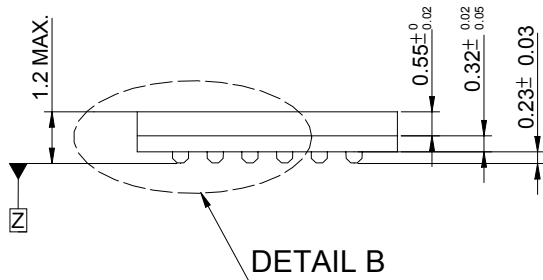
36 pin 6mmx8mm TFBGA Package Outline Dimension



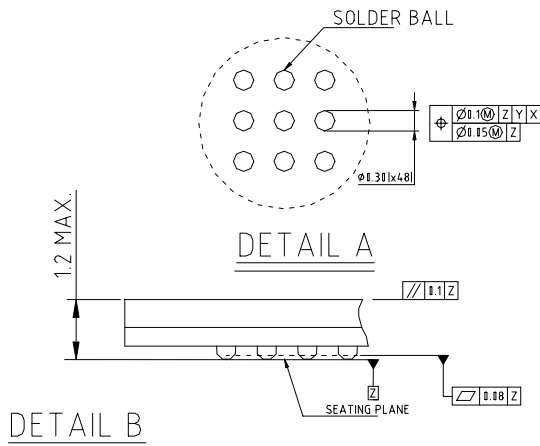
TOP VIEW (DIE VIEW)



BOTTOM VIEW (BALL SIDE)



SIDE VIEW





UTRON

Preliminary Rev. 0.1

UT62L1024(I)

128K X 8 BIT LOW POWER CMOS SRAM

ORDERING INFORMATION

PART NO.	ACCESS TIME (ns)	PACKAGE
UT62L1024SC-55LI	55	32 PIN SOP
UT62L1024SC-55LLI	55	32 PIN SOP
UT62L1024SC-70LI	70	32 PIN SOP
UT62L1024SC-70LLI	70	32 PIN SOP
UT62L1024LC-55LI	55	32 PIN TSOP-I
UT62L1024LC-55LLI	55	32 PIN TSOP-I
UT62L1024LC-70LI	70	32 PIN TSOP-I
UT62L1024LC-70LLI	70	32 PIN TSOP-I
UT62L1024LS-55LI	55	32 PIN STSOP
UT62L1024LS-55LLI	55	32 PIN STSOP
UT62L1024LS-70LI	70	32 PIN STSOP
UT62L1024LS-70LLI	70	32 PIN STSOP
UT62L1024BS-55LI	55	36 PIN TFBGA
UT62L1024BS-55LLI	55	36 PIN TFBGA
UT62L1024BS-70LI	70	36 PIN TFBGA
UT62L1024BS-70LLI	70	36 PIN TFBGA



UTRON

Preliminary Rev. 0.1

UT62L1024(I)

128K X 8 BIT LOW POWER CMOS SRAM

REVISION HISTORY

REVISION	DESCRIPTION	DATE
Preliminary Rev. 0.1	Original.	Nov 15,. 2001