UTRON

UT62L1024(E)

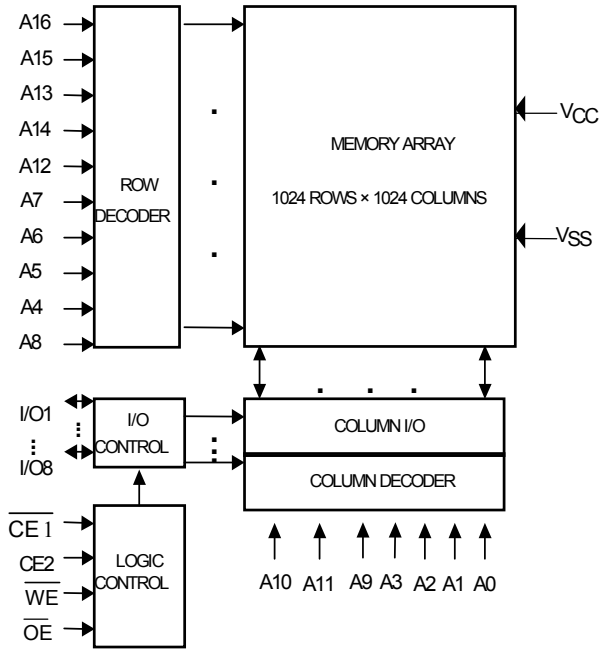
Rev. 1.1

128K X 8 BIT LOW POWER CMOS SRAM

FEATURES

- Access time : 35/55/70ns (max.)
- Low power consumption :
  Operating : 40/35/30 mA (typical)
  Standby : 1.0μA (typical) L-version
  0.5μA (typical) LL-version
- Power supply range : 2.7V to 3.6V
- All inputs and outputs TTL compatible
- Fully static operation
- Three state outputs
- Data retention voltage : 2V (min.)
- Extended Temperature : -20℃~80℃
- Package : 32-pin 600 mil PDIP
  32-pin 450 mil SOP
  32-pin 8x20mm TSOP-1
  32-pin 8x13.4mm STSOP

FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTION

SYMBOL	DESCRIPTION
A0 - A16	Address Inputs
I/O1 - I/O8	Data Inputs/Outputs
$\overline{CE1}$,CE2	Chip enable 1,2 Inputs
$\overline{WE}$	Write Enable Input
$\overline{OE}$	Output Enable Input
V_{CC}	Power Supply
V_{SS}	Ground
NC	No Connection

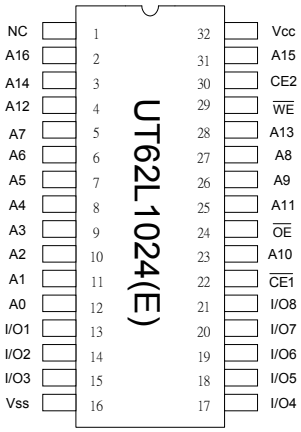
GENERAL DESCRIPTION

The UT62L1024(E) is a 1,048,576-bit low power CMOS static random access memory organized as 131,072 words by 8 bits. It is fabricated using high performance, high reliability CMOS technology.

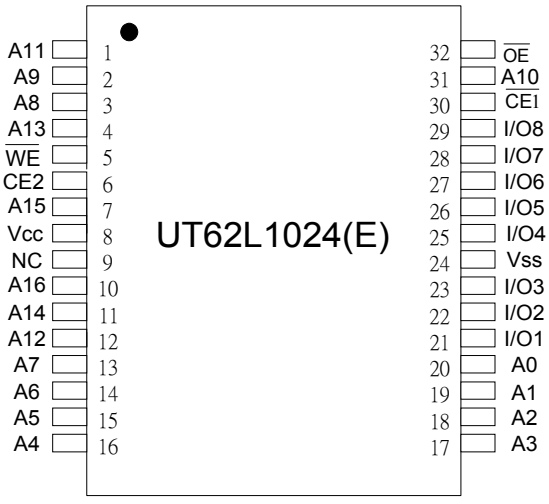
The UT62L1024(E) is designed for low power application. It is particularly well suited for battery back-up nonvolatile memory application.

The UT62L1024(E) operates from a single 2.7V ~ 3.6V power supply and all inputs and outputs are fully TTL compatible.

PIN CONFIGURATION



PDIP / SOP



TSOP-1/STSOP

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ABSOLUTE MAXIMUM RATINGS*

PARAMETER	SYMBOL	RATING	UNIT
Terminal Voltage with Respect to Vss	V_{TERM}	-0.5 to +4.6	V
Operating Temperature	T_A	-20 to 80	℃
Storage Temperature	T_{STG}	-65 to +150	℃
Power Dissipation	P_D	1	W
DC Output Current	I_{OUT}	50	mA
Soldering Temperature (under 10 sec)	T_{solder}	260	℃

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect device reliability.

TRUTH TABLE

MODE	$\overline{CE1}$	CE2	$\overline{OE}$	$\overline{WE}$	I/O OPERATION	SUPPLY CURRENT
Standby	H	X	X	X	High - Z	I_{SB},I_{SB1}
Standby	X	L	X	X	High -Z	I_{SB},I_{SB1}
Output Disable	L	H	H	H	High - Z	I_{CC}, I_{CC}1
Read	L	H	L	H	D_{OUT}	I_{CC}, I_{CC}1
Write	L	H	X	L	D_{IN}	I_{CC}, I_{CC}1,

Note: H = V_{IH}, L=V_{IL}, X = Don't care.

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 2.7V ~ 3.6V, T_A = -20℃~80℃)

PARAMETER	SYMBOL	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
Input High Voltage	V_{IH}			2.0	-	V_{CC}+0.5	V
Input Low Voltage	V_{IL}			- 0.5	-	0.6	V
Input Leakage Current	I_{IL}	$V_{SS} \leqq V_{IN} \leqq V_{CC}$		- 1	-	1	μA
Output Leakage Current	I_{OL}	$V_{SS} \leqq V_{I/O} \leqq V_{CC}$ $\overline{CE1}$ =V_{IH} or CE2 = V_{IL} or $\overline{OE}$ = V_{IH} or $\overline{WE}$ = V_{IL}		- 1	-	1	μA
Output High Voltage	V_{OH}	I_{OH} = - 1mA		2.0	-	-	V
Output Low Voltage	V_{OL}	I_{OL}= 4mA		-	-	0.4	V
Average Operating Power Supply Courrent	I_{CC}	Cycle time = Min.,100% Duty,	35	-	40	60	mA
		$\overline{CE1}$ =V_{IL}, CE2 = V_{IH},	55	-	35	50	mA
		$I_{I/O}$ = 0mA	70	-	30	40	mA
	I_{CC1}	Cycle time = 1μs, 100% Duty, $\overline{CE1} \leqq$0.2V,CE2$\geqq V_{CC}$-0.2V, $I_{I/O}$ = 0Ma		-	-	5	mA
Standby Power Supply Current	I_{SB}	$\overline{CE1}$ =V_{IH} or CE2 = V_{IL}		-	-	1.0	mA
	I_{SB1}	$\overline{CE1} \geqq V_{CC}$-0.2V or CE2$\leqq$0.2V	- L	-	1.0	100 20*	μA
			- LL	-	0.5	50 10*	μA

*Those parameters are for reference only under 50℃

CAPACITANCE (T_A=25℃, f=1.0MHz)

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
Input Capacitance	C_{IN}	-	6	pF
Input/Output Capacitance	$C_{I/O}$	-	8	pF

Note : These parameters are guaranteed by device characterization, but not production tested.

AC TEST CONDITIONS

Input Pulse Levels	0.4V to 2.4V
Input Rise and Fall Times	5ns
Input and Output Timing Reference Levels	1.5V
Output Load	C_L=50pF, I_{OH}/I_{OL}=-1mA/2mA

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 2.7V ~ 3.6V , T_A = -20℃~80℃)

(1) READ CYCLE

PARAMETER	SYMBOL	UT62L1024(E)-35		UT62L1024(E)-55		UT62L1024(E)-70		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Read Cycle Time	t_{RC}	35	-	55	-	70	-	ns
Address Access Time	t_{AA}	-	35	-	55	-	70	ns
Chip Enable Access Time	t_{ACE1}, t_{ACE2}	-	35	-	55	-	70	ns
Output Enable Access Time	t_{OE}	-	25	-	30	-	35	ns
Chip Enable to Output in Low-Z	t_{CLZ1}*, t_{CLZ2}*	10	-	10	-	10	-	ns
Output Enable to Output in Low-Z	t_{OLZ}*	5	-	5	-	5	-	ns
Chip Disable to Output in High-Z	t_{CHZ1}*, t_{CHZ2}*	-	25	-	30	-	35	ns
Output Disable to Output in High-Z	t_{OHZ}*	-	25	-	30	-	35	ns
Output Hold from Address Change	t_{OH}	5	-	5	-	5	-	ns

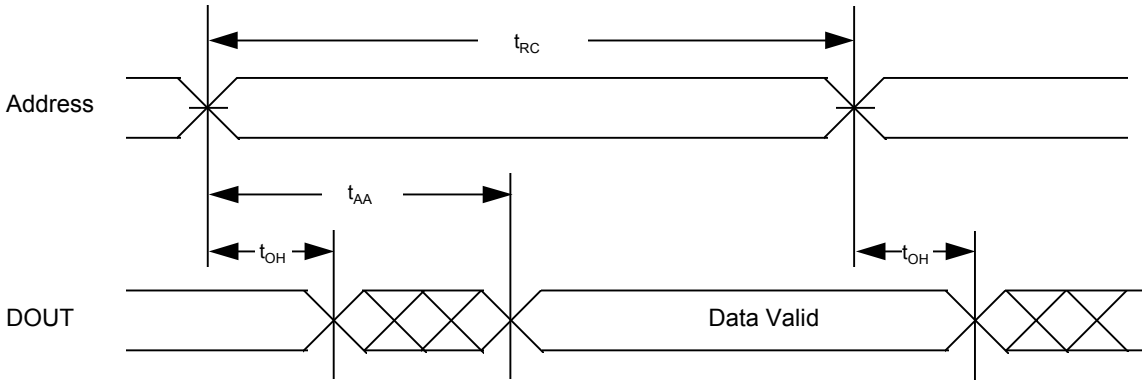
(2) WRITE CYCLE

PARAMETER	SYMBOL	UT62L1024(E)-35		UT62L1024(E)-55		UT62L1024(E)-70		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Write Cycle Time	t_{WC}	35	-	55	-	70	-	ns
Address Valid to End of Write	t_{AW}	30	-	50	-	60	-	ns
Chip Enable to End of Write	t_{CW1}, t_{CW2}	30	-	50	-	60	-	ns
Address Set-up Time	t_{AS}	0	-	0	-	0	-	ns
Write Pulse Width	t_{WP}	25	-	40	-	45	-	ns
Write Recovery Time	t_{WR}	0	-	0	-	0	-	ns
Data to Write Time Overlap	t_{DW}	20	-	25	-	30	-	ns
Data Hold from End of Write-Time	t_{DH}	0	-	0	-	0	-	ns
Output Active from End of Write	t_{OW}*	5	-	5	-	5	-	ns
Write to Output in High-Z	t_{WHZ}*	-	15	-	20	-	25	ns

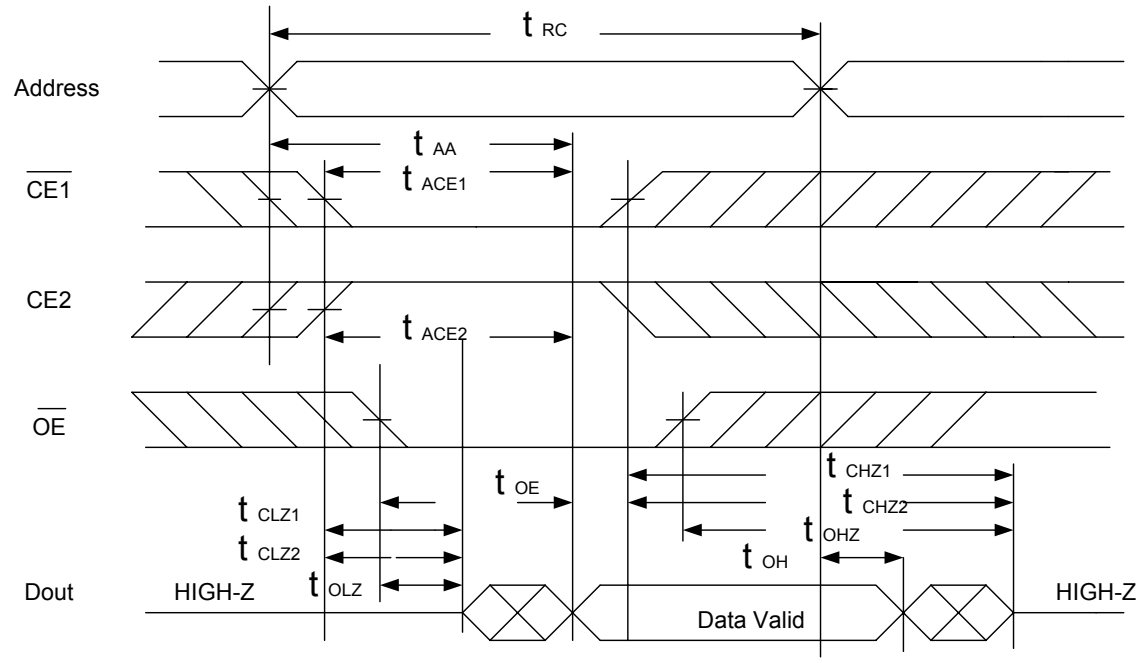
*These parameters are guaranteed by device characterization, but not production tested.

TIMING WAVEFORMS

READ CYCLE 1 (Address Controlled) (1,2,4)



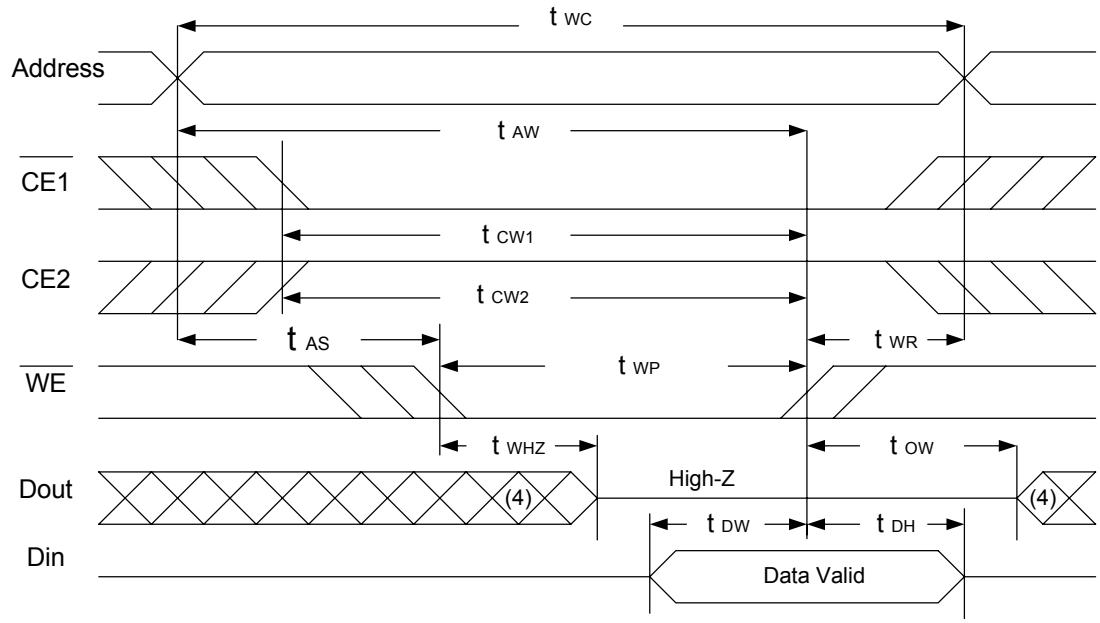
READ CYCLE 2 ($\overline{CE1}$, CE2 and $\overline{OE}$ Controlled) (1,3,5,6)



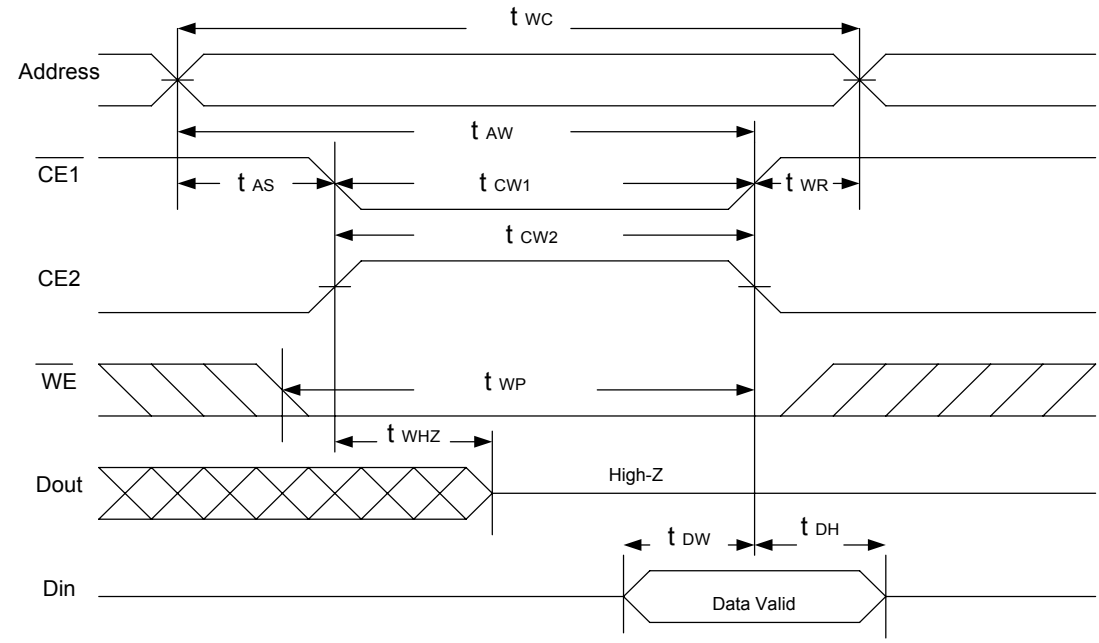
Notes :

1. $\overline{WE}$ is HIGH for a read cycle.
2. Device is continuously selected $\overline{OE}$, $\overline{CE1}$ =V_{IL} and CE2=V_{IH}.
3. Address must be valid prior to or coincident with $\overline{CE1}$ low and CE2 high transition; otherwise t_{AA} is the limiting parameter.
4. $\overline{OE}$ is low.
5. t_{CLZ1}, t_{CLZ2}, t_{OLZ}, t_{CHZ1}, t_{CHZ2} and t_{OHZ} are specified with C_L=5pF. Transition is measured ± 500mV from steady state.
6. At any given temperature and voltage condition, t_{CHZ1} is less than t_{CLZ1}, t_{CHZ2} is less than t_{CLZ2}, t_{OHZ} is less than t_{OLZ}.

WRITE CYCLE 1 ($\overline{WE}$ Controlled) (1,2,3,5)



WRITE CYCLE 2 ($\overline{CE1}$ and CE2 Controlled) (1,2,5)



Notes :

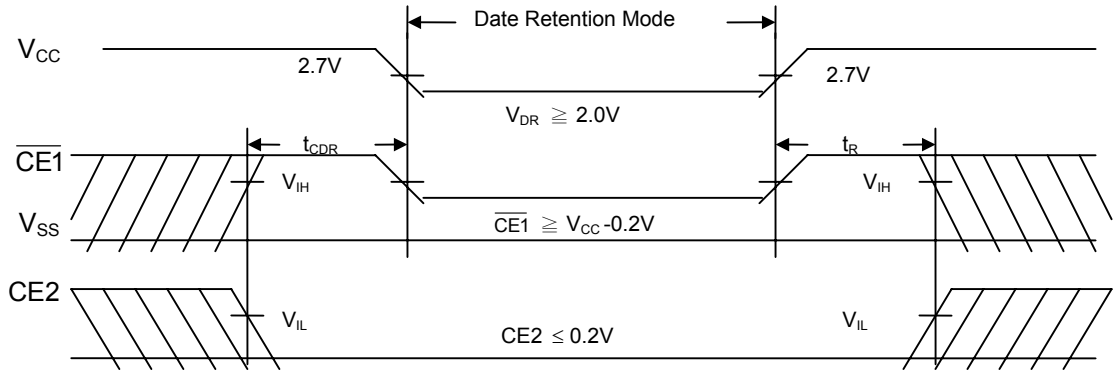
1. $\overline{WE}$ or $\overline{CE1}$ must be HIGH or CE2 must be LOW during all address transitions.
2. A write occurs during the overlap of a low $\overline{CE1}$, a high CE2 and a low $\overline{WE}$.
3. During a $\overline{WE}$ controlled with write cycle with $\overline{OE}$ LOW, t_{WP} must be greater than $t_{WHZ}+t_{DW}$ to allow the I/O drivers to turn off and data to be placed on the bus.
4. During this period, I/O pins are in the output state, and input singals must not be applied.
4. If the $\overline{CE1}$ LOW transition occurs simultaneously with or after $\overline{WE}$ LOW transition, the outputs remain in a high Impedance state.
6. t_{OW} and t_{WHZ} are specified with C_L=5pF. Transition is measured ± 500mV from steady state.

DATA RETENTION CHARACTERISTICS (T_A = -20℃~80℃)

PARAMETER	SYMBOL	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
Vcc for Data Retention	V_{DR}	$\overline{CE1} \geqq V_{CC}$-0.2V or CE2 ≤ 0.2V		2.0	-	-	V
Data Retention Current	I_{DR}	Vcc=3V	- L	-	1	60	μA
						10*	
		$\overline{CE1} \geqq V_{CC}$-0.2V or CE2 ≤ 0.2V	- LL	-	0.3	30	μA
						10*	
Chip Disable to Data Retention Time	t_{CDR}	See Data Retention Waveforms (below)		0	-	-	ns
Recovery Time	t_R			t_{RC}*	-	-	ns

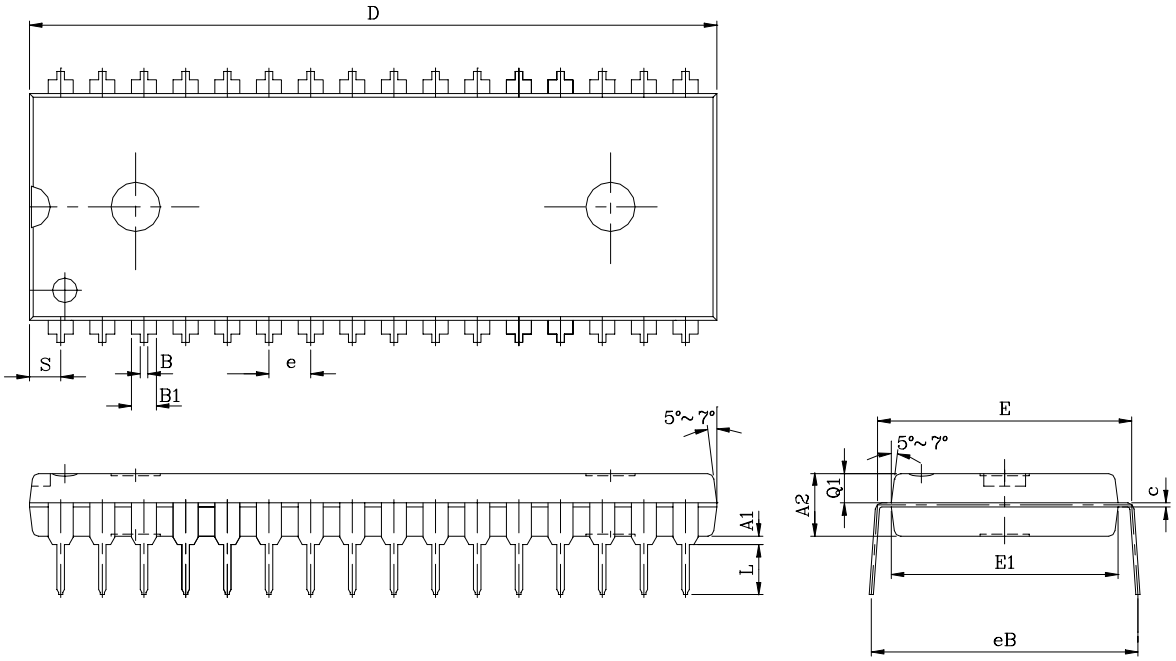
t_{RC}* = Read Cycle Time
*Those parameters are for reference only under 50℃

DATA RETENTION WAVEFORM



PACKAGE OUTLINE DIMENSION

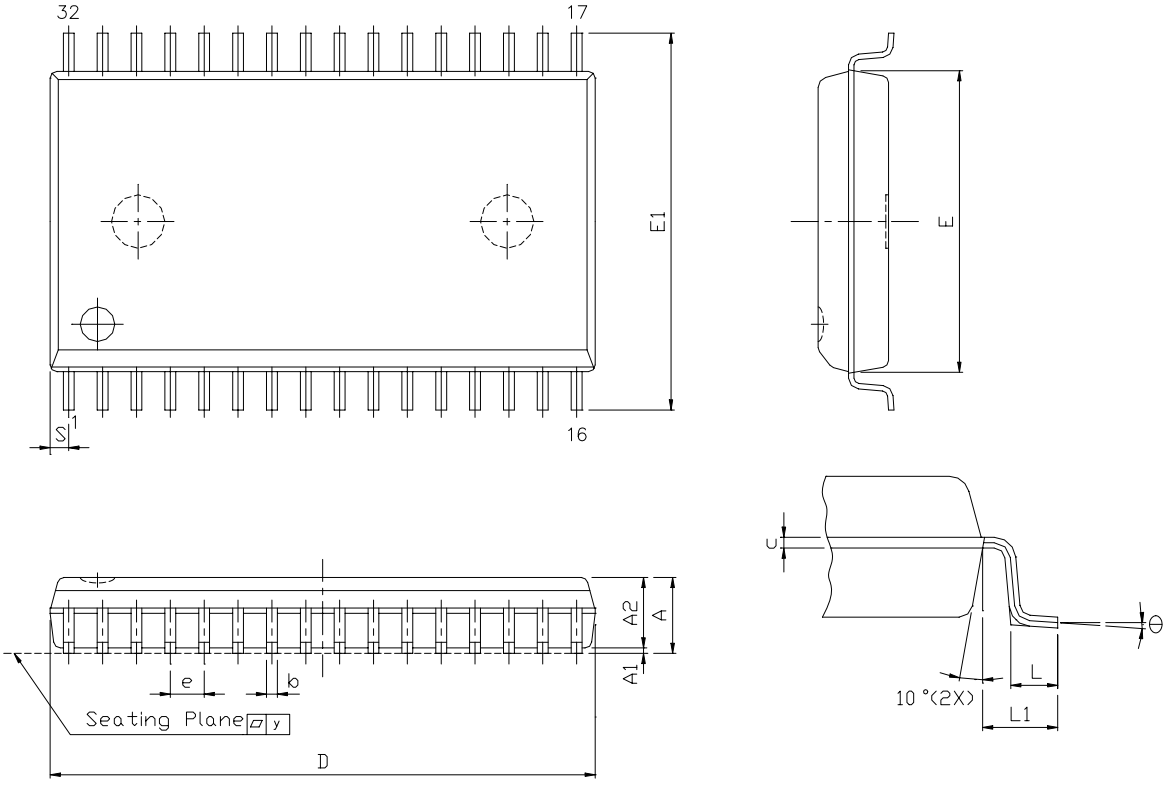
32 pin 600 mil PDIP Package Outline Dimension



SYMBOL \ UNIT	INCH(BASE)	MM(REF)
A1	0.010 (MIN)	0.254 (MIN)
A2	0.150 ± 0.005	3.810 ± 0.127
B	0.018 ± 0.005	0.457± 0.127
B1	0.050 ± 0.005	1.270± 0.127
c	0.010 ± 0.004	0.254± 0.102
D	1.650 ± 0.005	41.910 ± 0.127
E	0.600 ± 0.010	15.240 ± 0.254
E1	0.544 ± 0.004	13.818 ± 0.102
e	0.100 (TYP)	2.540 (TYP)
eB	0.640± 0.020	16.256 ± 0.508
L	0.130 ± 0.010	3.302 ± 0.254
S	0.075 ± 0.010	1.905 ± 0.254
Q1	0.070 ± 0.005	1.778 ± 0.127

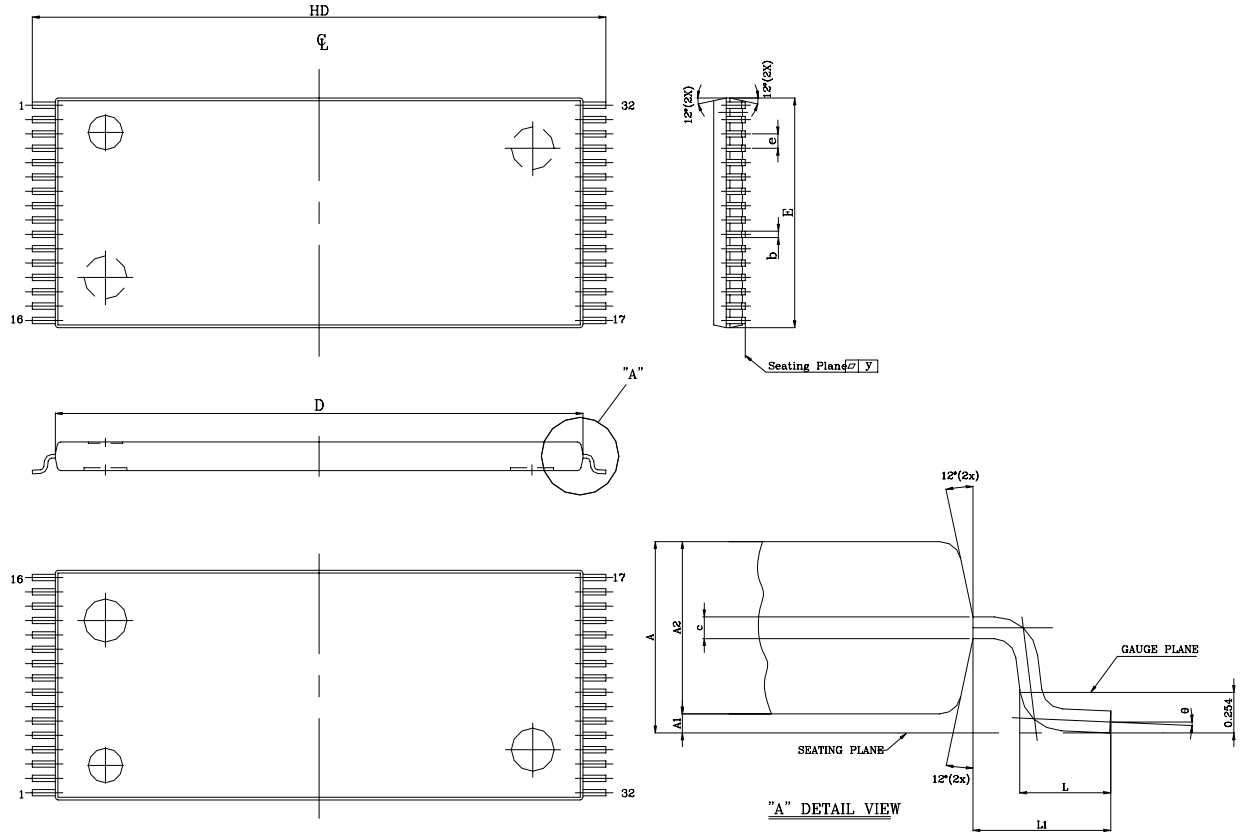
Note:
1. D/E1/S DIMENSION DO NOT INCLUDE MOLD FLASH.

32 pin 450mil SOP Package Outline Dimension



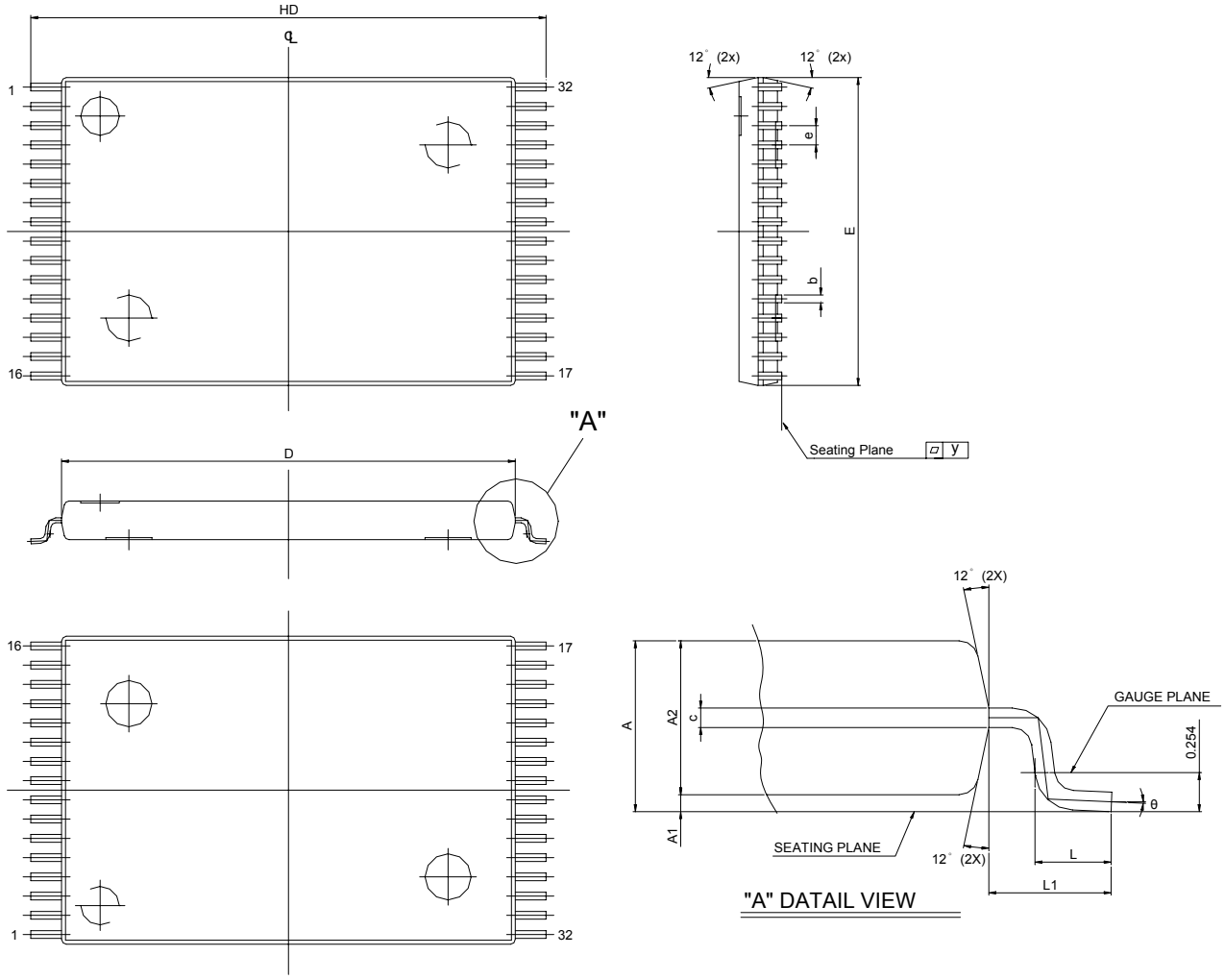
UNIT / SYMBOL	INCH(BASE)	MM(REF)
A	0.118 (MAX)	2.997 (MAX)
A1	0.004(MIN)	0.102(MIN)
A2	0.111(MAX)	2.82(MAX)
b	0.016(TYP)	0.406(TYP)
c	0.008(TYP)	0.203(TYP)
D	0.817(MAX)	20.75(MAX)
E	0.445 ± 0.005	11.303 ± 0.127
E1	0.555 ± 0.012	14.097 ± 0.305
e	0.050(TYP)	1.270(TYP)
L	0.0347 ± 0.008	0.881 ± 0.203
L1	0.055 ± 0.008	1.397 ± 0.203
S	0.026(MAX)	0.066 (MAX)
y	0.004(MAX)	0.101(MAX)
θ	0^o -10^o	0^o -10^o

32 pin TSOP-I Package Outline Dimension



UNIT / SYMBOL	INCH(BASE)	MM(REF)
A	0.047 (MAX)	1.20 (MAX)
A1	0.004 ± 0.002	0.10 ± 0.05
A2	0.039 ± 0.002	1.00 ± 0.05
b	0.008 + 0.002 - 0.001	0.20 + 0.05 -0.03
c	0.005 (TYP)	0.127 (TYP)
D	0.724 ± 0.004	18.40 ± 0.10
E	0.315 ± 0.004	8.00 ± 0.10
e	0.020 (TYP)	0.50 (TYP)
HD	0.787 ± 0.008	20.00 ± 0.20
L	0.0197 ± 0.004	0.50 ± 0.10
L1	0.0315 ± 0.004	0.08 ± 0.10
y	0.003 (MAX)	0.076 (MAX)
θ	0°～5°	0°～5°

32 pin 8mm x 13.4mm STSOP Package Outline Dimension



UNIT / SYMBOL	INCH(BASE)	MM(REF)
A	0.049 (MAX)	1.25 (MAX)
A1	0.005 ± 0.002	0.130 ± 0.05
A2	0.039 ± 0.002	1.00 ± 0.05
b	0.008 ± 0.01	0.20± 0.025
c	0.005 (TYP)	0.127 (TYP)
D	0.465 ± 0.004	11.80 ± 0.10
E	0.315 ± 0.004	8.00 ± 0.10
e	0.020 (TYP)	0.50 (TYP)
HD	0.528± 0.008	13.40 ± 0.20.
L	0.0197 ± 0.004	0.50 ± 0.10
L1	0.0315 ± 0.004	0.8 ± 0.10
y	0.003 (MAX)	0.076 (MAX)
θ	0°～5°	0°～5°

ORDERING INFORMATION

PART NO.	ACCESS TIME (ns)	STANDBY CURRENT (μA)	PACKAGE
UT62L1024PC-35LE	35	80	32 PIN PDIP
UT62L1024PC-35LLE	35	40	32 PIN PDIP
UT62L1024SC-35LE	35	80	32 PIN SOP
UT62L1024SC-35LLE	35	40	32 PIN SOP
UT62L1024LC-35LE	35	80	32 PIN TSOP-I
UT62L1024LC-35LLE	35	40	32 PIN TSOP-I
UT62L1024LS-35LE	35	80	32 PIN STSOP
UT62L1024LS-35LLE	35	40	32 PIN STSOP
UT62L1024PC-55LE	55	80	32 PIN PDIP
UT62L1024PC-55LLE	55	40	32 PIN PDIP
UT62L1024SC-55LE	55	80	32 PIN SOP
UT62L1024SC-55LLE	55	40	32 PIN SOP
UT62L1024LC-55LE	55	80	32 PIN TSOP-I
UT62L1024LC-55LLE	55	40	32 PIN TSOP-I
UT62L1024LS-55LE	55	80	32 PIN STSOP
UT62L1024LS-55LLE	55	40	32 PIN STSOP
UT62L1024PC-70LE	70	80	32 PIN PDIP
UT62L1024PC-70LLE	70	40	32 PIN PDIP
UT62L1024SC-70LE	70	80	32 PIN SOP
UT62L1024SC-70LLE	70	40	32 PIN SOP
UT62L1024LC-70LE	70	80	32 PIN TSOP-I
UT62L1024LC-70LLE	70	40	32 PIN TSOP-I
UT62L1024LS-70LE	70	80	32 PIN STSOP
UT62L1024LS-70LLE	70	40	32 PIN STSOP

REVISION HISTORY

REVISION	DESCRIPTION	DATE
Rev. 1.0	Original.	Jun. 26. 2001
Rev. 1.1	Vcc is revised : 3.0V⇨2.7V	Jul 27,2001