



FEATURES

- Fast access time : 8/12/15 ns (max.)
- Low operating power consumption : 100 mA (typical)
- Single 5V power supply
- All inputs and outputs TTL compatible
- Fully static operation
- Three state outputs
- Package : 32-pin 300 mil SOJ

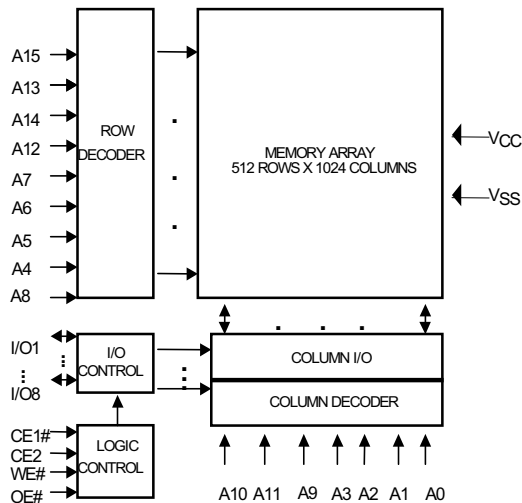
GENERAL DESCRIPTION

The UT61512 is a 524,288-bit high-speed CMOS static random access memory organized as 655,036 words by 8 bits. It is fabricated using high performance, high reliability CMOS technology.

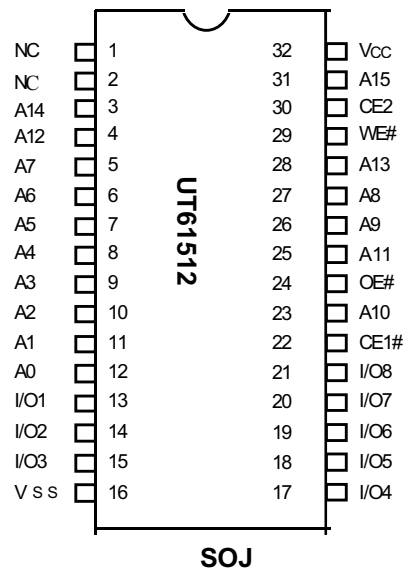
The UT61512 is designed for high-speed system applications. It is particularly suited for use in high-density high-speed system applications.

The UT61512 operates from a single 5V power supply and all inputs and outputs are fully TTL compatible.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



PIN DESCRIPTION

SYMBOL	DESCRIPTION
A0 - A15	Address Inputs
I/O1 - I/O8	Data Inputs/Outputs
CE1#	Chip Enable 1 input
CE2	Chip Enable 2 input
WE#	Write Enable Input
OE#	Output Enable Input
V <sub>CC</sub>	Power Supply
V <sub>SS</sub>	Ground
NC	No Connection

**ABSOLUTE MAXIMUM RATINGS\***

PARAMETER	SYMBOL	RATING	UNIT
Terminal Voltage with Respect to V <sub>SS</sub>	V <sub>TERM</sub>	-0.5 to +6.5	V
Operating Temperature	T <sub>A</sub>	0 to +70	°C
Storage Temperature	T <sub>STG</sub>	-65 to +150	°C
Power Dissipation	P <sub>D</sub>	1	W
DC Output Current	I <sub>OUT</sub>	50	mA
Soldering Temperature (under 10 sec)	T <sub>solder</sub>	260	°C

\*Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.

This

is a stress rating only and functional operation of the device or any other conditions above those indicated in the

operational sections of this specification is not implied. Exposure to the absolute maximum rating conditions for

extended period may affect device reliability.

**TRUTH TABLE**

MODE	CE1#	CE2	OE#	WE#	I/O OPERATION	SUPPLY CURRENT
Standby	H	X	X	X	High - Z	I <sub>SB</sub> , I <sub>SB1</sub>
Standby	X	L	X	X	High -Z	I <sub>SB</sub> , I <sub>SB1</sub>
Output Disable	L	H	H	H	High - Z	I <sub>CC</sub>
Read	L	H	L	H	D <sub>OUT</sub>	I <sub>CC</sub>
Write	L	H	X	L	D <sub>IN</sub>	I <sub>CC</sub>

Note: H = V<sub>IH</sub>, L=V<sub>IL</sub>, X = Don't care.

**DC ELECTRICAL CHARACTERISTICS (V<sub>CC</sub> = 5.0V± 10%, T<sub>A</sub> = 0°C to 70°C)**

PARAMETER	SYMBOL	TEST CONDITION	MIN.	MAX.	UNIT	
Input High Voltage	V <sub>IH</sub>		2.2	V <sub>CC</sub> +0.5	V	
Input Low Voltage	V <sub>IL</sub>		- 0.5	0.8	V	
Input Leakage Current	I <sub>LI</sub>	V <sub>SS</sub> ≤ V <sub>IN</sub> ≤ V <sub>CC</sub>	- 1	1	μA	
Output Leakage Current	I <sub>LO</sub>	V <sub>SS</sub> ≤ V <sub>IO</sub> ≤ V <sub>CC</sub> CE1# = V <sub>IH</sub> or CE2 = V <sub>IL</sub> or OE# = V <sub>IH</sub> or WE# = V <sub>IL</sub>	- 1	1	μA	
Output High Voltage	V <sub>OH</sub>	I <sub>OH</sub> = - 4mA	2.4	-	V	
Output Low Voltage	V <sub>OL</sub>	I <sub>OL</sub> = 8mA	-	0.4	V	
Operating Power Supply Current	I <sub>CC</sub>	CE1# = V <sub>IL</sub> , CE2 = V <sub>IH</sub> I <sub>IO</sub> = 0mA, Cycle=Min.	- 8	-	190	mA
			- 12	-	160	mA
			- 15	-	140	mA
Standby Power Supply Current	I <sub>SB</sub>	CE1# = V <sub>IH</sub> or CE2 = V <sub>IL</sub>	-	30	mA	
	I <sub>SB1</sub>	CE1# ≥ V <sub>CC</sub> -0.2V or CE2 ≤ 0.2V	-	5	mA	

**CAPACITANCE** ( $T_A=25^{\circ}\text{C}$ ,  $f=1.0\text{MHz}$ )

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
Input Capacitance	$C_{IN}$	-	8	pF
Input/Output Capacitance	$C_{I/O}$	-	10	pF

Note : These parameters are guaranteed by device characterization, but not production tested.

**AC TEST CONDITIONS**

Input Pulse Levels	0V to 3.0V
Input Rise and Fall Times	3ns
Input and Output Timing Reference Levels	1.5V
Output Load	$C_L=30\text{pF}$ , $I_{OH}/I_{OL}=-4\text{mA}/8\text{mA}$

**AC ELECTRICAL CHARACTERISTICS** ( $V_{CC} = 5V \pm 10\%$ ,  $T_A = 0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ )**(1) READ CYCLE**

PARAMETER	SYMBOL	UT61512-8		UT61512-12		UT61512-15		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Read Cycle Time	$t_{RC}$	8	-	12	-	15	-	ns
Address Access Time	$t_{AA}$	-	8	-	12	-	15	ns
Chip Enable Access Time	$t_{ACE}$	-	8	-	12	-	15	ns
Output Enable Access Time	$t_{OE}$	-	4	-	6	-	7	ns
Chip Enable to Output in Low Z	$t_{CLZ}^*$	2	-	3	-	4	-	ns
Output Enable to Output in Low Z	$t_{OLZ}^*$	0	-	0	-	0	-	ns
Chip Disable to Output in High Z	$t_{CHZ}^*$	-	4	-	6	-	7	ns
Output Disable to Output in High Z	$t_{OHZ}^*$	-	4	-	6	-	7	ns
Output Hold from Address Change	$t_{OH}$	3	-	3	-	3	-	ns

**(2) WRITE CYCLE**

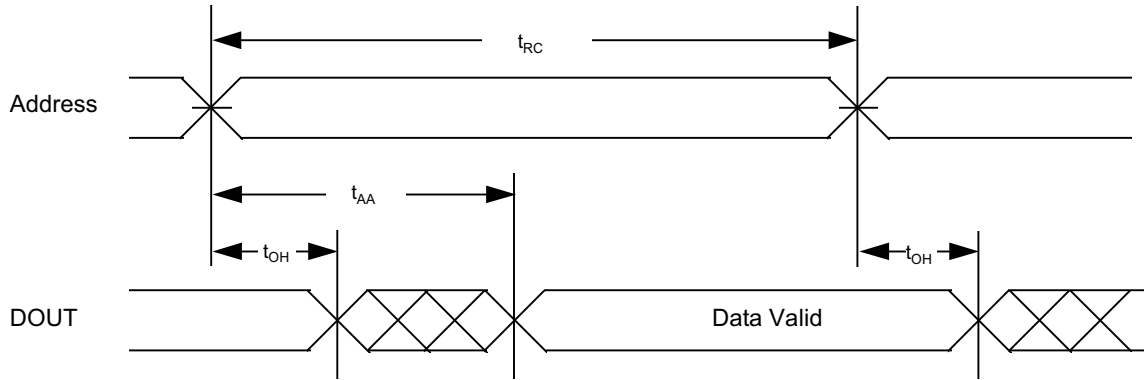
PARAMETER	SYMBOL	UT61512-8		UT61512-12		UT61512-15		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Write Cycle Time	$t_{WC}$	8	-	12	-	15	-	ns
Address Valid to End of Write	$t_{AW}$	6.5	-	10	-	12	-	ns
Chip Enable to End of Write	$t_{CW}$	6.5	-	10	-	12	-	ns
Address Set-up Time	$t_{AS}$	0	-	0	-	0	-	ns
Write Pulse Width	$t_{WP}$	6.5	-	9	-	10	-	ns
Write Recovery Time	$t_{WR}$	0	-	0	-	0	-	ns
Data to Write Time Overlap	$t_{DW}$	4	-	6	-	7	-	ns
Data Hold from End of Write Time	$t_{DH}$	0	-	0	-	0	-	ns
Output Active from End of Write	$t_{OW}^*$	1.5	-	3	-	4	-	ns
Write to Output in High Z	$t_{WHZ}^*$	-	4	-	6	-	7	ns

\*These parameters are guaranteed by device characterization, but not production tested.

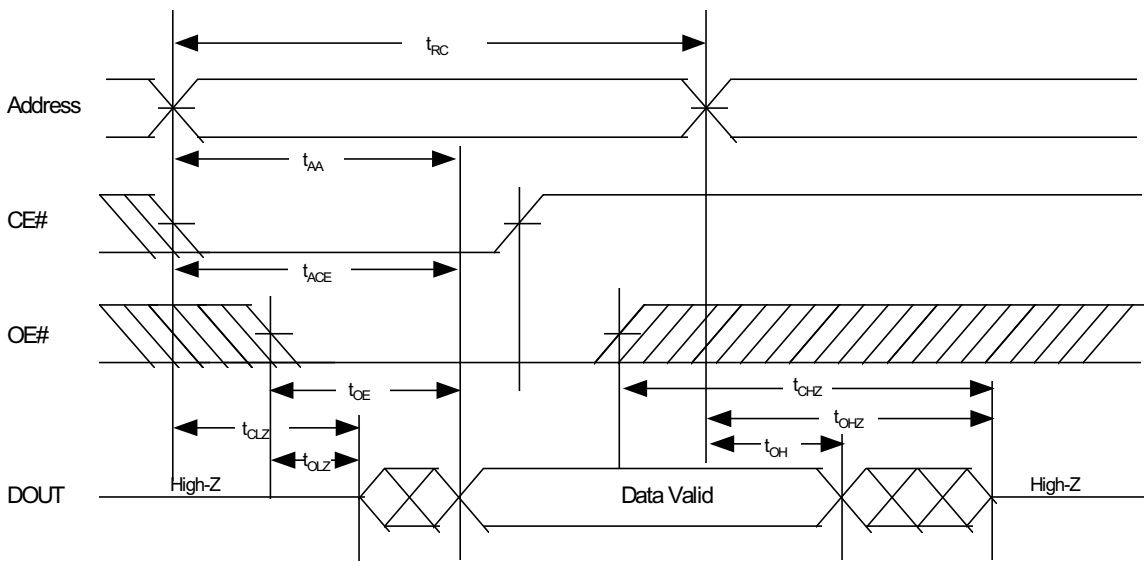


### TIMING WAVEFORMS

#### READ CYCLE 1 (Address Controlled) (1,2,4)



#### READ CYCLE 2 (CE# and OE# Controlled) (1,3,5,6)

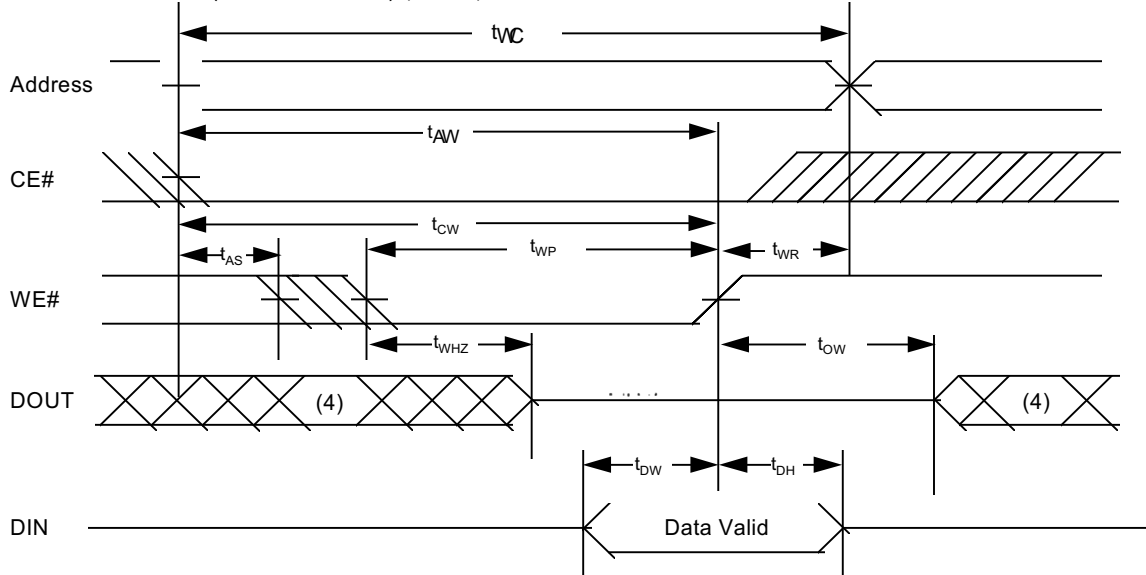


Notes :

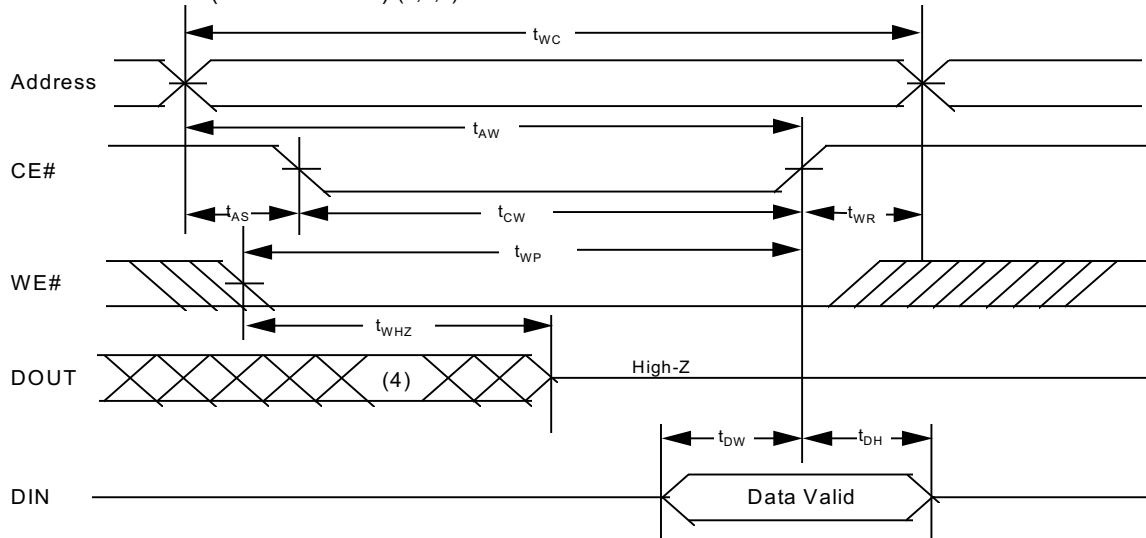
1. WE# is HIGH for read cycle.
2. Device is continuously selected CE#=V<sub>IL</sub>.
3. Address must be valid prior to or coincident with CE# transition; otherwise  $t_{AA}$  is the limiting parameter.
4. OE# is LOW.
5.  $t_{CLZ}$ ,  $t_{OLZ}$ ,  $t_{CHZ}$  and  $t_{OH}$  are specified with  $C_L = 5pF$ . Transition is measured  $\pm 500mV$  from steady state.
6. At any given temperature and voltage condition,  $t_{CHZ}$  is less than  $t_{CLZ}$ ,  $t_{OH}$  is less than  $t_{OLZ}$ .



**WRITE CYCLE 1 (WE# Controlled) (1,2,3,5)**



**WRITE CYCLE 2 (CE# Controlled) (1,2,5)**



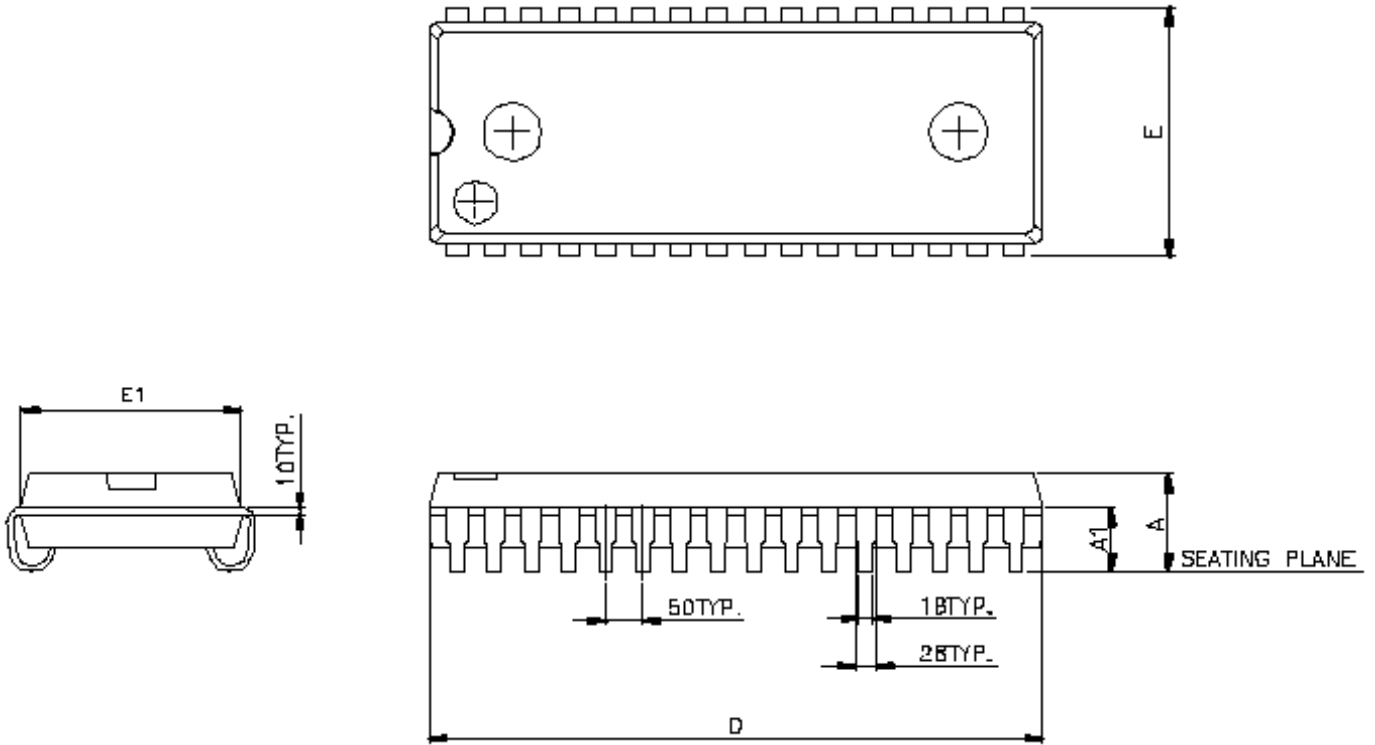
Notes :

1. WE# or CE# must be HIGH during all address transitions.
2. A write occurs during the overlap of a low CE# and a low WE#.
3. During a WE# controlled with write cycle with OE# LOW,  $t_{WP}$  must be greater than  $t_{WHZ} + t_{DW}$  to allow the drivers to turn off and data to be placed on the bus.
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the CE# LOW transition occurs simultaneously with or after WE# LOW transition, the outputs remain in a high impedance state.
6.  $t_{OW}$  and  $t_{WHZ}$  are specified with  $C_L = 5pF$ . Transition is measured  $\pm 500mV$  from steady state.



PACKAGE OUTLINE DIMENSION

32 pin 300 mil SOJ Package Outline Dimension



SYMBOLS	MIN.	NOR.	MAX.
A	0.128	0.138	0.148
A1	0.082	--	--
D	0.820	0.825	0.830
E	0.335 BSC.		
E1	0.295	0.300	0.305

UNIT : INCH

NOTE :

1. JEDEC OUTLINE : MO-077 AC
2. DIMENSION D AND E1 DO NOT INCLUDE MOLD PROTRUSION. MOLD PROTRUSION SHALL NOT EXCEED 0.006 INCH PER SIDE.



**UTRON**

Preliminary V1.1

**UT61512**

**64K X 8 BIT HIGH SPEED CMOS SRAM**

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**ORDERING INFORMATION**

<b>PART NO.</b>	<b>ACCESS TIME (ns)</b>	<b>PACKAGE</b>
UT61512JC-8	8	32PIN SOJ
UT61512JC-12	12	32PIN SOJ
UT61512JC-15	15	32PIN SOJ