REVISION HISTORY

REVISION	DESCRIPTION	Draft Date
Rev. 1.0	Original.	Apr 30 ,1999
Rev. 1.1	Add 40 pin TSOP-II Package.	Jun 7 ,1999
Rev. 1.2	Add 3.3V range.	Jul 30,1999
Rev. 1.3	Revised Datasheet name to be UT51C164/UT51L164.	Sep 22,2000
Rev. 1.4	1.Separated V_{DD}=5V and V_{DD}=3.3V version. 2.Revise symbols “RAS#、CAS#、OE#、WE#” to be “$\overline{RAS}$ 、 $\overline{CAS}$ 、 $\overline{OE}$ 、 $\overline{WE}$ ”.	Jan 23,2002
Rev. 1.5	1. Add access time 25ns, delete 60ns 2. Add DC/AC characteristics for –25ns	Oct 22,2002

FEATURES

- $\overline{RAS}$ access time: 25, 35, 40, 50
- 2 $\overline{CAS}$ Byte/Word Read/Write operation
- $\overline{CAS}$ - before – $\overline{RAS}$ refresh capability
- $\overline{RAS}$ only and Hidden refresh capability
- Early write or output enable controlled write
- Extended Data Out operation
- Package : 40 pin 400mil SOJ
  40 / 44 pin 400mil TSOP-Ⅱ
- Single 5V±10% power supply
- TTL compatible inputs and outputs
- 512 refresh cycles /8ms

Speed	-25	-35	-40	-50
t_{RAC}	25ns	35ns	40ns	50ns
t_{CAA}	12ns	18ns	20ns	24ns
t_{PC}	10ns	14ns	15ns	19ns
t_{CAC}	7ns	11ns	12ns	14ns
t_{RC}	45ns	70ns	75ns	90ns

GENERAL DESCRIPTION

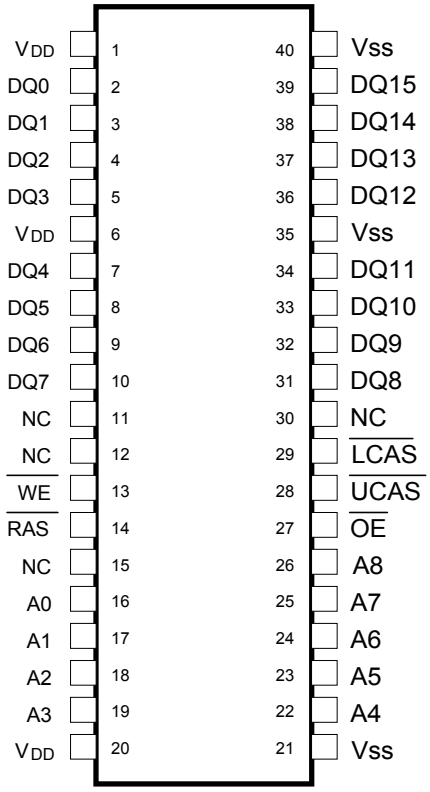
The UT51C164 is high speed 5V EDO DRAMs organized as 256K bit X 16 I/O and fabricated with the CMOS process. The UT51C164 offers a combination of unique features including : EDO Page Mode operation for higher bandwidth with Page Mode cycle time as short as 14ns. All inputs are TTL compatible. Input and output capacitance is significantly lowered to increase performance and minimize loading. These features make the UT51C164 suited for wide variety of high performance computer systems and peripheral applications

PIN DESCRIPTION

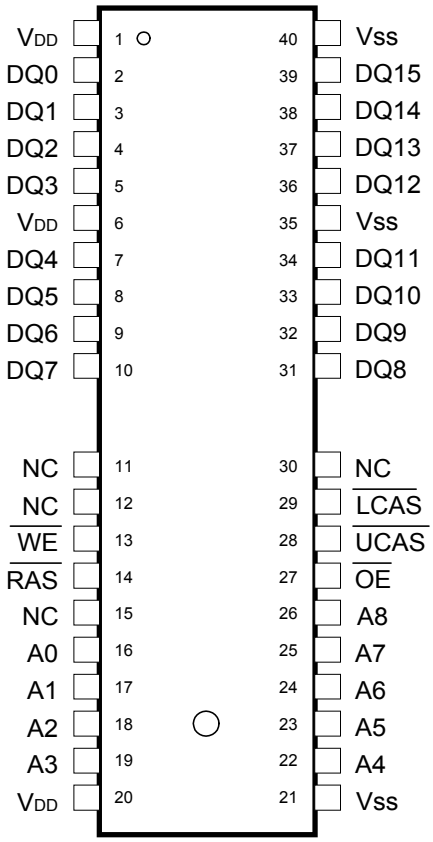
SYMBOL	DESCRIPTION
A0-A8	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{UCAS}$	Column Address Strobe / Upper Byte Control
$\overline{LCAS}$	Column Address Strobe / Lower Byte Control
$\overline{WE}$	Write enable
$\overline{OE}$	Output enable
DQ0-DQ15	Data Inputs, Data Outputs
V_{DD}	+5V Supply
Vss	0V Supply
NC	No Connect

PIN CONFIGURATIONS

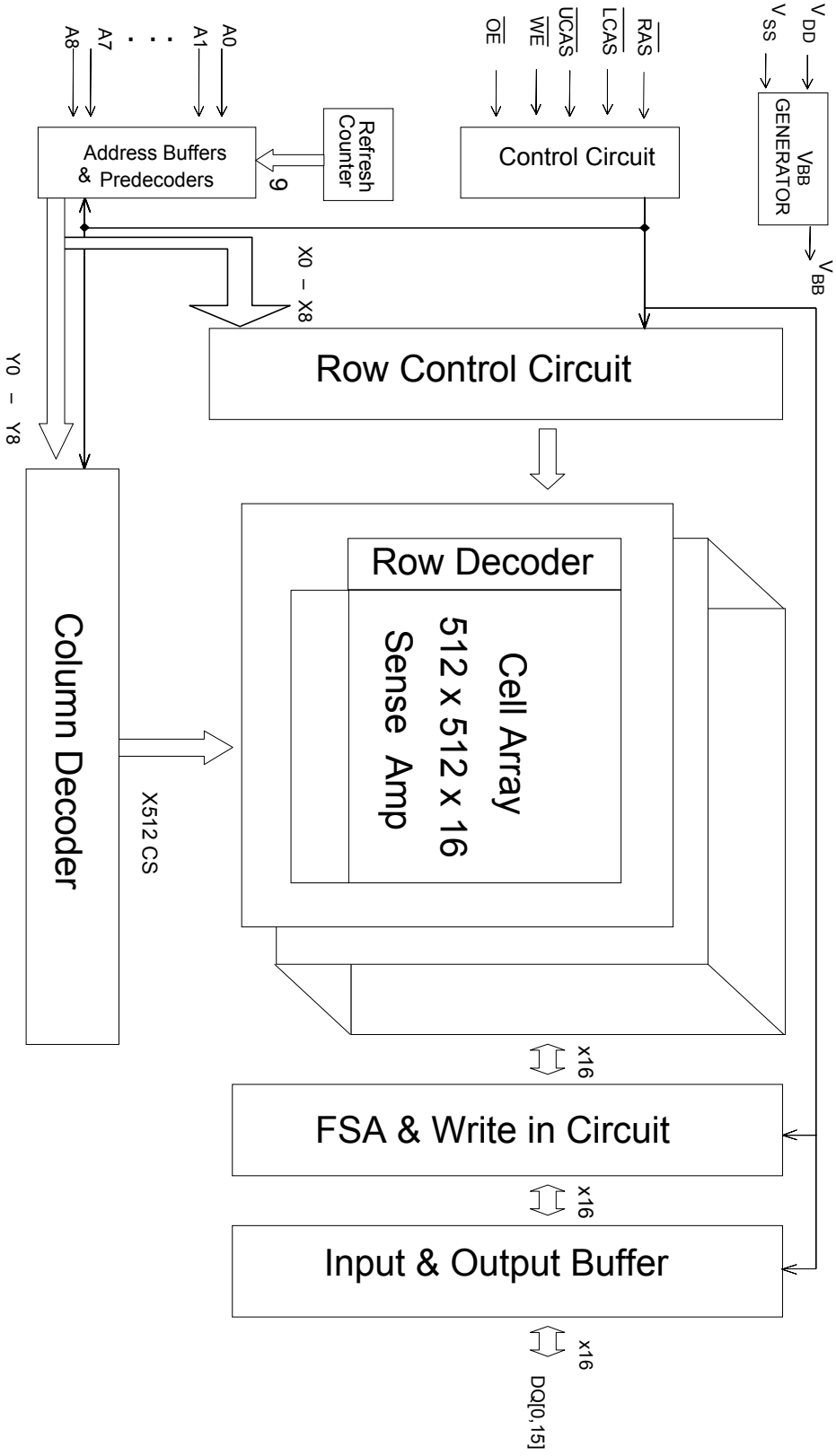
UT51C164
40 - pin SOJ



UT51C164
40-pin TSOP II



FUNCTION BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Voltage on any pin relative to Vss	V_T	-1.0 to +7	V
Supply voltage relative to V_{SS}	V_{DD}	-1.0 to +7	V
Short circuit output current	I_{OUT}	50	mA
Power dissipation	P_D	1.0	W
Operating temperature	T_A	0 to + 70	ºC
Storage temperature	T_{STG}	-55 to +125	ºC

Notes: Permanent device damage may occur if absolute maximum ratings are exceed.

RECOMMENDED DC OPERATING CONDITIONS (T_A = 0℃ to 70ºC)

PARAMETER	SYMBOL	5.0V		UNIT	NOTES
		MIN	MAX		
Supply voltage	V_{DD}	4.5	5.5	V	1
	Vss	0	0	V	-
Input high voltage	V_{IH}	2.4	V_{DD} +1V	V	1
Input low voltage	V_{IL}	-0.3	0.8	V	1

Notes: 1. All Voltage referred to Vss

CAPACITANCE (T_A = 25ºC, V_{DD}= 5V±0.5V，f=1MHz)

PARAMETER	SYMBOL	TYP	MAX	UNIT
Input capacitance (A0-A8)	$C_{IN}1$	3	4	pF
Input Capacitance ($\overline{RAS}$, $\overline{UCAS}$, $\overline{LCAS}$, $\overline{WE}$, $\overline{OE}$)	$C_{IN}2$	4	5	pF
Output capacitance(DQ0-DQ15)	C_{DQ}	5	7	pF

DC CHARACTERISTICS (T_A = 0℃ to 70ºC, V_{DD} = 5.0 V ± 0.5 V, Vss = 0 V)

SYMBOL	PARAMETER	SPEED (t_{RAC})	UT51C164 Min	UT51C164 Max	UNIT	TEST CONDITION
I_{DD1}	Operating Current, V_{DD} Supply	-25	-	200	mA	$t_{RC} = t_{RC}$ (min.)
		-35	-	190		
		-40	-	180		
		-50	-	170		
I_{DD2}	Standby Current (TTL Input)	-	-	3	mA	$\overline{RAS} = \overline{UCAS} = \overline{LCAS} = V_{IH}$
I_{DD3}	$\overline{RAS}$ Only Refresh Current	-25	-	200	mA	$t_{RC} = t_{RC}$ (min.)
		-35	-	190		
		-40	-	180		
		-50	-	170		
I_{DD4}	EDO Page Mode Current	-25	-	220	mA	$t_{PC} = t_{PC}$ (min.)
		-35	-	220		
		-40	-	200		
		-50	-	190		
I_{DD5}	CBR Refresh Current	-25	-	200	mA	$t_{RC} = t_{RC}$ (min.)
		-35	-	190		
		-40	-	180		
		-50	-	170		
I_{DD6}	Standby Current (CMOS Input)	-	-	2	mA	$\overline{RAS} \geqq V_{DD}$-0.2V $\overline{CAS} \geqq V_{DD}$-0.2V All other inputs $\geqq V_{SS}$
V_{DD}	Power Supply	-	4.5	5.5	V	
I_{LI}	Input Leakage Current	-	-10	10	uA	$V_{SS} \leqq V_{IN} \leqq V_{DD}$
I_{LO}	Output Leakage Current	-	-10	10	uA	$V_{SS} \leqq V_{OUT} \leqq V_{DD}$ $\overline{RAS} = \overline{CAS} = V_{IH}$
V_{IL}	Input Low Voltage	-	-1	0.8	V	
V_{IH}	Input High Voltage	-	2.4	V_{DD} +1	V	
V_{OL}	Output Low Voltage	-	-	0.4	V	I_{OL} = 2mA
V_{OH}	Output High Voltage	-	2.4	-	V	I_{OH} = 2mA

Notes: I_{DD1}, I_{DD3}, I_{DD4}, I_{DD5} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{DD} is specified as an average current. In I_{DD1}, I_{DD3}, and I_{DD5} address can be changed maximum once while $\overline{RAS}$ =V_{IL}. In I_{DD4}, address can be changed maximum once within one EDO page cycle time, t_{PC}.

AC CHARACTERISTICS (T_A = 0℃ to 70°C)

Test condition: V_{DD} = 5.0V±0.5V, V_{IH} / V_{IL}=3V / 0V, V_{OH} / V_{OL}=2.0 / 0.8)

	SYMBOL	PARAMETER	25		35		40		50		UNIT	NOTE
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
1	t_{RAS}	$\overline{RAS}$ Pulse Width	25	75K	35	75K	40	75K	50	75K	ns	
2	t_{RC}	Read or Write Cycle Time	45		70		75		90		ns	
3	t_{RP}	$\overline{RAS}$ Precharge Time	15		25		25		30		ns	
4	t_{CSH}	$\overline{CAS}$ Hold Time	20		35		40		50		ns	
5	t_{CAS}	$\overline{CAS}$ Pulse Width	5		8		8		10		ns	
6	t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay	10	17	13	24	17	28	19	36	ns	
7	t_{RCS}	Read Command Setup Time	0		0		0		0		ns	*1
8	t_{ASR}	Row Address Setup Time	0		0		0		0		ns	
9	t_{RAH}	Row Address Hold Time	5		6		7		9		ns	
10	t_{ASC}	Column Address Setup Time	0		0		0		0		ns	
11	t_{CAH}	Column Address Hold Time	4		6		7		9		ns	
12	t_{RSH}	$\overline{RAS}$ to $\overline{CAS}$ Hold Time	7		10		12		14		ns	
13	t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	3		5		5		5		ns	
14	t_{RCH}	Read Command Hold Time Reference $\overline{CAS}$	0		0		0		0		ns	*2
15	t_{RRH}	Read Command Hold Time Reference $\overline{RAS}$	0		0		0		0		ns	*2
16	t_{ROH}	$\overline{RAS}$ Hold Time Referenced to $\overline{OE}$	7		7		8		10		ns	
17	t_{OAC}	Access Time from $\overline{OE}$		8		11		12		14	ns	*9
18	t_{CAC}	Access Time from $\overline{CAS}$		7		11		12		14	ns	*3,4,11
19	t_{RAC}	Access Time from $\overline{RAS}$		25		35		40		50	ns	*3,5,6
20	t_{CAA}	Access Time From Column Address		12		18		20		24	ns	*3,4,7
21	t_{LZ}	$\overline{OE}$ or $\overline{CAS}$ to Low-Z Output	0		0		0		0		ns	*13
22	t_{HZ}	$\overline{OE}$ or $\overline{CAS}$ to High-Z Output	0	5	0	5	0	6	0	8	ns	*13
23	t_{AR}	Column Address Hold Time from $\overline{RAS}$	19		25		30		40		ns	
24	t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	8	12	10	17	12	20	14	26	ns	*8
25	t_T	Transition Time	1.5	50	1.5	50	1.5	50	1.5	50	ns	*12
26	t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	5		8		10		10		ns	
27	t_{WCS}	Write Command Setup Time	0		0		0		0		ns	*9,10
28	t_{WCH}	Write Command Hold time	4		5		6		7		ns	
29	t_{WP}	Write Pulse Width	4		5		6		7		ns	

AC CHARACTERISTICS (continued)

	SYMBOL	PARAMETER	25		35		40		50		UNIT	NOTE
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
30	t_{WCR}	Write Command Hold Time from $\overline{RAS}$	19		25		30		40		ns	
31	t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	8		11		12		14		ns	
32	t_{DS}	Data in Setup Time	0		0		0		0		ns	*11
33	t_{DH}	Data in Hold Time	4		5		6		7		ns	*11
34	t_{WOH}	Write to $\overline{OE}$ Hold time	3		5		6		8		ns	*11
35	t_{OED}	$\overline{OE}$ to Data Delay Time	3		5		6		8		ns	*11
36	t_{RWC}	Read-Modify-Write Cycle Time	65		105		110		130		ns	
37	t_{RRW}	Read-Modify-Write Cycle Time $\overline{RAS}$ Pulse Width	50		70		75		85		ns	
38	t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay in Read-Modify-Write Cycle	17		28		30		34		ns	*9
39	t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay in Read-Modify-Write Cycle	34		54		58		68		ns	*9
40	t_{CRW}	$\overline{CAS}$ pulse Width in RMW	26		46		48		52		ns	
41	t_{AWD}	Column Address to $\overline{WE}$ Delay Time	21		35		38		42		ns	*9
42	t_{PC}	EDO Page Mode Read or Write Cycle Time	10		14		15		19		ns	
43	t_{CP}	$\overline{CAS}$ Precharge Time	3		4		5		7		ns	
44	t_{CAR}	Column Address to $\overline{RAS}$ Setup Time	12		18		20		24		ns	
45	t_{CAP}	Access Time from Column Precharge		14		20		23		27	ns	*4
46	t_{DHR}	Data in Hold Time Referenced to $\overline{RAS}$	19		25		30		40		ns	
47	t_{CSR}	$\overline{CAS}$ Setup Time in CBR Refresh	5		8		10		10		ns	
48	t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	0		0		0		0		ns	
49	t_{CHR}	$\overline{CAS}$ Hold Time in CBR Refresh	7		8		9		12		ns	
50	t_{PCM}	EDO Page Mode Cycle Time in RMW	32		55		60		70		ns	
51	t_{COH}	Output Hold After $\overline{CAS}$ Low	3		3		3		3		ns	
52	t_{OES}	$\overline{OE}$ Low to $\overline{CAS}$ High Setup Time	4		3		4		6		ns	
53	t_{OEH}	$\overline{OE}$ Hold Time from $\overline{WE}$ in RMW Cycle	4		5		6		8		ns	
54	t_{OEP}	$\overline{OE}$ Pulse Width	4		8		10		14		ns	
55	t_{REF}	Refresh Interval (512 Cycles)	8			8		8		8	ms	*14

Notes:

1. t_{RCD} (Max.) is specified for reference only. Operation within t_{RCD} (Max.) limits insures that t_{RAC} (Max.) and t_{CAA} (Max.) can be met. If t_{RCD} is greater than the specified t_{RCD} (Max.), the access time is controlled by t_{CAA} and $t_{CAC.}$
2. Either t_{RRH} or t_{RCH} must be satisfied for Read Cycle to occur.
3. Measured with a load equivalent to one TTL input and 50pF.
4. Access time is determined by the longest of t_{CAA} , t_{CAC} and t_{CAP} .
5. Assumes that $t_{RAD} \leqq t_{RAD}$ (Max.). If t_{RCD} is greater than t_{RCD} (Max.), t_{RAC} will increase by the amount that t_{RCD} exceeds t_{RCD} (Max.)
6. Assumes that $t_{RCD} \leqq t_{RCD}$ (Max.). If t_{RCD} is greater than t_{RCD} (Max.), t_{RAC} will increase by the amount that t_{RAD} exceeds t_{RAD} (Max.)
7. Assumes that $t_{RAD} \geqq t_{RAD}$ (Max.).
8. Operation within the t_{RAD} (Max.) limits ensures that t_{RA} can be met. t_{RAD} (Max.) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD} (Max.), the access time is controlled by t_{CAA} and $t_{CAC.}$
9. t_{WCS} , t_{RWD} , t_{AWD} and t_{CWD} are not restrictive operating parameters.
10. t_{WCS} (min.) must be satisfied in an Early Write Cycle.
11. t_{DS} and t_{DH} are referenced to the latter occurrence of $\overline{CAS}$ or $\overline{WE}$.
12. t_T is measured between V_{IH} (min.) and V_{IL} (max.). AC-measurements assume t_T = 3ns.
13. Assumes a tri-state test load (5pF and a 500Ohm Thevenin equivalent).
14. An initial pause of 200us is required after power-up followed by any 8 CBR or ROR cycles before device operation is achieved.

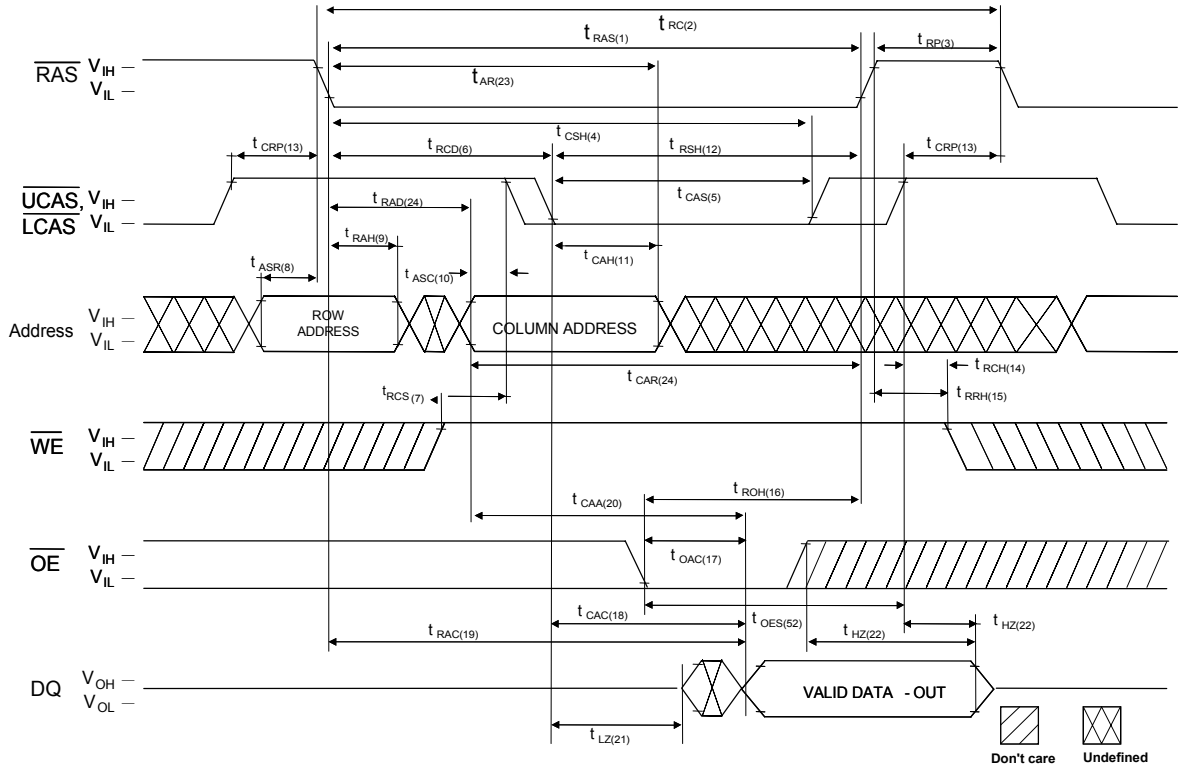
TRUTH TABLE

FUNCTION	$\overline{RAS}$	$\overline{LCAS}$	$\overline{UCAS}$	$\overline{WE}$	$\overline{OE}$	ADDRESS	DQ(0-7)	DQ(8-15)	NOTE
Standby	H	H	H	X	X	X	High-Z	High-Z	
Read: Word	L	L	L	H	L	ROW/COL	DQ-OUT		
Read: Lower Byte	L	L	H	H	L	ROW/COL	DQ-OUT	High-Z	
Read: Upper Byte	L	H	L	H	L	ROW/COL	High-Z	DQ-OUT	
Write: Word (Early-Write)	L	L	L	L	X	ROW/COL	DQ-IN		
Write: Lower Byte (Early-Write)	L	L	H	L	X	ROW/COL	DQ-IN	High-Z	
Write: Upper Byte (Early-Write)	L	H	L	L	X	ROW/COL	High-Z	DQ-IN	
Read-Write	L	L	L	H→L	L→H	ROW/COL	DQ-OUT,DQ-IN		*1,2
EDO Page-Mode Read	L	H→L	H→L	H	L	COL	DQ-OUT		*2
EDO Page-Mode Write	L	H→L	H→L	L	X	COL	DQ-IN		*2
EDO Page –Mode Read-Write	L	H→L	H→L	H→L	L→H	COL	DQ-OUT,DQ-IN		*1,2
Hidden Refresh Read	L→H→L	L	L	H	L	ROW/COL	DQ-OUT		*2
$\overline{RAS}$ Only Refresh	L	H	H	X	X	ROW	High-Z		
CBR Refresh	H→L	L	L	X	X	X	High-Z		

Notes:
1. Byte Write cycles $\overline{LCAS}$ or $\overline{UCAS}$ active.
2. Byte Read cycles $\overline{LCAS}$ or $\overline{UCAS}$ active.

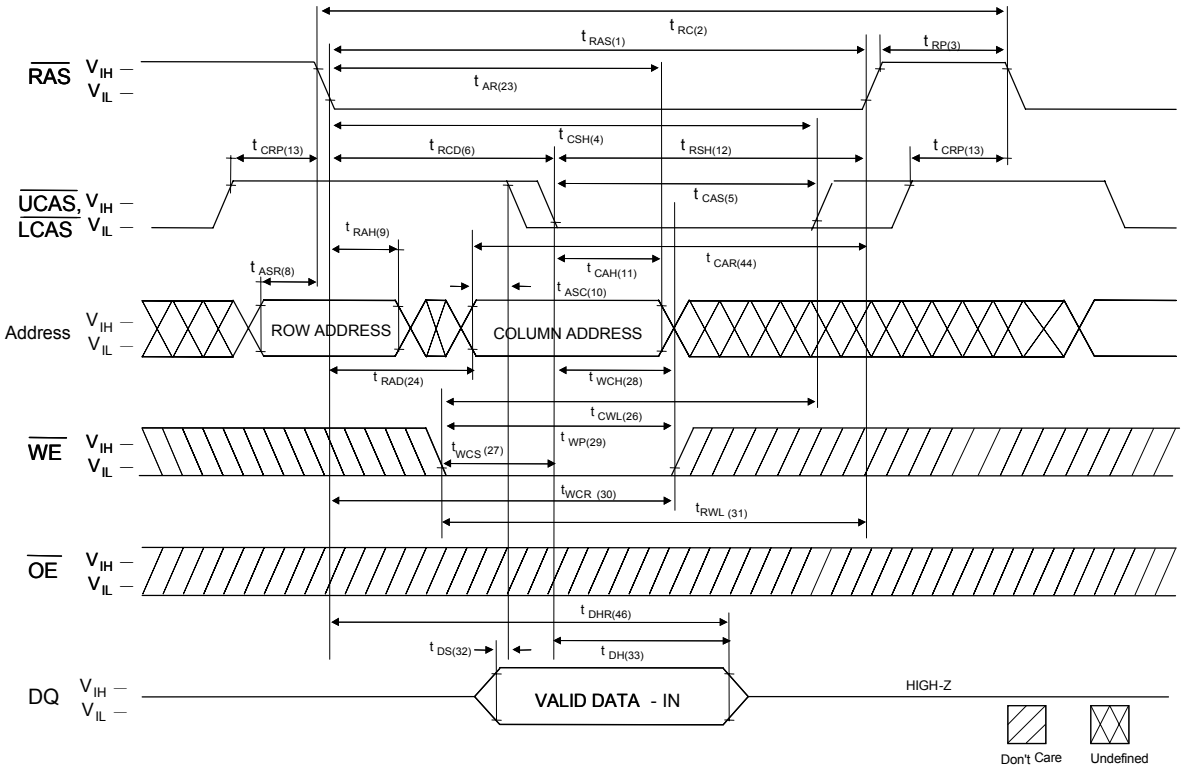
UTRON EDO Mode, X16 (2$\overline{CAS}$) Device Timing Diagram

– Waveforms of Read Cycle



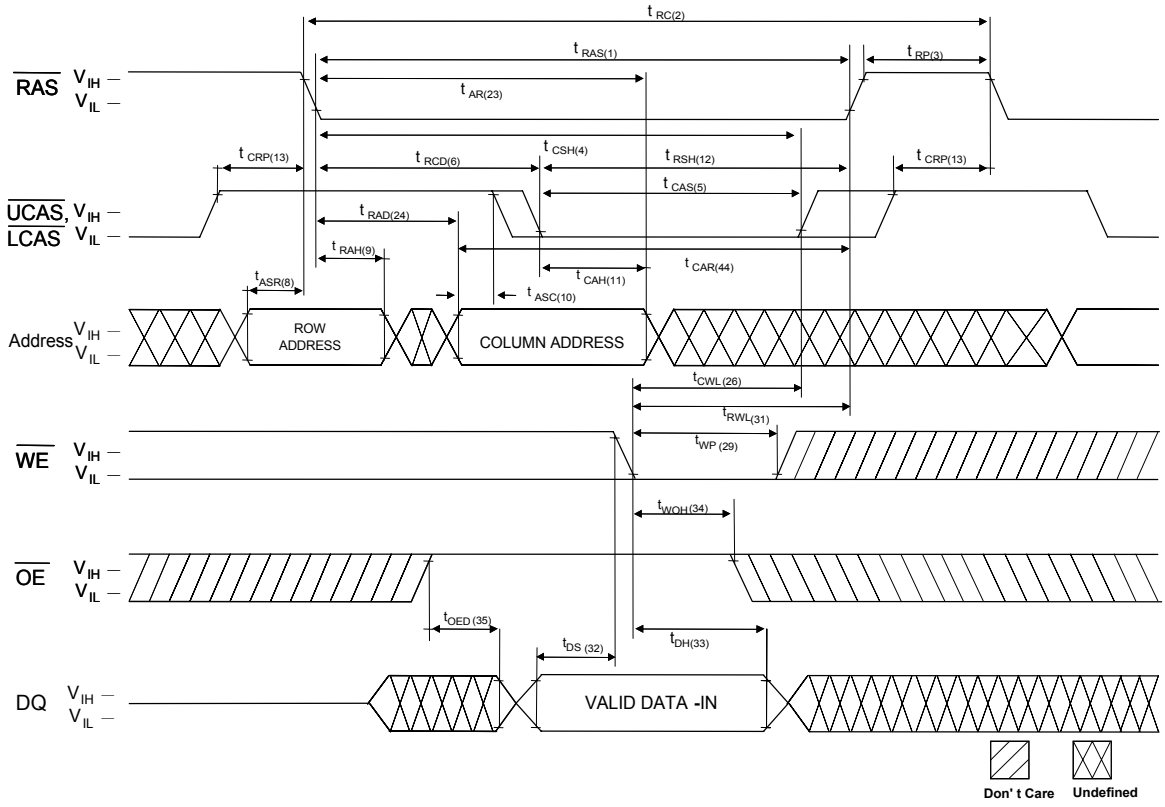
UTRON EDO Mode, X16 (2$\overline{CAS}$) Device Timing Diagram

— Waveforms of Early Write Cycle



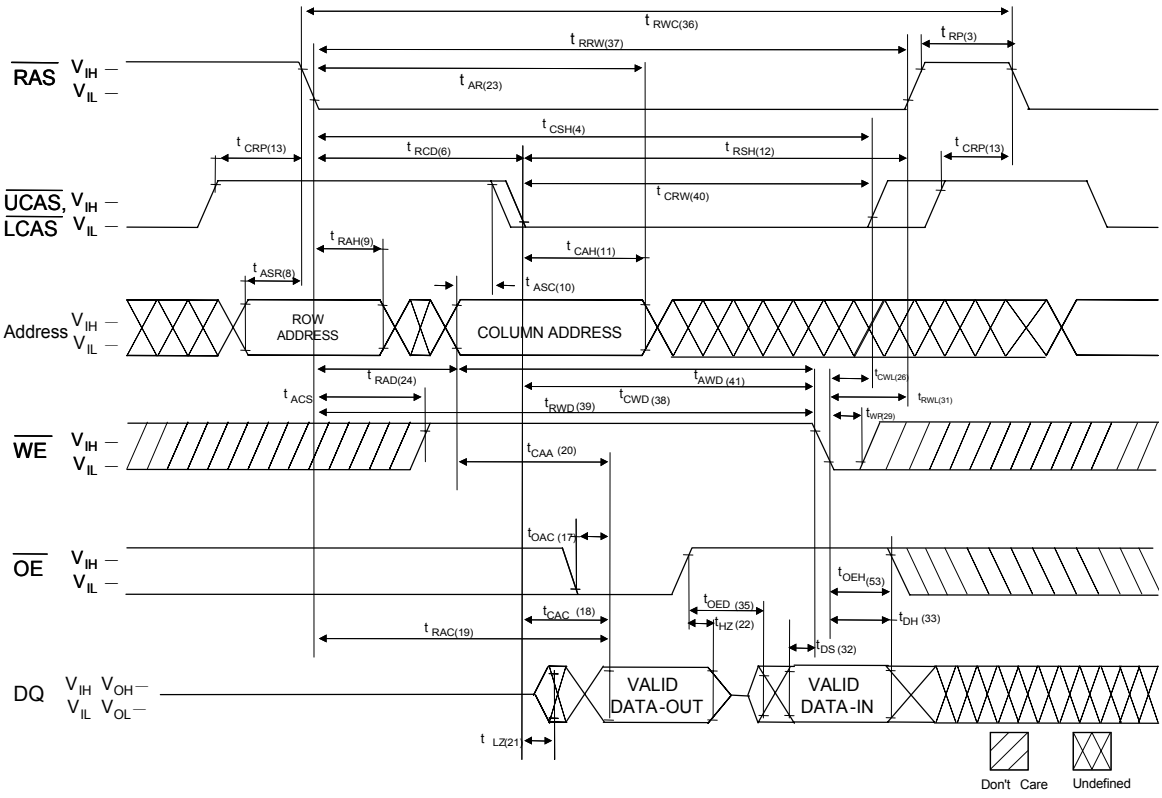
UTRON EDO Mode, X16 (2$\overline{CAS}$) Device Timing Diagram

— Waveforms of $\overline{OE}$-Contrilled Write Cycle



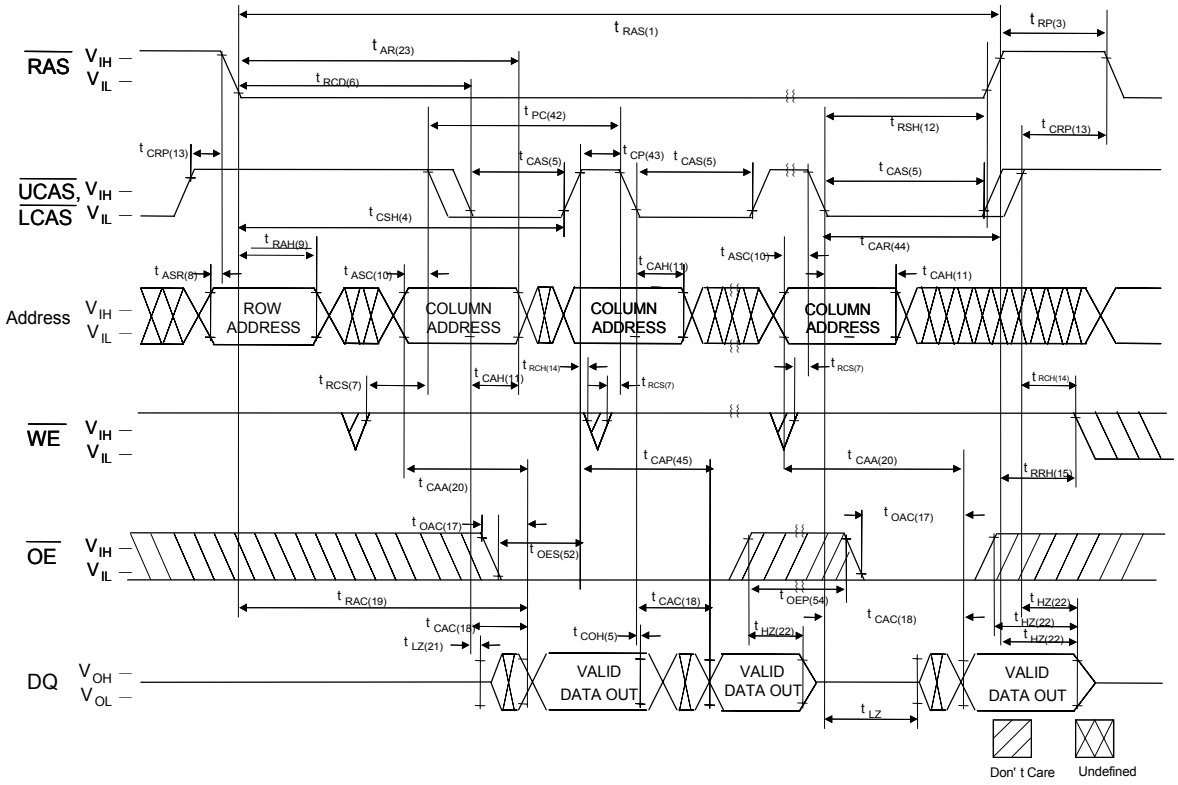
UTRON EDO Mode, X16 (2$\overline{CAS}$) Device Timing Diagram

— Waveforms of Read -Modify-Write Cycle



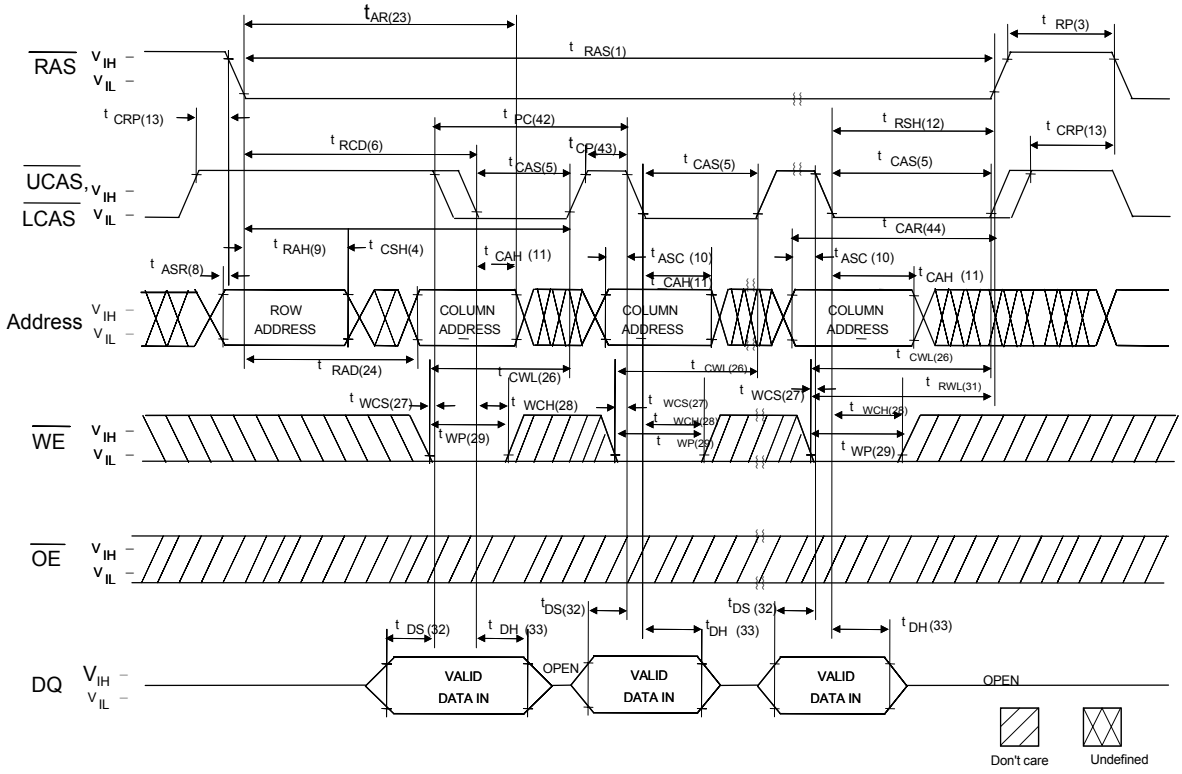
UTRON EDO Mode, X16 (2$\overline{CAS}$) Device Timing Diagram

— EDO Page Mode Read Cycle



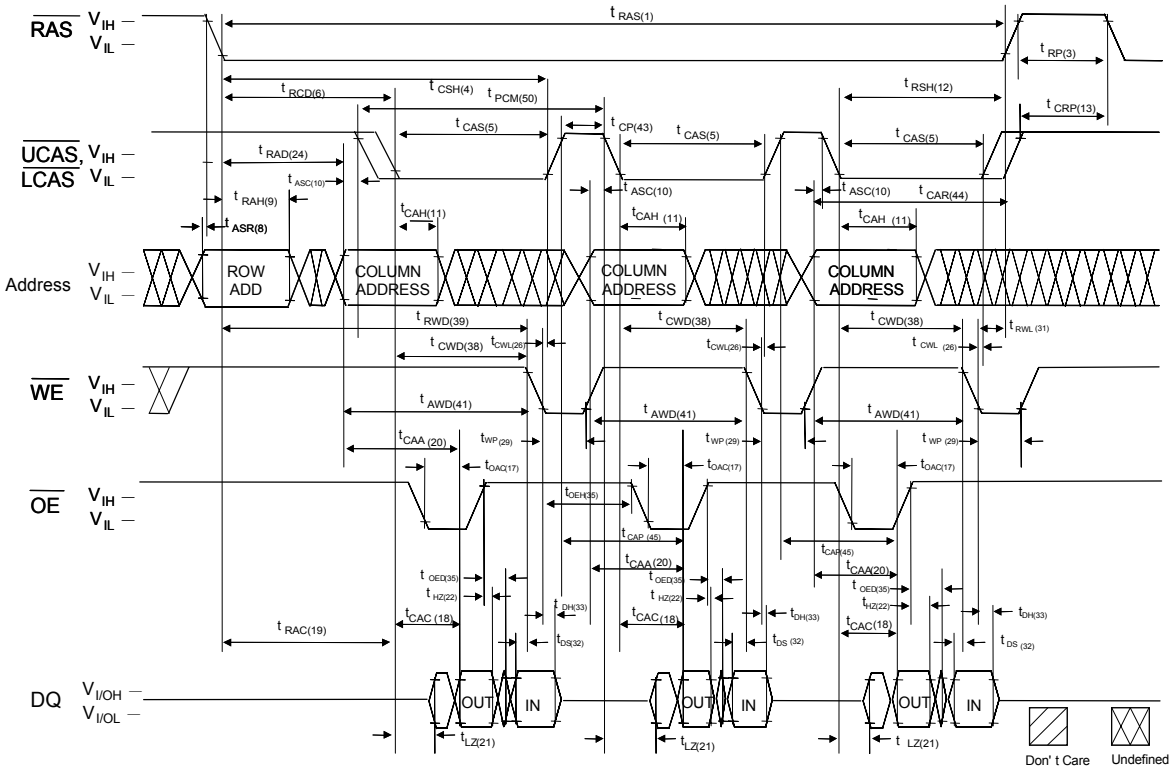
UTRON EDO Mode, X16 (2$\overline{CAS}$) Device Timing Diagram

– EDO Page Mode Write Cycle



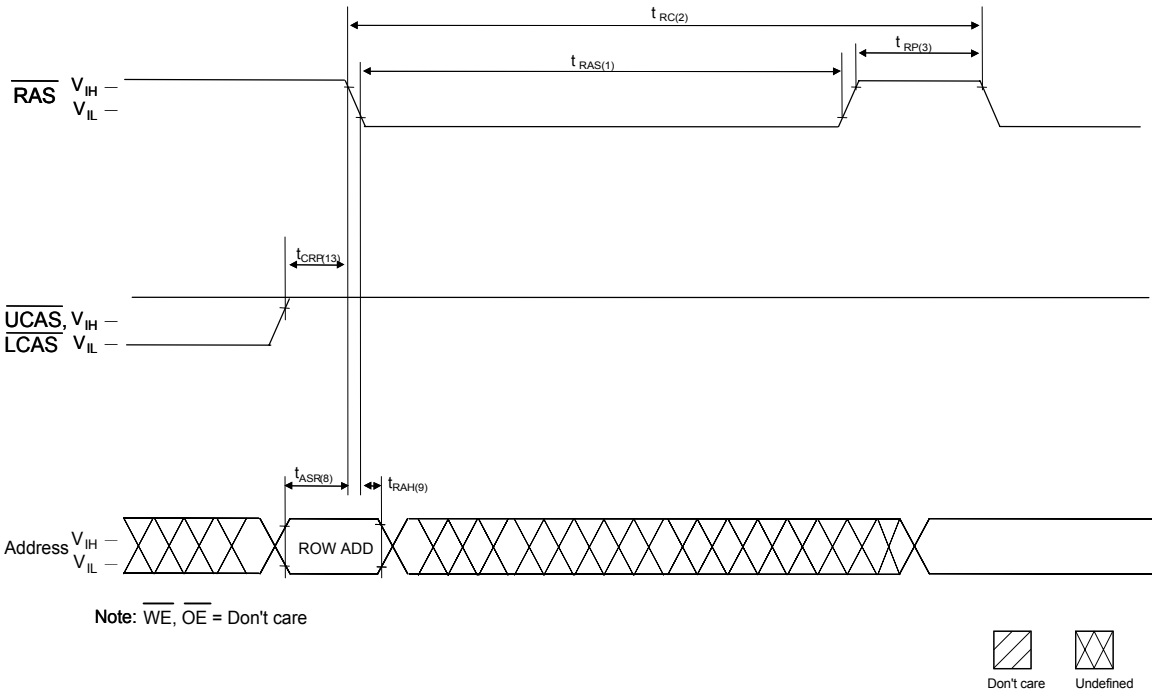
UTRON EDO Mode, X16 (2$\overline{CAS}$) Device Timing Diagram

— EDO Page Mode Read-Write Cycle



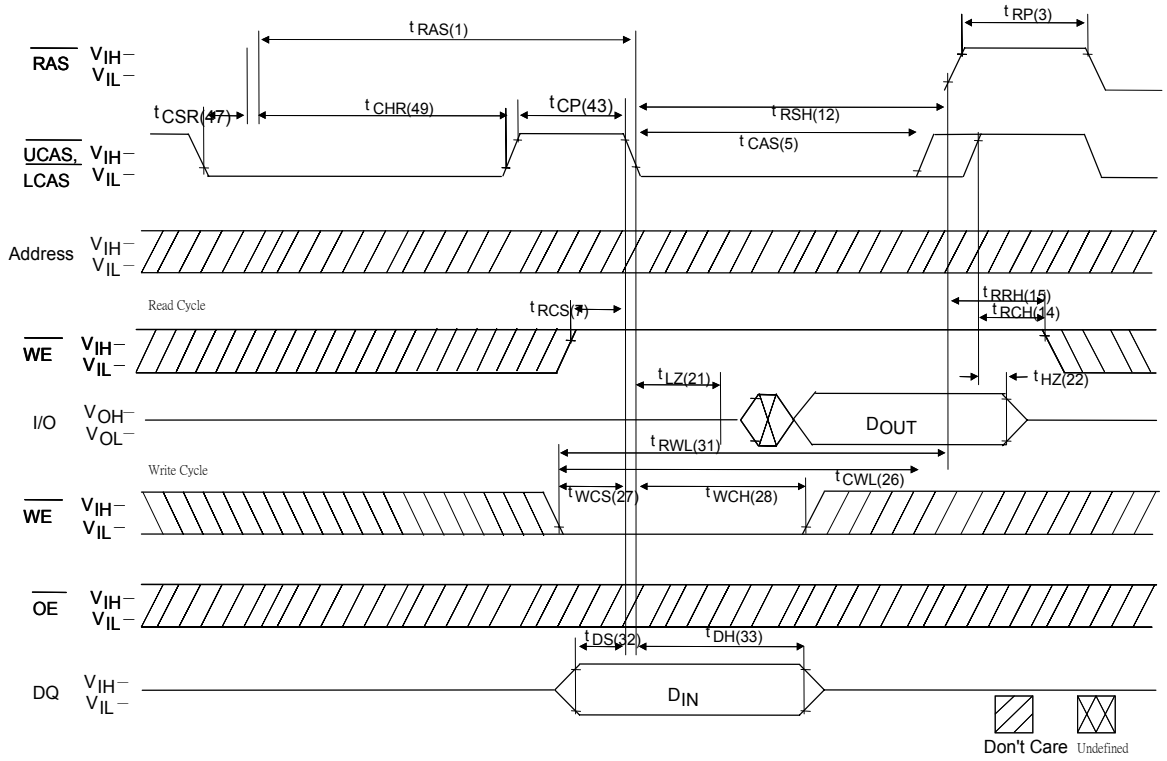
UTRON EDO Mode, X16 (2$\overline{CAS}$) Device Timing Diagram

— Waveforms of $\overline{RAS}$ - Only Refresh Cycle



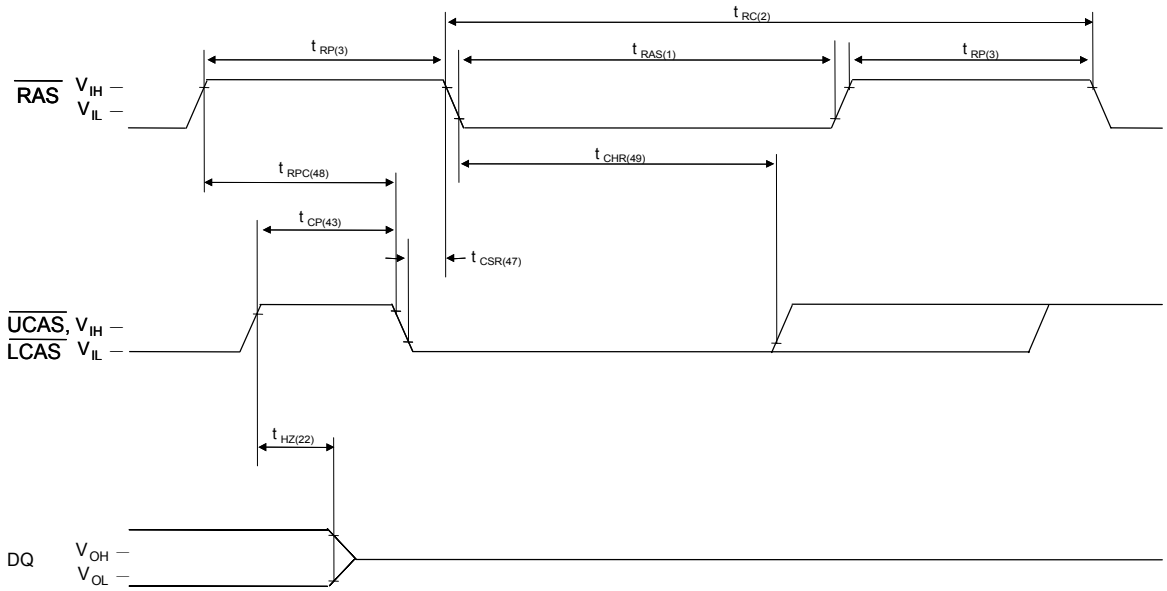
UTRON EDO Mode, X16 (2CAS) Device Timing Diagram

— Waveforms of CAS - before - RAS Refresh Counter Test Cycle



UTRON EDO Mode, X16 (2$\overline{CAS}$) Device Timing Diagram

— Waveforms of $\overline{CAS}$ - before - $\overline{RAS}$ Refresh Cycle

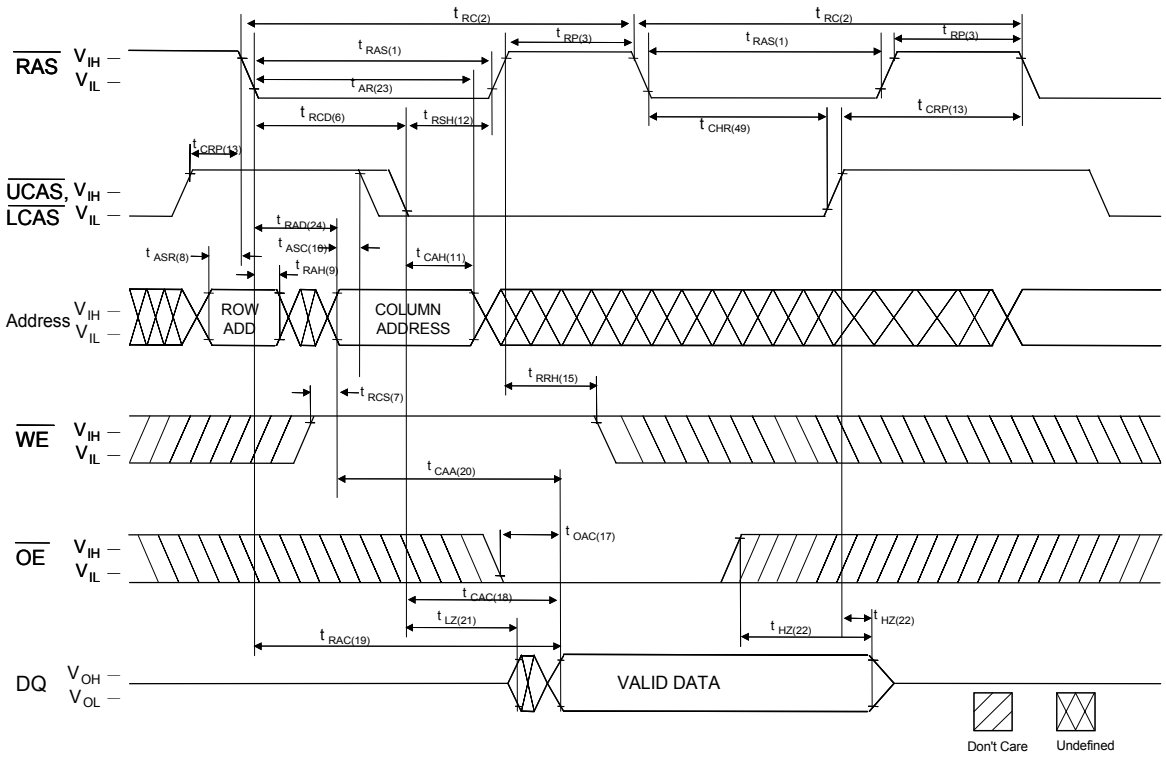


Note: $\overline{WE}$, $\overline{OE}$ = A_0 - A_8 = Don't care

Don't care Undefined

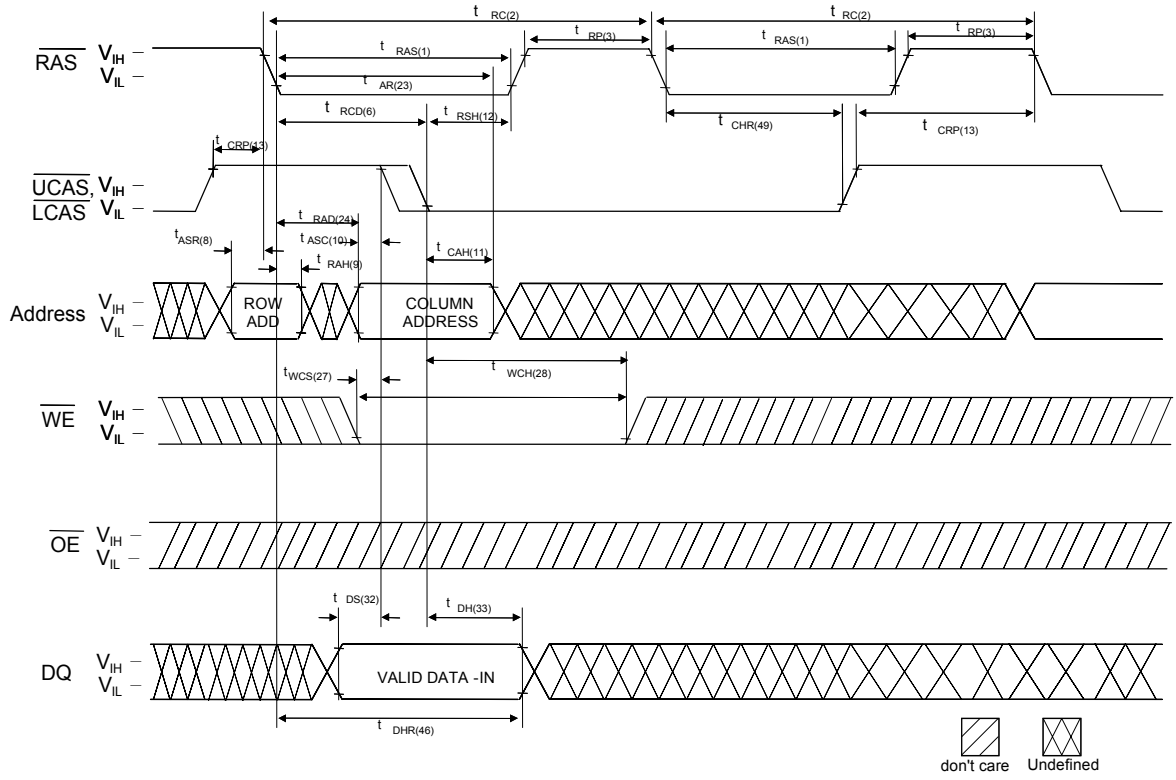
UTRON EDO Mode, X16 (2$\overline{CAS}$) Device Timing Diagram

— Waveforms of Hidden Refresh Cycle (Read)



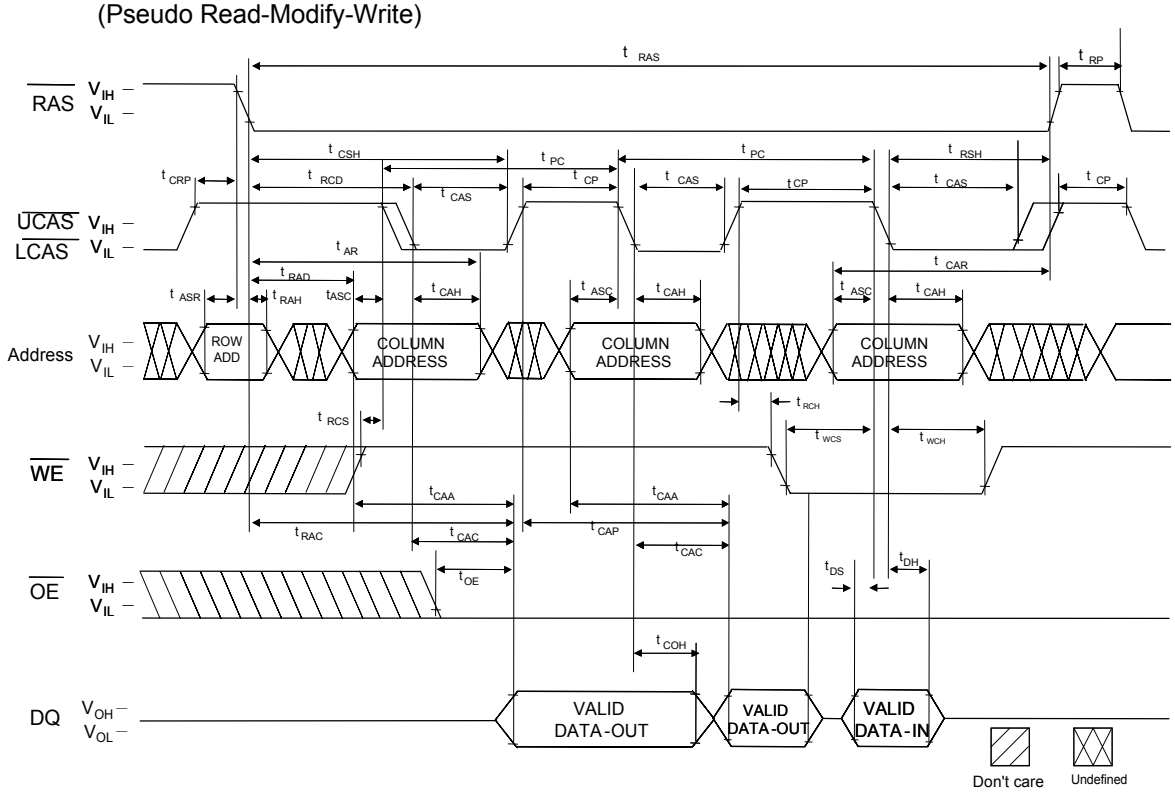
UTRON EDO Mode, X16 (2$\overline{CAS}$) Device Timing Diagram

– Waveforms of Hidden Refresh Cycle (Write)



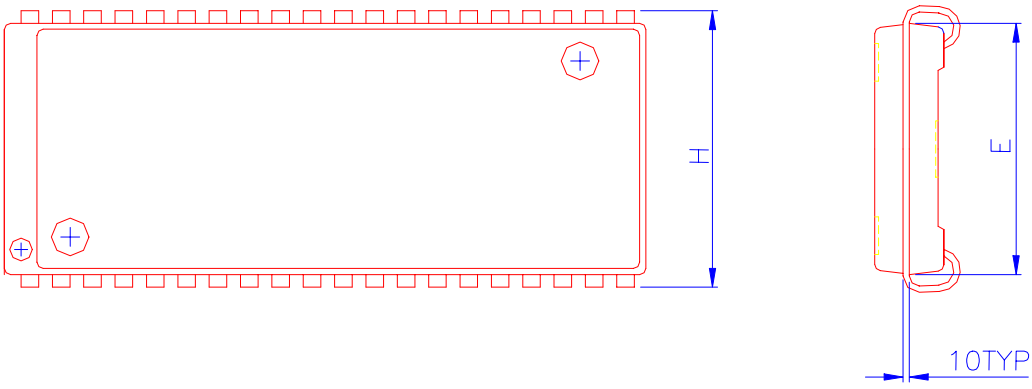
UTRON EDO Mode, X16 (2$\overline{CAS}$) Device Timing Diagram

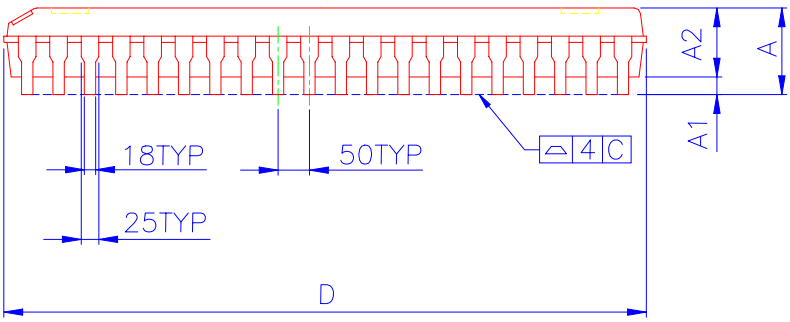
Waveforms of EDO-Page-Mode Read-Early-Write Cycle
(Pseudo Read-Modify-Write)



PACKAGE OUTLINE DIMENSION

40 pin 400mil SOJ Package Outline Dimension

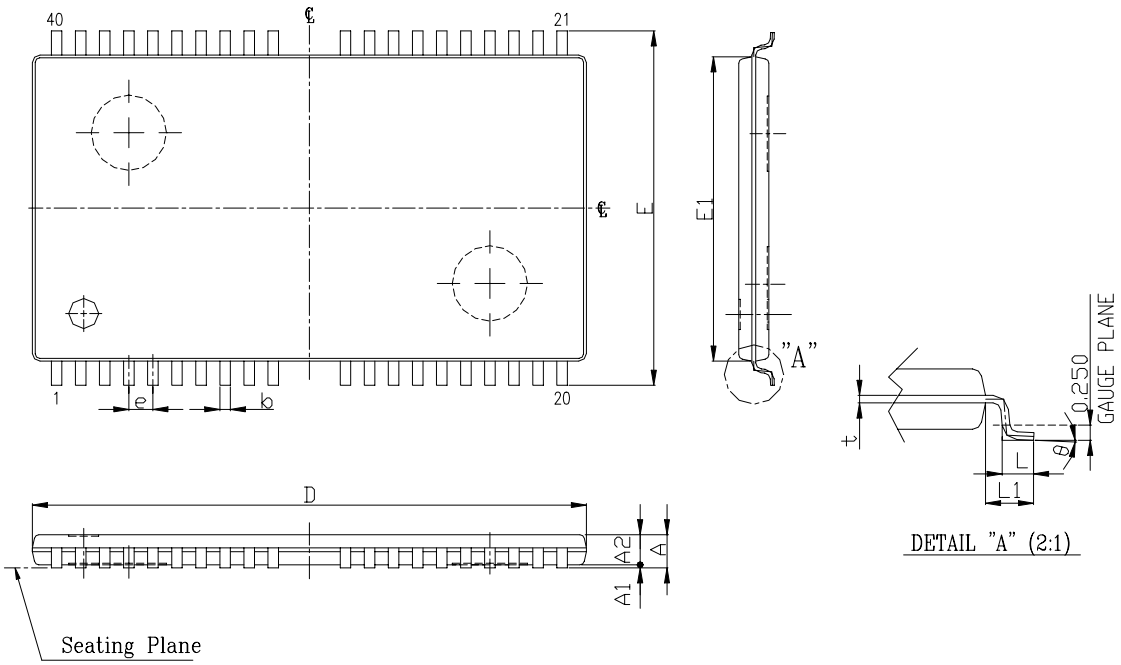




UNIT：MIL

SYMBOLS	MIN.	NOR.	MAX.
A	130	134	138
A1	0.24	-	-
A2	106	110	114
D		1025 BSC.	
E		400 BSC.	
H	430	440	450

40 pin 400mil TSOP-Ⅱ Package Outline Dimension



UNIT / SYMBOL	MM(BASE)
A	1.20(MAX)
A1	0.10± 0.05
A2	1.00± 0.05
b	0.30~0.45
t	0.13(TYP)
D	18.41± 0.10
E1	10.16± 0.10
E	11.76± 0.20
e	0.80(TYP)
L	0.50± 0.10
L1	0.80(REF)
θ	0° ~8°

ORDERING INFORMATION

PART NO.	ACCESS TIME (ns)	PACKAGE
UT51C164JC-25	25	40-PIN SOJ
UT51C164JC-35	35	40-PIN SOJ
UT51C164JC-40	40	40-PIN SOJ
UT51C164JC-50	50	40-PIN SOJ
UT51C164MC-25	25	40-PIN TSOP-II
UT51C164MC-35	35	40-PIN TSOP-II
UT51C164MC-40	40	40-PIN TSOP-II
UT51C164MC-50	50	40-PIN TSOP-II