UT1553 Remote Terminal Multi-Protocol

FEATURES

- Complete MIL-STD-1553 Remote Terminal Interface
- Mode selectable to comply with either MIL-STD-1553A or MIL-STD-1553B bus protocol
- Mil-STD-1773 compatible
- Remote terminal operation is certified by ASD/ ENASC (SEAFAC)
- Implements all dual-redundant Remote Terminal mode codes and operational functions including broadcast commands
- Provides handshake control for quad-redundant systems
- Data pointers permit programmable memory mapping for 1553 data over the entire 64K host memory space
- Provides all handshaking signals for a DMA interface
- Stores 1553 command word and time-tag information with all incoming data for enhanced data management
- Three-state address bus, databus, and control signals simplify DMA operations
- Supports end-of-command activity and data bus error interrupts
- Self-test capability
- Available as a gate array macrocell
- Available in 84-pin pingrid array, 84-lead leadless chip carrier, or 84-lead flatpack packages
- Standard Microcircuit Drawing 5962-88645 available - QML Q compliant

INTRODUCTION

The UT1553 RTMP (figures 1 and 4) is a monolithic, CMOS, VLSI integrated circuit that meets all requirements for a dual-redundant MIL-STD-1553 Remote Terminal interface. The RTMP's advanced design supports both MIL-STD-1553A and MIL-STD-1553B serial data bus protocols, including differences in the status word response time and bit definitions, providing the system designer a single-chip solution to most Remote Terminal interface requirements.

The UT1553 RTMP provides all requisite 1553 protocol and data handling, 1553 message error checking, DMA handshake and control signals, and comprehensive self-test capabilities. The RTMP's pointer-based, programmable memory-mapping architecture permits the host to map 1553 message data anywhere in the 64K memory space. This advanced memory mapping, along with the RTMP's control and status functions, minimize the host system's 1553 interface overhead.

The UT1553 RTMP is a member of UTMC's complete family of high-reliability monolithic MIL-STD-1553 interface products.

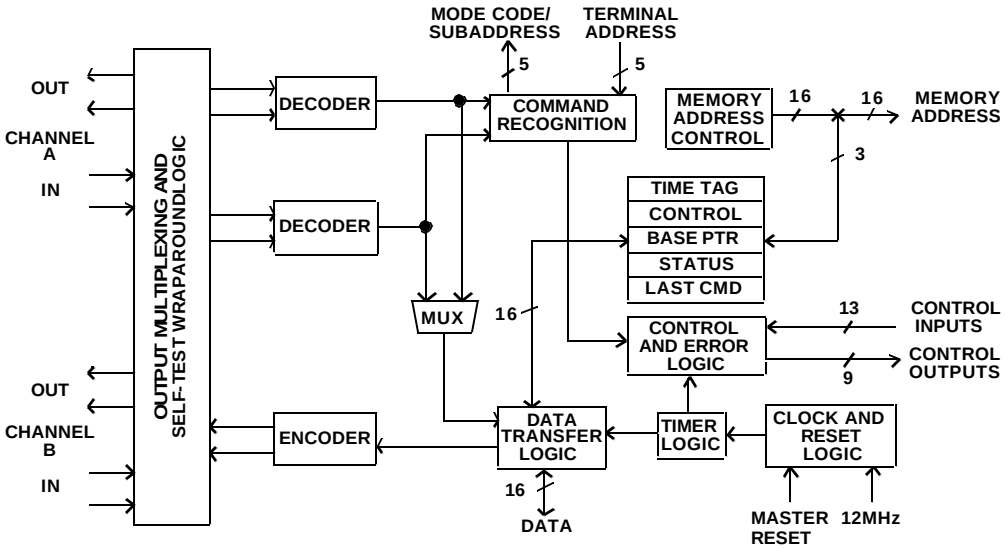

Figure 1. UT1553 RTMP Functional Block Diagram

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FUNCTIONAL DESCRIPTION

General Description

The RTMP is an interface device linking a MIL-STD-1553 serial data bus and a host microprocessor system (figure 2). By selecting the correct state of the 1553 protocol select pin (PRA/B = 1 for 1553A, 0 for 1553B), the system designer can program the RTMP to comply fully with either MIL-STD-1553A or MIL-STD-1553B.

The link between the 1553 data bus and the RTMP is the shared memory area. All the data the RTMP transmits or receives over the 1553 bus is stored in this shared memory area. The RTMP accesses the shared memory with its DMA signals (DMAR, DMAG, and DMAEN), the 16-bit bidirectional data bus (D0-D15), and the 16-bit address bus (A0-A15).

Since the RTMP's architecture is based on a series of data pointers, the 1553 transmit and receive data can be placed anywhere in the 64K memory space, allowing the system designer to optimize memory usage. The system designer can program the RTMP to store the data received over the 1553 bus in one of two ways. The RTMP can store the received data in a single data buffer or in separate buffers. When the RTMP stores the received data in a single buffer, all received data, regardless of subaddress, is stored in contiguous locations in the shared memory. When the RTMP stores the received data in separate buffers, the RTMP stores the data associated with each of the 30 subaddresses in unique locations in memory.

The RTMP has six internal registers that provide the host subsystem with RTMP control and status information. Three of these registers are read/write: Time Tag Data Register (TTD), the Control Register (CTL), and the Base Pointer Data Register (BPD). Two are read only: Operational Status Register (OPS), and the Last Command Register (LCM). The Stop Self-Test Register (SST) is a write-only register. To control the RTMP and the 1553 interface, the host begins by programming the Base Pointer Data Register. By programming the BPD, the system designer tells the RTMP where in the shared memory the 64-word Pointer Block will reside, whether the RTMP will store the 1553 received data in single or separate buffers, and how deep these data buffers will actually be. Figure 3 is a simple representation of the RTMP's memory-mapping architecture.

After the host has programmed the BPD, the 1553 interface is enabled by setting either CHAEN or CHBEN in the RTMP's Control Register. The RTMP now monitors the 1553 data bus for a valid command word or mode code to its particular terminal address. When received, the RTMP looks at the mode bit (single/separate) in the BPD, the 1553 command transmit/receive bit, and the mode code or subaddress portion of the 1553 command to determine which of the address pointers in the 64-word Pointer Block the RTMP will use for this particular memory transaction.

Each memory transaction consists of memory writes for receive command words and memory reads for transmit command words. This process continues until all 1553 data words have been received or transmitted. If the host has enabled any of the RTMP's interrupts, the RTMP asserts them when the memory transaction is complete.

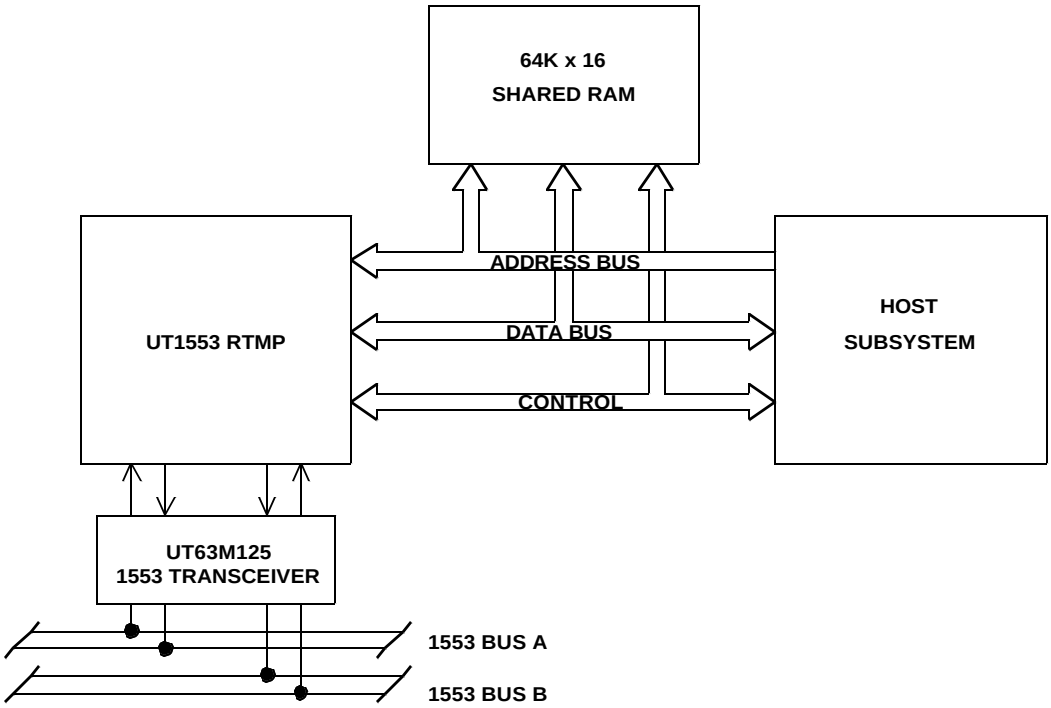


Figure 2. RTMP General System Diagram

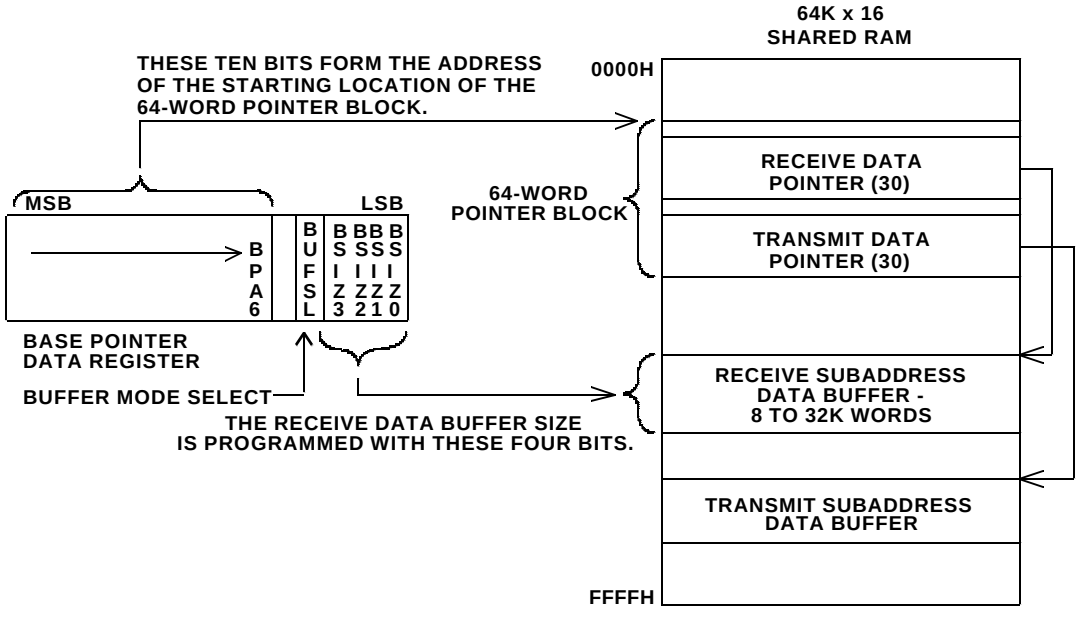


Figure 3. RTMP Receiveand Transmit Data Memory Mapping

2.0 PIN IDENTIFICATION AND DESCRIPTION

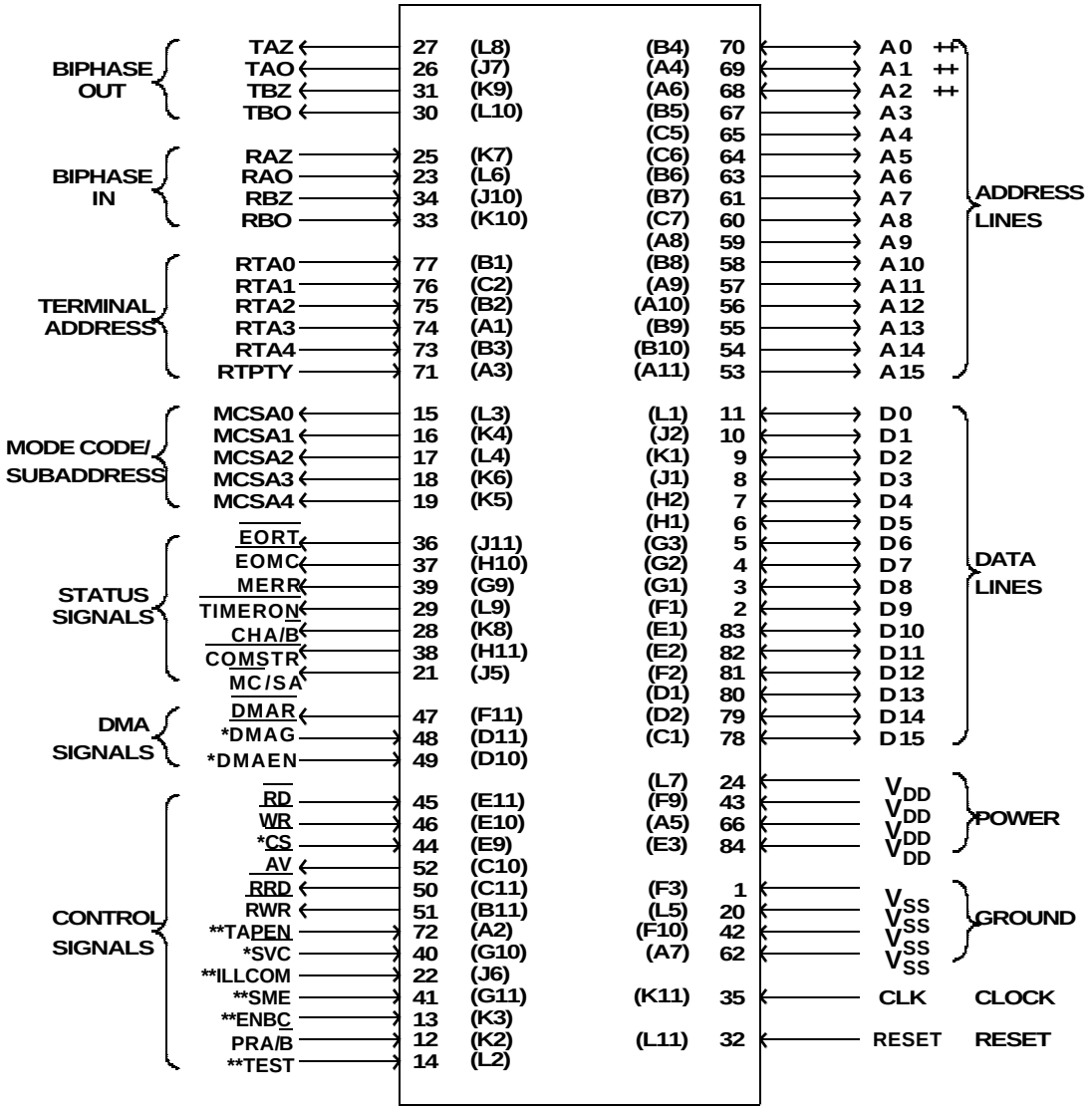


Figure 4. RTMP Functional Pin Description

Legend for TYPE and ACTIVE fields:

TO = TTL output
I = TTL input
TUI = TTL input (pull-up)
TDI = TTL input (pull-down)
TTO = Three-state TTL output
TTB = Three-state TTL bidirectioal
AH =Active high
AL = Active low

DATA BUS

NAME	PIN NUMBER		TYPE	ACTIVE	DESCRIPTION
	LCC	PGA			
D15	78	C1	TTB	–	Bit 15 (MSB) of the bidirectional Data bus.
D14	79	D2	TTB	–	Bit 14 of the bidirectional Data bus.
D13	80	D1	TTB	–	Bit 13 of the bidirectional Data bus.
D12	81	F2	TTB	–	Bit 12 of the bidirectional Data bus.
D11	82	E2	TTB	–	Bit 11 of the bidirectional Data bus.
D10	83	E1	TTB	–	Bit 10 of the bidirectionalData bus.
D9	2	F1	TTB	–	Bit 9 of the bidirectional Data bus.
D8	3	G1	TTB	–	Bit 8 of the bidirectional Data bus.
D7	4	G2	TTB	–	Bit 7 of the bidirectional Data bus.
D6	5	G3	TTB	–	Bit 6 of the bidirectional Data bus.
D5	6	H1	TTB	–	Bit 5 of the bidirectional Data bus.
D4	7	H2	TTB	–	Bit 4 of the bidirectional Data bus.
D3	8	J1	TTB	–	Bit 3 of the bidirectional Data bus.
D2	9	K1	TTB	–	Bit 2 of the bidirectional Data bus.
D1	10	J2	TTB	–	Bit 1 of the bidirectional Data bus.
D0	11	L1	TTB	–	Bit 0 (LSB) of the bidirectional Data bus.

ADDRESS BUS

NAME	PIN NUMBER		TYPE	ACTIVE	DESCRIPTION
	LCC	PGA			
A15	53	A11	TTO	--	Bit 15 (MSB) of the Address bus.
A14	54	B10	TTO	--	Bit 14 of the Address bus.
A13	55	B9	TTO	--	Bit 13 of the Address bus.
A12	56	A10	TTO	--	Bit 12 of the Address bus.
A11	57	A9	TTO	--	Bit 11 of the Address bus.
A10	58	B8	TTO	--	Bit 10 of the Address bus.
A9	59	A8	TTO	--	Bit 9 of the Address bus.
A8	60	C7	TTO	--	Bit 8 of the Address bus.
A7	61	B7	TTO	--	Bit 7 of the Address bus.
A6	63	B6	TTO	--	Bit 6 of the Address bus.
A5	64	C6	TTO	--	Bit 5 of the Address bus.
A4	65	C5	TTO	--	Bit 4 of the Address bus.
A3	67	B5	TTO	--	Bit 3 of the Address bus.
A2	68	A6	TTB	--	Bit 2 of the Address bus. Address bits A2 - A0 are bidirectional so the host can select one of the RTMP's internal registers during internal I/O operations.
A1	69	A4	TTB	--	Bit 1 of the Address Bus. (Reference A2)
A0	70	B4	TTB	--	Bit 0 (LSB) of the Address Bus. (Reference A2)

DMA SIGNALS

NAME	PIN NUMBER		TYPE	ACTIVE	DESCRIPTION
	LCC	PGA			
DMAR	47	F11	TO	AL	DMA Request. Indicates the RTMP is requesting use of the Data bus from the current bus master.
$\overline{\text{DMAG}}$	48	D11	TUI	AL	DMA Grant. Gives control of the Data bus to the RTMP. DMAG is recognized only if DMAEN is high. DMAG must remain asserted until AV goes high to ensure that the RTMP completes the current DMA cycle.
DMAEN	49	D10	TUI	AH	DMA Enable. When high, this input allows the RTMP to recognize DMAG. When low, DMAEN places all three-state pins in a high-impedance state and disables the RTMP's memory access cycle.

CONTROL SIGNALS

NAME	PIN NUMBER		TYPE	ACTIVE	DESCRIPTION
	LCC	PGA			
CS	44	E9	TUI	AL	Chip Select. This input, along with RD and WR, allows the host to access the RTMP's internal data registers.
$\overline{RD}$	45	E11	TI	AL	Read. When used in conjunction with $\overline{CS}$, $\overline{RD}$ allows the RTMP to place data from the selected internal register on the Data bus (D15-D0).
$\overline{WR}$	46	E10	TI	AL	Write. When used in conjunction with $\overline{CS}$, $\overline{WR}$ latches data from the Data bus (D15-D0) into the selected RTMP internal register.
$\overline{AV}$	52	C10	TTO	AL	Address Valid. The RTMP asserts $\overline{AV}$ to indicate that the address (A15-A0) is valid.
$\overline{RRD}$	50	C11	TTO	AL	RAM Read. The RTMP asserts $\overline{RRD}$ during DMA cycles that require data from system RAM.
$\overline{RWR}$	51	B11	TTO	AL	RAM Write. The RTMP asserts $\overline{RWR}$ during DMA cycles to write data to system memory.
$\overline{SVC}$	40	G10	TUI	AL	Superseding Valid Command. The host system uses this input when more than one RT is present in the system; i.e., a quad-redundant system. When asserted, this input causes the RTMP to terminate all present activity and perform an internal reset of encoders/decoders, RT state machine, and DMA state machine. Registers are not affected. Do not assert while DMAR is asserted (tpw 250ns minimum).
SME	41	G11	TDI	AH	Set Message Error. Asserting this input causes the Message Error bit in thestatus word to be set.
ILLCOM	22	J6	TDI	AH	Illegal Command. This input illegalizes a command word that the RTMP accepts but the system does not support. When set, the RTMP responds with the Message Error bit set in the status word. ILLCOM is used in conjunction with the Mode Code/ Subaddress outputs.
PRA/$\overline{B}$	12	K2	TI	--	Program A/$\overline{B}$. This input is the 1553 mode select input. A high input places the RTMP in the MIL-STD-1553A mode; a low places the RTMP in the MIL-STD-1553B mode.
ENBC	13	K3	TDI	AH	Enable Broadcast. A high on this input, when the RTMP is in the 1553B mode, allows the RTMP to recognize a broadcast command word.
TEST	14	L2	TDI	AH	Test. The TEST input pin allows the user to select between internal (TEST = 0) or external (TEST = 1) self-test. When TEST equals a logic one and DMAEN equals a logic zero, MCSA (4:0) and MC/SA three-state.

STATUS SIGNALS

NAME	PIN NUMBER LCC	PIN NUMBER PGA	TYPE	ACTIVE	DESCRIPTION
EORT	36	J11	TTO	AL	End of Receive/Transmit. This interrupt is a pulse that is maskable by writing to the Control Register. The user can select EORT to occur at the end of receive command activity, at the end of transmit command activity, under either of these conditions, or disable it completely. The EORT output is designed to simulate an open-collector output and requires a pull-up resistor. (250ns pulse width). This signal is not generated if a message error condition exists.
$\overline{\text{EOMC}}$	37	H10	TTO	AL	End of Mode Code. this non-maskable interrupt is a pulse that occurs at the end of all memory accesses associated with any mode code command. The EOMC output is designed to simulate an open-collector output and requires a pull-up resistor. EOMC and EORT can be logically ORed together to form a composite interrupt. The 250ns pulse width is generated after command word is stored. This signal is not generated if a message error condition exists.
$\overline{\text{COMSTR}}$	38	H11	TO	AL	Command Strobe. This low-going pulse identifies receipt of a valid 1553 command word.
MERR	39	G9	TO	AH	Message Error. Active when the RTMP detects an error in the 1553 transmission and sets the Message Error bit in the status word. MERR is reset when the RTMP receives the next valid command word. (COMSTR assertion)
CHA/$\overline{\text{B}}$	28	K8	TO	--	Channel A/$\overline{\text{B}}$. When high, this output indicates the RTMP received the last command on Channel A; when low, the last command was received on Channel B.
$\overline{\text{TIMERON}}$	29	L9	TO	AL	Timer On. Indicates the RTMP is transmitting data. The output remains active until the data transmission is complete or the internal fail-safe timer times out (600ms for 1553A and 800ms for 1553B). The RTMP internally disables both transmitters and keeps them disabled until the RTMP receives a valid command word. This signal is asserted approximately 250ns before beginning of status word transmission.

MODE CODE/SUBADDRESS

NAME	PIN NUMBER LCC	PIN NUMBER PGA	TYPE	ACTIVE	DESCRIPTION
$\overline{\text{MC}}$/SA	21	J5	TTO	AL	Mode Code/Subaddress. MC/SA = 0 indicates that the MCSAO-MCSA4 pins contain the Mode Code bits of the most recently received mode code. MC/SA = 1 indicates that MCSA0-MCSA4 pins contain the Subaddress bits of the most recently received command word.
MCSA0 MCSA1 MCSA2 MCSA3 MCSA4	15 16 17 18 19	L3 K4 L4 K6 K5	TTO	--	Mode Code/Subaddress. These five bits are used in conjunction with the MC/SA output. MC/SA = 0 indicates that these five bits are the five least significant bits of the mode code command word. MC/SA = 1 indicates these five bits are the 1553 command word subaddress.

REMOTE TERMINAL ADDRESS

NAME	PIN NUMBER		TYPE	ACTIVE	DESCRIPTION
	LCC	PGA			
RTA4 RTA3 RTA2 RTA1 RTA0	73 74 75 76 77	B3 A1 B2 C2 B1	TI	--	Remote Terminal Address Inputs. The RTMP uses these inputs to select the terminal address for this specific remote terminal.
TAPEN	72	A2	TDI	AH	Terminal Address Parity Enable. Enables the RTMP's Terminal Address parity-checking function.
RTPTY	71	A3	TI	--	Remote Terminal Parity. When the Terminal Address parity-checking function is enabled (TAPEN = 1), RTPTY must provide odd parity for the terminal address input pins (RTA4-RTA0).

MASTER RESET AND CLOCK

NAME	PIN NUMBER		TYPE	ACTIVE	DESCRIPTION
	LCC	PGA			
$\overline{\text{RESET}}$	32	L11	TI	AL	Reset. Initializes all internal functions of the RTMP. RESET must be asserted before normal RTMP operation.
CLK	35	K11	TI	--	Clock. The clock input requires a 50%± 10% duty cycle with an accuracy of 12MHz ± 0.01%.

CHANNEL A BIPHASE SIGNALS

NAME	PIN NUMBER		TYPE	ACTIVE	DESCRIPTION
	LCC	PGA			
RAO	23	L6	TI	--	Receiver (Channel) A One. Manchester input from the 1553 bus receiver.
RAZ	25	K7	TI	--	Receiver (Channel) A Zero. This input is the complement of RAO.
TAO	26	J7	TO	--	Transmitter (Channel) A One. This Manchester-encoded data output is connected to the 1553 bus transmitter input. The output is idle low.
TAZ	27	L8	TO	--	Transmitter (Channel) A Zero. This output is the complement of TAO. The output is idle low.

CHANNEL B BIPHASE SIGNALS

NAME	PIN NUMBER		TYPE	ACTIVE	DESCRIPTION
	LCC	PGA			
RBO	33	K10	TI	--	Receiver (Channel) B One. Manchester data input from the 1553 bus receiver.
RBZ	34	J10	TI	--	Receiver (Channel) B Zero. This input is the complement of RBO.
TBO	30	L10	TO	--	Transmitter (Channel) B One. This Manchester-encoded output is connected to the 1553 bus transmitter input. The output is idle low.
TBZ	31	K9	TO	--	Transmitter (Channel) B Zero. This output is the complement of TBO. The output isidle low.

POWER AND GROUND

NAME	PIN NUMBER		TYPE	ACTIVE	DESCRIPTION
	LCC	PGA			
V_{DD}	24 43 66 84	L7 F9 A5 E3	--	--	+5 V_{DC} Power. Power supply input must be
V_{SS}	1 20 42 62	F3 L5 F10 A7	--	--	Reference Ground. Zero V_{DC} logic ground.

3.0 REMOTE TERMINAL ARCHITECTURE

3.1 Internal Registers

The RTMP has six internal registers that allow the host to control the RTMP's actions and also to obtain its operational status. The host can read from or write to three of these registers: the Time Tag Data Register (TTD), the Control Register (CTL), and the Base Pointer Data Register (BPD). Two of the registers are read-only: the Operational Status Register (OPS), and the Last Command Register (LCM). The Stop Self-Test Register (SST) is a write-only register.

Six signals allow the host to access the RTMP's internal registers. Three of the six signals are control signals: Chip Select (CS), Read (RD), and Write (WR). The other three signals are the RTMP's bidirectional address lines, A0 - A2. When the CS = 0, the three least significant address lines, A0 - A2, become inputs to the RTMP. The RTMP decodes these three address lines, along with CS, RD, and WR, to determine which of the six internal registers the host is attempting to access. Table 1 shows the addresses for the RTMP's internal registers for read and write operations.

3.2 Read/Write Registers

The RTMP has three internal read/write registers. These three registers are:

- The Time Tag Data Register
- The Control Register
- The Base Pointer Data Register

Time Tag Data Register (TTD)

The TTD contains a free-running, 16-bit, ripple counter. The Time Tag clock has a resolution of 64ms. The TTD is initialized to 0000H when the host asserts the RESET input. All TTD bits are programmable by performing a write to the TTD with the desired bit pattern.

The RTMP stores the TTD's value in the shared memory area at the end of each 1553 receive message. The host can also directly read the TTD. Since the TTD is a free-running counter, the host may read the TTD while the counter is rippling, resulting in the host reading erroneous data. If this situation presents a problem, the host should read the TTD data twice. Figure 5 represents the TTD. (0000H after Master Reset.)

Table 1. RTMP Internal Register Addresses

1. RTMP Register Write Addresses

$\overline{CS}$	$\overline{WR}$	A2	A1	A0	
0	0	0	0	0	Time Tag Data Register
0	0	0	0	1	Control Register
0	0	0	1	0	Base Pointer Data Register
0	0	0	1	1	Stop Self-Test Register
0	0	1	X	X	Don't Care

2. RTMP Register Read Addresses

$\overline{CS}$	$\overline{RD}$	A2	A1	A0	
0	0	0	0	0	Time Tag Data Register
0	0	0	0	1	Control Register
0	0	0	1	0	Base Pointer Data Register
0	0	0	1	1	Operational Status Register
0	0	1	0	0	Last 1553 Command Register
0	0	1	0	1	Don't Care
0	0	1	1	0	Don't Care
0	0	1	1	1	Don't Care

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CNT15	CNT14	CNT13	CNT12	CNT11	CNT10	CNT9	CNT8	CNT7	CNT6	CNT5	CNT4	CNT3	CNT2	CNT1	CNT0

MSB LSB

Figure 5. The Time Tag Data Register

3.4 Control Register (CTL)

The CTL provides the host with the ability to control four functions: (1) programming the bits in 1553 status word; (2) masking the End of Receive/Transmit message activity interrupt (output pin EORT); (3) enabling and selecting the channel for the self-test; and (4) selecting the active 1553 channel. The definition of the 1553 status word bits in the CTL is different when the RTMP is operating in the 1553A mode (PRA/B = 1) as opposed to the1553B mode (PRA/B = 0). Figure 6 shows the bit definitions in the CTL for the 1553A mode; figure 7 shows the definition for the 1553B mode.

The host determines the CTL functions status by reading the CTL Register.

CTL Bit Definitions - 1553A Mode

Bit 15	CHAEN [0]	Channel A Enable. When CHAEN = 1, the RTMP responds to a 1553 command word or mode code on bus Channel A. CHAEN = 0 disables the RTMP from responding to 1553 command word or mode code on 1553 bus Channel A.
Bit 14	CHBEN [0]	Channel B Enable. When CHBEN = 1, the RTMP responds to a 1553 command word or mode code on bus Channel B. CHBEN = 0 disables the RTMP from responding to 1553 command word or mode code on 1553 bus Channel B. Disable for internal self-test.
Bit 13	STEN [0]	Self-Test Enable. STEN enables the RTMP's internal self-test.
Bit 12	STCS [0]	Self-Test Channel Select. If the host has enabled an RTMP self-test (STEN = 1), STCS selects the RTMP receiver channel to test. STCS = 1 selects Channel A, and STCS = 0 selects Channel B.
Bit 11	IM1 [0]	Interrupt Mask One. If IM1 = 1, the $\overline{\text{EORT}}$ interrupt output is active at the end of 1553 receive command memory activity. IM1 = 0 masks this interrupt function.
Bit 10	IM2 [0]	Interrupt Mask Two. If IM2 = 1, the $\overline{\text{EORT}}$ interrupt output is active at the end of 1553 transmit command memory activity. IM2 = 0 masks this interrupt function.
Bit 9	SWB10 [0]	Status Word Bit 10. When the host sets this bit, SWB10 = 1, the bit in the RTMP's status word that is transmitted during bit time ten is set (see figure 30 for status word bit time definitions). The bits in the status word are system-defined in MIL-STD-1553A.
Bit 8	SWB11 [0]	Status Word Bit 11. When the host sets this bit (SWB11 = 1), the bit in the RTMP's status word transmitted during bit time 11 is set.
Bit 7	SWB12 [0]	Status Word Bit 12. When the host sets this bit (SWB12 = 1), the bit in the RTMP's status word transmitted during bit time 12 is set.
Bit 6	SWB13 [0]	Status Word Bit 13. When the host sets this bit (SWB13 = 1), the bit in the RTMP's status word transmitted during bit time 13 is set.
Bit 5	SWB14 [0]	Status Word Bit 14. When the host sets this bit (SWB14 = 1), the bit in the RTMP's status word transmitted during bit time 14 is set.
Bit 4	SWB15 [0]	Status Word Bit 15. When the host sets this bit (SWB15 = 1), the bit in the RTMP's status word transmitted during bit time 15 is set.
Bit 3	SWB16 [0]	Status Word Bit 16. When the host sets this bit (SWB16 = 1), the bit in the RTMP's status word transmitted during bit time 16 is set.
Bit 2	SWB17 [0]	Status Word Bit 17. When the host sets this bit (SWB17 = 1), the bit in the RTMP's status word transmitted during bit time 17 is set.
Bit 1	SWB8 [0]	Status Word Bit 18. When the host sets this bit (SWB18 = 1), the bit in the RTMP's status word transmitted during bit time 18 is set.
Bit 0	TFLG	Terminal Flag. TFLG = 1 sets the Terminal Flag bit in the 1553A status word. TFLG = 0 resets the Terminal Flag bit in the 1553A status word.

CTL Bit Definitions - 1553B Mode

Bit 15	CHAEN [0]	Channel A Enable. Same as 1553A mode. Disable for internal self-test.
Bit 14	CHBEN [0]	Channel B Enable. Same as 1533A mode. Disable for internal self-test.
Bit 13	STEN [0]	Self-Test Enable. Same as 1553A mode.
Bit 12	STCS [0]	Self-Test Channel Select. Same as 1553A mode.
Bit 11	IM1 [0]	Interrupt Mask One. Same as 1553A mode.
Bit 10	IM2 [0]	Interrupt Mask Two. Same as 1553A mode.
Bit 9	INSTR [0]	Instrumentation Bit. When INSTR = 1, the RTMP's 1553 status word response has the Instrumentation bit set. This bit remains set until INSTR is set to 0.
Bit 8	SVREQ [0]	Service Request Bit. When SVREQ = 1, the RTMP's 1553 status word response has the Service Request bit set. This bit remains set until SVREQ is set to 0.
Bit 7	N/A	This bit is defined as a reserved bit in MIL-STD-1553B and is not used. Setting this bit has no effect on the status word response.
Bit 6	N/A	Same as bit 7.
Bit 5	N/A	Same as bit 7.
Bit 4	BDCST [0]	Broadcast Bit. When BDCST = 1, the RTMP's 1553 status word response has the Broadcast bit set. Manual override; not cleared by receipt of next command. Broadcast bit in outgoing status word is set to a logical one on the receipt of broadcast command.
Bit 3	BUSY [0]	Busy Bit. When BUSY = 1, the RTMP's 1553 status word response has the Busy bit set. This bit remains set until is set to 0.
Bit 2	SFLG [0]	Subsystem Flag. When SFLG = 1, the RTMP's 1553 status word response has the Subsystem Flag bit set. This bit remains set until SFLG is set to 0.
Bit 1	N/A	Same as bit 7.
Bit 0	TFLG [0]	Terminal Flag. Same as 1553A mode.

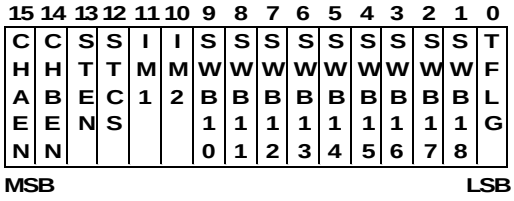


Figure 6. The Control Register in 1553A Mode

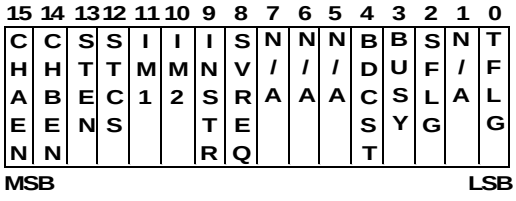


Figure 7. The Control Register in 1553B Mode

3.5 Base Pointer Data Register

The BPD provides three types of information: (1) the location in memory for the 64-word Pointer Block; (2) the receive-data storage-buffer select for either single or separate data buffers; and (3) the size or depth of the single or separate data buffers (figure 8). (0000H after Master Reset.)

BPD Bit Definitions

Bit 15-	BPA15-BPA 6	Block Pointer Address. These ten bits provide the RTMP with the Bit 6 ten most significant address lines for the location, within the 64K word addressing range, of the 64-word Pointer Block.
Bit 5	N/A	This bit is not used.
Bit 4	BUFSL	Buffer Select. When BUFSL = 1, the host selects the RTMP's single buffer mode of storing 1553 receive data. If BUFSL = 0, the host selects the separate buffer mode of storing 1553 receive data.
Bit 3-	BSIZ3-BSIZ0	Buffer Size Select. These four bits select the size of the receive data Bit 0 buffers and can range from 3 (0011B) to 15 (1111B). The actual size of the data buffer is equal to 2^X where X is the decimal equivalent of BSIZ3-BSIZ0. The size of the data buffers can range from eight (2^3) words to 32K (2^{15}) words. The variable X is not defined for zero through two.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BPA15	BPA14	BPA13	BPA12	BPA11	BPA10	BPA9	BPA8	BPA7	BPA6	N/A	BUFSL	BSIZ3	BSIZ2	BSIZ1	BSIZ0
MSB															LSB

Figure 8. The Base Pointer Data Register

3.6 Read Only Registers

The RTMP has two internal registers that are read-only. These two registers provide status information on the operation of the RTMP:

- The Operational Status Register
- The Last 1553 Command Register

3.6.1 Operational Status Register (OPS)

The OPS provides the host with the operational status of the RTMP while the RTMP is active. Figure 9 shows the information bits stored in the OPS.

OPS Bit Definitions

Bit 15	MACT [0]	Message Active. MACT = 1 indicates that the RTMP is actively processing a message. The RTMP clears MACT upon completing the message.
Bit 14	VMPRO [0]	Valid Message Processed. VMPRO = 1 indicates that the RTMP has processed a valid 1553 message. The host clears VMPRO bit when the OPS is read.
Bit 13	ME [0]	Message Error. ME = 1 indicates that a 1553 message error has occurred. The host clears ME when the OPS is read *unless* the condition that caused the MERR still persists after the register read.
Bit 12	PE [X]	Parity Error. PE = 0 indicates that the RTMP has detected an error in the Terminal Address parity. This bit can only be active when TAPEN = 1.
Bit 11	STACT [0]	Self-Test Active. STACT = 1 indicates that the RTMP is performing a built-in self-test.
Bit 10	BDCEN [X]	Broadcast Enable. BDCEN = 1 indicates that the RTMP will accept a 1553 broadcast command as a valid command.
Bit 9	TFGEN [1]	Terminal Flag Enable. When the RTMP is in the 1553B mode, TFGEN = indicates that the Terminal Flag option is set. Mode code 00110 (Inhibit Terminal Flag) will clear this bit.
Bit 8	CHAEN [0]	1553 Channel A Enable. CHAEN = 1 indicates that Channel A is enabled and ready to process 1553 bus messages.
Bit 7	CHBEN [0]	1553 Channel B Enable. CHBEN = 1 indicates that Channel B is enabled and ready to process 1553 bus messages.
Bit 6	MSEL [X]	Mode Select. When MSEL = 1, the RTMP is in the 1553A mode of operation. MSEL = 0 indicates the RTMP is in the 1553B mode of operation.
Bit 5	MDRCV [0]	Mode Received. MDRCV = 0 indicates that the last valid 1553 command the RTMP received was a mode command.
Bit 4	XMTAC [0]	Transmitter Active. XMTAC = 1 indicates that the RTMP's transmitter is transmitting data.
Bit 3	ILCMD [X]	Illegal Command. ILCMD = 1 indicates that the last 1553 command the RTMP received was illegal. ILCMD is cleared when the host reads the OPS. In 1553A mode, this bit reflects input pin ILLCOM. In 1553B mode, this bit reflects either input pin ILLCOM or internal hardware. Internal illegalization is reviewed in table 2.
Bit 2	CHA/$\overline{B}$ [0]	Channel A or . CHA/$\overline{B}$ = 1 indicates that the last valid 1553 command word the RTMP received was on Channel A. CHA/B = 0 indicates that the last valid command word was on Channel B.
Bit 1	VCMD [0]	Valid 1553 Command. VCMD = 1 indicates that the last command word the RTMP received was valid. VCMD is reset when the host reads the OPS.
Bit 0	OE [0]	Overrun Error (Framing Error). OE = 1 indicates that the RTMP has detected an overrun error. This bit is reset when the host performs an OPS read *unless* the error condition persists.

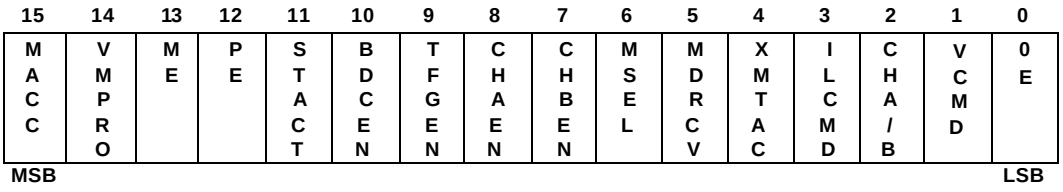


Figure 9. The Operational Status Register

3.6.2 Last 1553 Command Register (LCM)

The RTMP stores the last valid 1553 command word it received in the LCM. The only exception is if the RTMP is in the 1553B mode and it receives a Transmit Last Command Word mode code. Figure 10 shows the configuration of the LCM. (0410H after Master Reset.)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TA4	TA3	TA2	TA1	TA0	T/R	SA4	SA3	SA2	SA1	SA0	WC4	WC3	WC2	WC1	WC0
MSB															LSB

3.7 Write Only Register

The RTMP has one register that is write only. This register is the Stop Self-Test Register (SST). The host can terminate the RTMP's self-test execution by writing to the SST. When the host performs a write to the SST, the RTMP terminates all memory activity. The Self-Test Enable (STEN) bit in the CTL is also reset, and the Self-Test Active (STACT) bit in the OPS is reset. When writing to the SST, the 16-bit data word is a Don't Care.

4.0 REMOTE TERMINAL INTERFACE OPERATION

The RTMP's remote terminal interface is based on a shared memory concept where the shared memory is the link between the MIL-STD-1553 data bus and the host subsystem (figure 11). All 1553 data, whether transmitted or received, must at one time be stored in this defined memory area. The RTMP accesses the shared memory area with a conventional Direct Memory Access (DMA) interface.

Since the RTMP can access data anywhere within the 64K memory space, the host has to specify exactly where in memory the data associated with each valid transmit or receive command word or mode code is located. The host specifies the 1553 data area locations by programming the RTMP's Base Pointer Data Register (BPD) and by initializing the 64-word Pointer Block. The BPD tells the RTMP where in memory the Pointer Block is located. The Pointer Block in turn specifies the location in memory where the data associated with each valid command word or mode code resides.

Therefore, to control the RTMP's operation, the host first programs the BPD to provide the RTMP with three essential pieces of information: (1) the location in memory of the 64-word Pointer Block; (2) the type of data buffer -- single or separate; and (3) the receive data buffer size. The host can update the Base Pointer Data Register if a new 64-word Pointer Block needs to be selected, but *do not* update the BPD while the RTMP is processing a message transaction. Figure 8 shows the BPD.

4.1 Programming the BPD

The host programs the ten most significant bits of the BPD (BPA15 - BPA6) to point to the starting address of the 64-word Pointer Block within the RTMP's 64K address space. The RTMP generates the least significant six address lines to determine which of the words within the 64-word Pointer Block to use for a specific 1553 transmission. The RTMP does this by detecting the T/R bit and the subaddress bits of the last 1553 command word (figure 12). Usually the six least significant address lines, BPA5-BPA0, are part of the T/R bit and subaddress or mode code bits of the last command word, respectively. In some cases, BPA5-BPA0 are forced to specific values: (1) when the RTMP stores the command word on the data buffer; (2) when the single buffer mode of operation is chosen; and (3) when a mode code is received.

The Data Buffer Mode bit, BUFSL, is the next bit in the BPD that the host programs. The state of BUFSL determines whether the RTMP stores the 1553 receive data in a single data buffer (BUFSL = 1) or in separate data buffers (BUFSL = 0).

Finally, the host programs bits BSIZ3-BSIZ0 in the BPD to tell the RTMP how large to make the separate data buffers. A formula determines the size of the data buffer(s): take the decimal equivalent of the binary number represented by BSIZ3-BSIZ0, where BSIZ3 is the MSB. This number, represented by X, can range in size from three to fifteen. The actual size of the data buffers is equal to 2^X. This means the data buffers can range from 8 to 32K words in length. In the single buffer mode, bits BSIZ3-BSIZ0 determine the size of this single buffer. In the separate buffer mode, *all* data buffers are the *same* size. This means the system designer must program the buffer size so the *largest* possible message the RTMP can receive over the 1553 bus fits within the programmed buffer size.

4.2 RTMP Pointer Block

The RTMP's Pointer Block is a contiguous block of 64, 16-bit words. The RTMP uses this block of data as the actual address pointer locations for the memory accesses associated with each 1553 message transaction. Therefore, the Pointer Block is divided into receive data pointers, of which one location is for the single buffer mode, transmit data pointers, a mode code command pointer location, and a location for the current 1553 command word (figure 13). The host must initialize the Pointer Block *before* enabling the RTMP's 1553 receivers

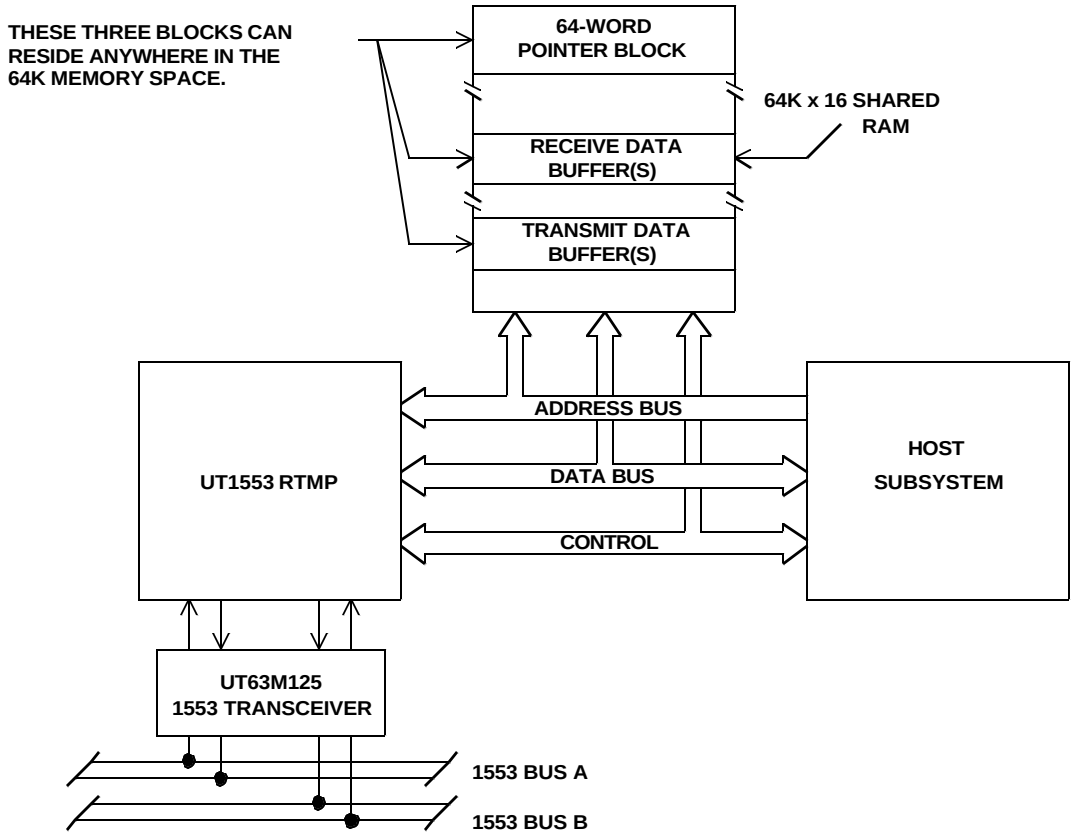


Figure 11. The Memory Link between the RTMP and the Host Subsystem

The host can program the 16-bit pointer addresses that make up the Pointer Block to point to any memory location in the RTMP's 64K memory space. In this respect, the host has total flexibility to determine where in RAM it stores the actual transmit, receive, and mode code data. The RTMP's data storage flexibility allows the host to buffer 1553 receive messages and maintain data integrity.

The host can update the pointer data within the Pointer Block at any time, but the recommended procedure is for the host *not* to update the pointer data for 1553 receive command data while the RTMP is actively processing a message. To prevent this action, the host can program the RTMP to generate an end-of-activity interrupt for every valid 1553 message with associated data words. In addition, the host can read the Operational Status Register to determine if the RTMP is active.

The RTMP uses the present 1553 command word and the selected mode of operation, single or separate mode, to determine which pointer within the 64-word Pointer Block to use as an address pointer for the memory accesses during 1553 message activity. The 1553 command word T/R Bit and the subaddress bits, or the mode code bits for a mode command, specify the exact location of the address pointer in the Pointer Block for transmit, receive, and mode code command words. If the host has selected the single mode of operation, the RTMP forces selection of the address pointer stored in the single mode location for all receive commands. The RTMP stores the present command word in the first

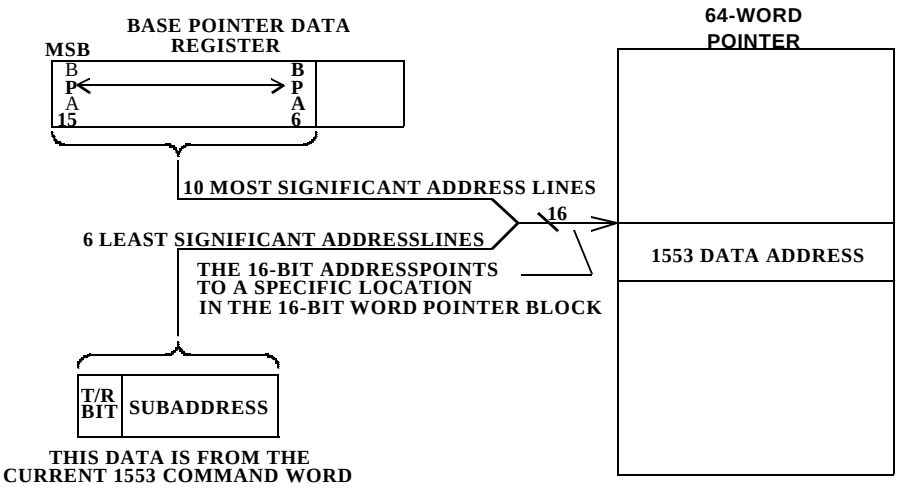


Figure 12. Constructionof the Block Pointer Address (BPA) Bits

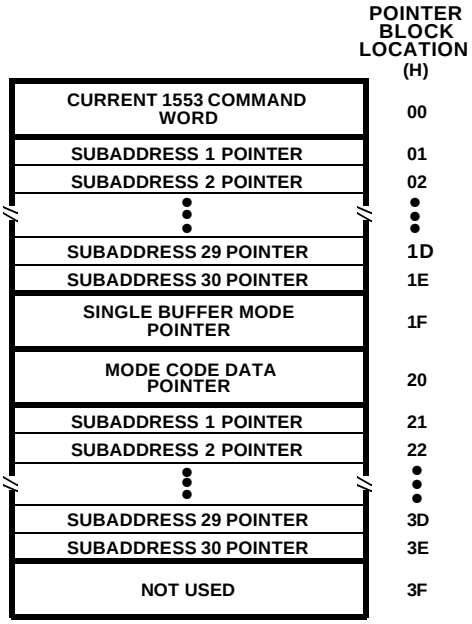


Figure 13. The 64-Word Pointer Block

4.3 Pointer Block Location Definitions

For the following description of the Pointer Block locations, please refer to figure 13.

Command Word Data - Location 0-0H of the Pointer Block contains the last valid 1553 command word the RTMP received. Bit times 4 through 19 (figure 14) of the 1553 command word are stored in bit positions 15 through 0, respectively. The RTMP updates this location with the most recent command word except when the RTMP is in the 1553B mode and it receives a Transmit Last Command mode code.

Separate Mode, Receive Data Pointers - Pointer Block address locations 1-30 (01H-1EH) contain the pointer values for each receive command word subaddress if the RTMP is operating in the separate mode (Bit 4 of the BPD = 0). The RTMP selects the address pointer data from one of these locations by using the subaddress of the most recent receive command word. The RTMP internally stores this pointer value. This stored pointer value points to the memory location where the RTMP stores the received data associated with this subaddress. After the RTMP has stored all data associated with this subaddress in memory, the RTMP stores the updated pointer value back into the selected location in the Pointer Block. The updated pointer value points to the next available location in memory.

Single Mode, Data Pointer - When the host selects the single mode of operation (bit 4 of the BPD = 1), the pointer value at location 31 (1FH) of the Pointer Block is the address the RTMP uses to store *all* 1553 receive data, regardless of the command word's subaddress. After the RTMP has stored all data associated with a 1553 receive command word, the RTMP stores an updated pointer value back into location 31 of the Pointer Block. The updated pointer value points to the next available location in memory.

Mode Code Pointer - The RTMP uses the pointer value stored in location 32 (20H) of the Pointer Block when it recognizes a valid mode code command with an associated data word. A mode code with data word is only valid when the RTMP is operating in the 1553B mode. When the RTMP is operating in the 1553A mode, it does not recognize or process any mode code with an associated data word.

- 1553A mode: No mode codes with data word allowed.
- 1553A mode: $\overline{MC}$/SA field = 00000 or 11111 is a mode code.
- 1553B mode: $\overline{MC}$/SA field = 00000 or 11111 is a mode code.

The RTMP stores the pointer value from location 32 internally. The RTMP uses bits 15-4 of this pointer value to point to a memory location of a data block containing the data words associated with each mode code. Bits 3-0 of the pointer address are the four least significant bits of the mode code the RTMP received. These four bits specify the data word within this data block that the RTMP uses for this specific mode code. Figure 15 shows how the RTMP handles mode codes with associated data words.

Transmit Data Pointers - Pointer Block address locations 33 - 62 (21H-3EH) contain the pointer values for each of the 1553 transmit command word subaddresses. The RTMP

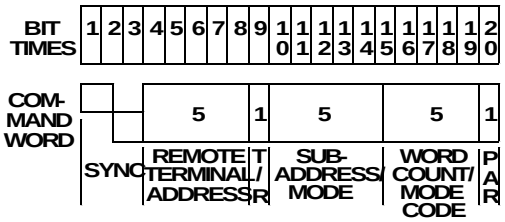
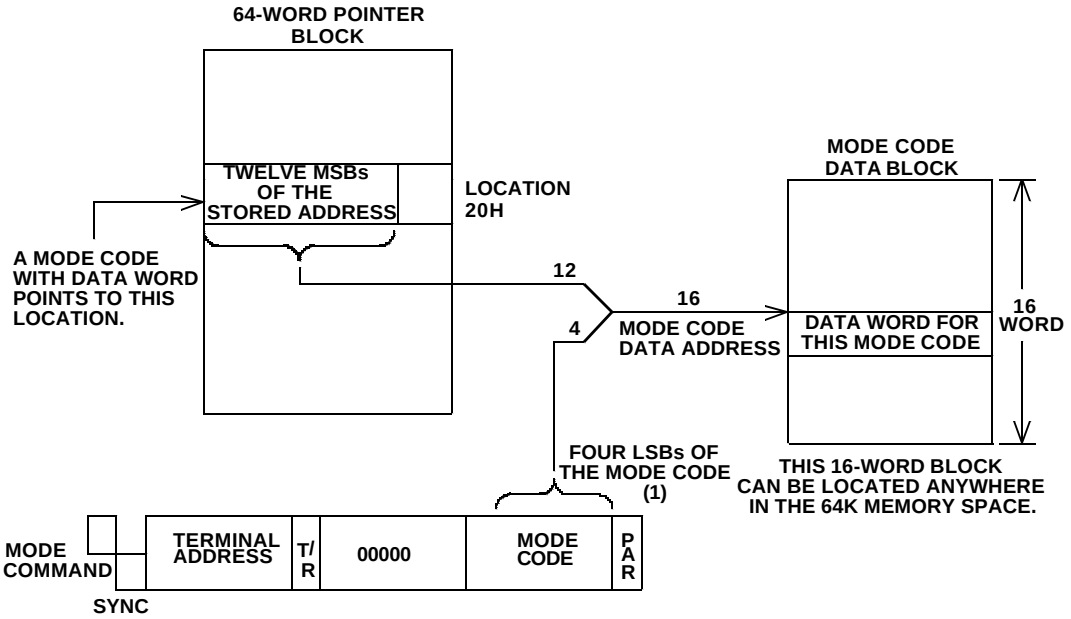


Figure 14. Command WordBit-Time Definitions



Note:

0000 Transmit Vector Word	0011 Transmit BIT Word
0001 Synchronize with data	0100 Selected Transmitter Shutdown
0010 Transmit Last Command	0101 Override Selected Transmitter Shutdown

Figure 15. Mode Code with Associated Data Word Memory Mapping

selects the address pointer data from one of these locations using the subaddress of the most recent valid command word. The RTMP internally stores this pointer value. This stored pointer value points to the memory location where the RTMP accesses the data to transmit with this subaddress. Every RTMP memory access for transmitted data increments the pointer value by one until the RTMP has transmitted all data. *Only* the host can update the pointer values stored in the Pointer Block. Therefore, if the host requires transmit data buffering, the host must control the pointer values stored in the Pointer Block. No identification word or time tag is associated with transmit commands.

Note that the RTMP does not use address location 63 (3FH) of the Pointer Block.

4.4 RTMP Data Storage

The RTMP uses two modes of allocating memory for 1553 receive messages: (1) the single buffer mode, and (2) the separate buffer mode. The user selects the buffer mode by programming bit 4 (BUFSL) of the Base Pointer Data (BPD) Register.

Both modes of operation are based on a ring-buffer type of memory mapping. Ring-buffer memory mapping means the RTMP stores all incoming 1553 data words sequentially in memory starting with an initial address value. The initial address value is one of the address values stored in the 64-word Block Pointer. Note that the initial pointer address must be set up on a boundary consistent with the chosen buffer size. Example: If the buffer size is sixteen (0010H), the initial pointer address must be some multiple of sixteen.

After the RTMP selects an address pointer within the Pointer Block, it loads the selected address pointer into an internal up-counter. Every time the RTMP performs a memory store operation, the up-counter increments by one. Therefore, the address pointer always points to the next sequential memory location. The RTMP continues to increment the address pointer until it reaches the programmed buffer size, which the user programs with bits 3 through 0 of the BPD (BSIZ3-BSIZ0). When the RTMP reaches the programmed buffer size, the internal up-counter ripples over; i.e., it returns to all zeros. At this time, the address pointer once again points to the initial block boundary memory address. To avoid the possibility of corrupting the initial receive data after the up-counter has rippled over, the user must read the data in the block before this event occurs. After the RTMP completes all memory accesses, the RTMP stores the updated address pointer in its initial 64-word Pointer Block location.

When the user chooses the single buffer mode of operation (BUFSL = 1), the RTMP always accesses the same address pointer within the 64-word Pointer Block for every 1553 receive command. Since the RTMP stores all 1553 data words in the same buffer during this mode of operation, the user needs to program the buffer size large enough to allow the RTMP to store several 1553 messages before it overwrites the data at the beginning of the buffer.

When the user chooses the separate buffer mode of operation (BUFSL = 0), the RTMP uses the subaddress of the present 1553 command word to select which of the address pointers within the 64-word Pointer Block it will use to store the received data. Therefore, the user can define up to 30 separate data buffers, one for each receive subaddress, anywhere in memory. The starting memory location of each buffer is stored in the receive section of the Pointer Block. In the separate buffer mode, the user needs to program the buffer size so it is large enough to keep the RTMP from overwriting the current data in any of the separate data buffers if the RTMP receives a new message with the same subaddress before the host can read the data from that data buffer.

Figures 16a and 16b show how each mode operates for a sample receive transmission.

In addition to the data words associated with a receive command, the RTMP also stores two additional words, an identification word, which the RTMP stores immediately before the data words, and a time tag word, which the RTMP stores immediately after the data words. The identification word is the 1553 command word associated with the data in this data block, and the time tag word is the output of the Time Tag Register. Command word bit time four (figure 14) is stored as the MSB of the identification word and command word bit time 19 is stored as the LSB of the identification word. Therefore, each receive message requires two additional memory locations to allow the RTMP to store the message successfully.

For example, a receive message with twelve data words actually requires fourteen memory locations. Therefore, the user needs to program the buffer size to be sixteen (2^4) since buffer sizes defined in the BPD can only be a length of two raised to an integer power from three to fifteen. If, on the other hand, a receive message has fifteen data words, this message actually requires seventeen memory locations. In this case, the user must program a buffer size of 32 (2^5), since this is the next power of two that accommodates seventeen data words.

In the separate buffer mode of operation, the RTMP makes all buffers the same length. Therefore, the host must be sure to program the RTMP so the buffer size is large enough to accommodate the largest message the RTMP can receive for any subaddress.

4.5 RTMP Interrupt Functions

The RTMP has two outputs that provide the host subsystem processor with interrupt control capability: (1) the End of Receive/Transmit Message Activity ($\overline{\text{EORT}}$) interrupt; and (2) the End of Mode Code Activity (OEMC) interrupt. The host subsystem can use these two outputs in conjunction with the information the Operational Status Register (OPS) provides to determine the condition of the RTMP after an interrupt condition occurs.

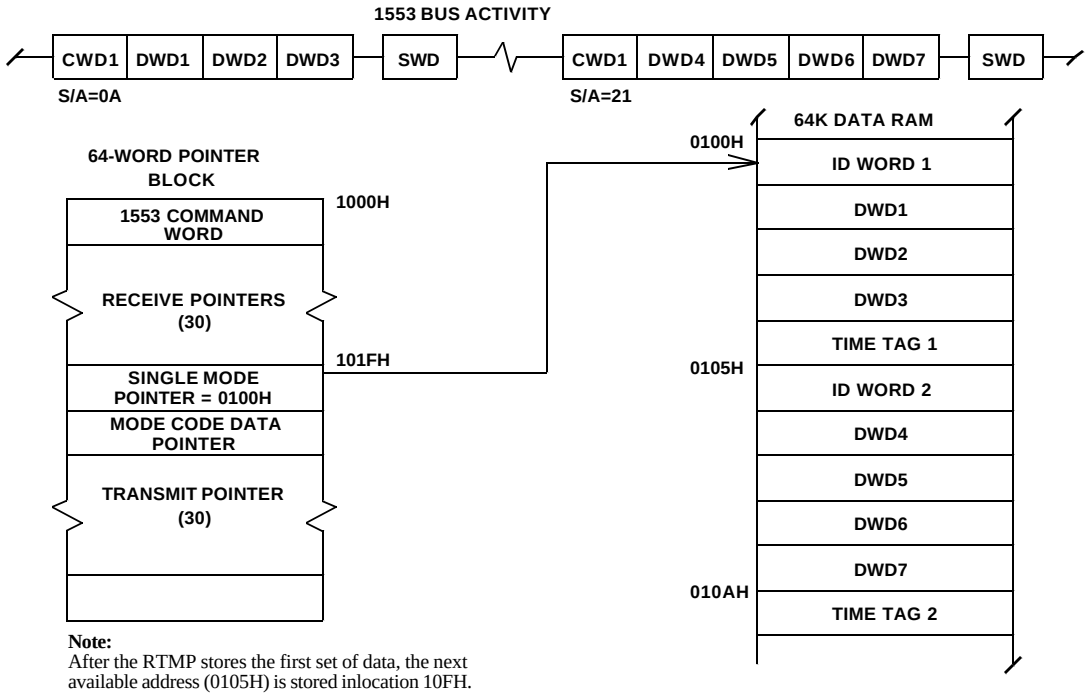


Figure 16a. RTMP Single Buffer Mode of Operation

The End of Receive/Transmit Message Activity ($\overline{\text{EORT}}$) interrupt is a maskable interrupt the user can select to occur (1) only when the 1553 receive command activity is complete; (2) only when the 1553 transmit command activity is complete; or (3) when either receive *or* transmit command activity is complete. The host masks the EORT interrupt by resetting the appropriate bits (bit 11-IM1 and bit 10-IM2) in the RTMP's Control Register (CTL). IM1 = 0 keeps EORT from occurring at the end of receive command activity. IM2 = 0 keeps EORT from occurring at the end of transmit command activity. If the host does not mask either IM1 or IM2, the EORT interrupt pulses low. This pulse occurs at the end of either the receive or transmit command activity.

The End of Mode Code Activity ($\overline{\text{EOMC}}$) interrupt is a non-maskable interrupt. The EOMC interrupt, like the EORT interrupt, is also a low pulse, except the EOMC interrupt occurs at the end of all memory accesses associated with any 1553 mode code command. Both EORT and EOMC require an external pull-up resistor and, if necessary, the user can wire-OR the two outputs together to form a composite RTMP interrupt.

If any one of the following conditions occurs during normal RTMP operation, the RTMP does not generate either the EORT or the EOMC interrupt: (1) if a Message Error occurs; (2) if a Framing (Overrun) Error occurs; (3) if the RTMP receives an illegal 1553 command; (4) if the RTMP receives a superseding command word; or (5) if the Busy bit in the Control Register is set (1553B mode of operation only).

4.6 RTMP Error Detection Capabilities

The RTMP provides the host with significant error-detection capabilities. The RTMP can detect the following types of errors:

- Terminal Address Parity Errors
- Framing or Overrun Errors
- 1553 Message Errors

4.6.1 Terminal Address Parity Errors

The RTMP can check the the Terminal Address parity inputs (RTA4-RTA0) when the Terminal Address Parity Enable (TAPEN) input is active high. If TAPEN = 1, then RTA4-

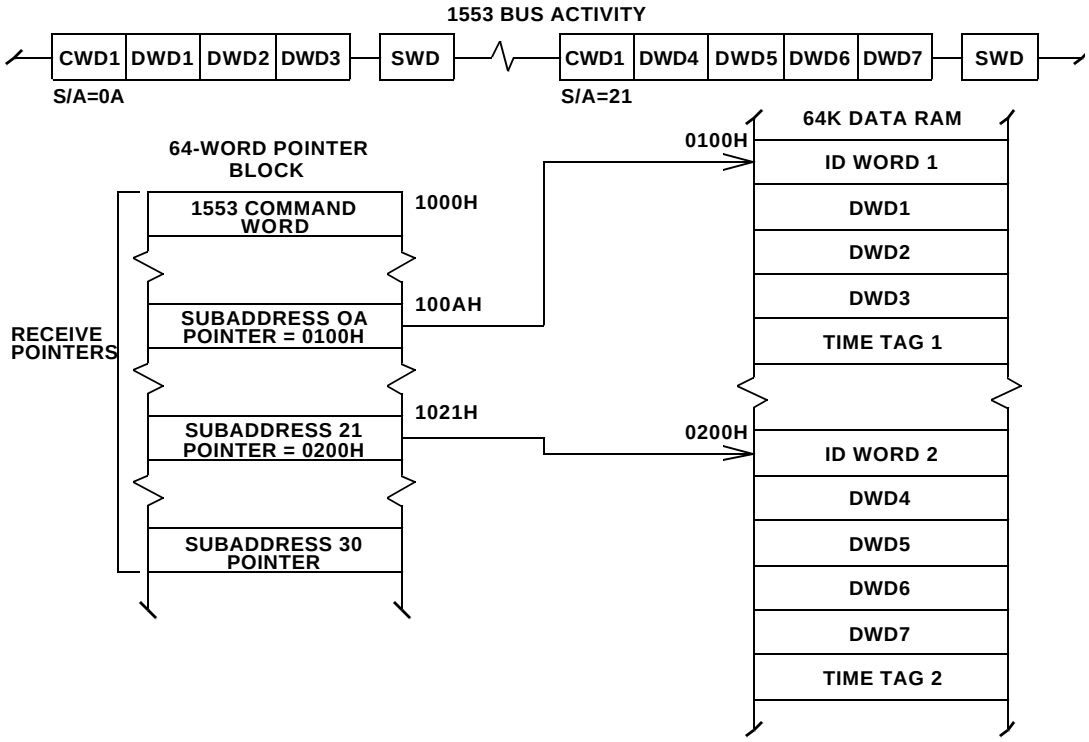


Figure 16b. RTMP Separate Buffer Mode of Operation

RTA0 and the Remote Terminal Parity (RTPTY) input must provide the RTMP with odd parity, or the RTMP flags a Terminal Address Parity Error. For example:

- If the TA = 01000, then RTPTY must equal 0 to prevent a parity error.
- If the TA = 00110, then RTPTY must equal 1 to prevent a parity error.

If the RTMP detects a Terminal Address Parity Error, this error prevents the RTMP from recognizing any valid commands on either channel, preventing the RTMP from responding to a 1553 command word not actually intended for this remote terminal.

4.6.2 Framing or Overrun Errors

A framing error occurs when the RTMP is not permitted to access memory at a sufficient rate to service the requirements of the 1553 data bus. For receive messages, after the RTMP generates a DMA Request (DMAR) signal, the host must generate a DMA Grant (DMAG) signal before the RTMP receives the next incoming data word to prevent a framing error. For transmit messages, after the RTMP generates DMAR, the host must generate a DMAG before the RTMP completes transmitting the previous 1553 data word to prevent a framing error. When a framing error occurs during a receive command, all RTMP memory accesses cease. When a framing error occurs during a transmit command, the RTMP terminates all data transmissions.

The worst-case timing for receive commands requires the RTMP to make four memory accesses within 40ms. The worst-case timing for transmit commands depends on whether the RTMP is operating in 1553B or 1553A mode. When the RTMP is operating in the 1553A mode, the worst-case timing requires the RTMP to make three memory accesses within 22ms; when in the 1553B mode, the worst-case timing requires the RTMP to make three memory accesses within 28ms. The difference in the timing here is due to the difference in the status word response time between 1553A and 1553B.

The worst-case timing for a transmit command consists of the remote terminal response time, which is mode-dependent, and the time it takes to transmit the 1553 status word (20ms). During this time, the RTMP must fetch the address pointer from the 64-word Pointer Block, store the 1553 command word in the first location of the Pointer Block, then fetch the first data word from memory before it completes transmitting the status word.

When the RTMP detects a receive command word, it must make four separate memory accesses before it receives the second 1553 data word. The RTMP must (1) fetch the appropriate address pointer from the 64-word Pointer Block; (2) store the 1553 command word in the first location of the Pointer Block; (3) store the identification word at the memory location pointed to by the address pointer; and (4) store the first received data word in the memory location immediately after the identification word.

4.6.3 1553 Message Errors

The RTMP sets the Message Error bit in the 1553 status word and also asserts the MERR output if the RTMP detects a failure in one of the following areas.

1553 Data Word Tests:

- Invalid sync field for any data word
- Incorrect Manchester II format
- Incorrect data word or command word parity
- Too few data bits per word
- Too many data bits per word
- Too few data words per message
- Too many data words per message (1553B mode only)
- Non-contiguous data words

RT-to-RT Transfer Tests:

During an RT-to-RT command sequence, the RTMP monitors the 1553 bus and compares the terminal address of the transmit command word with the terminal address of the status word from the transmitting RT. The RTMP declares the RT-to-RT transfer invalid if no match occurs. The RTMP then sets the Message Error bit. The RTMP also sets the Message Error bit if it detects one of the following errors:

- Data word transmission before the status word transmission
- Excessive time before the transmitting RT sends the status word
- Any deviation from the proper sequence of events for RT-to-RT transfers

Illegal Mode Commands:

When the RTMP is operating in the 1553A mode, it does not automatically declare any received mode code as illegal. To illegalize any mode code, the RTMP outputs the Mode Code/Subaddress outputs (MCSA0-MCSA4) along with the Mode Code/Subaddress status signal (MC/SA). The host uses these signals to decode when the RTMP receives a mode code and what mode code was received. If the mode code is illegal for this application, the host asserts the RTMP's Illegal Command (ILLCOM) input and the Message Error bit is set in the RTMP's 1553 status word response.

When the RTMP is operating in the 1553B mode, it automatically illegalizes the following mode codes:

- Mode Code 00000 - Dynamic Bus Control
- Reserved Mode Codes 01001 through 01111 (no associated data word)
- Reserved Mode Codes 10110 through 11111 (with associated data word)

In these cases, the RTMP status word response has the Message Error bit set.

4.7 RTMP Self-Test Functions

The RTMP performs a self-test by wrapping the encoder output back into the decoder inputs. Self-test is either internal or external to the RTMP. An internal self-test wraps the RTMP encoder output back into the decoder input via a multiplexer internal to the RTMP. External self-test loops the RTMP encoder back into the decoder via the bus transceiver. In normal operation the transceiver transmitter is connected to the receiver. This connection closes the loop from the encoder to decoder. Self-test has the ability to check the function of Channel A and B, command recognition logic, data transfer logic, and memory address control.

The RTMP's self-test capability is based on the fact that the MIL-STD-1553 status word sync pulse is identical to the command word sync pulse. Thus, if the status from the encoder is fed back to the decoder, the RTMP will recognize the status word as a command and thus cause the RTMP to process the validated command word. After the host invokes self-test, the RTMP self-test logic forces the transmission of a status word even though the RTMP has not received a valid command. By reading the RTMP's Operational Status Register the host can monitor self-test. The host compares self-test results to expected results; data mismatches result in self-test failure. Normal operation is inhibited during self-test.

Anytime during the RTMP's self-test execution, the host can monitor the Operational Status Register's (OPS) Self-Test Active bit (STACT), bit 11. STACT=1 signifies that the RTMP is performing a self-test. STACT is active until the RTMP completes all self-test memory activity. If the host has enabled the activity interrupts (EORT and EOMC), EOMC occurs after the memory fetch for the data word that the RTMP wraps around during the self-test, and EORT occurs when the self-test is complete. Do not send mode code commands in self-test while operating in the A mode. In B mode the RTMP can verify 3 mode codes (Synchronize with Data, Selected Transmitter Shutdown, Override Selected Transmitter Shutdown). All of these mode codes have the T/R bit set to zero.

Note: When monitoring self-test via the Operational Status Register, each OPS read will clear any bits the RTMP set.

Control and invoke self-test by using the TEST input pin, along with Control Register bits 12, 13, 14, and 15 (i.e., STCS, STEN, CHBEN, and CHAEN). Control Register bit 12, Self-test Channel Select (STCS), determines whether internal self-test is performed on Channel A or Channel B. Control external self-test channel select via Control Register bit 12 (STCS) and Control Register bit 14 or bit 15. These three bits determine which channel is active during self-test. STCS identifies which channel, bit 15 or bit 14, enables the hardware. Disable Channels A and B, via Control Register bits 15 and 14, for internal self-test. Control Register bit 13, Self-test Enable, initiates the self-test routine. See Control Register bit descriptions for more information on the function of bits 12 and 13. Input pin TEST determines whether the self-test is external or internal (TEST = 1 external, TEST = 0 internal).

Note: External self-test will corrupt an operational bus since a remote terminal transmits command word information. Also note that bus activity received by the RTMP decoder (specifically command word validation) will corrupt self-test.

After the host processor enables a self-test, the RTMP's internal self-test logic remains in a "wait" state until the RTMP is not receiving or transmitting any information. Once the RTMP determines that there is no 1553 bus activity, the STEN bit of the Control Register is reset and self-test begins.

Essentially, the self-test makes the RTMP behave as if it just received a Transmit Vector Word mode code. The Transmit Vector Word mode code tells the RTMP to transmit a status word and one associated data word. The RTMP wraps this status word and data word back around into the channel under test. Since a status word and a command word have the same sync pulse, when the RTMP decoder sees this status word, the receiver thinks it has received a valid command from the 1553 data bus.

The status word the RTMP transmits during the self-test, which is wrapped around to the decoder as the 1553 command word, is host-programmable. The RTMP forces bit 11 of this status word to logic zero, hence the status word is recognized as a receive command word. All commands used in self-test are receive commands. The host can program bits 1 through 10 of this status word by writing to bits 0 through 9 of the Control Register. When the RTMP's decoder sees these ten bits in the wrapped-around command word, these bits are decoded as the command word's subaddress and word-count fields. Only one data word is transmitted with the status word, therefore setting the word count field not equal to 1 results in a message error.

The RTMP accesses the data word that it wraps around during the self-test from memory just as it would any other data word. The RTMP reads the data word for the wrap-around test from the memory location to which the address in the Mode Code Pointer (location 20H) points. The twelve most significant bits of this address come from the data programmed in the Mode Code Pointer location. The RTMP always the four least significant address bits to zero (Transmit Vector Word Mode Code).

The RTMP's decoder on the selected test channel recognizes the status word that is wrapped around during the self-test as a valid 1553 receive command word. The RTMP's internal sequencer and error detection logic begin processing the received command word and its associated data in a normal sequence. The host programs the outgoing status/command word to receive one data word at a specific subaddress. Then the RTMP goes to the location in the 64-word Pointer Block corresponding to the actual memory location subaddress where the RTMP stores the data word wrapped around during the self-test, if the host has chosen the separate buffer mode of operation. If the host has selected the single buffer mode of operation, the RTMP stores the wrapped-around data word at the memory location to which the Single Mode Data Pointer in the 64-word Pointer Block points. The RTMP suppresses transmitting a status word after receiving the wrapped-around command word and data word during self-test execution. At this time, the self-test terminates and the RTMP resets the Self-Test Active (STACT) bit in the Operational Status Register.

The host has complete control over the RTMP's self-test processing and can terminate a self-test at any time by performing a write to the Stop Self-test Register (SST). When the host writes to the SST, the RTMP terminates all memory activity, resets STEN, and resets the Self-Test Active (STACT) bit in the OPS.

5.0 1553A AND 1553B MODES OF OPERATION

The RTMP provides two modes of operation -- one to meet the requirements of MIL-STD-1553A and another to meet the requirements of MIL-STD-1553B. The user selects the mode of operation for the specific application by programming the 1553 mode select input (PRA/B). When the host sets PRA/B = 1, the RTMP is in the 1553A mode of operation. When PRA/B = 0, the RTMP is in the 1553B mode of operation.

In either the 1553A or 1553B mode, the RTMP's basic operation remains the same with three major differences among the modes of operation. These differences are: status word bit definitions, mode code responses, and status word response time.

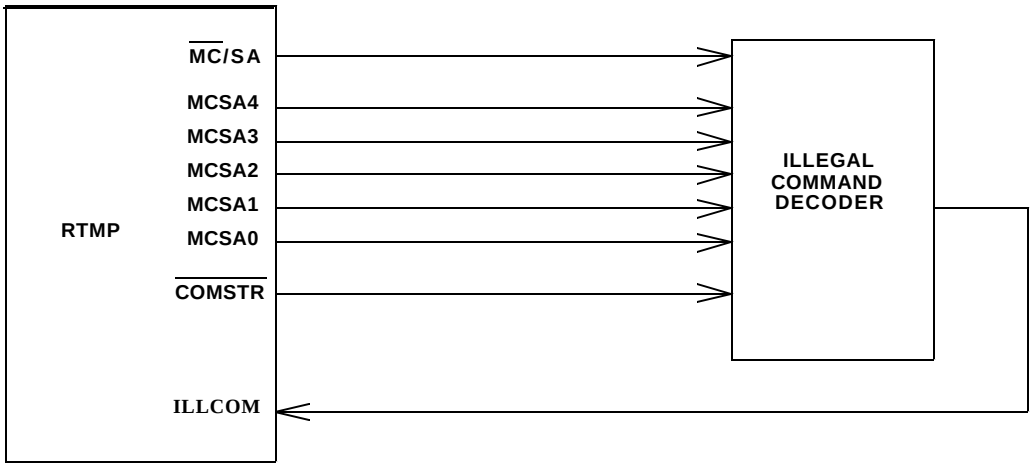


Figure 17. Mode Code/Subaddress Illegalization Circuit

5.1 Status Word Bit Definition

When the RTMP operates in the 1553A mode, the only bits of the status word it defines are the Message Error bit (bit 11) and the Terminal Flag bit (bit 1). The RTMP does not specifically define the rest of the bits in the status word (bits 2 through 10). The user can define these bits for a specific application by programming the corresponding bits in the Control Register (CTL bits 1-9).

In the 1553B mode of operation, the RTMP defines all status word bits in the CTL that correspond to a specific function in the transmitted 1553 status word. The host controls some of the status word bits in the CTL, namely the Instrumentation, Service Request, Broadcast, Busy, Subsystem Flag, and Terminal Flag bits. Finally, if the host sets any undefined status word bits in the CTL, the RTMP masks these bits (i.e., sets to logic zero) before they can be transmitted in the status word.

5.2 Mode Code Responses

When the RTMP operates in the 1553A mode, it does not internally detect any mode codes as being illegal. The RTMP recognizes all other mode codes as being valid, and responds to these mode codes with a status word only. The 1553A mode of operation does not support mode codes with an associated data word.

- Do not send mode codes with data to the RTMP when operating in the 1553A mode.
- No auto-execution of mode codes is performed in the 1553A mode of operation.

The host can illegalize any mode code by decoding the Mode Code/Subaddress outputs (MCSA0-4) and the MC/SA output with an external device (figure 17). The host can program the external decoder to generate the Illegal Command (ILLCOM) input whenever the RTMP receives a mode code that the system declares illegal. Asserting ILLCOM causes the RTMP to transmit a status word with the Message Error bit set. Illegalization does not stop the auto-execution of mode codes.

In the 1553B mode of operation, the RTMP internally detects the Dynamic Bus Control mode code and all reserved mode codes as illegal. The host can illegalize any other mode code by setting the ILLCOM input, just as described for the 1553A mode of operation.

Table 2 shows the action the RTMP takes for each of the mode codes.

5.3 Status Word Response Time

When the RTMP operates in the 1553B mode, it checks to see if too many data words are received while processing a receive command. While operating in the 1553A mode, the RTMP does not make this check. Therefore, the status word response time for the RTMP in the 1553A mode is different from the status word response time in the 1553B mode.

Operating in the 1553A mode, the RTMP's status word response time is from 4.25 to 5.75ms (reference figure 29). This time is measured from midbit of the command word parity bit to midbit of the status word sync pulse.

Operating in the 1553B mode, the RTMP's status word response time is from 9.25 to 10ms (reference figure 29). This time is also measured from midbit of the command word parity bit to midbit of the status word sync pulse.

These midbit-to-midbit response times are measured from the midbit time of the parity bit at the RTMP's inputs to the midbit time of the sync pulse at the RTMP's outputs. These measurements do not include any delays attributable to external devices such as transformers or transceivers.

Table 2. Mode Code Operation

Mode Code (7)	Number	Legal (L)/ Illegal (I)	Operation (see below)	1553A Mode	Notes
Dynamic Bus Control	00000	I	1	L(2)	
Synchronize	00001	L	2	L(2)	
Transmit Status Word	00010	L	3	L(2)	
Initiate Self-Test	00011	L	2	L(2)	
Transmitter Shutdown	00100	L	3,8	L(2)	
Override Transmitter Shutdown	00101	L	3,8	L(2)	
Inhibit Terminal Flag Bit	00110	L	3,8	L(2)	
Override Inhibit Terminal Flag Bit	00111	L	3,8	L(2)	
Reset Remote Terminal	01000	L	2	L(2)	
Reserved	01001 01111	I	1	L(2)	
Transmit Vector Word	10000	L	4	L(2)	
Synchronize	10001	L	4	N/A	No mode code with data
Transmit Last Command	10010	L	5	L(2)	Status word only
Transmit Bit Word	10011	L	4	L(2)	
Selected Transmitter Shutdown	10100	L	4	N/A	No mode code with data
Override Selected Transmitter Shutdown (6)	10101	L	4	N/A	No mode code with data
Reserved	10110-11111	I	1	L(2)	

Definition of operations:

1. The RTMP sets the Message Error bit, sends a status word, and stores the 1553 command word, but takes no internal action.
2. The RTMP sends a status word, stores the 1553 command word, but takes no internal action
3. The RTMP sends a status word, stores the 1553 command word, and takes the appropriate internal action.
4. The RTMP sends a status word, stores the 1553 command word, accesses memory for the associated data word, but takes no internal action.
5. The RTMP sends a status word, updates the 1553 command word in an internal register, accesses memory for the associated data word, but takes no internal action.
6. The RTMP must receive an Override Selected Transmitter Shutdown before the channel that was disabled can be enabled.
7. Undefined mode codes in MIL-STD-1553B are illegalized.
8. Illegalized mode code is still executed.

6.0 RTMP SYSTEM INTERFACE

The RTMP system interface consists of the major functional interfaces between the host processor and the RTMP. These interfaces (1) allow the host to control the functions of the RTMP and determine its operational status; (2) permit the RTMP and the host to exchange the information from the 1553 data bus; and (3) allow the host to select the RTMP's terminal address.

The system interface provides a description of the following aspects of the RTMP's operation:

- Assigning the RTMP's terminal address
- Controlling the RTMP's DMA interface
- Interfacing with the RTMP's internal registers

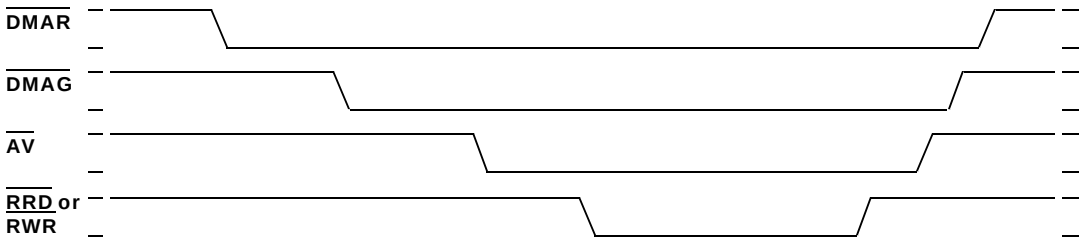


Figure 18. General RTMP DMA Timing Relationships

6.1 Assigning the Terminal Address

The RTMP's terminal address input pins (RTA0-RTA4) are static inputs. This means the RTMP does not require a latching signal of any sort to assign the RTMP its terminal address. The host simply has to present the correct terminal address on inputs RTA0-RTA4 and the RTMP recognizes this as the terminal address for all 1553 command words.

The RTMP can check the parity of the assigned terminal address by using the Remote Terminal Parity input (RTPTY) and the Terminal Address Parity Enable input (TAPEN) in conjunction with the RTA0-RTA4 inputs. In most applications, it is important that the host enable the terminal address parity checking input to prevent the RTMP from inadvertently responding to a command word not meant for it. If the host requires the RTMP to check the parity of the terminal address, TAPEN must be high and RTPTY must provide the RTMP with odd parity (an odd number of high inputs) for the assigned terminal address.

If for some reason, such as a broken or missing terminal address input or an inadvertent terminal address change, the RTMP detects bad parity, it ignores all incoming command words. The RTMP also sets bit 12 in the Operational Status Register, the Parity Error (PAERR) bit. If the host can re-establish the correct terminal address and parity, the RTMP resumes communication on the 1553 data bus.

6.2 Controlling the DMA Interface

The RTMP has a standard DMA interface that consists of a set of three arbitration signals between the RTMP and the host processor: (1) DMA Request (DMAR); (2) DMA Grant (DMAG); and (3) DMA Enable (DMAEN). After the bus controller grants the RTMP control of the address and data buses, the RTMP uses three additional signals to control the shared memory: (1) RAM Read (RRD); (2) RAM Write (RWR); and (3) Address Valid (AV). Figure 18 shows the general relationship of these signals during bus arbitration and data acquisition.

When the RTMP requires access to the shared memory, it initiates the bus arbitration sequence by generating DMAR. For a transmit message, the RTMP generates DMAR when the internal transmitter buffer is empty. Therefore, the RTMP must be granted control of the data bus before the current data word transmission is finished or an overrun error occurs. The RTMP continues to generate DMARs until it has transmitted the proper number of data words or until an error condition occurs. For a receive message, the RTMP generates DMAR after a received data word is validated. In this situation, the RTMP must receive a bus grant signal before receiving the next data word or an overrun error occurs.

After the RTMP generates $\overline{\text{DMAR}}$, it waits until the bus master generates DMAG. After the bus master generates DMAG, bus arbitration is complete (provided DMAEN is high) and the RTMP takes control of the address and data buses by first enabling the address three-state buffers. After the address lines have settled, the RTMP generates AV signifying the address is valid.

The next step in the sequence depends on whether the present memory access is for a receive or a transmit message. If the RTMP is processing a receive command, RWR goes active allowing the RTMP to write the received 1553 data to the shared memory. If, on the other hand, the RTMP is processing a transmit command, RRD goes active allowing the RTMP to access data from the shared memory. In either case, the data is read from or written to shared memory on the rising edge of RRD or RWR, respectively, thus signifying the end of this memory access cycle.

If a memory access bus cycle is pending, i.e., the RTMP has generated DMAR but the bus controller has not acknowledged with a DMAG, four events can terminate the current bus cycle: (1) the RTMP receives a superseding 1553 command word on the same or opposite channel; (2) an overrun error occurs; (3) a message error occurs; or (4) a write to the Stop Self-Test (SST) Register occurs.

6.3 Interfacing with the RTMP's Internal Registers
The host interfaces with the RTMP's six internal registers to control the RTMP's operation and to determine the RTMP's operational status while the RTMP is active. Six signals between the host and the RTMP control this interface: (1) the three least significant address lines (A2-A0); (2) Chip Select (CS); (3) register read (RD); and (4) register write (WR). Figure 19 shows the general timing relationship of these signals. The RTMP's three least significant address bits (A2-A0) are bidirectional. When the host drives these inputs along with CS, RD, and WR, the RTMP uses this information to select which of its six internal registers the host will access during this operation (table 1).

Before the host attempts to access the RTMP's internal registers, it must make sure the RTMP is not performing a DMA operation. Accessing the RTMP's internal registers during a DMA operation causes data corruption because the CS input takes precedence over all other RTMP memory operations and causes the RTMP immediately to place its address and data buffers in a high-impedance state. Therefore, after the bus master has granted the RTMP control of the buses, the host *must not* attempt any internal register reads or writes until the RTMP completes its memory operation.

The interface timing between the host and the RTMP's internal registers follows standard microprocessor interfacing techniques. After the host has determined that the RTMP is not using the address and data buses, it generates the address for the selected RTMP internal register. The host asserts CS, informing the RTMP that an internal register operation is about to occur. The RTMP responds by placing its address and data bus signals in a high-impedance state and allowing the three least significant address lines to become inputs.

At this point, the host asserts either $\overline{RD}$ or $\overline{WR}$ telling the RTMP the direction of the data flow. The host completes the current register access cycle on the rising edge of WR for data input operations and on the rising edge of RD for data output operations.

6.4 RTMP Hardware Interface

6.4.1 The RTMP - 1553 Transceiver Interface
The RTMP's Manchester II encoder/decoders interface directly with the 1553 bus transceiver as shown in figure 20. The RTMP uses the RAO, RAZ, TAO, and TAZ pins to interface with bus Channel A. The RTMP uses the RBO, RBZ, TBO, and TBZ pins to interface with bus Channel B. The RTMP's encoder outputs (TAO, TAZ, TBO, and TBZ) are low when they are inactive.

In addition to the signals listed above, the RTMP also provides two signals that assist the RTMP in meeting the MIL-STD-1553 fail-safe timer requirements. These signals are the Timer On (TIMERON) and the Channel A/ (CHA/ B) outputs. These signals are also shown in figure 20.

6.4.2 The RTMP DMA Interface
When the RTMP is in its standard DMA configuration, its address, data, and control signals are directly connected to each other as shown in figure 21. The RTMP's signals remain in a high-impedance state until the RTMP is granted control of the buses after DMA arbitration has occurred, or until the host asserts CS signifying that the host is about to access one of the RTMP's internal registers.

The host can disable all DMA transfers by setting the Busy bit (bit 3) of the Control Register (CTL).

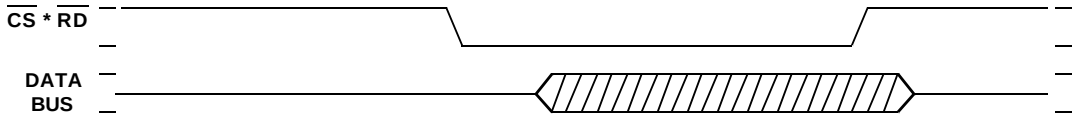


Figure 19a. General RTMP Register Read Timing

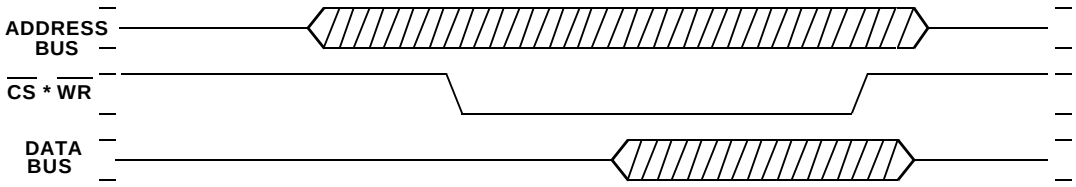


Figure 19b. General RTMP Register Write Timing

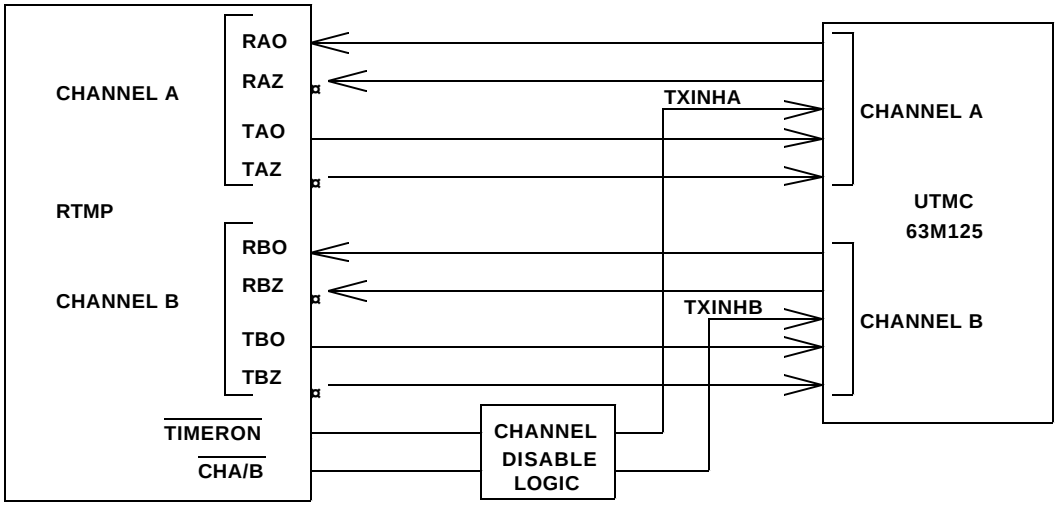


Figure 20. RTMP-to-Transceiver Interface Diagram

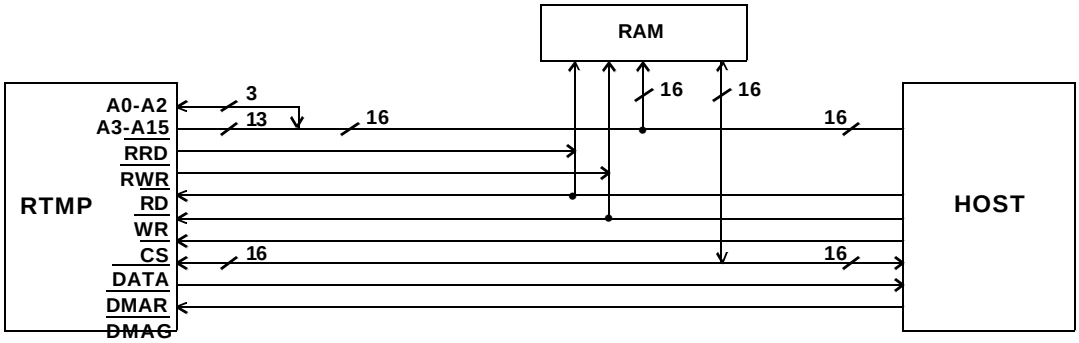


Figure 21. RTMP-to Host Interface

7.0 OPERATING CONDITIONS*

(REFERENCED TO V_{SS})

SYMBOL	PARAMETER	LIMITS	UNIT
V_{DD}	DC supply voltage	-0.3 to +7.0	V
$V_{I/O}$	Voltage on any pin	-0.3 to V_{DD}+0.3	V
I_I	DC input current	±10	mA
T_{STG}	Storage temperature	-64 to +150	°C
P_D	Power dissipation	300	mW
Θ	Thermal resistance, junction-to-case	10	°C/W
T_J	Maximum junction temperature	+175	°C

* Stresses outside the listed absolute maximum ratings may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond limits indicated in the operational sections of this specification is notrecommended. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

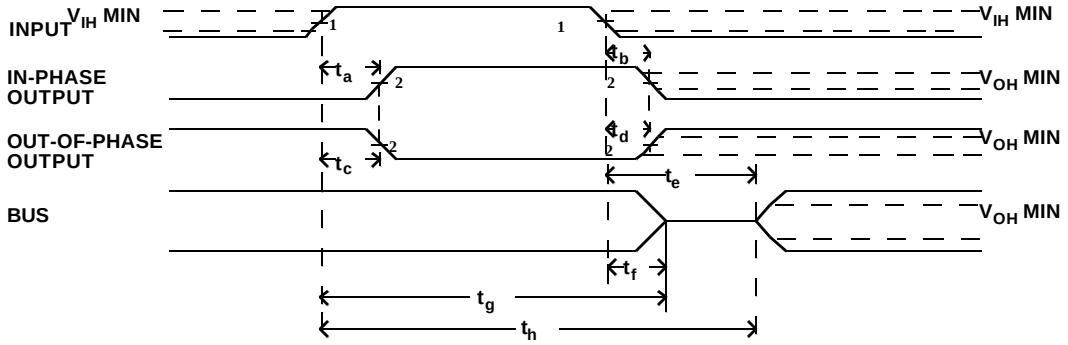
SYMBOL	PARAMETER	LIMITS	UNIT
V_{DD}	DC supply voltage	4.5 to 5.5	V
T_A	Temperature range	-55 to +125	°C
F_O	Operating frequency	12 ± .01%	MHz
V_{IN}	DC input voltage	0 to V_{DD}	V

8.0 DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITION	MINIMUM	MAXIMUM	UNIT
V_{IL}	Low-level input voltage TTL inputs			0.8	V
V_{IH}	High-level input voltage TTL inputs		2.0		V
I_{IN}	Input leakage current TTL inputs Inputs with pull-down resistors Inputs with pull-down resistors Inputs with pull-up resistors	$V_{IN} = V_{DD}$ or V_{SS} $V_{IN} = V_{DD}$ $V_{IN} = 2.4V$ $V_{IN} = V_{SS}$	-1 100 -1000	1 1000 400 -100	µA µA µA µA
V_{OL}	Low-level output voltage TTL outputs	I_{OL} = 3.2mA		0.4	V
V_{OH}	High-level output voltage TTL outputs	I_{OH} = -400mA	2.4		V
I_{OZ}	Three-state output leakage current TTL outputs	$V_O = V_{DD}$ or V_{SS}	-10	+10	µA
I_{OS}	Short-circuit output current [2, 5]	V_{DD} = 5.5V, $V_O = V_{DD}$ V_{DD} = 5.5V, V_O = 0V	 -100	100	mA mA
C_{IN}	Input capacitance [1]	F = 1MHz @ 0V		10	pF
C_{OUT}	Output capacitance [1]	F = 1MHz @ 0V		15	pF
C_{IO}	Bidirect I/O capacitance [1]	F = 1MHz @ 0V		20	pF
I_{DD}	Average operating current [3, 5]	F = 12MHz, C_L = 50pF		50	mA
QI_{DD}	Quiescent current	See Note 4		1	mA

Notes:
1. Measured only for initial qualification and after process or design changes which may affect input/output capacitance.
2. Not more than one output may be shorted at a time for a maximum duration of one second.
3. Includes current through input pull-ups. Instantaneous surge currents on the order of 1 amp can occur during output switching. Voltage supply should be adequately sized and decoupled to handle a large current surge.
4. All inputs with internal pull-ups and pull-downs should be left floating. All other inputs should be tied high or low.
5. Guaranteed by design or characterization.

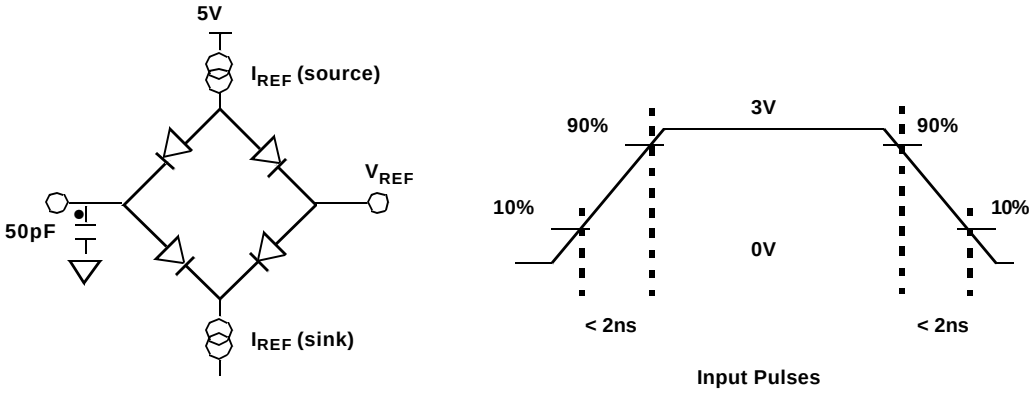
9.0 AC ELECTRICAL CHARACTERISTICS



SYMBOL	PARAMETER
t_a	INPUT↑ to response↑
t_b	INPUT↓ to response↓
t_c	INPUT↑ to response↓
t_d	INPUT↓ to response↑
t_e	INPUT↓ to data valid
t_f	INPUT↓ to high Z
t_g	INPUT↑ to high Z
t_h	INPUT↑ to data valid

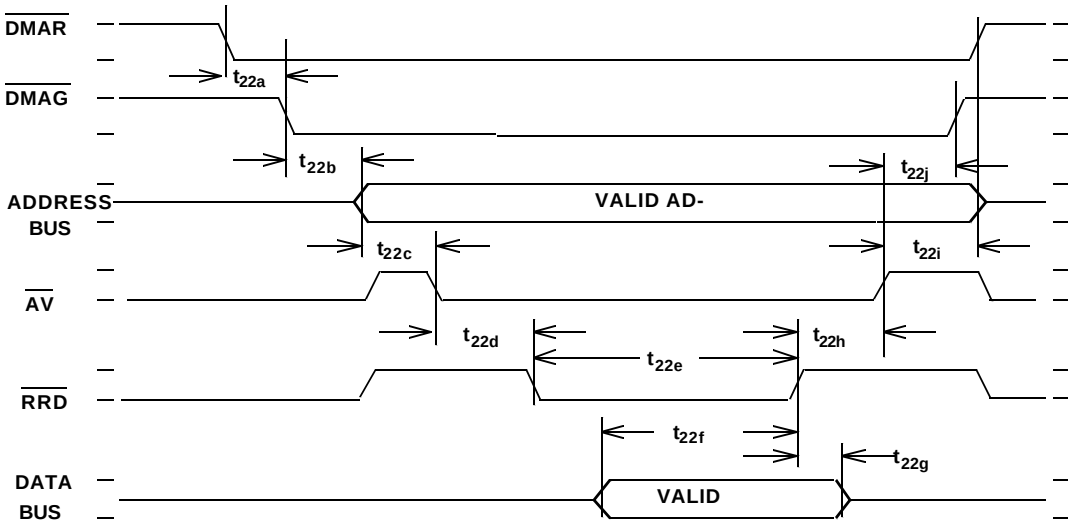
Notes:
1. Timing measurements made at (V_{IH} MIN + V_{IL} MAX)/2.
2. Timing measurements made at (V_{OL} MAX + V_{OH} MIN)/2
3. Based on 50pF load.
4. Unless otherwise noted, all AC electrical characteristics are guaranteed by design or characterization.

Figure 22. Typical Timing Measurements



Note:
50pF including scope probe and test socket

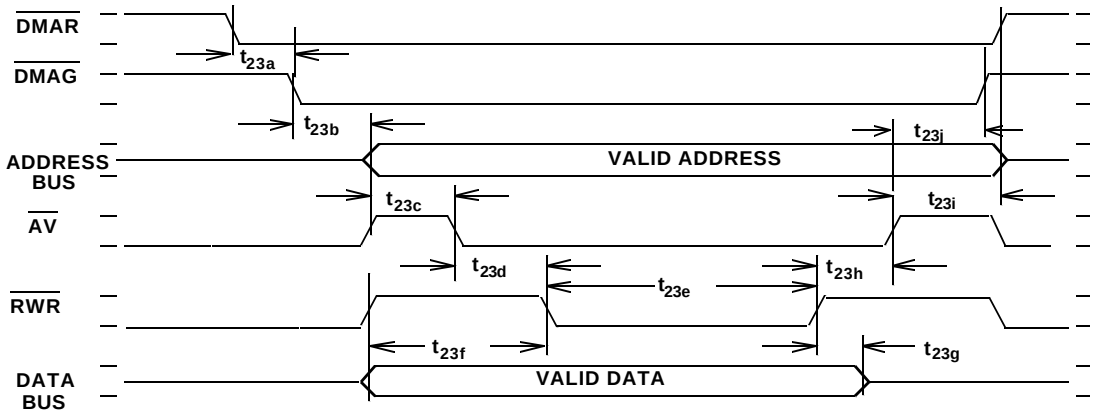
Figure 23. AC Test Loads and Input Waveforms



SYMBOL	PARAMETER	MIN	MAX	UNITS
t_{22a}	$\overline{DMAR}\downarrow$ to $\overline{DMAG}\downarrow$	0	7.3	µs
t_{22b} (1)	$\overline{DMAG}\downarrow$ to Address Bus Valid	0	134	ns
t_{22c}	Address Bus Valid to $\overline{AV}\downarrow$	40	176	ns
t_{22d}	$\overline{AV}\downarrow$ to $\overline{RRD}\downarrow$	80	90	ns
t_{22e}	$\overline{RRD}$ Pulsewidth	95	140	ns
t_{22f}	Data Setup Time to $\overline{RRD}\uparrow$	50	—	ns
t_{22g}	Data Hold Time from $\overline{RRD}\uparrow$	0	—	ns
t_{22h}	$\overline{RRD}\uparrow$ to $\overline{AV}\uparrow$	32	70	ns
t_{22i}	$\overline{AV}\uparrow$ to Address High-Impedance (Hold) and $\overline{DMAR}\uparrow$	0	62	ns
t_{22j}	$\overline{AV}\uparrow$ to $\overline{DMAG}\uparrow$	0	—	ns

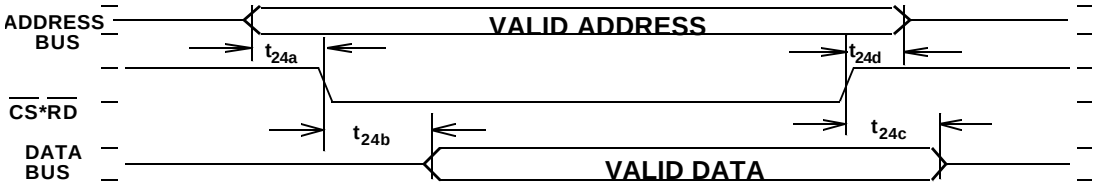
Note:
1. Guaranteed by test.

Figure 24. Detailed Timing - RTMP DMA Read Cycle



SYMBOL	PARAMETER	MIN	MAX	UNITS
t_{23a}	$\overline{DMAR}\downarrow$ to $\overline{DMAG}\downarrow$	0	7.3	µs
t_{23b} [1]	$\overline{DMAG}\downarrow$ to Address Bus Valid	0	134	ns
t_{23c}	Address Bus Valid to $\overline{AV}\downarrow$	40	176	ns
t_{23d}	$\overline{AV}\downarrow$ to $\overline{RWR}\downarrow$	80	90	ns
t_{23e}	$\overline{RWR}$ Pulsewidth	95	140	ns
t_{23f}	Data Setup Time to $\overline{RWR}\downarrow$	145	311	ns
t_{23g}	$\overline{RWR}\uparrow$ to Data Bus High-Impedance	20	90	ns
t_{23h}	$\overline{RWR}\uparrow$ to $\overline{AV}\uparrow$	32	70	ns
t_{23i}		0	62	ns
t_{23j}		0	—	ns

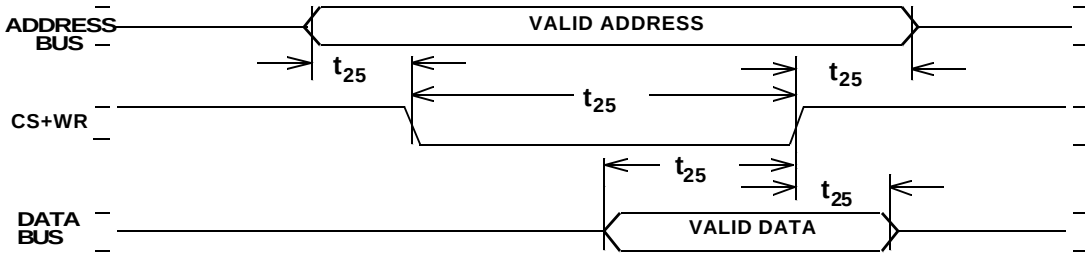
Figure 25. Detailed Timing - RTMP DMA Write Cycle



SYMBOL	PARAMETER	MIN	MAX	UNITS
t_{24a}	Address Bus Valid to $(\overline{CS}*\overline{RD})\downarrow$	20	—	ns
t_{24b} [1]	$(\overline{CS}*\overline{RD})\downarrow$ to Data Bus Valid	0	93	ns
t_{24c}	$(\overline{CS}*\overline{RD})\uparrow$ to Data Bus High-Impedence	10	100	ns
t_{24d}	$(\overline{CS}*\overline{RD})\uparrow$ to Address Bus High-Impedence	20	—	ns

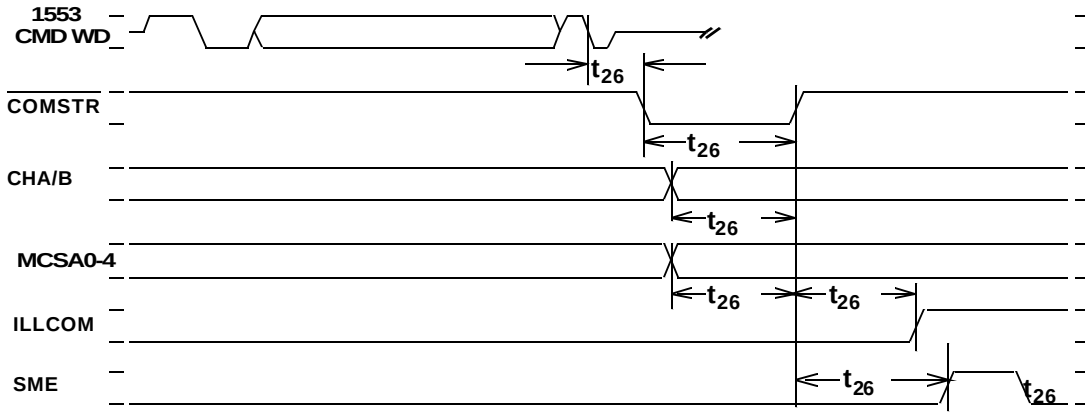
Note:
1. Guaranteed by test.

Figure 26. Detailed Timing X0106 RTMP Register Reads



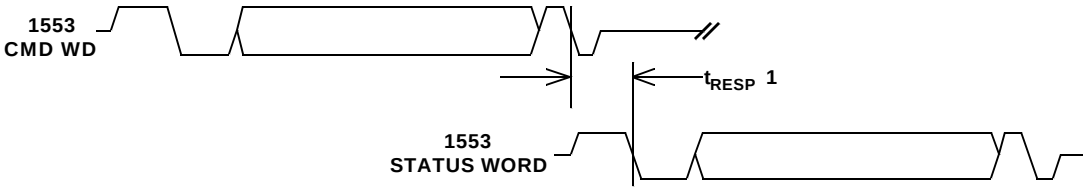
SYMBOL	PARAMETER	MIN	MAX	UNITS
t_{25}	Address Bus Valid to ($\overline{CS}$+$\overline{WR}$)↓	80	—	ns
t_{25}	$\overline{WR}$ Pulsewidth	50	—	ns
t_{25}	$\overline{WR}$↑ to Data Bus High-Impedance (Hold time)	70	—	ns
t_{25}	($\overline{CS}$*$\overline{WR}$)↑ to Address Bus High-Impedance	50	—	ns
t_{25}	Data Valid to ($\overline{CS}$*$\overline{WR}$)↑ (Set-up Time)	20	—	ns

Figure 27. Detailed Timing - RTMP Register Writes



SYMBOL	PARAMETER	MIN	MAX	UNITS
	Mid-bit of Command Word Parity to COMSTRØ	—	3.7	µs
t26a	$\overline{COMSTR}$ Pulsewidth	240	—	ns
t26b	CHA/B Valid to $\overline{COMSTR}$¦	230	—	ns
t26c	MCSA0-4 Valid to $\overline{COMSTR}$¦	240	—	ns
t26d	$\overline{COMSTR}$¦ to ILLCOM¦ (Active)	—	100	ns
t26e	$\overline{COMSTR}$¦ to SME¦ (Active)	—	500	ns
t26f	SME	.100	1.0	µs

Figure 28. 1553 Command Strobeand Channel Timing



SYMBOL	PARAMETER	MIN	MAX	UNITS
t_{RESP} (PRA/B=1)	1553A Mode Status Word Response Time	4.25	5.75	µs
t_{RESP} (PRA/B=0)	1553B Mode Status Word Response Time	9.25	10.0	µs

Note:
1. This timing is for RTMP signals only and does not include delays from other sources.

Figure 29. 1553 Status Word Response Times

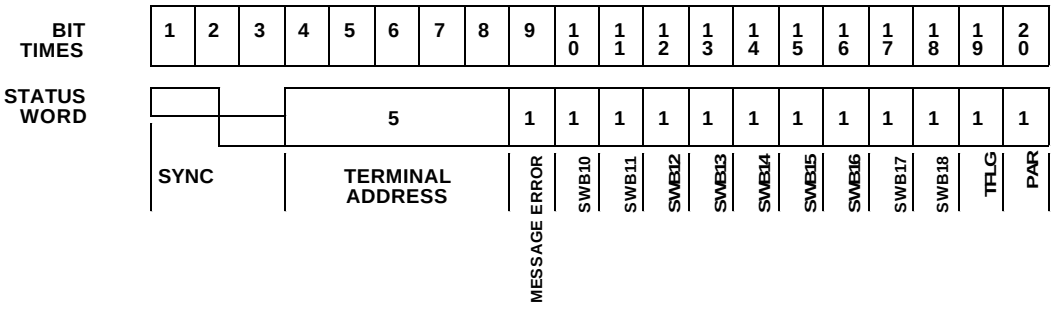
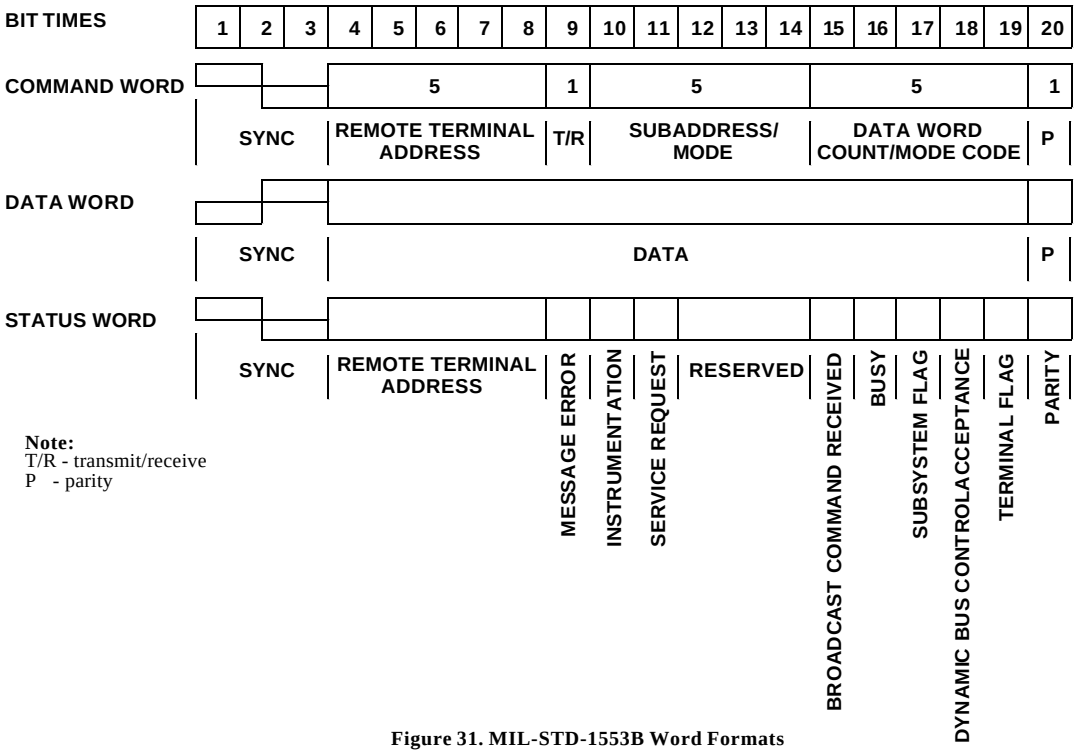


Figure 30. Status Word Bit-Time Definitions for 1553A Mode



Note:
T/R - transmit/receive
P - parity

Figure 31. MIL-STD-1553B Word Formats

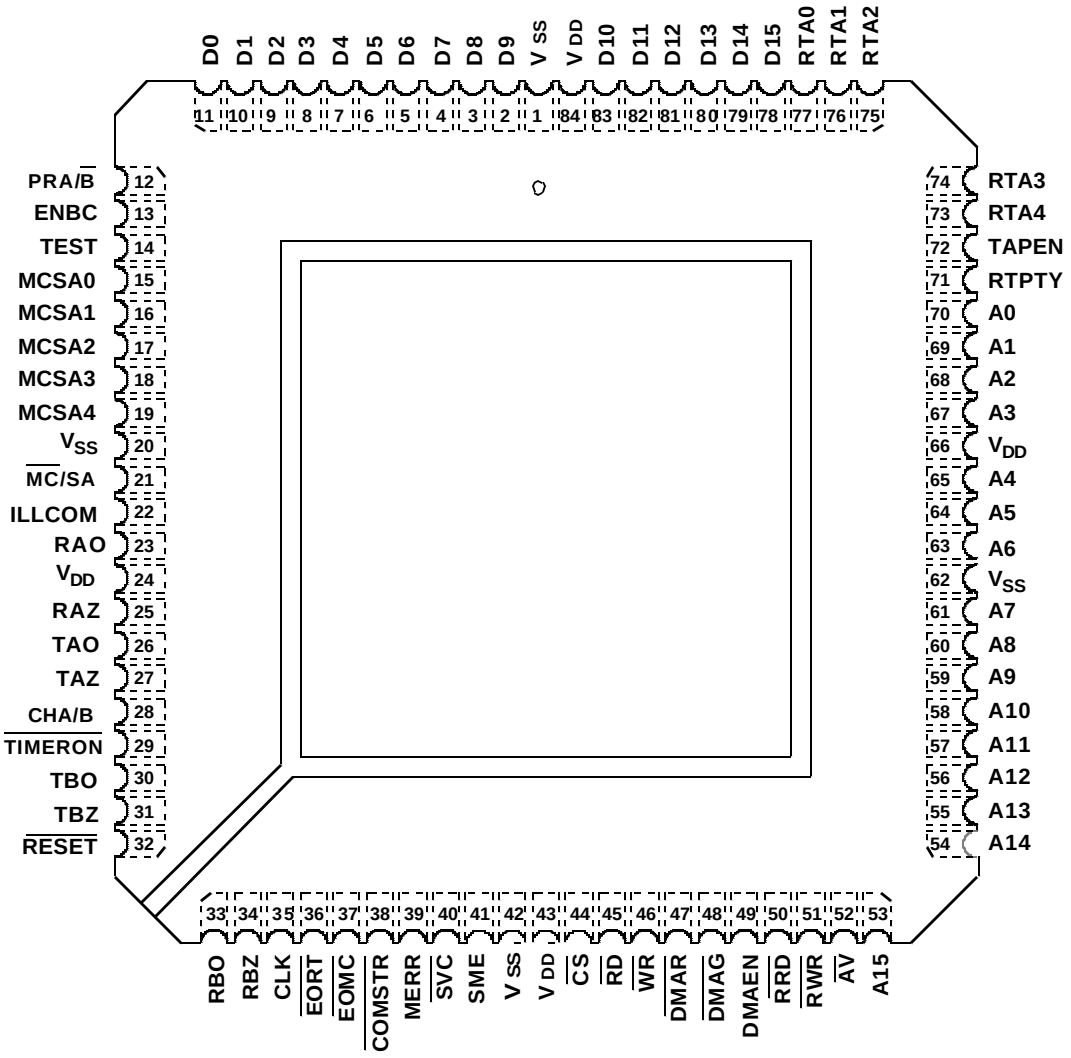


Figure 32a. Leadless Chip Carrier Functional Pin Identification (Top View)

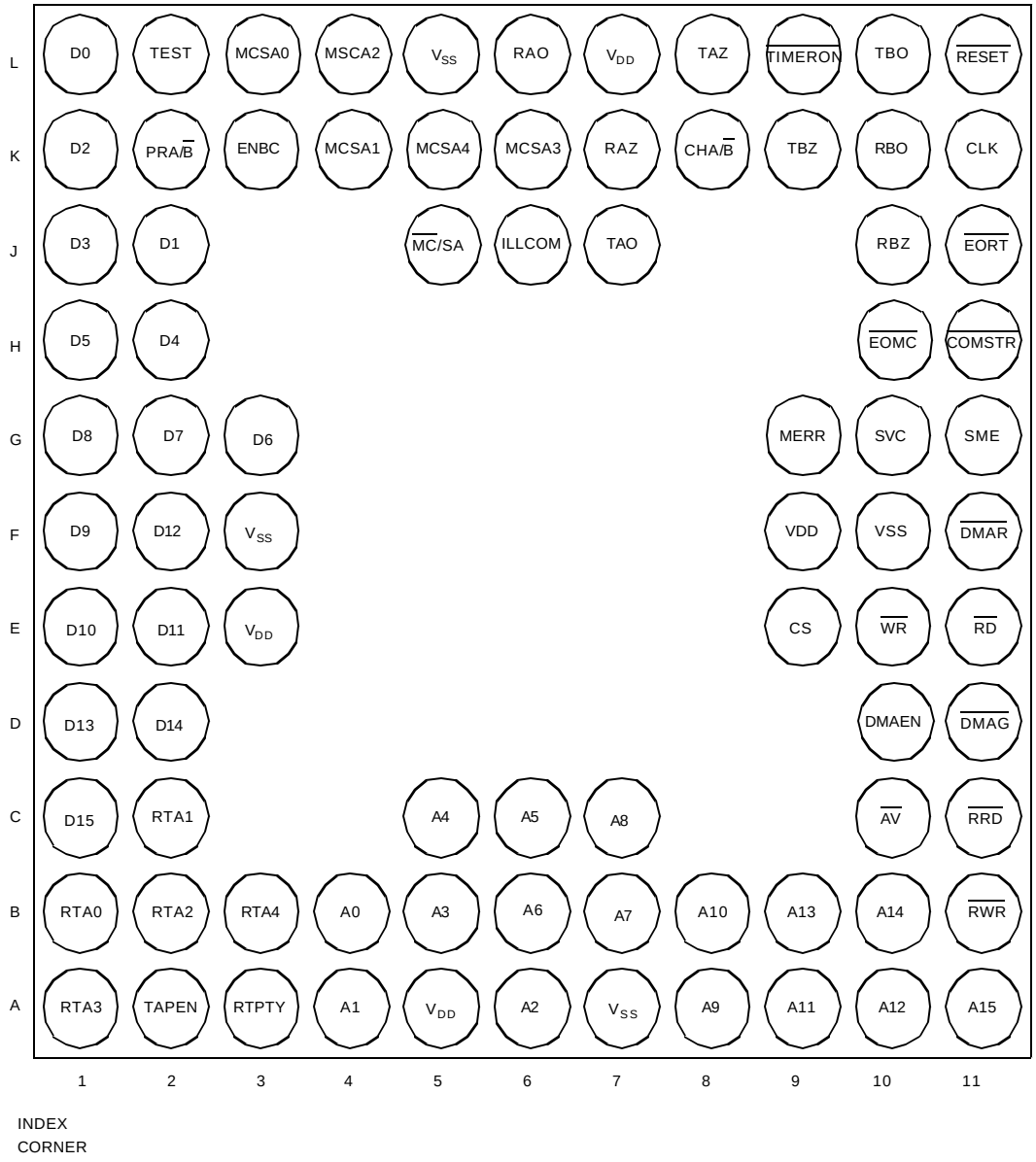


Figure 32b. Pingrid Array Functional Pin Identification (Bottom View)