NEC

MOS INTEGRATED CIRCUIT

μPD78062Y,78063Y,78064Y

8-BIT SINGLE-CHIP MICROCOMPUTER

DESCRIPTION

μPD78062Y, 78063Y and 78064Y are versions of μPD78062, 78063 and 78064 with I^2C bus control function added, respectively. They are ideal for AV product applications.

In addition to a high-speed and high-performance CPU, they incorporate a wide variety of peripheral hardware such as an LCD controller/driver, 8-bit resolution A/D converter, timer, serial interface, interrupt function.

A one-time PROM product capable of operating in the same power supply voltage range as of the mask ROM product, EPROM product and other development tools are also under development.

For the details of functional description, refer to the following user's manual.
The μPD78064Y Subseries User's Manual (Preliminary) : In preparation

FEATURES

- Large on-chip ROM & RAM

Item / Product Name	Program Memory (ROM)	Data Memory		Package
		Internal High-Speed RAM	LCD Display RAM	
μPD78062Y	16K bytes	512 bytes	40 × 4 bits	100-pin plastic QFP (fine pitch) (□14 mm, 0.5 mm pitch) 100-pin plastic QFP (14 × 20 mm, 0.65 mm pitch)
μPD78063Y	24K bytes	1024 bytes		
μPD78064Y	32K bytes			

- Instruction execution time can be varied from high speed (0.4 μs) to ultra-low speed (122 μs)
- I/O ports: 57 (including segment signal output dual-function pins)
- LCD controller/driver
- Operating voltage range V_{DD} = 2.0 to 6.0 (Static) ★
  V_{DD} = 2.5 to 6.0 (1/3 bias)
  V_{DD} = 2.7 to 6.0 (1/2 bias)
- 8-bit resolution A/D converter : 8 channels
- Serial interface : 2 channels
- Timer: 5 channels
- Operating voltage range : 2.0 to 6.0 V ★

APPLICATION

Pocket telephone, CD player, cameras, etc.

The information contained in this document is being issued in advance of the production cycle for the device. The parameters for the device may change before final production or NEC Corporation, at its own discretion, may withdraw the device prior to its production.

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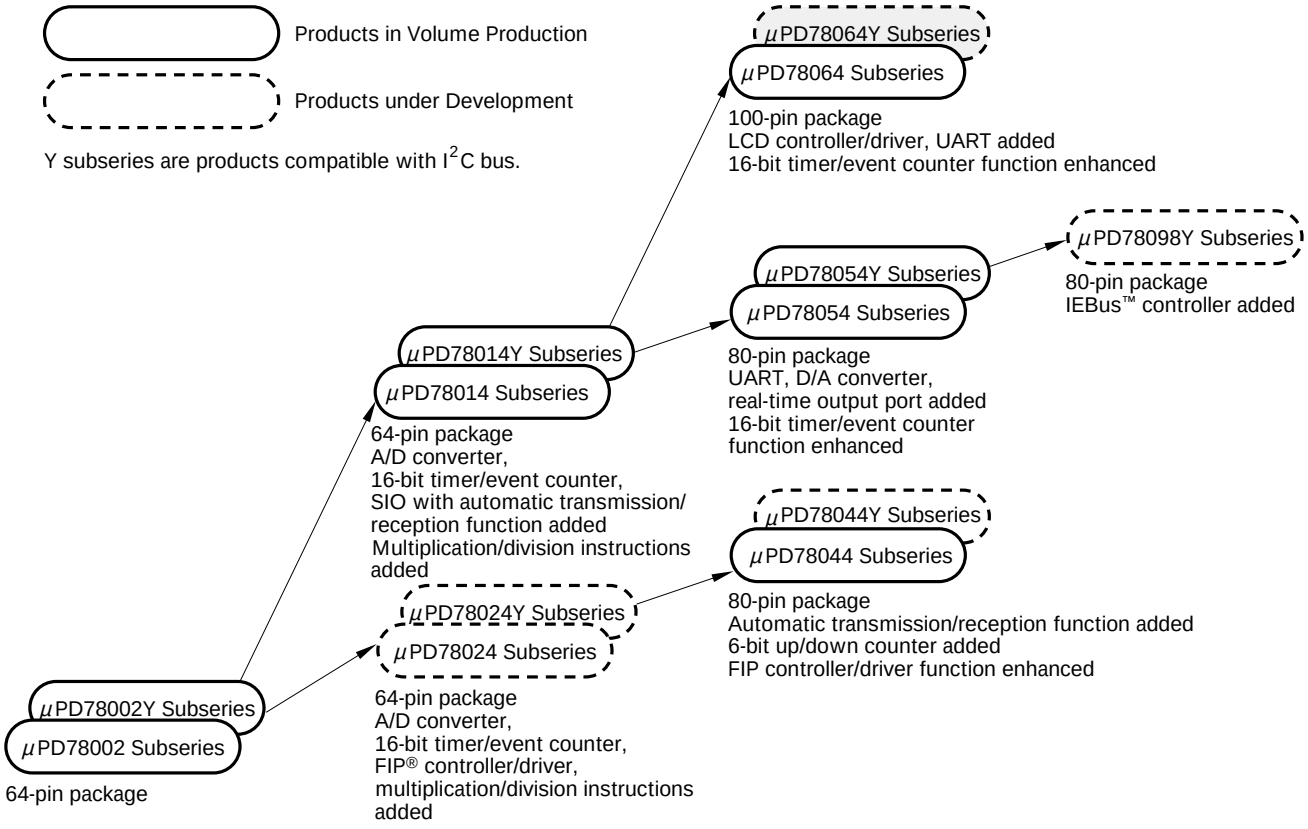
The mark ★ shows major revised points.

ORDERING INFORMATION

Ordering Code	Package	Quality Grade
μPD78062YGC-×××-7EA	100-pin plastic QFP (Fine pitch) (□14 mm)	Standard
μPD78062YGF-×××-3BA	100-pin plastic QFP (14 × 20mm)	Standard
μPD78063YGC-×××-7EA	100-pin plastic QFP (Fine pitch) (□14 mm)	Standard
μPD78063YGF-×××-3BA	100-pin plastic QFP (14 × 20mm)	Standard
μPD78064YGC-×××-7EA	100-pin plastic QFP (Fine pitch) (□14 mm)	Standard
μPD78064YGF-×××-3BA	100-pin plastic QFP (14 × 20mm)	Standard

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

★ 78K/0 SERIES DEVELOPMENT



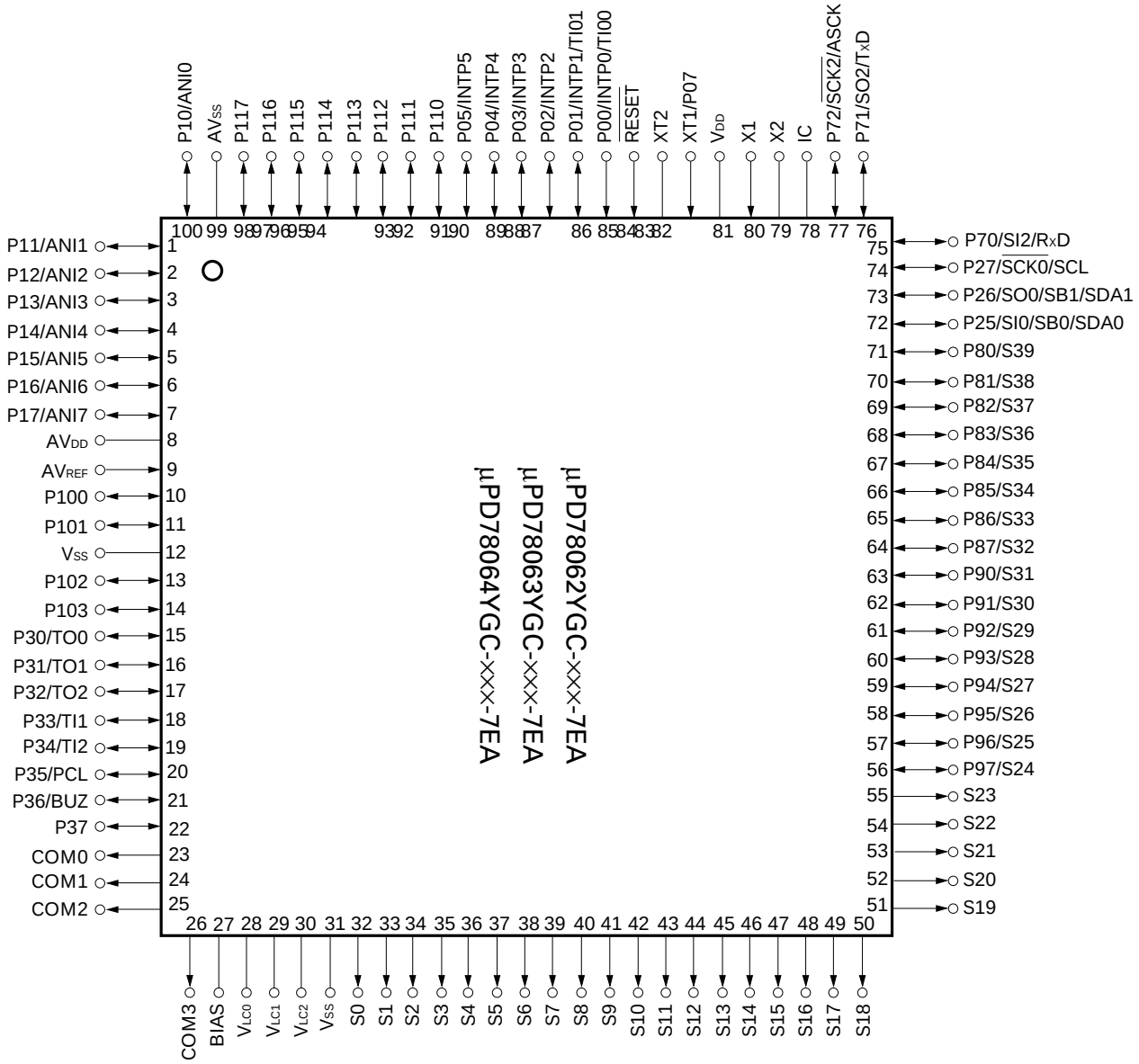
OVERVIEW OF FUNCTION

Item \ Product Name		μPD78062Y	μPD78063Y	μPD78064Y
Internal memory	ROM	16K bytes	24K bytes	32K bytes
	Internal high-speed RAM	512 bytes	1024 bytes	
	LCD display RAM	40 × 4 bits		
General registers		8 bits × 32 registers (8 bits × 8 registers × 4 banks)		
Instruction cycle		On-chip instruction execution time cycle modification function		
	When main system clock selected	0.4 μs/0.8 μs/1.6 μs/3.2 μs/6.4 μs/12.8 μs (at 5.0 MHz operation)		
	When subsystem clock selected	122 μs (at 32.768 kHz operation)		
Instruction set		• 16-bit operation • Multiplication/division (8 bits × 8 bits, 16 bits " 8 bits) • Bit manipulation (set, reset, test, boolean operation) • BCD correction, etc.		
I/O ports (including segment signal output pins)		Total : 57 • CMOS input : 2 • CMOS I/O : 55		
A/D converter		• 8-bit resolution × 8 channels		
LCD controller/driver		• Segment signal output : Maximum 40 • Common signal output : Maximum 4 • Bias : 1/2 or 1/3 switchable		
Serial interface		• 3-wired/2-wired/I²C bus mode selectable: 1 channel • 3-wired/UART mode selectable : 1 channel		
Timer		• 16-bit timer/event counter : 1 channel • 8-bit timer/event counter : 2 channels • Watch timer : 1 channel • Watchdog timer : 1 channel		
Timer output		3 (one 14-bit PWM output capability)		
Clock output		19.5 kHz, 39.1 kHz, 78.1 kHz, 156 kHz, 313 kHz, 625 kHz, 1.25 MHz, 2.5 MHz, 5.0 MHz (at main system clock 5.0 MHz operation) 32.7 kHz (at subsystem clock 32.768 kHz operation)		
Buzzer output		1.2 kHz, 2.4 kHz, 4.9 kHz, 9.8 kHz (at main system clock 5.0 MHz operation)		
Vectored interrupts	Maskable interrupts	Internal : 12, external : 6		
	Non-maskable interrupts	Internal : 1		
	Software interrupts	Internal : 1		
Test input		Internal: 1, External: 1		
Operating voltage range		V_{DD} = 2.0 to 6.0 V		
Package		• 100-pin plastic QFP (Fine pitch)(□ 14 mm) • 100-pin plastic QFP (14 × 20 mm)		

CONTENTS

1. PIN CONFIGURATION (TOP VIEW)

100-pin plastic QFP (Fine pitch)(□ 14 mm)

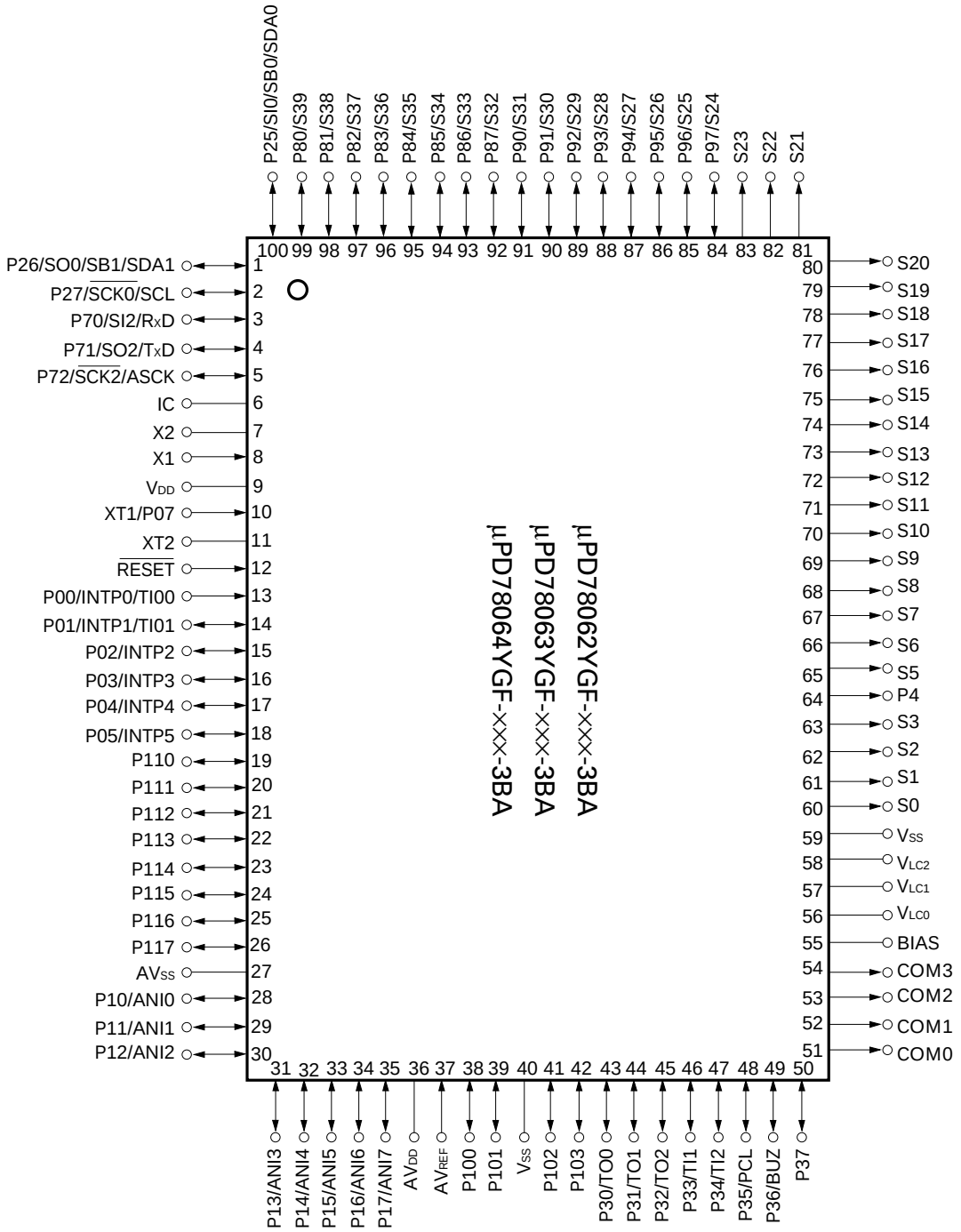


Note 1. Connect directly the IC (Internally Connected) pin to V_{SS}.

2. Connect the AV_{DD} pin to V_{DD}.

3. Connect the AV_{SS} pin to V_{SS}.

100-pin plastic QFP (14 × 20 mm)



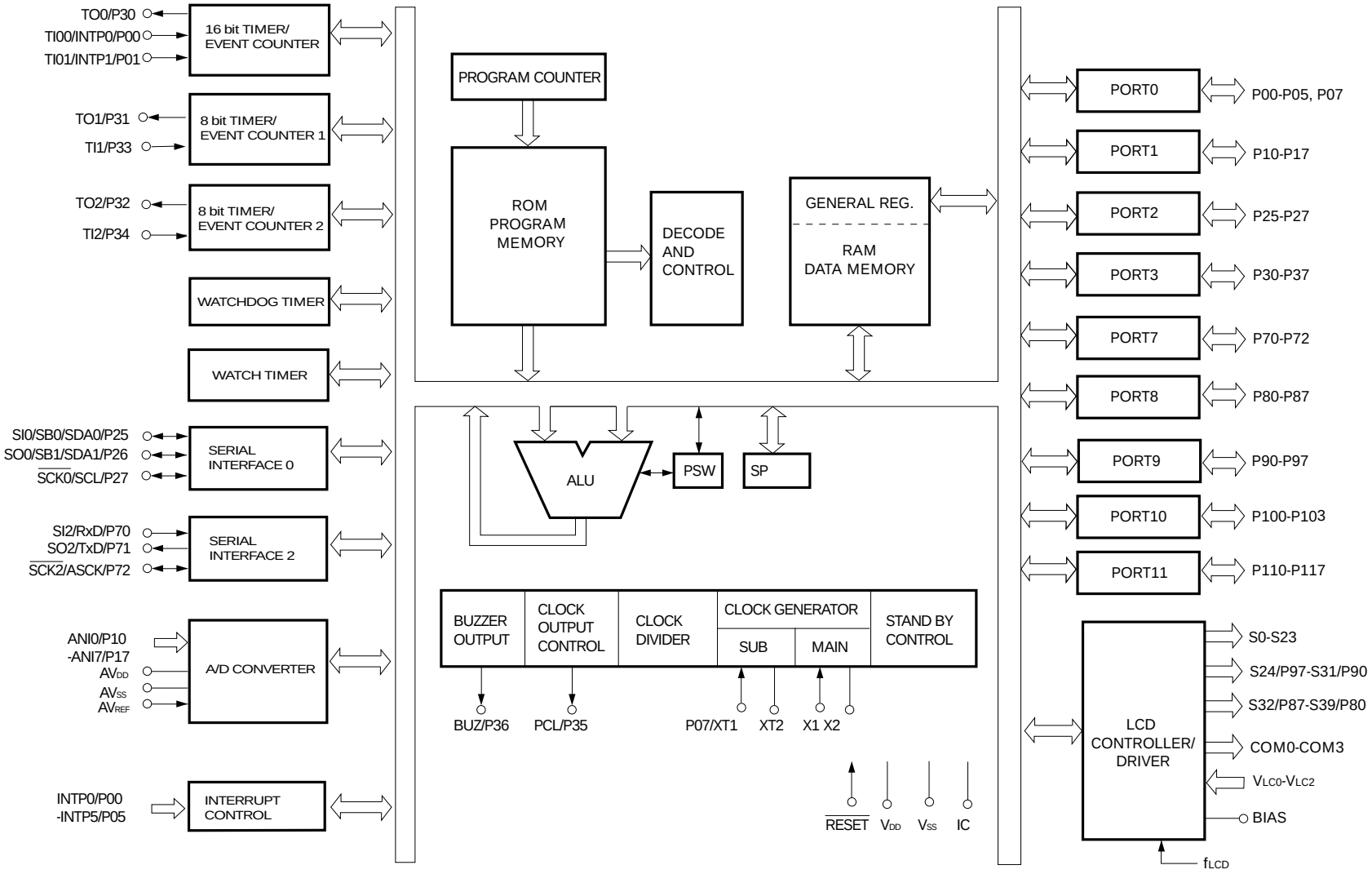
Note 1. Connect directly the IC (Internally Connected) pin to V_{SS}.

2. Connect the AV_{DD} pin to V_{DD}.

3. Connect the AV_{SS} pin to V_{SS}.

P00 to P05, P07 : Port0
P10 to P17 : Port1
P25 to P27 : Port2
P30 to P37 : Port3
P70 to P72 : Port7
P80 to P87 : Port8
P90 to P97 : Port9
P100 to P103 : Port10
P110 to P117 : Port11
INTP0 to INTP5 : Interrupt From Peripherals
TI00, TI01 : Timer Input
TI1, TI2 : Timer Input
TO0 to TO2 : Timer Output
SB0, SB1 : Serial Bus
SI0, SI2 : Serial Input
$\overline{SO0}$, $\overline{SO2}$: Serial Output
$\overline{SCK0}$, $\overline{SCK2}$: Serial Clock
SCL : Serial Clock
SDA0/SDA1 : Serial Data
RxD : Receive Data
TxD : Transmit Data
ASCK : Asynchronous Serial Clock
PCL : Programmable Clock
BUZ : Buzzer Clock

S0 to S39 : Segment Output
COM0 to COM3 : Common Output
V_{LC0} to V_{LC2} : LCD Power Supply
BIAS : LCD Power Supply Bias Control
X1, X2 : Crystal (Main System Clock)
$\overline{XT1}$, XT2 : Crystal (Subsystem Clock)
$\overline{RESET}$: Reset
ANI0 to ANI7 : Analog Input
AV_{DD} : Analog Power Supply
AV_{SS} : Analog Ground
AV_{REF} : Analog Reference Voltage
V_{DD} : Power Supply
V_{SS} : Ground
IC : Internally Connected



Note The internal ROM & RAM capacity depends on the product.

3. PIN FUNCTIONS

3.1 PORT PINS (1/2)

Pin Name	I/O	Function		After Reset	Dual-Function Pin
P00	Input	Port 0 7-bit I/O port.	Input only	Input	INTP0/TI00
P01	Input/output		Input/output can be specified bit-wise. When used as an input port, pull-up resistor can be con-nected by software.	Input	INTP1/TI01
P02					INTP2
P03					INTP3
P04					INTP4
P05					INTP5
P07*1	Input		Input only	Input	XT1
P10 to P17	Input/output	Port 1 8-bit input/output port. Input/output can be specified bit-wise. When used as an input port, pull-up resistor can be connected by software.*2		Input	ANI0 to ANI7
P25	Input/output	Port 2 3-bit input/output port. Input/output can be specified bit-wise. When used as an input port, pull-up resistor can be connected by software.		Input	SI0/SB0/SDA0
P26					SO0/SB1/SDA1
P27					$\overline{SCK0}$/SCL
P30	Input/output	Port 3 8-bit input/output port. Input/output can be specified bit-wise. When used as an input port, pull-up resistor can be connected by software.		Input	TO0
P31					TO1
P32					TO2
P33					TI1
P34					TI2
P35					PCL
P36					BUZ
P37					——
P70	Input/output	Port 7 3-bit input/output port. Input/output can be specified bit-wise. When used as an input port, pull-up resistor can be connected by software.		Input	SI2/RxD
P71					SO2/TxD
P72					$\overline{SCK2}$/ASCK

* **1.** When using the P07/XT1 pins as an input port, set (1) bit 6 (FRC) of the processor clock control register (the on-chip feedback resistor of the subsystem clock oscillator should not be used).

2. When using the P10/ANI0 to P17/ANI7 pins as the A/D converter analog input, port 1 is set to input mode. However, pull-up resistor is not automatically used.

3.1 PORT PINS (2/2)

Pin Name	I/O	Function	After Reset	Dual-Function Pin
P80 to P87	Input/output	Port 8 8-bit input/output port Input/output can be specified bit-wise. When used as an input port , pull-up resistor can be connected by software. Input/output port/segment signal output function can be specified in 2-bit unit by the LCD control register.	Input	S39 to S32
P90 to P97	Input/output	Port 9 8-bit input/output port Input/output can be specified bit-wise. When used as an input port, pull-up resistor can be connected by software. Input/output port/segment signal output function can be specified in 2-bit unit by the LCD control register.	Input	S31 to S24
P100 to P103	Input/output	Port 10 4-bit input/output port Input/output can be specified bit-wise. When used as an input port, pull-up resistor can be connected by software. LED direct drive capability.	Input	——
P110 to P117	Input/output	Port 11 8-bit input/output port Input/output can be specified bit-wise. When used as an input port, pull-up resistor can be connected by software. Falling edge detection capability.	Input	——

3.2 OTHER PINS (1/2)

Pin Name	I/O	Function	After Reset	Dual-Function Pin
INTP0	Input	External interrupt input by which the effective edge (rising edge, falling edge, or both rising edge and falling edge) can be specified.	Input	P00/TI00
INTP1				P01/TI01
INTP2				P02
INTP3				P03
INTP4				P04
INTP5				P05
SI0	Input	Serial interface serial data input.	Input	P25/SB0/SDA0
SI2				P70/RxD
SO0	Output	Serial interface serial data output.	Input	P26/SB1/SDA1
SO2				P71/TxD
SB0	Input /output	Serial interface serial data input/output.	Input	P25/SI0/SDA0
SB1				P26/SO0/SDA1
SDA0				P25/SI0/SB0
SDA1				P26/SO0/SB1
$\overline{SCK0}$	Input /output	Serial interface serial clock input/output.	Input	P27/SCL
$\overline{SCK2}$				P72/ASCK
SCL				P27/$\overline{SCK0}$
RxD	Input	Asynchronous serial interface serial data input.	Input	P70/SI2
TxD	Output	Asynchronous serial interface serial data output.	Input	P71/SO2
ASCK	Input	Asynchronous serial interface serial clock input.	Input	P72/SCK2
TI00	Input	External count clock input to 16-bit timer (TM0).	Input	P00/INTP0
TI01		Capture trigger signal input to capture register (CR00).		P01/INTP1
TI1		External count clock input to 8-bit timer (TM1).		P33
TI2		External count clock input to 8-bit timer (TM2).		P34
TO0	Input	16-bit timer output (shared with 14-bit PWM output).	Input	P30
TO1		8-bit timer output.		P31
TO2				P32
PCL	Output	Clock output (for main system clock, subsystem clock trimming).	Input	P35
BUZ	Output	Buzzer output.	Input	P36
S0 to S23	Output	LCD controller/driver segment signal output.	Output	——
S24 to S31			Input	P97 to P90
S32 to S39				P87 to P80
COM0 to COM3	Output	LCD controller/driver common signal output.	Output	——
V_{LC0} to V_{LC2}	——	LCD drive voltage. Split resistors can be incorporated by mask option.	——	——
BIAS	——	LCD drive power supply.	——	——

3.2 OTHER PINS (2/2)

Pin Name	I/O	Function	After Reset	Dual-Function Pin
ANI0 to ANI7	Input	A/D converter analog input.	Input	P10 to P17
AV_{REF}	Input	A/D converter reference voltage input.	——	——
★ AV_{DD}	——	A/D converter analog power supply. Connect directly to V_{DD} pin.	——	——
★ AV_{SS}	——	A/D converter ground potential. Connect directly to V_{SS} pin.	——	——
$\overline{RESET}$	Input	System reset input.	——	——
X1	Input	Main system clock oscillation crystal connection.	——	——
X2	——		——	——
XT1	Input	Subsystem clock oscillation crystal connection.	Input	P07
XT2	——		——	——
V_{DD}	——	Positive power supply.	——	——
V_{SS}	——	Ground potential.	——	——
IC	——	Internal connection. Connect directly to V_{SS} pin.	——	——

3.3 PIN I/O CIRCUITS AND RECOMMENDED CONNECTION OF UNUSED PINS

The input/output circuit type of each pin and recommended connection of unused pins are shown in Table 1-1. For the input/output circuit configuration of each type, see Fig. 3-1.

Table 3-1 Input/Output Circuit Type of Each Pin (1/2)

Pin Name	Input/output Circuit Type	I/O	Recommended Connection when not Used
P00/INTP0/TI00	2	Input	Connected to V_{SS}.
P01/INTP1/TI01	8-A	Input/output	Input : Connected to V_{SS}. Output : Leave open.
P02/INTP2			
P03/INTP3			
P04/INTP4			
P05/INTP5			
P07/XT1	16	Input	Connected to V_{SS}.
P10/ANI0 to P17/ANI7	11	Input/output	Input : Connected to V_{DD} or V_{SS}. Output : Leave open.
P25/SI0/SB0/SDA0	10-A	Input/output	Input : Connected to V_{DD} or V_{SS}. Output : Leave open.
P26/SO0/SB1/SDA1			
P27/$\overline{SCK0}$/SCL			
P30/TO0	5-A	Input/output	Input : Connected to V_{DD} or V_{SS}. Output : Leave open.
P31/TO1			
P32/TO2			
P33/TI1	8-A		
P34/TI2			
P35/PCL	5-A		
P36/BUZ			
P37			
P70/SI2/RxD	8-A	Input/output	Input : Connected to V_{DD} or V_{SS}. Output : Leave open.
P71/SO2/TxD	5-A		
P72/$\overline{SCK2}$/ASCK	8-A		

Table 3-1 Input/Output Circuit Type of Each Pin (2/2)

Pin Name	Input/output Circuit Type	I/O	Recommended Connection when not Used
P80/S39 to P87/S32	17-A	Input/ output	Input : Connected to V_{DD} or V_{SS} . Output : Leave open.
P90/S31 to P97/S24	17-A	Input/ output	Input : Connected to V_{DD} or V_{SS} . Output : Leave open.
P100 to P103	5-A	Input/ output	Input : Connected to V_{DD} or V_{SS} . Output : Leave open.
P110 to P117	5-D	Input/ output	Input : Connected to V_{DD} or V_{SS} . Output : Leave open.
S0 to S23	17	Output	Leave open.
COM0 to COM3	18		
V_{LC0} to V_{LC2}	——	——	
BIAS			
$\overline{\text{RESET}}$	2	Input	——
XT2	16	——	Leave open.
AV_{REF}	——		Connected to V_{SS} .
AV_{DD}			Connected to V_{DD} .
AV_{SS}			Connected to V_{SS} .
★ IC			Connected directly to V_{SS} .

Fig. 3-1 Pin Input/Output Circuits (1/2)

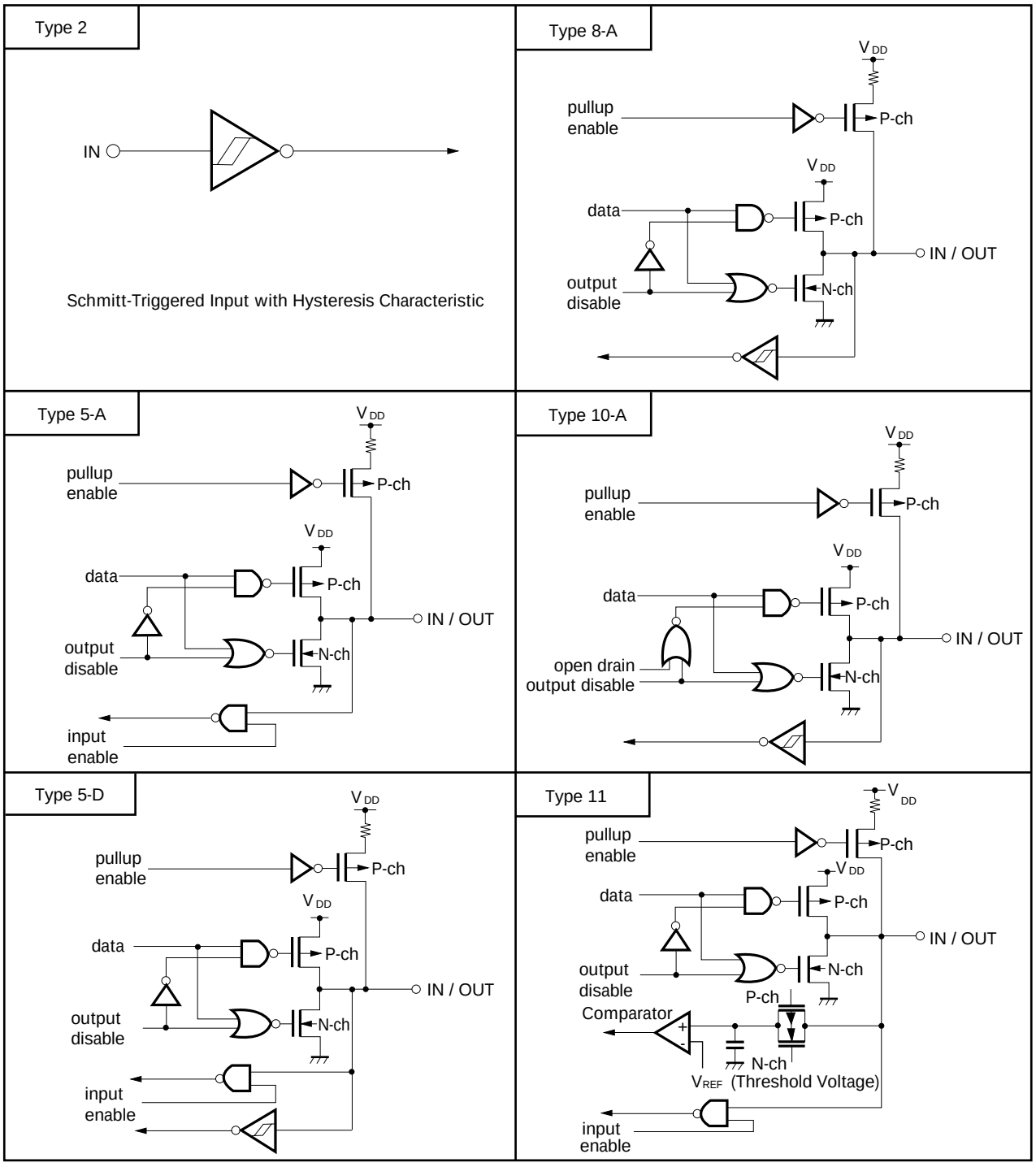
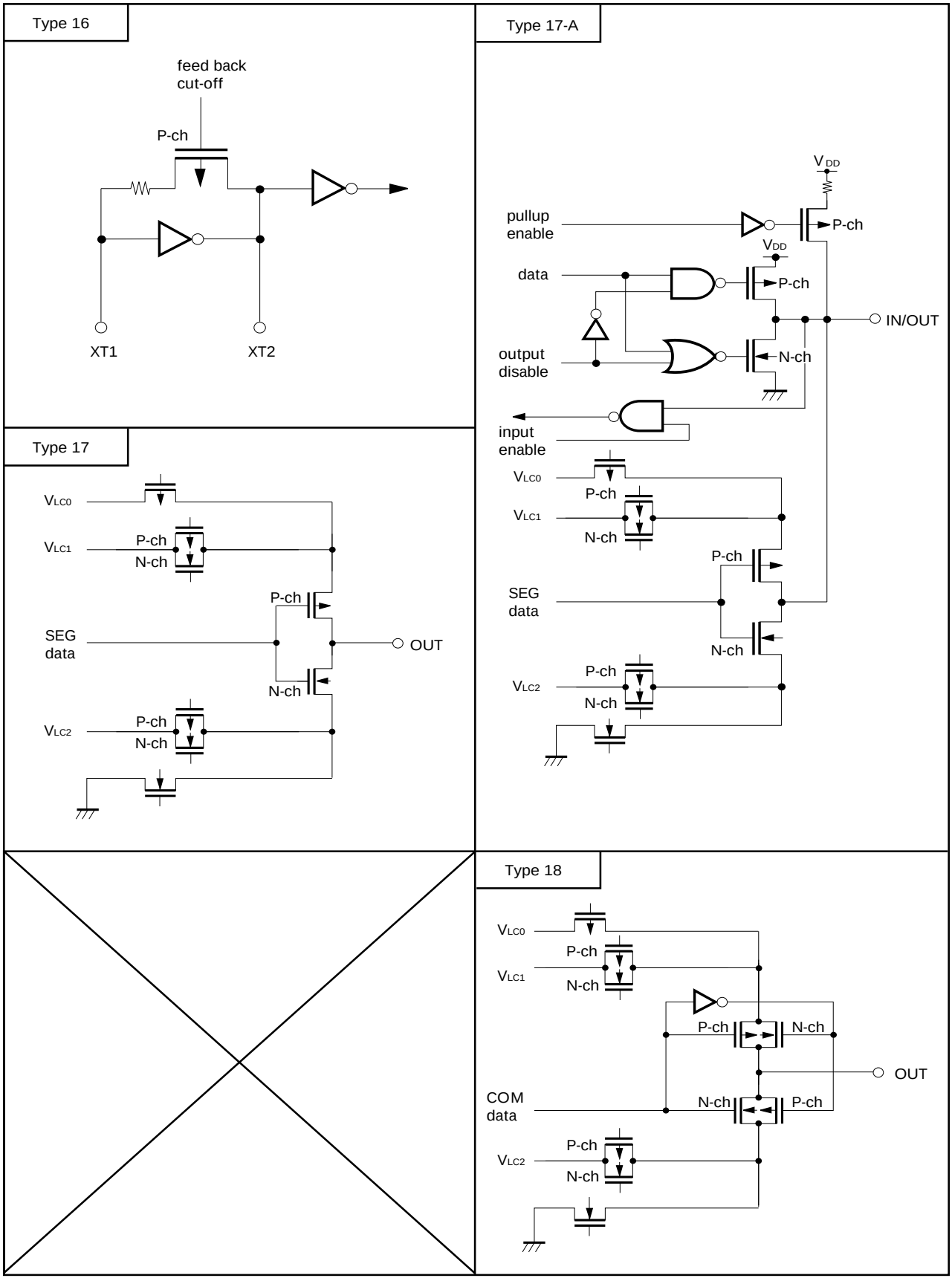


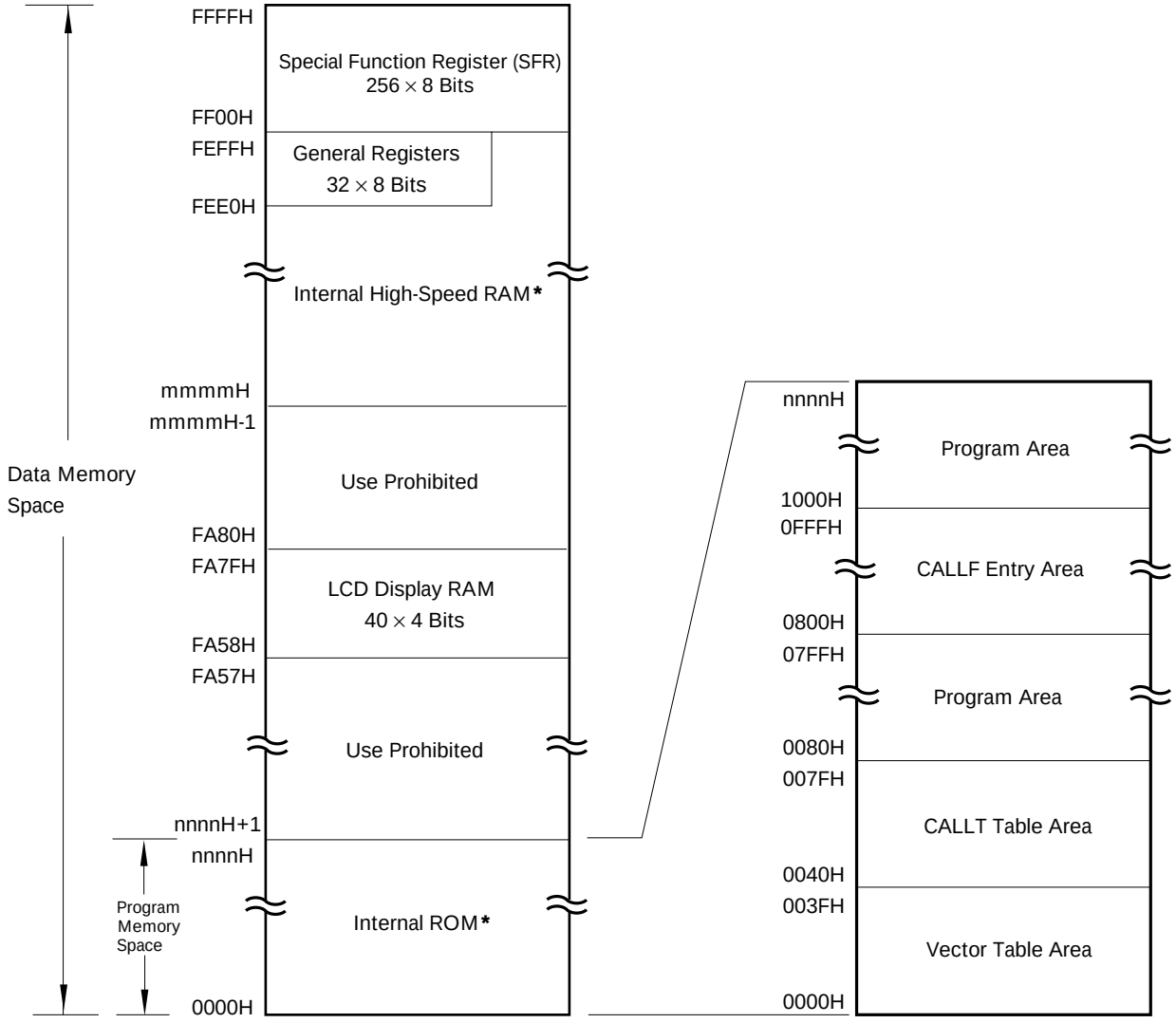
Fig. 3-1 Pin Input/Output Circuits (2/2)



4. MEMORY SPACE

The memory map of μPD78062Y/78063Y/PD78064Y is shown in Fig. 4-1.

Fig. 4-1 Memory Map



* The capacity if Internal ROM and Internal High-Speed RAM differs according to product. (refer to the following table.)

Product	Last Address of Internal ROM nnnnH	Stant Address of Internal High-Speed RAM mmmmH
μPD78062Y	3FFFH	FD00H
μPD78063Y	5FFFH	FB00H
μPD78064Y	7FFFH	

5. PERIPHERAL HARDWARE FUNCTION FEATURE

5.1 PORT

There are two kinds of I/O port.

• CMOS input (P00, P07)	: 2
• CMOS input/output (P01 to P05, Port 1 to 3, 7 to 11)	: 55
Total	: 57

Table 5-1 Functions of Ports

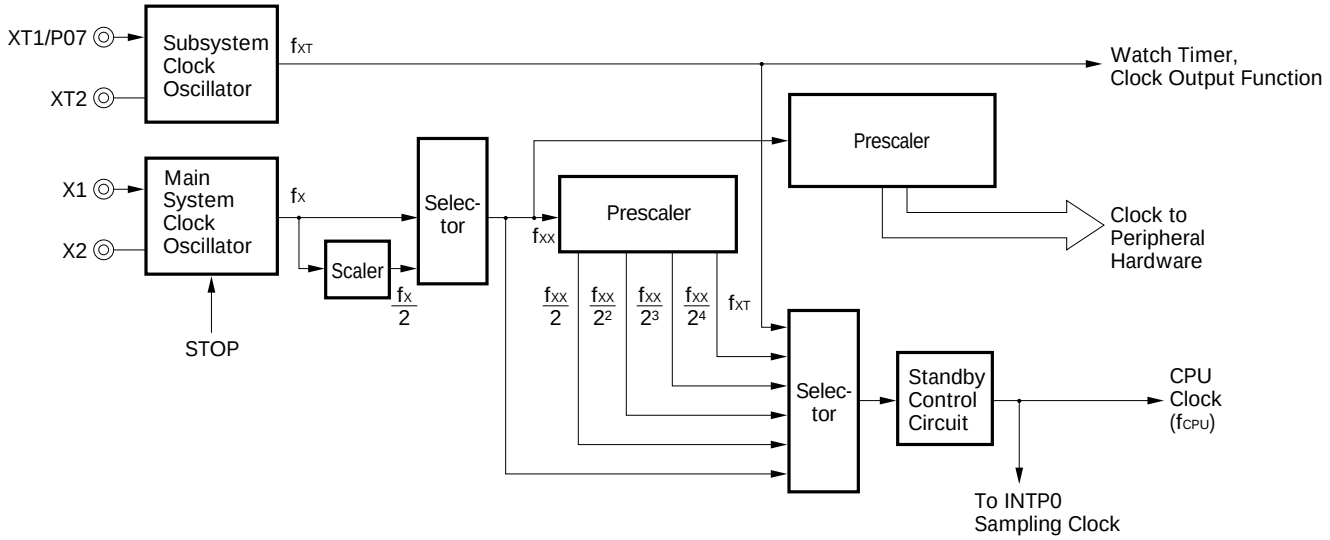
Name	Pin Name	Function
Port 0	P00, P07	Dedicated input port
	P01 to P05	Input/output port. Input/output specifiable bit-wise. When used as input port, on-chip pull-up resistor can be used by software .
Port 1	P10 to P17	Input/output port. Input/output specifialbe bit-wise. When used as input port, on-chip pull-up resistor can be used by software .
Port 2	P25 to P27	Input/output port. Input/output specifiable bit-wise. When used as input port, on-chip pull-up resistor can be used by software .
Port 3	P30 to P37	Input/output port. Input/output specifiable bit-wise. When used as input port, on-chip pull-up resistor can be used by software.
Port 7	P70 to P72	Input/output port. Input/output specifiable bit-wise. When used as input port, on-chip pull-up resistor can be used by software.
Port 8	P80 to P87	Input/output port. Input/output specifiable bit-wise. When used as input port, on-chip pull-up resistor can be used by software. Input/output port/segment signal output function specifiable in 2-bit units by LCD control register.
Port 9	P90 to P97	Input/output port. Input/output specifiable bit-wise. When used as input port, on-chip pull-up resistor can be used by software. Input/output port/segment signal output function specifiable in 2-bit units by LCD control register.
Port 10	P100 to P103	Input/output port. Input/output specifiable bit-wise. When used as input port, on-chip pull-up resistor can be used by software. Direct LED drive capability.
Port 11	P110 to P117	Input/output port. Input/output specifiable bit-wise. When used as input port, on-chip pull-up resistor can be used by software. Test flag (KRIF) is set to 1 by falling edge detection.

5.2 CLOCK GENERATOR

There are two kinds of clocks, main system clock and subsystem clock.
The instruction execution time can also be changed.

- 0.4 μs/0.8 μs/1.6 μs/3.2 μs/6.4 μs/12.8 μs (main system clock: at 5.0 MHz operation)
- 122 μs (subsystem clock: at 32.768 kHz operation)

Fig. 5-1 Clock Generator Block Diagram ★



5.3 TIMER/EVENT COUNTER

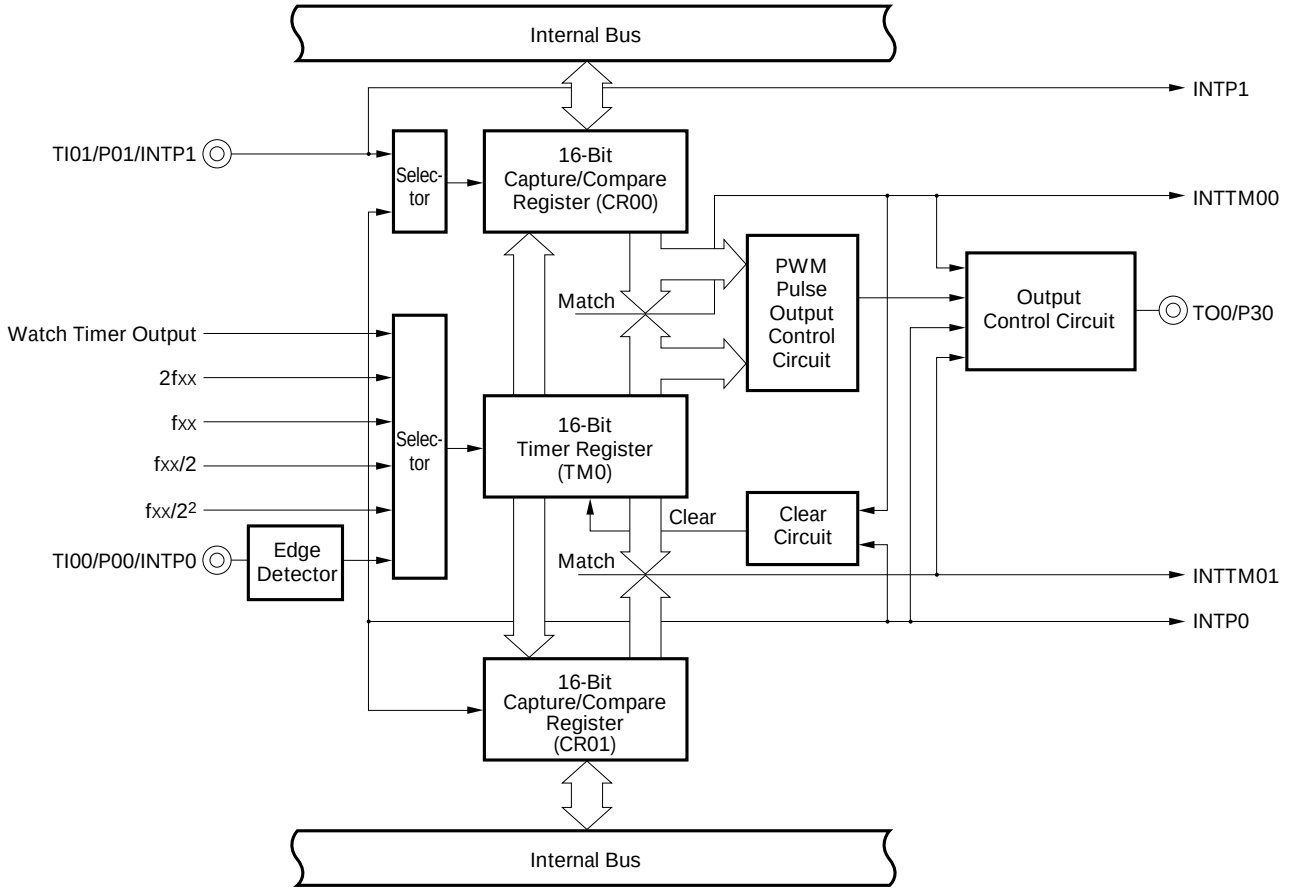
Five timer/event counter channels are incorporated.

- 16-bit timer/event counter : 1 channel
- 8-bit timer/event counter : 2 channels
- Watch timer : 1 channel
- Watchdog timer : 1 channel

Table 5-2 Timer/Event Counter Types and Functions

		16-bit Timer/ Event Counter	8-bit Timer/ Event Counter	Watch Timer	Watchdog Timer
Type	Interval timer	1 channel	2 channels	1 channel	1 channel
	External event counter	1 channel	2 channels	–	–
Function	Timer output	1 output	2 outputs	–	–
	PWM output	1 output	–	–	–
	Pulse width measurement	1 input	–	–	–
	Square wave output	1 output	2 outputs	–	–
	One-shot pulse output	1 output	–	–	–
	Interrupt request	2	2	2	1

★ **Fig. 5-2 16-Bit Timer/Event Counter Block Diagram**



★ **Fig. 5-3 8-Bit Timer/Event Counter Block Diagram**

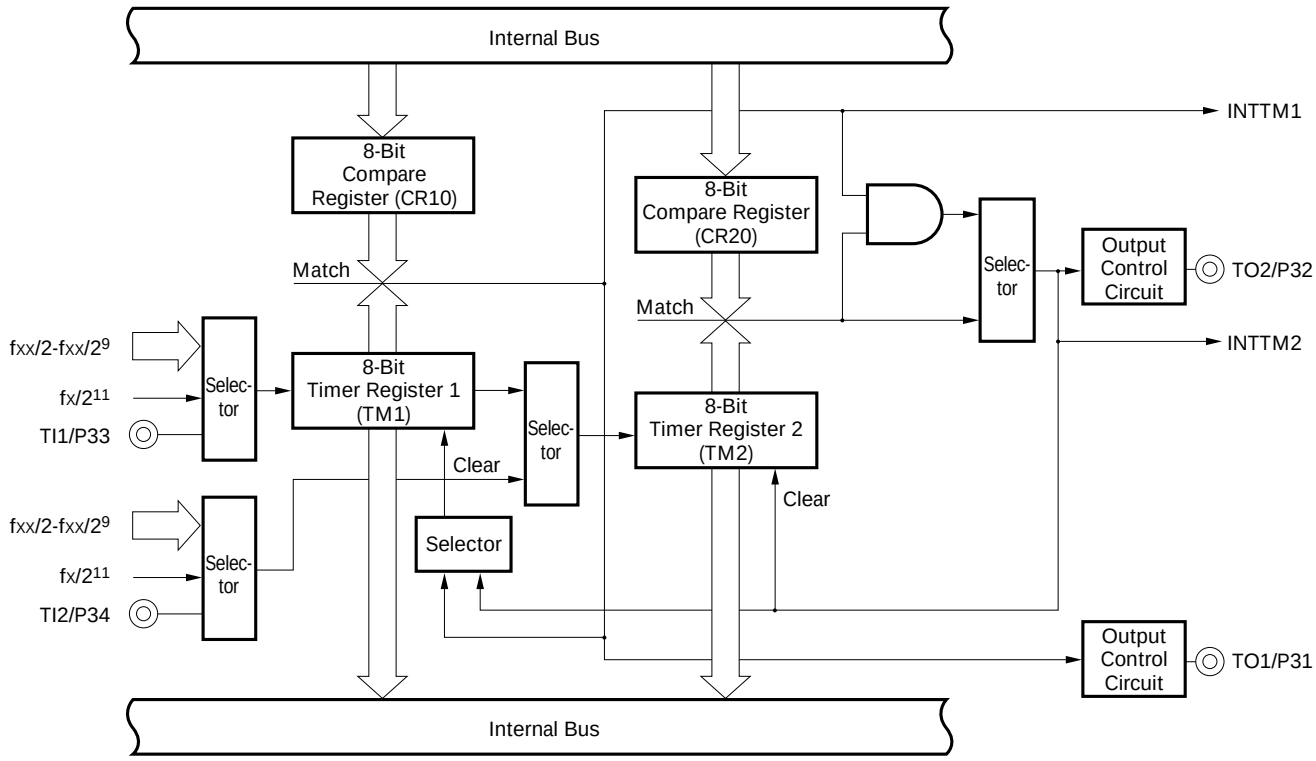


Fig. 5-4 Watch Timer Block Diagram ★

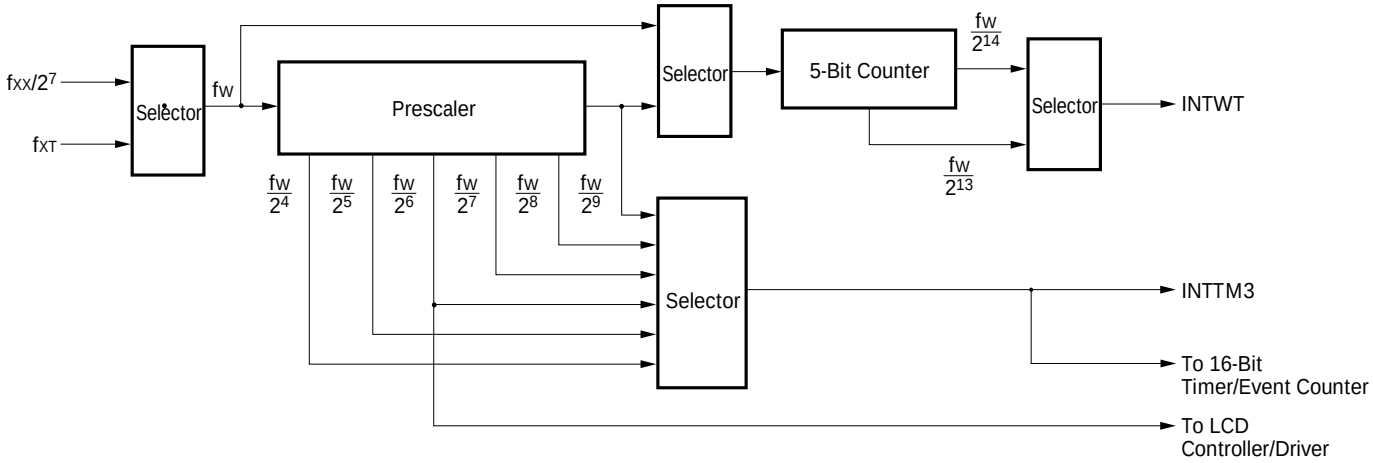
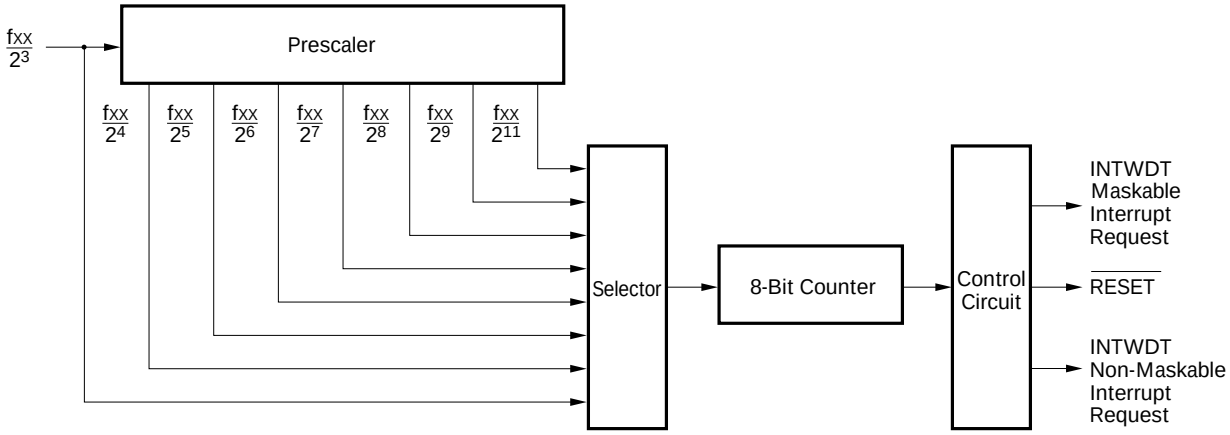


Fig. 5-5 Watchdog Timer Block Diagram ★

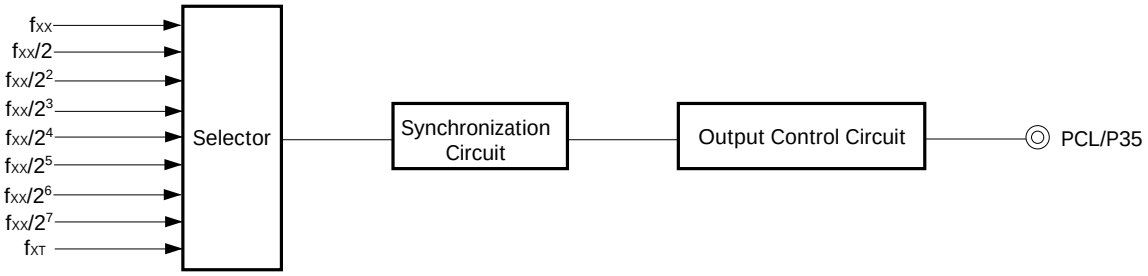


5.4 CLOCK OUTPUT CONTROL CIRCUIT

Clocks of the following frequency can be output as clock outputs.

- 19.5 kHz/39.1kHz/78.1 kHz/156 kHz/313 kHz/625 kHz/1.25 MHz/2.5 MHz/5.0 MHz (main system clock: at 5.0 kHz operation)
- 32.768 kHz (subsystem clock: at 32.768 kHz operation)

★ **Fig. 5-6 Clock Output Circuit Block Diagram**

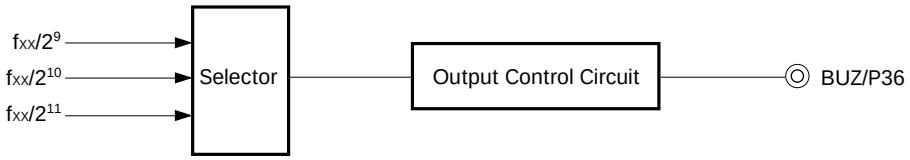


5.5 BUZZER OUTPUT CONTROL CIRCUIT

Clocks of the following frequency can be output as buzzer outputs.

- 1.2 kHz/2.4 kHz/4.9 kHz/9.8 kHz (main system clock : at 5.0 MHz operation)

★ **Fig. 5-7 Buzzer Output Control Circuit Block Diagram**



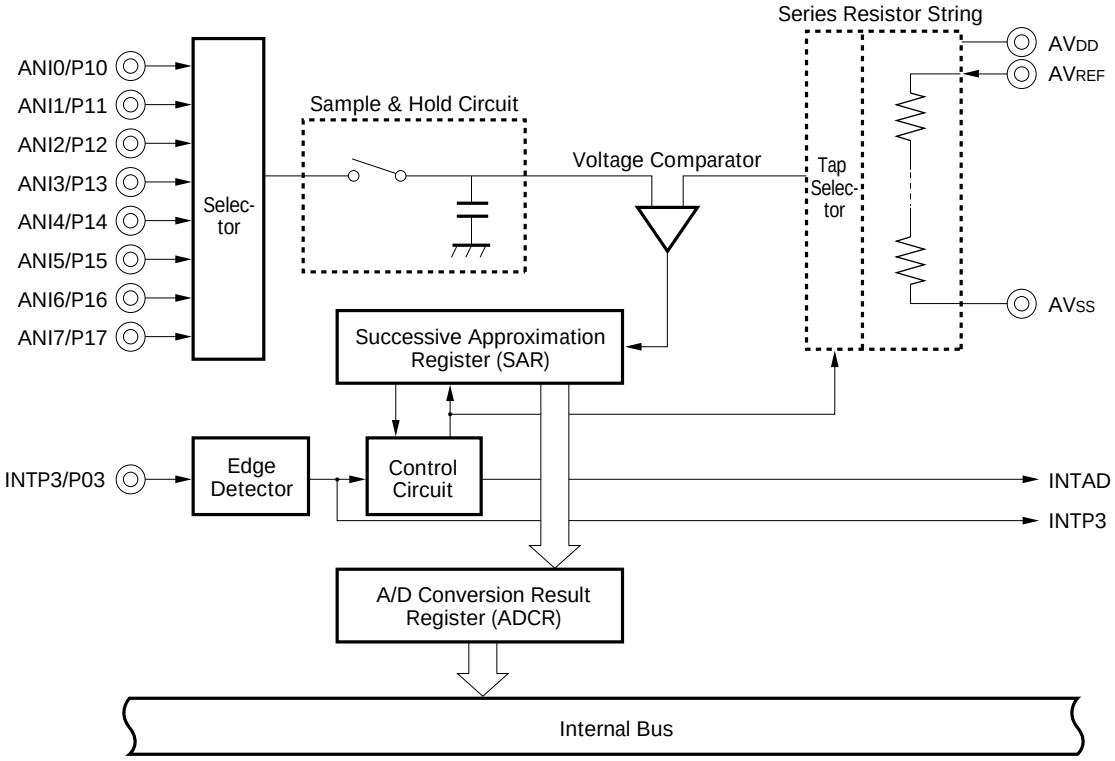
5.6 A/D CONVERTER

Eight 8-bit resolution A/D converter channels are incorporated.

The following two types of start-up method are available.

- Hardware start
- Software start

Fig. 5-8 A/D Converter Block Diagram ★



5.7 SERIAL INTERFACE

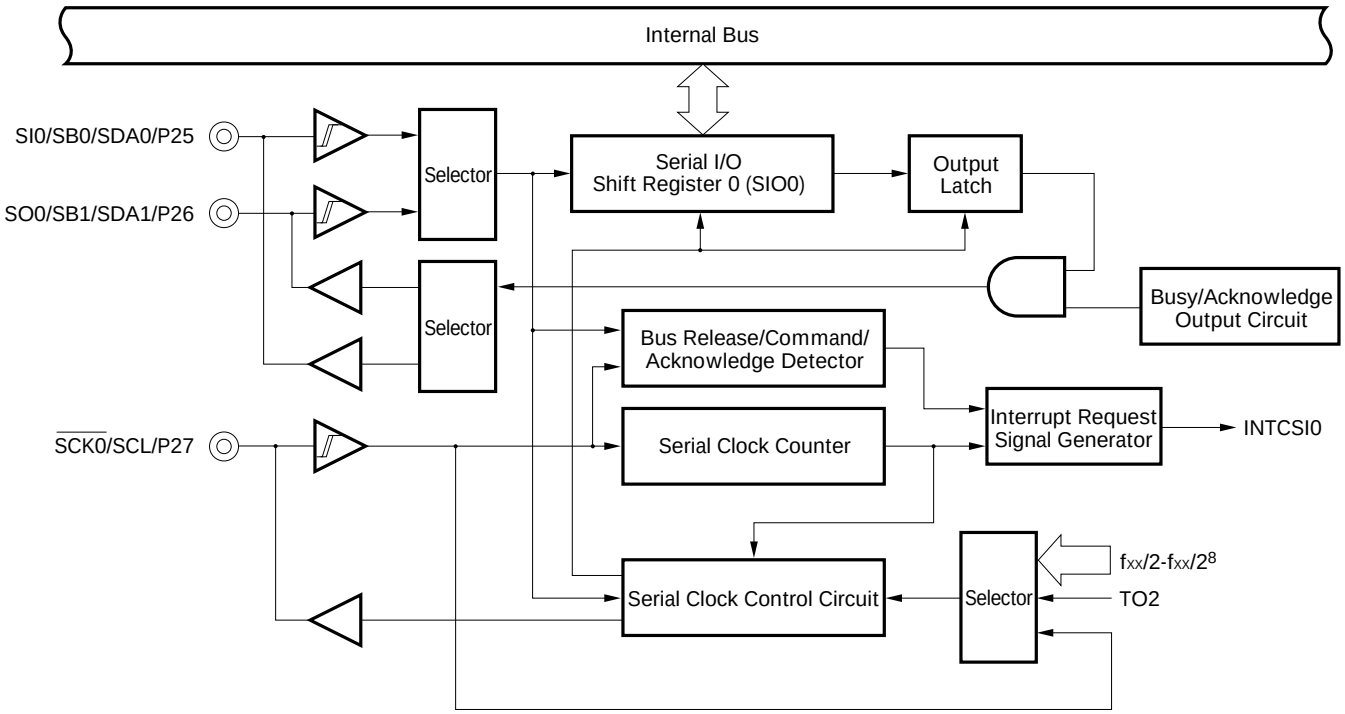
Two clocked serial interface channels are incorporated.

- Serial interface channel 0
- Serial interface channel 2

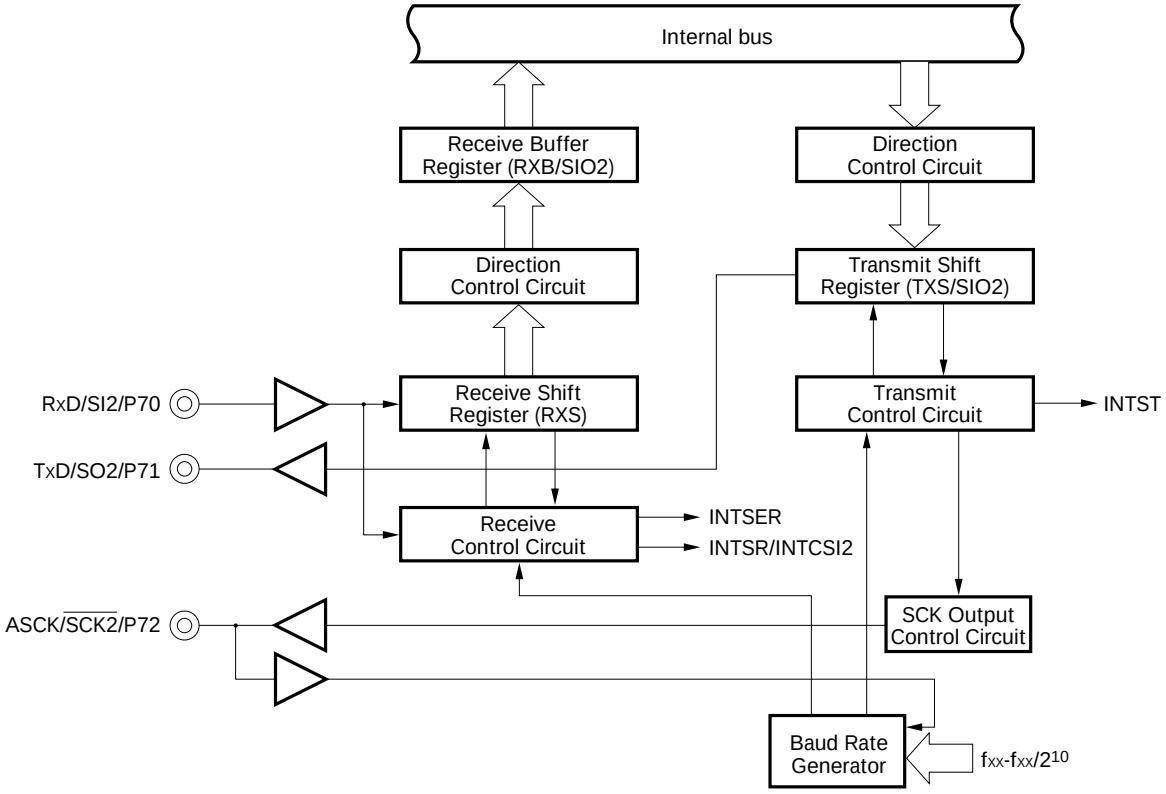
Table 5-3 Serial Interface Channel Block Diagram ★

Function	Serial Interface Channel 0	Serial Interface Channel 2
3-wire serial I/O mode	● (MSB/LSB-first switchable)	● (MSB/LSB-first switchable)
2-wire serial I/O mode	● (MSB-first)	——
Asynchronous serial interface (UART) mode	——	● (Dedicated baud rate generator incorpoorated)
I²C bus mode	● (MSB-first)	——

★ **Fig. 5-9 Serial Interface Channel 0 Block Diagram**



★ **Fig. 5-10 Serial Interface Channel 2 Block Diagram**



5.8 LCD CONTROLLER/DRIVER

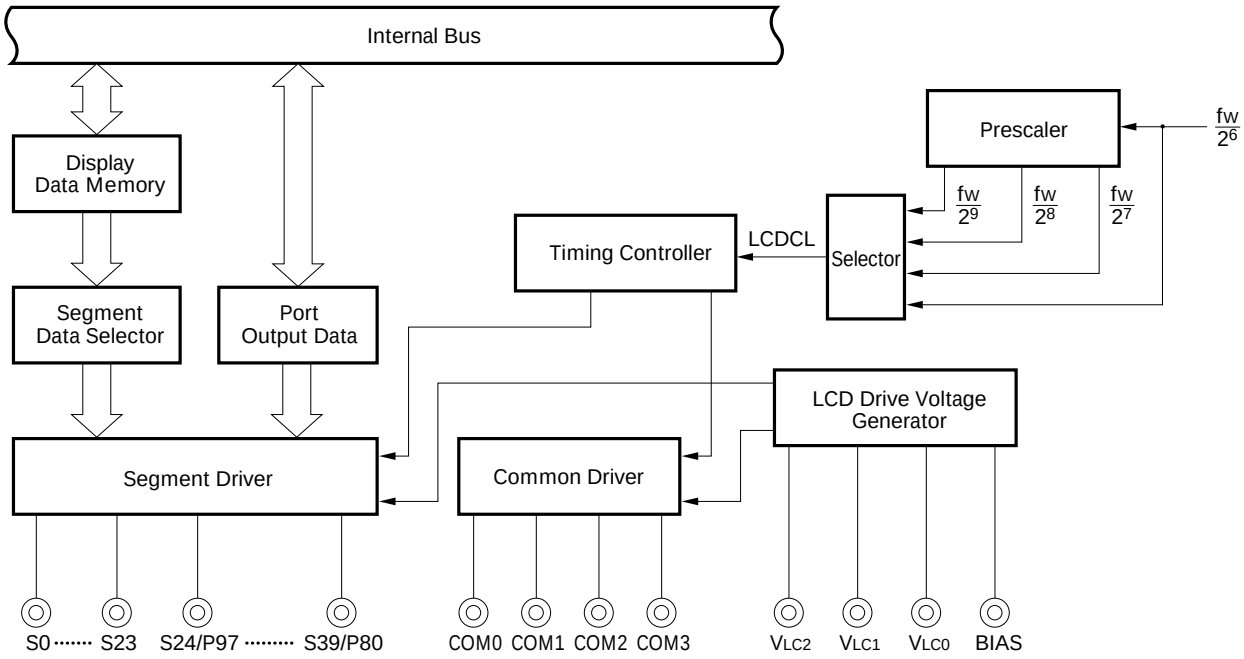
An LCD controller/driver with the following functions is incorporated.

- Selection of 5 types of display mode
- 16 of the segment signal of outputs can be switched to input/output ports in units of 2. (P80 /S39 to P87/S32, P90/S31 to P97/S24)

Table 5-4 Display Mode Types and Maximum Number of Display Pixels

Bias Method	Time Multiplexing	Common Signal Used	Maximum Number of Display Pixels
——	Static	COM0 (COM1 to COM3)	40 (40 segments × 1 common)
1/2	2	COM0, COM1	80 (40 segments × 2 commons)
	3	COM0 to COM2	120 (40 segments × 3 commons)
1/3	3	COM0 to COM2	
	4	COM0 to COM3	160 (40 segments × 4 commons)

Fig. 5-11 LCD Controller/Driver Block Diagram ★



★ 6. INTERRUPT FUNCTIONS AND TEST FUNCTIONS

6.1 INTERRUPT FUNCTIONS

There are twenty of interrupt functions of three different kinds, as shown below.

- Non-maskable interrupt : 1
- Maskable interrupt : 18
- Software interrupt : 1

Table 6-1 Interrupt Source List

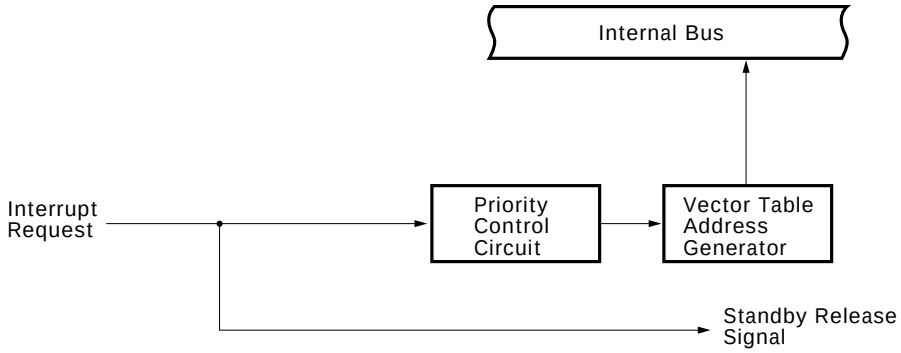
Interrupt Type	Default Priority *1	Interrupt Source		Internal/ External	Vector Table Address	Basic Configuration Type *2
		Name	Trigger			
Non-maskable	——	INTWDT	Watchdog timer overflow (in case of non-maskable interrupt selection)	Internal	0004H	A
Maskable	0	INTWDT	Watchdog timer overflow (in case of interval timer selection)			B
	1	INTP0	Pin input edge detection	External	0006H	C
	2	INTP1			0008H	D
	3	INTP2			000AH	
	4	INTP3			000CH	
	5	INTP4			000EH	
	6	INTP5			0010H	
	7	INTCSI0	Serial interface channel 0 transfer termination	Internal	0014H	B
	8	INTSER	Serial interface channel 2 UART reception error generation		0018H	
	9	INTSR	Serial interface channel 2 UART reception termination		001AH	
		INTCSI2	Serial interface channel 2 3-wire transfer termination			
	10	INTST	Serial interface channel 2 UART transmission termination		001CH	
	11	INTTM3	Reference time interval signal from watch timer		001EH	
	12	INTTM00	16-bit timer register and capture/compare register (CR00) match signal generation		0020H	
	13	INTTM01	16-bit timer register and capture/compare register (CR01) match signal generation		0022H	
	14	INTTM1	8-bit timer/event counter 1 match signal generation		0024H	
	15	INTTM2	8-bit timer/event counter 2 match signal generation		0026H	
	16	INTAD	A/D converter conversion termination		0028H	
Software	——	BRK	BRK instruction execution	Internal	003EH	E

* **1.** Default priority is a priority order when more than one maskable interrupt is generated simultaneously. 0 is the highest and 16 the lowest.

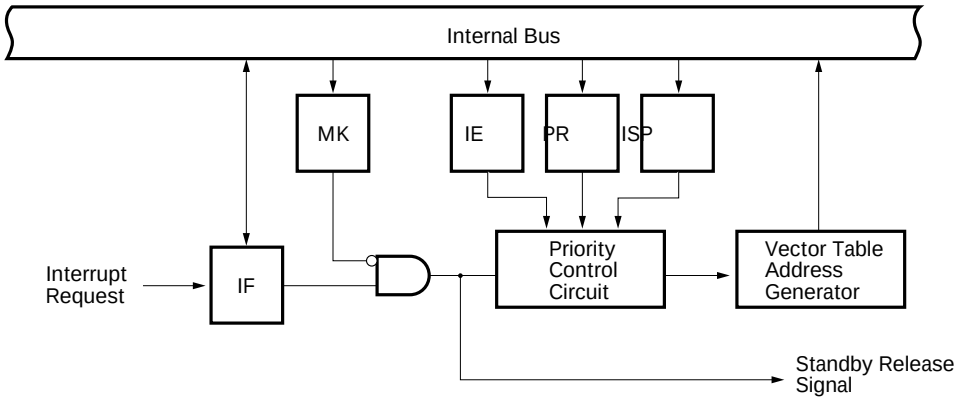
2. Basic configuration types A to E correspond to those shown on the next page.

Fig. 6-1 Basic Configuration of Interrupt Functions (1/2)

(A) Internal non-maskable interrupt



(B) Intrnal maskable interrupt



(C) External maskable interrupt (INTPO)

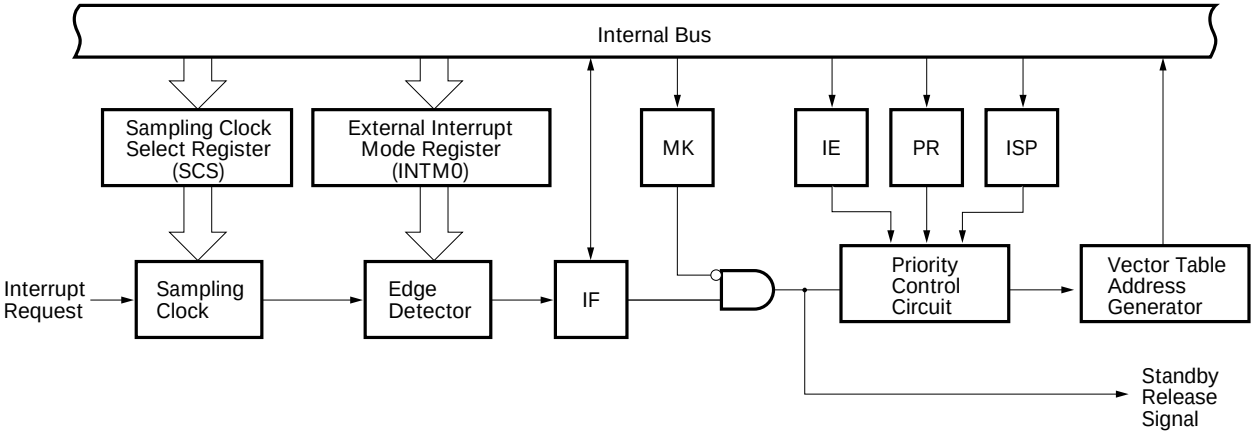
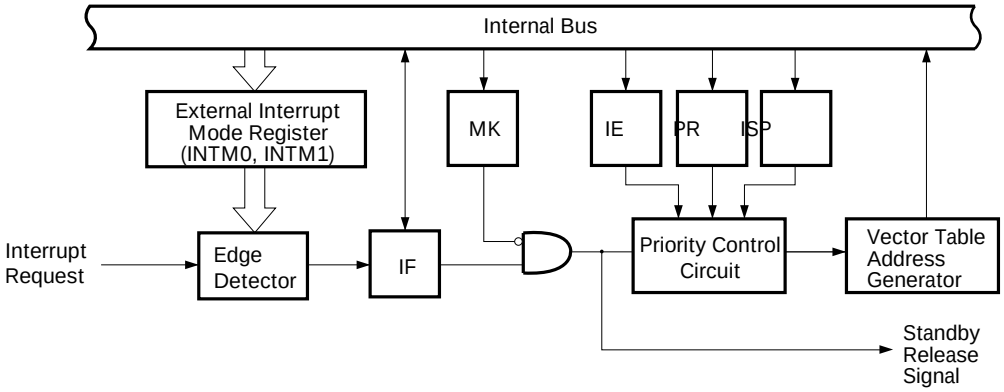
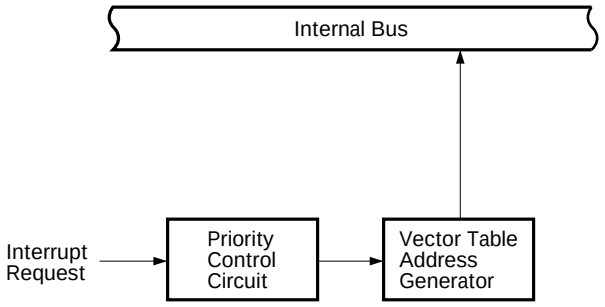


Fig. 6-1 Basic Configuration of Interrupt Functions (2/2)

(D) External maskable interrupt (except INTPO)



(E) Software interrupt



Remarks 1. IF : Interrupt request flag
2. IE : Interrupt enable flag
3. ISP : In-service priority flag
4. MK : Interrupt mask flag
5. PR : Priority specification flag

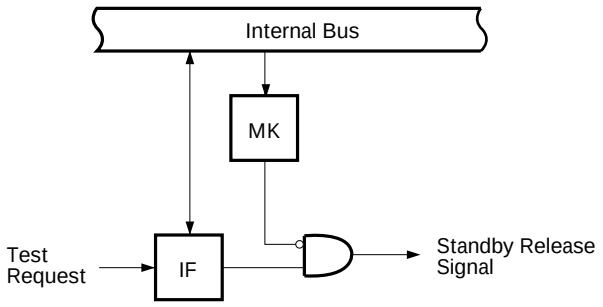
6.2 TEST FUNCTIONS

There are 2 test functions as shown in Table 6-2.

Table 6-2 Test Function List

Test Source		Internal/External
Name	Trigger	
INTWT	Watchtimer overflow	Internal
INTPT11	Port 11 falling edge detection	External

Fig. 6-2 Basic Configuration of Test Function



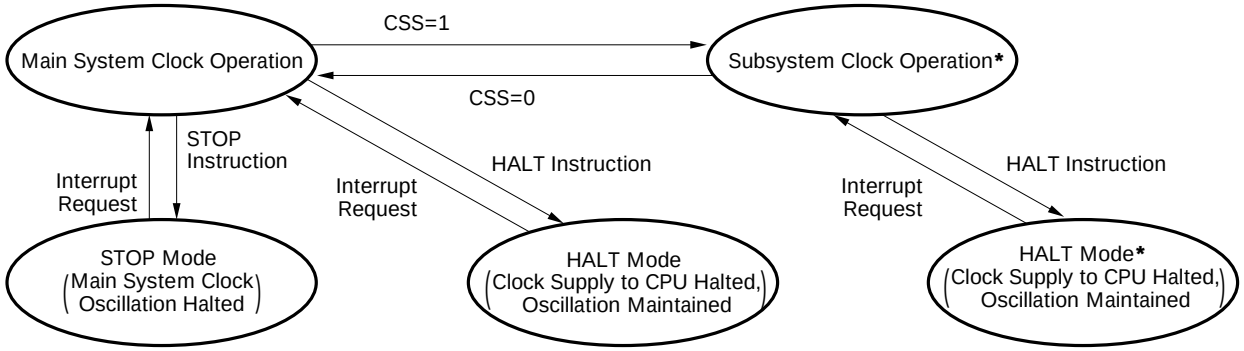
Remarks 1. IF : Test request flag
2. MK : Test mask flag

7. STANDBY FUNCTION ★

The standby function is a function to reduce the consumption current and there are the following two kinds of standby functions.

- HALT mode : Halts CPU operating clock and can reduce average consumption current by the intermittent operation along with the normal operation.
- STOP mode : Halts main system clock oscillation. Halts all operations with the main system clock and sets ultra-low consumption current state with subsystem clock only.

Fig. 7-1 Standby Function



* Halting the main system clock enables the consumption current to be reduced. When the CPU is operated by the subsystem clock, the main system clock should be halted by a MCC setting. The STOP instruction is not available.

Note When the main system clock is stopped and the system is operated by the subsystem clock, the main system clock should be returned to after securing the oscillation stabilization time by a program.

8. RESET FUNCTION

There are the following two kinds of resetting methods.

- External reset by $\overline{\text{RESET}}$ pin.
- Internal reset by watchdog timer runaway time detection.

9. INSTRUCTION SET

(1) 8-bit instruction

MOV, XCH, ADD, ADDC, SUB, SUBS, AND, OR, XOR, CMP, MULU, DIVUW, INC, DEC, ROR, ROL, RORC, ROLC, ROR4, ROL4, PUSH, POP, DBNZ

1st operand \ 2nd operand	#byte	A	r*	sfr	saddr	!addr16	PSW	[DE]	[HL]	[HL+byte] [HL+B] [HL+C]	$addr16	1	None
A	ADD ADDC SUB SUBC AND OR XOR CMP		MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV XCH	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV	MOV XCH	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP		FOR ROL RORC ROLC	
r	MOV	MOV ADD ADDC SUB SUBC AND OR XOR CMP											INC DEC
rl											DBNZ		
sfr	MOV	MOV											
saddr	MOV ADD ADDC SUB SUBC AND OR XOR CMP	MOV									DBNZ		INC DEC
!addr16		MOV											
PSW	MOV	MOV											PUSH POP
[DE]		MOV											
[HL]		MOV											ROR4 ROL4
[HL+byte] [HL+B] [HL+C]		MOV											
X													MULL
C													DIVUW

* Only when rp=BC, DE, HL

(2) 16-bit instruction

MOVW, XCHW, ADDW, SUBW, CMPW, PUSH, POP, INCW, DECW

1st operand \ 2nd operand	#word	AX	rp*	sfrp	saddrp	!addrp	SP	None
A	ADDW SUBW CMPW		MOVW XCHW	MOVW	MOVW	MOVW	MOVW	
rp	MOVW	MOVW*						INCW, DECW PUSH, POP
sfrp	MOVW	MOVW						
saddrp	MOVW	MOVW						
!addr16		MOVW						
SP	MOVW	MOVW						

* Only when rp=BC, DE, HL

(3) Bit manipulation instruction

MOV1, AND1, OR1, XOR1, SET1, CLR1, NOT1, BT, BF, BTCLR

1st operand \ 2nd operand	A.bit	sfr.bit	saddr.bit	PSW.bits	[HL].bit	CY	$addr16	None
A.bit						MOV1	BT BF BTCLR	SET1 CLR1
sfr.bit						MOV1	BT BF BTCLR	SET1 CLR1
saddr.bit						MOV1	BT BF BTCLR	SET1 CLR1
PSW.bit						MOV1	BT BF BTCLR	SET1 CLR1
[HL].bit						MOV1	BT BF BTCLR	SET1 CLR1
CY	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1			SET1 CLR1 NOT1

(4) Call instruction/branch instruction

CALL, CALLF, CALLT, BR, BC, BNC, BZ, BNZ, BT, BF, BTCLR, DBNZ

1st operand \ 2nd operand					
Basic instruction	BR	CALL BR	CALLF	CALLT	BR, BC, BNC, BZ, BNZ
Compound Instruction					BT, BF, BTCLR DBNZ

(5) Other instructions

ADJBA, ADJBS, BRK, RET, RETI, RETB, SEL, NOP, EI, DI, HALT, STOP

10. PACKAGE INFORMATION

100-Pin Plastic QFP (Fine Pitch) (□ 14) (Unit: mm)

100-Pin Plastic QFP (14 × 20) (Unit: mm)

APPENDIX A. DEVELOPMENT PRODUCTS

The following are development tools are available for system development using the μPD78062Y/78063Y/78064Y.

Language Processing Software

RA/78K/0	***1, 2**	Assembler package common to 78K/0 series
CC78K/0	***1, 2**	C compiler package common to 78K/0 series
CC78K/0-L	***1, 2**	C compiler library source file common to 78K/0 series

PROM Write Tool

PG-1500		PROM programmer
PA-78P064GC PA-78P064GF PA-78P064KL-T		Program adapter connected to PG-1500
PG-1500 controller	***1**	PG-1500 control program

Debugging Tool

IE-78000-R		In-circuit emulator common to 78K/0 series
IE-78000-R-BK		Break board common to 78K/0 series
IE-78064-R-EM		Emulation board common to μPD78064 subseries
EP-78064GC-R EP-78064GF-R		Emulation probe common to μPD78064 subseries
EV-9500GC-100		Adapter to be mounted in the user system board manufactured for 100-pin plastic QFP
EV-9200GF-100		Socket to be mounted on the user system board manufactured for 100-pin plastic QFP
SD78K/0	***1**	IE-78000-R screen debugger
DF78064	***1**	Device file common to μPD78064 subseries

Real-Time OS

RA/78K/0	***1, 2**	Real-time OS common to 78K/0 series

Fuzzy Inference Development Support System

FE9000/FE9200	***1**	Fuzzy knowledge creation tool
FT9080/FT9085	***1**	Translator
FI78K0	***1**	Fuzzy inference module
FD78K0	***1**	Fuzzy inference debugger

* 1. PC-9800 series (MS-DOS™) based, IBM PC/AT™ (PC DOS™) based
2. HP9000 series 300™ (HP-UX™) based, SPARCstation™ (Sun OS™) based, EWS-4800™ series (EWS-UX/V™) based

Development Tools Manufactured by 3rd Party

Inquiry Address	Emulator	Assembler	C compiler	Simulator	Debugger	Others
Advanced Data Controls Corporation (tel. : 03-3576-5351)	—	—*	○ (C cross 78K0 compiler)	○ (CXDB/S)	○ (CXDB/E)	—
Gaio Technology Corporation (tel. : 03-3662-3041)	—	○ (XASS-V)	—	○ (XDEB-V)	○ (XDDI-V)	—
Data I/O Japan Corporation (tel. : 03-3436-4041)	—	—	—	—	—	PROM Programmer
Lifeboat Inc. (tel. : 03-3293-4714)	—	—*	○ (ICC78000)	—	—	—
Yokogawa Digital Computer Corporation (tel. : 0422-56-9101)	○ (AD200)	—	—	—	○ (μVIEW)	—

* Assembler is included in C compiler package.

★ APPENDIX B. RELATED DOCUMENTS

Device Related Documents

Document Name	Document No. (Japanese)
μPD78064Y Subseries User's Manual	In preparation
78K/0 Series Instruction Application Table	IEM-5522
78K/0 Series Instruction Set	IEM-5521
μPD78064Y Series Special Function Register Application Table	IEM-5583

Development Tool Related Documents (User's Manual)

Document Name		Document No. (Japanese)
RA78K Series Assembler Package	Operation Volume	EEU-809
	Language Volume	EEU-815
RA78K Series Structured Assembler Preprocessor		EEU-817
CC78K Series C Compiler	Operation Volume	EEU-656
	Language Volume	EEU-655
CC78K Series Library Source File		EEU-777
PG-1500 PROM Programmer		EEU-651
PG-1500 Controller		EEU-704
IE-78000-R		EEU-810
IE-78000-R-BK		EEU-867
IE-78064-R-EM		EEU-905
EP-78064GF-R		EEU-934
SD78K/0 Screen Debugger	Primer	EEU-852
	Reference	EEU-816

Built-In Software Related Documents (User's Manuals)

Document Name		Document No. (Japanese)
78K/0 Series Real-Time OS	Introductory Volume	EEU-912
	Installation Volume	EEU-911
	Debugger Volume	EEU-930
	Technical Volume	EEU-913
Fuzzy Knowledge Data Creation Tools		EEU-829
78K/0, 78K/II, 87AD Series Fuzzy Inference Development Support System Translator		EEU-862
78K/0 Series Fuzzy Inference Development Support System Fuzzy Inference Module		EEU-858
78K/0 Series Fuzzy Inference Development Support System Fuzzy Inference Debugger		EEU-921

Note The above related documents are subject to change without notice. For design purpose, etc., be sure to use the latest documents.

Other Related Documents

Document Name	Document No. (Japanese)
Package Manual	IEI-635
Surface Mount Technology Manual	IEI-616
Quality Grades on Semiconductor Devices	IEI-620
NEC Semiconductor Device Reliability & Quality Control	IEM-5068
Electrostatic Discharge (ESD) Test	MEM-539
Semiconductor Devices Quality Guarantee Guide	MEI-603
Microcomputer Related Products Guide Other Manufacturers Volume	MEI-604

Note The above related documents are subject to change without notice. For design purpose, etc., be sure to use the latest documents.

[MEMO]

Note Purchase of NEC I²C components conveys a license under the Philips I²C Patent Rights to use these components in an I²C system, provided that the system conforms to the I²C Standard Specification as defined by Philips.

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