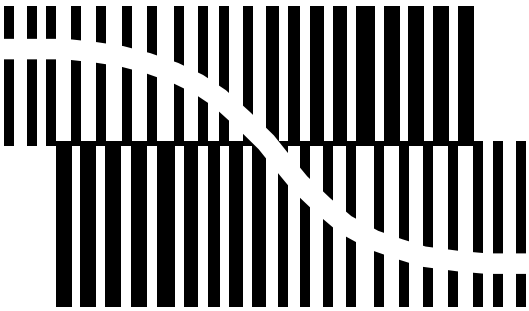
DATA SHEET



BITSTREAM CONVERSION

UDA1340

Low-voltage low-power stereo audio CODEC with DSP features

Preliminary specification
Supersedes data of 1997 May 20
File under Integrated Circuits, IC01

1997 Jul 09

Philips Semiconductors

PHILIPS

Low-voltage low-power stereo audio CODEC with DSP features

UDA1340

FEATURES

General

- Low power consumption
- 3.0 V power supply
- 256, 384 and 512f_s system clock
- Small package size (SSOP28)
- ADC plus integrated high pass filter to cancel DC offset
- Overload detector for easy record level control
- Separate power control for ADC and DAC
- Integrated digital filter plus DAC
- No analog post filter required for DAC
- Easy application
- Functions controllable by microcontroller interface.

Multiple format input interface

- I^2S-bus, MSB-justified and LSB-justified format compatible
- 1f_s input and output format data rate.

DAC digital sound processing

- Digital volume control
- Digital tone control, bass boost and treble
- dB-linear volume and tone control (low microcontroller load)
- Digital de-emphasis for 32, 44.1 and 48 kHz f_s
- Soft mute.

Advanced audio configuration

- Stereo single-ended input configuration
- Stereo line output (under microcontroller volume control)
- Power-down click prevention circuitry
- High linearity, dynamic range, low distortion.

BITSTREAM CONVERSION

GENERAL DESCRIPTION

The UDA1340 is a single-chip stereo Analog-to-Digital Converter (ADC) and Digital-to-Analog Converter (DAC) with signal processing features employing bitstream conversion techniques. The low power consumption and low voltage requirements make the device eminently suitable for use in low-voltage low-power portable digital audio equipment which incorporates recording and playback functions.

The UDA1340 supports the I^2S-bus data format with word lengths of up to 20 bits, the MSB-justified data format with word lengths of up to 20 bits and the LSB justified serial data format with word lengths of 16, 18 and 20 bits.

The UDA1340 has special sound processing features in playback mode, de-emphasis, volume, bass boost, treble, and soft mute, which can be controlled via the microcontroller interface.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
UDA1340M	SSOP28	plastic shrink small outline package; 28 leads; body width 5.3 mm	SOT341-1

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
$V_{DDA(ADC)}$	ADC analog supply voltage		2.7	3.0	3.6	V
$V_{DDA(DAC)}$	DAC analog supply voltage		2.7	3.0	3.6	V
V_{DDO}	operational amplifiers supply voltage		2.7	3.0	3.6	V
V_{DDD}	digital supply voltage		2.7	3.0	3.6	V
$I_{DDA(ADC)}$	ADC supply current		–	4.5	–	mA
$I_{DDA(DAC)}$	DAC supply current		–	3.5	–	mA
I_{DDO}	operational amplifier supply current		–	4	–	mA
I_{DDD}	digital supply current		–	6	–	mA
$I_{PD(ADC)}$	digital ADC power-down supply current		–	3	–	mA
$I_{PD(DAC)}$	digital DAC power-down supply current		–	3	–	mA
T_{amb}	operating ambient temperature		–20	–	+85	°C
Analog-to-digital converter						
$V_{I(rms)}$	input voltage (RMS value)		–	0.8	–	V
(THD + N)/S	total harmonic distortion plus noise-to-signal ratio	at 0 dB	–	–85	–80	dB
		at –60 dB; A-weighted	–	–35	–30	dBA
S/N	signal-to-noise ratio	V_i = 0 V; A-weighted	–	95	–	dBA
α_{cs}	channel separation		–	100	–	dB
Digital-to-analog converter						
$V_{o(rms)}$	output voltage (RMS value)		–	0.8	–	V
(THD + N)/S	total harmonic distortion plus noise-to-signal ratio	at 0 dB	–	–85	–80	dB
		at –60 dB; A-weighted	–	–35	–	dBA
S/N	signal-to-noise ratio	code = 0; A weighted	–	100	–	dBA
α_{cs}	channel separation		–	100	–	dB
Power performance						
P_{ADDA}	power consumption in record and playback mode		–	54	–	mW
P_{DA}	power consumption in playback only mode		–	33	–	mW
P_{AD}	power consumption in record only mode		–	27	–	mW
P_{PD}	power consumption in power-down mode		–	6	–	mW

BLOCK DIAGRAM

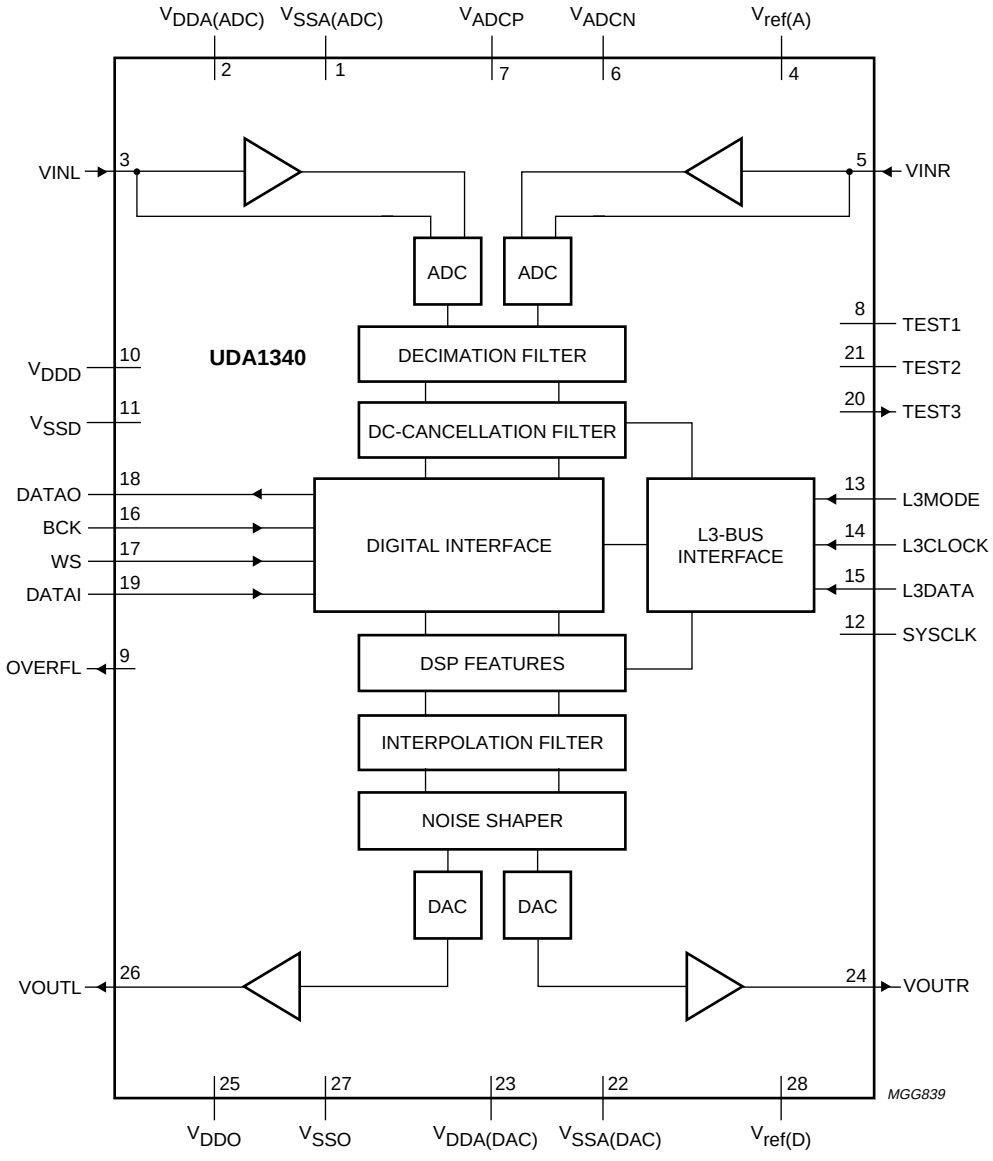


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	Description
$V_{SSA(ADC)}$	1	ADC analog ground
$V_{DDA(ADC)}$	2	ADC analog supply voltage
VINL	3	ADC input left
$V_{ref(A)}$	4	ADC reference voltage
VINR	5	ADC input right
V_{ADCN}	6	ADC negative reference voltage
V_{ADCP}	7	ADC positive reference voltage
TEST1	8	test control 1 (pull-down)
OVERFL	9	overload flag output
V_{DDD}	10	digital supply voltage
V_{SSD}	11	digital ground
SYSCLK	12	system clock 256, 384 or 512f_s
L3MODE	13	L3-bus mode input
L3CLOCK	14	L3-bus clock input
L3DATA	15	L3-bus data input
BCK	16	bit clock input
WS	17	word selection input
DATAO	18	data output
DATAI	19	data input
TEST3	20	test output
TEST2	21	test control 2 (pull-down)
$V_{SSA(DAC)}$	22	DAC analog ground
$V_{DDA(DAC)}$	23	DAC analog supply voltage
VOUTR	24	DAC output right
V_{DDO}	25	operational amplifier supply voltage
VOUTL	26	DAC output left
V_{SSO}	27	operational amplifier ground
$V_{ref(D)}$	28	DAC reference voltage

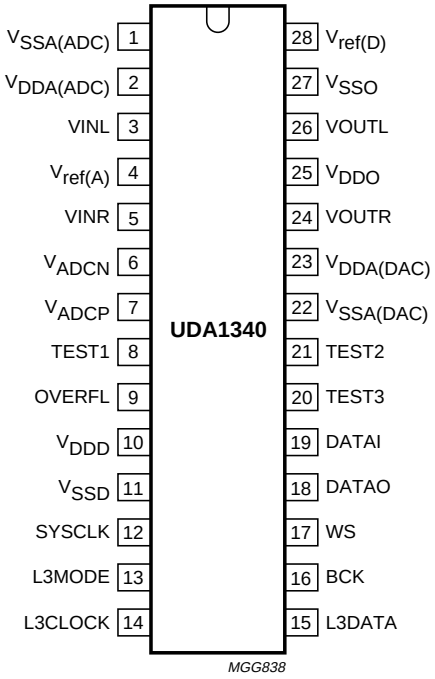


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

System clock

The UDA1340 accommodates slave mode only, this means that in all applications the system devices must provide the system clock. The system frequency is selectable. The options are $256f_s$, $384f_s$ and $512f_s$. The system clock must be locked in frequency to the digital interface input signals.

Multiple format input/output interface

The UDA1340 supports the following data input/output formats:

- I^2S-bus with data word length of up to 20 bits
- MSB justified serial format with data word length of up to 20 bits
- LSB justified serial format with data word lengths of 16, 18 or 20 bits.

The formats are illustrated in Fig.3. Left and right data-channel words are time multiplexed.

Analog-to-Digital Converter (ADC)

The stereo ADC of the UDA1340 consists of two third-order Sigma-Delta modulators. They have a modified Ritchie-coder architecture in a differential switched capacitor implementation. The over-sampling ratio is 128.

Decimation filter (ADC)

The decimation from $128f_s$ is performed in two stages.

The first stage realizes 3rd-order $\frac{\sin x}{x}$ characteristic. This filter decreases the sample rate by 16. The second stage, an FIR filter, consists of 3 half-band filters, each decimating by a factor of 2.

Table 1 Decimation filter characteristics

ITEM	CONDITION	VALUE (dB)
Passband Ripple	$0 - 0.45f_s$	±0.05
Stop band	$>0.55f_s$	–60
Dynamic range	$0 - 0.45f_s$	108
Gain	overall	–1.16

DC cancellation filter (ADC)

An optional IIR high-pass filter is provided to remove unwanted DC components. The operation is selected by the microcontroller via the L3-bus. The filter characteristics are given in Table 2.

Table 2 DC cancellation filter characteristics

ITEM	CONDITION	VALUE (dB)
Passband ripple		none
Passband gain		0
Droop	at $0.00045f_s$	0.031
Attenuation at DC	at $0.00000036f_s$	>40
Dynamic range	$0 - 0.45f_s$	>110

Mute (ADC)

On recovery from power-down or switching on of the system clock, the serial data output DATAO is held LOW until valid data is available from the decimation filter. This time depends on whether the DC cancellation filter is selected:

DC cancel off: time = $\frac{1024}{f_s}$, t = 23.2 ms when f_s = 44.1 kHz

DC cancel on: time = $\frac{12288}{f_s}$, t = 279 ms when f_s = 44.1 kHz

Overload detection (ADC)

In practice the output is used to indicate whenever the output data, in either the left or right channel, is greater than –1 dB (actual figure is –1.16 dB) of the maximum possible digital swing. When this condition is detected the OVERFL output is forced HIGH for at least $512f_s$ cycles (11.6 ms at f_s = 44.1 kHz). This time-out is reset for each infringement.

Interpolation filter (DAC)

The digital filter interpolates from $1f_s$ to $128f_s$ by means of a cascade of a recursive filter and an FIR filter.

Table 3 Interpolation filter characteristics

ITEM	CONDITION	VALUE (dB)
Passband ripple	$0 - 0.45f_s$	±0.03
Stop band	$>0.55f_s$	–50
Dynamic range	$0 - 0.45f_s$	108
Gain	DC	–3.5

Noise shaper (DAC)

The 3rd-order noise shaper operates at $128f_s$. It shifts in-band quantization noise to frequencies well above the audio band. This noise shaping technique enables high signal-to-noise ratios to be achieved. The noise shaper output is converted into an analog signal using a filter stream digital-to-analog converter.

The Filter Stream DAC (FSDAC)

The FSDAC is a semi-digital reconstruction filter that converts the 1-bit data stream of the noise shaper to an analog output voltage. The filter coefficients are implemented as current sources and are summed at virtual ground of the output operational amplifier. In this way very high signal-to-noise performance and low clock jitter sensitivity is achieved. A post-filter is not needed due to the inherent filter function of the DAC. On-board amplifiers convert the FSDAC output current to an output voltage signal capable of driving a line output.

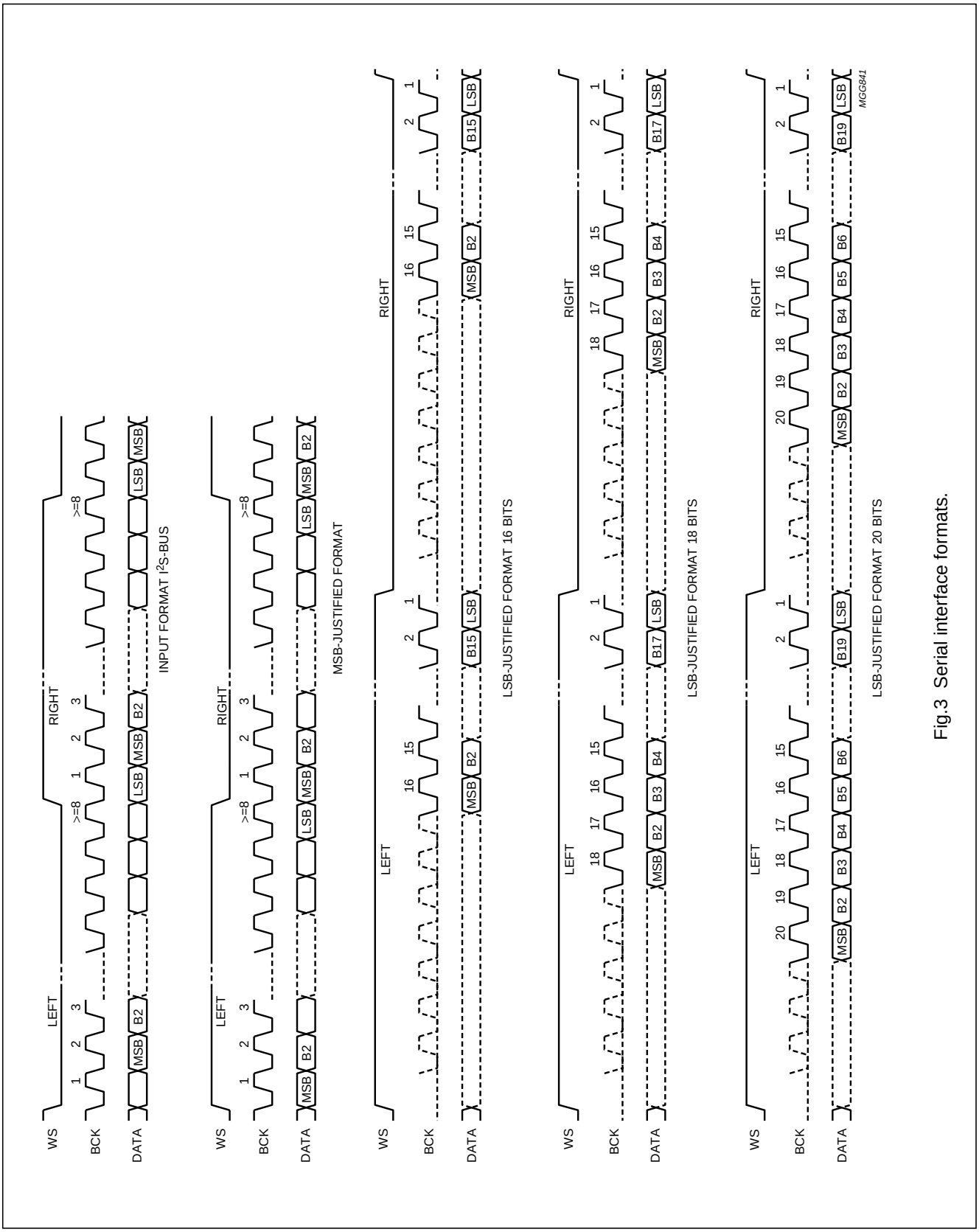


Fig.3 Serial interface formats.

L3-Interface

The UDA1340 has a microcontroller input mode. In the microcontroller mode, all the digital sound processing features and the system controlling features can be controlled by the microcontroller. The controllable features are:

- System clock frequency
- Data input format
- Power control
- DC-filtering
- De-emphasis
- Volume
- Flat/min/max switch
- Bass boost
- Treble
- Mute.

The exchange of data and control information between the microcontroller and the UDA1340 is accomplished through a serial hardware interface comprising the following pins:

L3DATA: microcontroller interface data line

L3MODE: microcontroller interface mode line

L3CLOCK: microcontroller interface clock line.

Information transfer via the microcontroller bus is organized in accordance with the so called ‘L3’ format, in which two different modes of operation can be distinguished; address mode and data transfer mode (see Figs 4 and 5).

The address mode is required to select a device communicating via the L3-bus and to define the destination registers for the data transfer mode. Data transfer for the UDA1340 can only be in one direction, input to the UDA1340 to program its sound processing and other functional features.

Address mode

The address mode is used to select a device for subsequent data transfer and to define the destination registers. The address mode is characterized by L3MODE being LOW and a burst of 8 pulses on L3CLOCK, accompanied by 8 data bits. The fundamental timing is shown in Fig.4. Data bits 0 to 1 indicate the type of subsequent data transfer as given in Table 4.

Table 4 Selection of data transfer

BIT 1	BIT 0	TRANSFER
0	0	DATA (volume, bass boost, treble, de-emphasis, mute, mode and power control)
0	1	not used
1	0	STATUS (system clock frequency, data input format and DC-filter)
1	1	not used

Data bits 7 to 2 represent a 6-bit device address, with bit 7 being the MSB and bit 2 the LSB. The address of the UDA1340 is 000101 (bit 7 to bit 2). In the event that the UDA1340 receives a different address, it will deselect its microcontroller interface logic.

Data transfer mode

The selection preformed in the address mode remains active during subsequent data transfers, until the UDA1340 receives a new address command.
The fundamental timing of data transfers is essentially the same as in the address mode, shown in Fig.4.
The maximum input clock and data rate is $64f_s$.
All transfers are byte wise, i.e. they are based on groups of 8 bits. Data will be stored in the UDA1340 after the eighth bit of a byte has been received. A multibyte transfer is illustrated in Fig.6.

Programming the sound processing and other features

The sound processing and other feature values are stored in independent registers. The first selection of the registers is achieved by the choice of data type that is transferred. This is performed in the address mode, BIT 1 and BIT 0 (see Table 4). The second selection is performed by the 2 MSBs of the data byte (BIT 7 and BIT 6). The other bits in the data byte (BIT 5 to BIT 0) is the value that is placed in the selected registers.

When the data transfer of type ‘data’ is selected, the features VOLUME, BASS BOOST, TREBLE, DE-EMPHASIS, MUTE, MODE and POWER CONTROL can be controlled. When the data transfer of type ‘status’ is selected, the features SYSTEM CLOCK FREQUENCY, DATA INPUT FORMAT and DC-FILTER can be controlled.

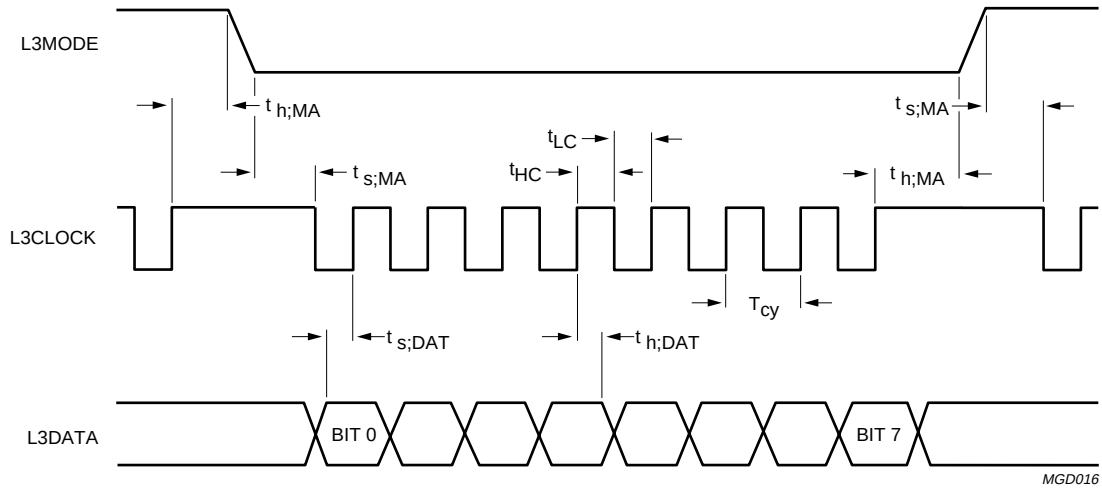


Fig.4 Timing address mode.

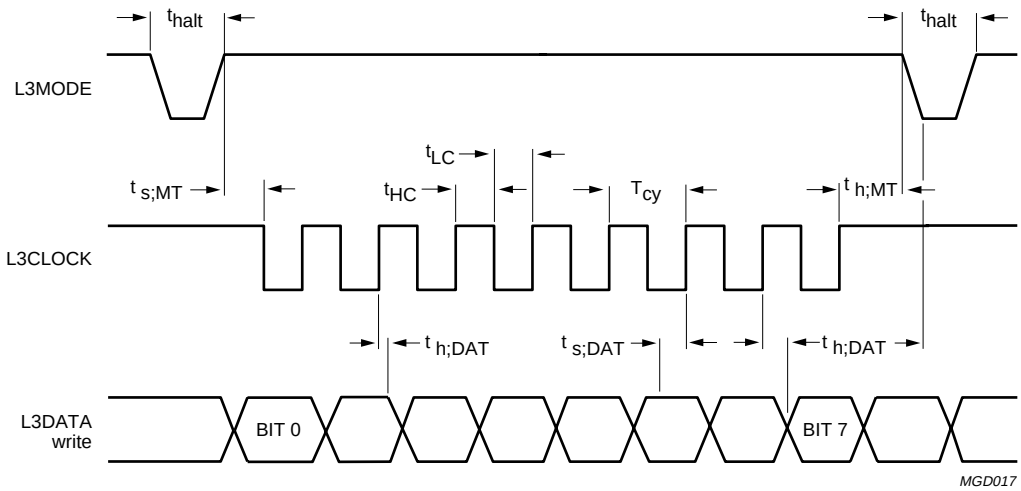


Fig.5 Timing for data transfer mode.

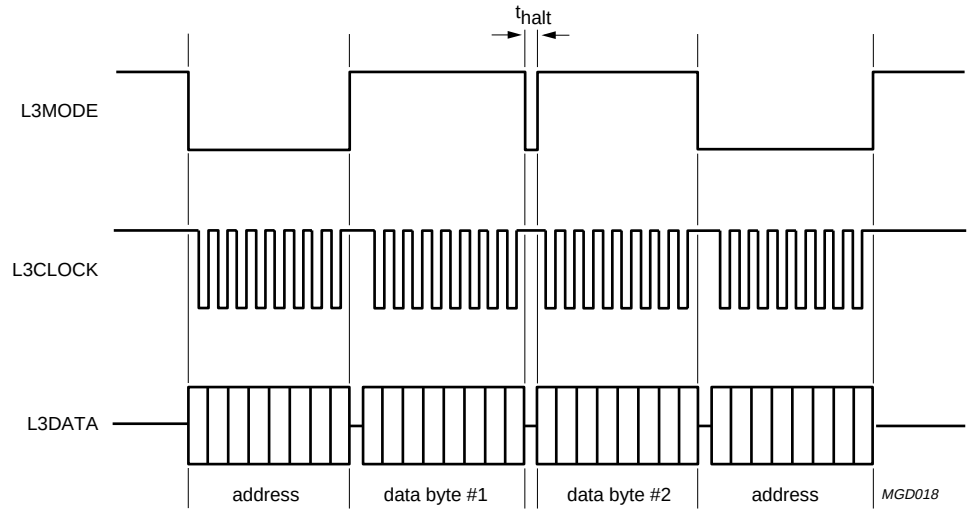


Fig.6 Multibyte transfer.

Table 5 Data transfer of type ‘status’; note 1

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	REGISTER SELECTED
0	X	SC1	SC0	IF2	IF1	IF0	DC	System Clock frequency (1 : 0) data Input Format (2 : 0) DC-filter
1	X	X	X	X	X	X	X	not used

Note

1. X = don’t care.

Table 6 Data transfer of type ‘data’; note 1

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	REGISTER SELECTED
0	0	VC5	VC4	VC3	VC2	VC1	VC0	Volume Control (5 : 0)
0	1	BB3	BB2	BB1	BB0	TR1	TR0	Bass Boost (3 : 0) Treble (1 : 0)
1	0	X	DE1	DE0	MT	M1	M0	DE-emphasis (1 : 0) MuTe Mode (1 : 0)
1	1	X	X	X	X	PC1	PC0	Power Control (1 : 0)

Note

1. X = don’t care.

SYSTEM CLOCK FREQUENCY

A 2-bit value (SC1 and SC0) to select the used external clock frequency (see Table 7).

Table 7 System clock frequency settings

SC1	SC0	FUNCTION
0	0	$512f_s$
0	1	$384f_s$
1	0	$256f_s$
1	1	not used

DATA INPUT FORMAT

A 3-bit value (IF2 to IF0) to select the used data format (see Table 8).

Table 8 Data input format settings

IF2	IF1	IF0	FUNCTION
0	0	0	I^2S-bus
0	0	1	LSB justified, 16 bits
0	1	0	LSB justified, 18 bits
0	1	1	LSB justified, 20 bits
1	0	0	MSB justified
1	0	1	not used
1	1	0	not used
1	1	1	not used

DC-FILTER

A 1-bit value to enable the digital DC-filter (see Table 9).

Table 9 DC-filtering

DC	FUNCTION
0	no DC-filtering
1	DC-filtering

VOLUME CONTROL

A 6-bit value to program the left and right channel volume attenuation (VC5 to VC0). The range is 0 dB to –∞ dB in steps of 1 dB (see Table 10).

Table 10 Volume settings

VC5	VC4	VC3	VC2	VC1	VC0	VOLUME (dB)
0	0	0	0	0	0	0
0	0	0	0	0	1	0
0	0	0	0	1	0	–1
0	0	0	0	1	1	–2
:	:	:	:	:	:	:
1	1	1	0	1	1	–58
1	1	1	1	0	0	–59
1	1	1	1	0	1	–60
1	1	1	1	1	0	–∞
1	1	1	1	1	1	–∞

BASS BOOST

A 4-bit value to program the bass boost setting. The used set depends on the MODE bits.

Table 11 Bass boost settings

BB3	BB2	BB1	BB0	BASS BOOST		
				FLAT SET (dB)	MIN. SET (dB)	MAX. SET (dB)
0	0	0	0	0	0	0
0	0	0	1	0	2	2
0	0	1	0	0	4	4
0	0	1	1	0	6	6
0	1	0	0	0	8	8
0	1	0	1	0	10	10
0	1	1	0	0	12	12
0	1	1	1	0	14	14
1	0	0	0	0	16	16
1	0	0	1	0	18	18
1	0	1	0	0	18	20
1	0	1	1	0	18	22
1	1	0	0	0	18	24
1	1	0	1	0	18	24
1	1	1	0	0	18	24
1	1	1	1	0	18	24

TREBLE

A 2-bit value to program the treble setting. The used set depends on the MODE bits.

Table 12 Treble settings

TR1	TR0	TREBLE		
		FLAT SET (dB)	MIN. SET (dB)	MAX. SET (dB)
0	0	0	0	0
0	1	0	2	2
1	0	0	4	4
1	1	0	6	6

DE-EMPHASIS

A 2-bit value to enable the digital de-emphasis filter.

Table 13 De-emphasis settings

DE1	DE0	FUNCTION
0	0	no de-emphasis
0	1	de-emphasis, 32 kHz
1	0	de-emphasis, 44.1 kHz
1	1	de-emphasis, 48 kHz

MUTE

A 1-bit value to enable the digital mute.

Table 14 Mute

MT	FUNCTION
0	no muting
1	muting

MODE

A 2-bit value to program the mode of the sound processing filters of Bass Boost and Treble. There are three modes: flat, min. and max.

Table 15 The flat/min./max. switch

M1	M0	FUNCTION
0	0	flat
0	1	min.
1	0	min.
1	1	max.

POWER CONTROL

A 2-bit value to disable the ADC and/or DAC to reduce power consumption.

Table 16 Power control settings

PC1	PC0	FUNCTION	
		ADC	DAC
0	0	off	off
0	1	off	on
1	0	on	off
1	1	on	on

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134). All voltage referenced to ground, $V_{DDD} = V_{DDA} = V_{DDO} = 3$ V; $T_{amb} = 25$ °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DDD}	supply voltage	note 1	–	5.0	V
$T_{xtal(max)}$	maximum crystal temperature		–	150	°C
T_{stg}	storage temperature		–65	+125	°C
T_{amb}	operating ambient temperature		–20	+85	°C
V_{es}	electrostatic handling	note 2	–3000	+3000	V
		note 3	–300	+300	V

Notes

1. All V_{DD} and V_{SS} connections must be made to the same power supply.
2. Equivalent to discharging a 100 pF capacitor via a 1.5 kΩ series resistor, except pins 24, 26 and 28 which can withstand ESD pulses of –1500 V to +1500 V.
3. Equivalent to discharging a 200 pF capacitor via a 2.5 μH series inductor.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air	90	K/W

DC CHARACTERISTICS

$V_{DDD} = V_{DDA} = V_{DDO} = 3$ V; $T_{amb} = 25$ °C; $R_L = 5$ kΩ; note 1; all voltages referenced to ground (pins 1, 11, 22 and 27); unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
$V_{DDA(ADC)}$	ADC analog supply voltage		2.7	3.0	3.6	V
$V_{DDA(DAC)}$	DAC analog supply voltage		2.7	3.0	3.6	V
V_{DDO}	operational amplifiers supply voltage		2.7	3.0	3.6	V
V_{DDD}	digital supply voltage		2.7	3.0	3.6	V
$I_{DDA(ADC)}$	ADC supply current	operation mode	–	4.5	–	mA
		ADC power-down	–	200	–	μA
$I_{DDA(DAC)}$	DAC supply current	operation mode	–	3.5	–	mA
		DAC power-down	–	15	–	μA
I_{DDO}	operational amplifier supply current	operation mode	–	4	–	mA
		DAC power-down	–	15	–	μA
I_{DDD}	digital supply current	operation mode	–	6	–	mA
		DAC power-down	–	3	–	mA
		ADC power-down	–	3	–	mA
Digital input pins						
V_{IH}	HIGH level input voltage		$0.8V_{DDD}$	–	$V_{DDD} + 0.5$	V
V_{IL}	LOW level input voltage		–0.5	–	$+0.2V_{DDD}$	V
$\lvert I_{LI} \rvert$	input leakage current		–	–	10	μA
C_i	input capacitance		–	–	10	pF
Digital output pins						
V_{OH}	HIGH level output voltage	$I_{OH} = -2$ mA	$0.85V_{DDD}$	–	–	V
V_{OL}	LOW level output voltage	$I_{OL} = 2$ mA	–	–	0.4	V
Analog-to-digital converter						
V_{ref}	reference voltage	with respect to V_{SSA}	$0.45V_{DDA}$	$0.5V_{DDA}$	$0.55V_{DDA}$	V
$R_{o(ref)}$	V_{refA} reference output resistance	pin 4	–	24	–	kΩ
R_i	input resistance	1 kHz	–	9.8	–	kΩ
C_i	input capacitance		–	20	–	pF
Digital-to-analog converter						
V_{ref}	reference voltage	with respect to V_{SSA}	$0.45V_{DDA}$	$0.5V_{DDA}$	$0.55V_{DDA}$	V
$R_{o(ref)}$	V_{refD} reference output resistance	pin 28	–	28	–	kΩ
R_o	DAC output resistance		–	0.13	3.0	Ω
$I_{o(max)}$	maximum output current	(THD + N)/S < 0.1% $R_L = 5$ kΩ	–	0.22	–	mA
R_L	load resistance		3	–	–	kΩ
C_L	load capacitance	note 2	–	–	200	pF

Notes

1. All power supply pins (V_{DD} and V_{SS}) must be connected to the same external power supply unit.
2. When higher capacitive loads must be driven then a 100 Ω resistor must be connected in series with the DAC output in order to prevent oscillations in the output operational amplifier.

AC CHARACTERISTICS (ANALOG)

$V_{DDD} = V_{DDA} = V_{DDO} = 3$ V; $f_i = 1$ kHz; $T_{amb} = 25$ °C; $R_L = 5$ kΩ all voltages referenced to ground (pins 1, 11, 22 and 27); unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Analog-to-digital converter						
$V_{i(rms)}$	input voltage (RMS value)		–	0.8	–	V
ΔV_i	unbalance between channels		–	0.1	–	dB
(THD + N)/S	total harmonic distortion plus noise-to-signal ratio	at 0 dB	–	–85	–80	dB
		at –60 dB; A-weighted	–	–35	–30	dBA
S/N	signal-to-noise ratio	$V_i = 0$ V; A-weighted	–	95	–	dBA
α_{CS}	channel separation		–	100	–	dB
PSRR	power supply rejection ratio	$f_{ripple} = 1$ kHz; $V_{ripple(p-p)} = 30$ mV	–	30	–	dB
Digital-to-analog converter						
$V_{o(rms)}$	output voltage (RMS value)		–	0.8	–	V
ΔV_o	unbalance between channels		–	0.1	–	dB
(THD + N)/S	total harmonic distortion plus noise-to-signal ratio	at 0 dB	–	–85	–80	dB
		at –60 dB; A-weighted	–	–35	–	dBA
S/N	signal-to-noise ratio	code = 0; A-weighted	–	100	–	dBA
α_{cs}	channel separation		–	80	–	dB
PSRR	power supply rejection ratio	$f_{ripple} = 1$ kHz; $V_{ripple(p-p)} = 100$ mV	–	50	–	dB

AC CHARACTERISTICS (DIGITAL)

$V_{DDD} = V_{DDA} = V_{DDO}$ = 2.7 to 3.6 V; T_{amb} = –20 to +85 °C; R_L = 5 kΩ; all voltages referenced to ground (pins 1, 11, 22 and 27); unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
T_{cy}	clock cycle	$f_{sys} = 256f_s$	78	88	131	ns
		$f_{sys} = 384f_s$	52	59	87	ns
		$f_{sys} = 512f_s$	39	44	66	ns
t_{CWL}	f_{sys} LOW level pulse width	f_{sys} < 19.2 MHz	30	–	70	$\%T_{sys}$
		$f_{sys} \geq$ 19.2 MHz	40	–	60	$\%T_{sys}$
t_{CWH}	f_{sys} HIGH level pulse width	f_{sys} < 19.2 MHz	30	–	70	$\%T_{sys}$
		$f_{sys} \geq$ 19.2 MHz	40	–	60	$\%T_{sys}$
Serial input/output data timing; see Fig.7						
t_{BCK}	bit clock period		$^1/_{64}f_s$	–	–	ns
$t_{BCK(H)}$	bit clock HIGH time		100	–	–	ns
$t_{BCK(L)}$	bit clock LOW time		100	–	–	ns
t_r	rise time		–	–	20	ns
t_f	fall time		–	–	20	ns
$t_{s;DATI}$	data input set-up time		20	–	–	ns
$t_{h;DATI}$	data input hold time		0	–	–	ns
$t_{d(DATO)(BCK)}$	data output delay time (from BCK falling edge)		–	–	80	ns
$t_{d(DATO)(WS)}$	data output delay time (from WS edge)	MSB-justified format	–	–	80	ns
$t_{h;DATO}$	data output hold time		0	–	–	ns
$t_{s;WS}$	word selection set-up time		20	–	–	ns
$t_{h;WS}$	word selection hold time		10	–	–	ns
Address and data transfer mode timing; see Figs 4 and 5						
T_{cy}	L3CLK cycle time		500	–	–	ns
t_{HC}	L3CLK HIGH period		250	–	–	ns
t_{LC}	L3CLK LOW period		250	–	–	ns
$t_{s;MA}$	L3MODE set-up time	address mode	190	–	–	ns
$t_{h;MA}$	L3MODE hold time	address mode	190	–	–	ns
$t_{s;MT}$	L3MODE set-up time	data transfer mode	190	–	–	ns
$t_{h;MT}$	L3MODE hold time	data transfer mode	190	–	–	ns
$t_{s;DAT}$	L3DATA set-up time	data transfer mode and address mode	190	–	–	ns
$t_{h;DAT}$	L3DATA hold time	data transfer mode and address mode	30	–	–	ns
t_{halt}	L3MODE halt time		190	–	–	ns

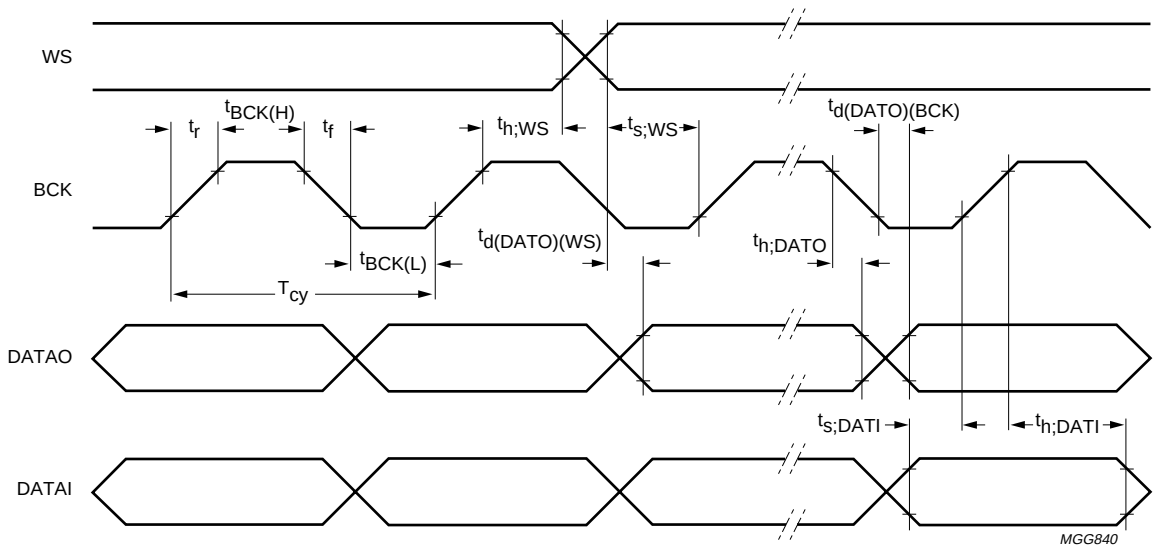


Fig.7 Serial interface timing.

APPLICATION INFORMATION

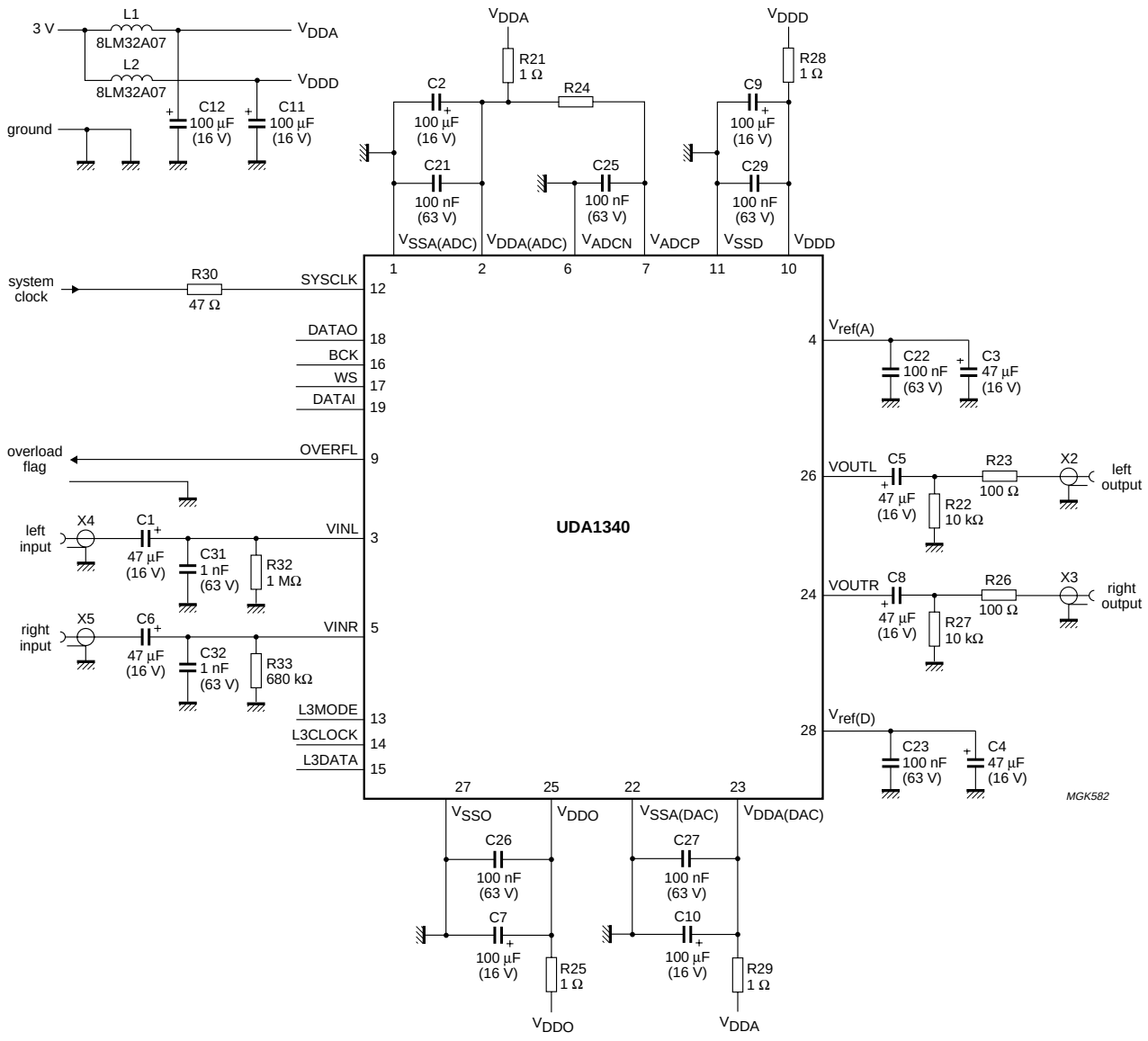
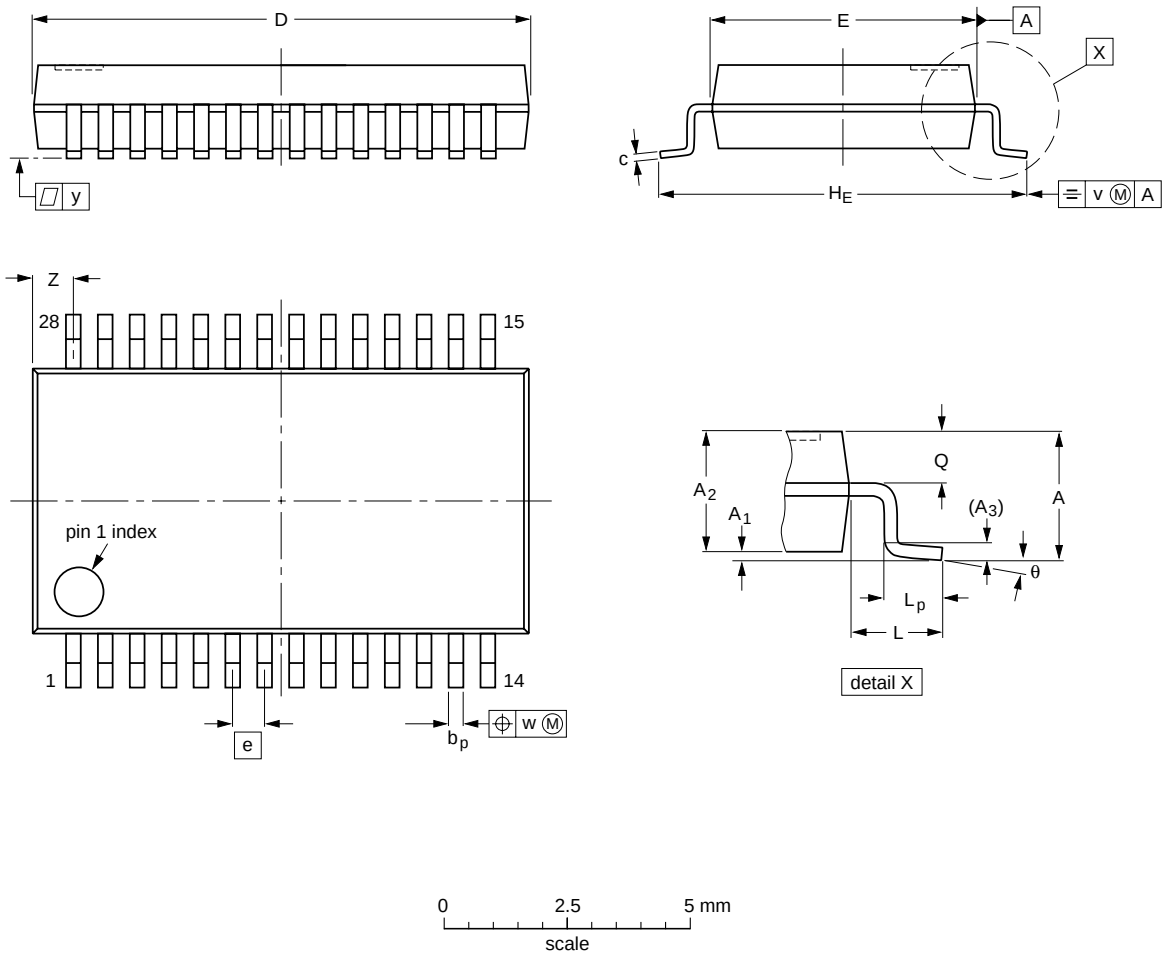


Fig.8 Application diagram.

PACKAGE OUTLINE

SSOP28: plastic shrink small outline package; 28 leads; body width 5.3 mm **SOT341-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.0	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	10.4 10.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.1 0.7	8^o 0^o

Note

1. Plastic or metal protrusions of 0.20 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT341-1		MO-150AH				~~93-09-08~~ 95-02-04

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

Reflow soldering

Reflow soldering techniques are suitable for all SSOP packages.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

Wave soldering

Wave soldering is **not** recommended for SSOP packages. This is because of the likelihood of solder bridging due to closely-spaced leads and the possibility of incomplete solder penetration in multi-lead devices.

If wave soldering cannot be avoided, the following conditions must be observed:

- **A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.**
- **The longitudinal axis of the package footprint must be parallel to the solder flow and must incorporate solder thieves at the downstream end.**

Even with these conditions, only consider wave soldering SSOP packages that have a body width of 4.4 mm, that is SSOP16 (SOT369-1) or SSOP20 (SOT266-1).

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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Printed in The Netherlands 547027/1200/02/pp24 Date of release: 1997 Jul 09 Document order number: 9397 750 02548

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