## Features

- High-performance CMOS non-volatile static RAM 2048 x 8 bits
- 25, 35 and 45 ns Access Times
- 12, 20 and 25 ns Output Enable Access Times
- $I_{CC}$ = 15 mA at 200 ns Cycle Time
- Automatic STORE to EEPROM on Power Down using system capacitance
- Software initiated STORE (STORE Cycle Time < 10 ms)
- Automatic STORE Timing
- $10^6$ STORE cycles to EEPROM
- 100 years data retention in EEPROM
- Automatic RECALL on Power Up
- Software RECALL Initiation (RECALL Cycle Time < 20 µs)
- Unlimited RECALL cycles from EEPROM
- Single 5 V ± 10 % Operation
- Operating temperature ranges:
  - 0 to 70 °C
  - -40 to 85 °C
- QS 9000 Quality Standard
- ESD protection > 2000 V (MIL STD 883C M3015.7-HBM)
- RoHS compliance and Pb- free
- Packages: PDIP24 (600 mil)
  - SOP24 (300 mil)

## Description

The U635H16 has two separate modes of operation: SRAM mode and nonvolatile mode. In SRAM mode, the memory operates as an ordinary static RAM. In nonvolatile operation, data is transferred in parallel from SRAM to EEPROM or from EEPROM to SRAM. In this mode SRAM functions are disabled.

The U635H16 is a fast static RAM (25, 35, 45 ns), with a nonvolatile electrically erasable PROM (EEPROM) element incorporated in each static memory cell. The SRAM can be read and written an unlimited number of times, while independent nonvolatile data resides in EEPROM. Data transfers from the SRAM to the EEPROM (the STORE operation) take place automatically upon power down using charge stored in system capacitance.

Transfers from the EEPROM to the SRAM (the RECALL operation) take place automatically on power up. The U635H16 combines the high performance and ease of use of a fast SRAM with nonvolatile data integrity.

STORE cycles also may be initiated under user control via a software sequence.

Once a STORE cycle is initiated, further input or output are disabled until the cycle is completed.
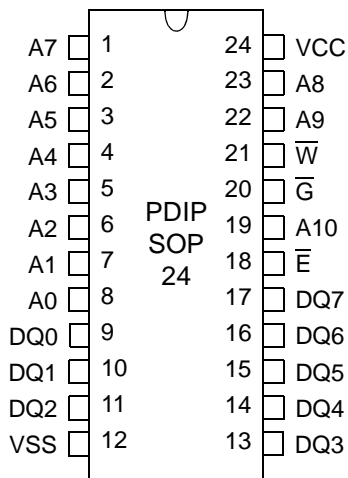
Because a sequence of addresses is used for STORE initiation, it is important that no other read or write accesses intervene in the sequence or the sequence will be aborted.

RECALL cycles may also be initiated by a software sequence.

Internally, RECALL is a two step procedure. First, the SRAM data is cleared and second, the nonvolatile information is transferred into the SRAM cells.

The RECALL operation in no way alters the data in the EEPROM cells. The nonvolatile data can be recalled an unlimited number of times.
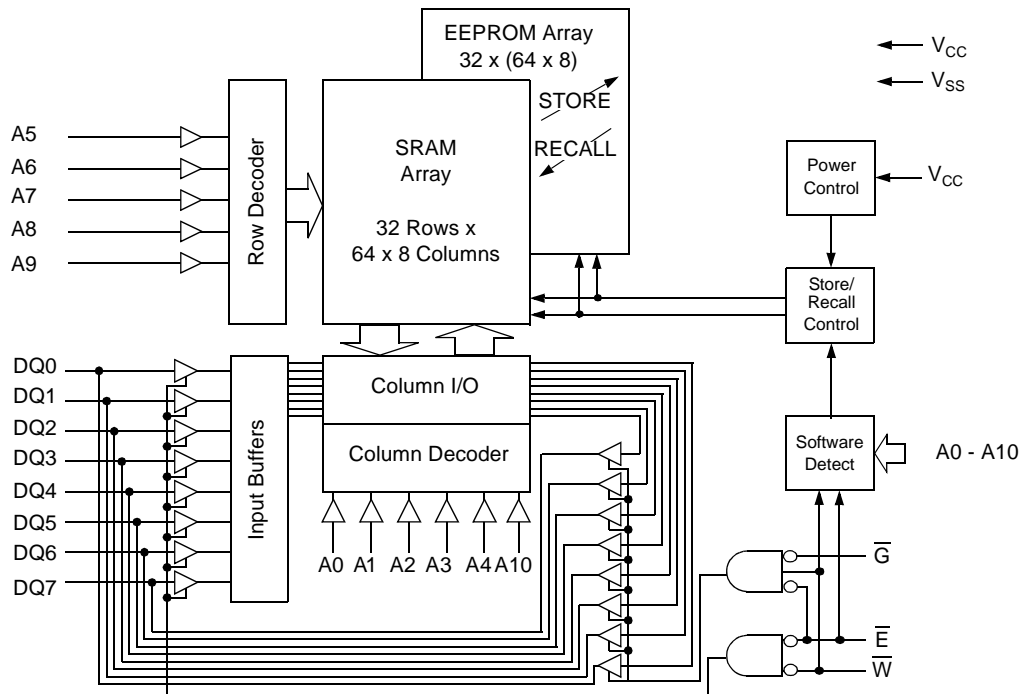
## Pin Configuration

| A7 | 1 | | 24 | VCC |
|---|---|---|---|---|
| A6 | 2 | | 23 | A8 |
| A5 | 3 | | 22 | A9 |
| A4 | 4 | | 21 | $\overline{W}$ |
| A3 | 5 | | 20 | $\overline{G}$ |
| A2 | 6 | PDIP SOP 24 | 19 | A10 |
| A1 | 7 | | 18 | $\overline{E}$ |
| A0 | 8 | | 17 | DQ7 |
| DQ0 | 9 | | 16 | DQ6 |
| DQ1 | 10 | | 15 | DQ5 |
| DQ2 | 11 | | 14 | DQ4 |
| VSS | 12 | | 13 | DQ3 |

Top View

## Pin Description

| Signal Name | Signal Description |
|---|---|
| A0 - A10 | Address Inputs |
| DQ0 - DQ7 | Data In/Out |
| $\overline{E}$ | Chip Enable |
| $\overline{G}$ | Output Enable |
| $\overline{W}$ | Write Enable |
| VCC | Power Supply Voltage |
| VSS | Ground |

# U635H16

**Block Diagram**



**Truth Table for SRAM Operations**

| Operating Mode | $\overline{E}$ | $\overline{W}$ | $\overline{G}$ | DQ0 - DQ7 |
|---|---|---|---|---|
| Standby/not selected | H | * | * | High-Z |
| Internal Read | L | H | H | High-Z |
| Read | L | H | L | Data Outputs Low-Z |
| Write | L | L | * | Data Inputs High-Z |

* H or L

## Characteristics

All voltages are referenced to $V_{SS}$ = 0 V (ground).

All characteristics are valid in the power supply voltage range and in the operating temperature range specified.

Dynamic measurements are based on a rise and fall time of $\leq$ 5 ns, measured between 10 % and 90 % of $V_I$, as well as input levels of $V_{IL}$ = 0 V and $V_{IH}$ = 3 V. The timing reference level of all input and output signals is 1.5 V, with the exception of the $t_{dis}$-times and $t_{en}$-times, in which cases transition is measured $\pm$ 200 mV from steady-state voltage.

| Absolute Maximum Ratings[a] | | Symbol | Min. | Max. | Unit |
|---|---|---|---|---|---|
| Power Supply Voltage | | $V_{CC}$ | -0.5 | 7 | V |
| Input Voltage | | $V_I$ | -0.3 | $V_{CC}$+0.5 | V |
| Output Voltage | | $V_O$ | -0.3 | $V_{CC}$+0.5 | V |
| Power Dissipation | | $P_D$ | | 1 | W |
| Operating Temperature | C-Type | $T_a$ | 0 | 70 | °C |
| | K-Type | | -40 | 85 | °C |
| Storage Temperature | | $T_{stg}$ | -65 | 150 | °C |

a: Stresses greater than those listed under „Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

| Recommended Operating Conditions | Symbol | Conditions | Min. | Max. | Unit |
|---|---|---|---|---|---|
| Power Supply Voltage | $V_{CC}$ | | 4.5 | 5.5 | V |
| Input Low Voltage | $V_{IL}$ | -2 V at Pulse Width 10 ns permitted | -0.3 | 0.8 | V |
| Input High Voltage | $V_{IH}$ | | 2.2 | $V_{CC}$+0.3 | V |

| DC Characteristics | Symbol | Conditions | C-Type | | K-Type | | Unit |
|---|---|---|---|---|---|---|---|
| | | | Min. | Max. | Min. | Max. | |
| Operating Supply Current[b] | $I_{CC1}$ | $V_{CC}$ = 5.5 V<br>$V_{IL}$ = 0.8 V<br>$V_{IH}$ = 2.2 V<br><br>$t_c$ = 25 ns<br>$t_c$ = 35 ns<br>$t_c$ = 45 ns | | 90<br>80<br>75 | | 95<br>85<br>80 | mA<br>mA<br>mA |
| Average Supply Current during STORE[c] | $I_{CC2}$ | $V_{CC}$ = 5.5 V<br>$\overline{E}$ ≤ 0.2 V<br>$\overline{W}$ ≥ $V_{CC}$-0.2 V<br>$V_{IL}$ ≤ 0.2 V<br>$V_{IH}$ ≥ $V_{CC}$-0.2 V | | 6 | | 7 | mA |
| Average Supply Current during *PowerStore* Cycle[c] | $I_{CC4}$ | $V_{CC}$ = 4.5 V<br>$V_{IL}$ = 0.2 V<br>$V_{IH}$ ≥ $V_{CC}$-0.2 V | | 4 | | 4 | mA |
| Standby Supply Current[d] (Cycling TTL Input Levels) | $I_{CC(SB)1}$ | $V_{CC}$ = 5.5 V<br>$\overline{E}$ = $V_{IH}$<br>$t_c$ = 25 ns<br>$t_c$ = 35 ns<br>$t_c$ = 45 ns | | 30<br>23<br>20 | | 34<br>27<br>23 | mA<br>mA<br>mA |
| Operating Supply Current at $t_{cR}$ = 200 ns[b] (Cycling CMOS Input Levels) | $I_{CC3}$ | $V_{CC}$ = 5.5 V<br>$\overline{W}$ ≥ $V_{CC}$-0.2 V<br>$V_{IL}$ ≤ 0.2 V<br>$V_{IH}$ ≥ $V_{CC}$-0.2 V | | 15 | | 15 | mA |
| Standby Supply Curent[d] (Stable CMOS Input Levels) | $I_{CC(SB)}$ | $V_{CC}$ = 5.5 V<br>$\overline{E}$ ≥ $V_{CC}$-0.2 V<br>$V_{IL}$ ≤ 0.2 V<br>$V_{IH}$ ≥ $V_{CC}$-0.2 V | | 3 | | 3 | mA |

b: $I_{CC1}$ and $I_{CC3}$ are depedent on output loading and cycle rate. The specified values are obtained with outputs unloaded. The current $I_{CC1}$ is measured for WRITE/READ - ratio of 1/2.

c: $I_{CC2}$ and $I_{CC4}$ are the average currents required for the duration of the respective STORE cycles (STORE Cycle Time).

d: Bringing $\overline{E}$ ≥ $V_{IH}$ will not produce standby current levels until any nonvolatile cycle in progress has timed out. See MODE SELECTION table. The current $I_{CC(SB)1}$ is measured for WRITE/READ - ratio of 1/2.

# U635H16

| DC Characteristics | Symbol | Conditions | | C-Type | | K-Type | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | Min. | Max. | Min. | Max. | |
| Output High Voltage<br>Output Low Voltage | $V_{OH}$<br>$V_{OL}$ | $V_{CC}$<br>$I_{OH}$<br>$I_{OL}$ | = 4.5 V<br>=-4 mA<br>= 8 mA | 2.4 | 0.4 | 2.4 | 0.4 | V<br>V |
| Output High Current<br>Output Low Current | $I_{OH}$<br>$I_{OL}$ | $V_{CC}$<br>$V_{OH}$<br>$V_{OL}$ | = 4.5 V<br>= 2.4 V<br>= 0.4 V | 8 | -4 | 8 | -4 | mA<br>mA |
| Input Leakage Current | | $V_{CC}$ | = 5.5 V | | | | | |
| High<br>Low | $I_{IH}$<br>$I_{IL}$ | $V_{IH}$<br>$V_{IL}$ | = 5.5 V<br>=   0 V | -1 | 1 | -1 | 1 | μA<br>μA |
| Output Leakage Current | | $V_{CC}$ | = 5.5 V | | | | | |
| High at Three-State- Output<br>Low  at Three-State- Output | $I_{OHZ}$<br>$I_{OLZ}$ | $V_{OH}$<br>$V_{OL}$ | = 5.5 V<br>=   0 V | -1 | 1 | -1 | 1 | μA<br>μA |

**SRAM Memory Operations**

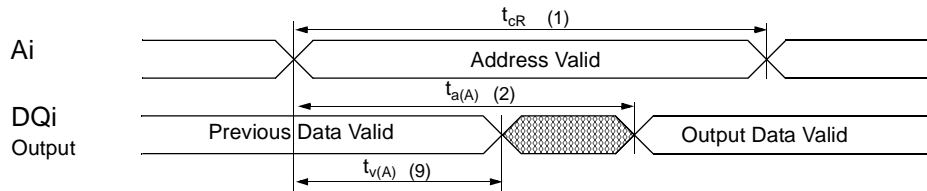| No. | Switching Characteristics Read Cycle | Symbol | | 25 | | 35 | | 45 | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Alt. | IEC | Min. | Max. | Min. | Max. | Min. | Max. | |
| 1 | Read Cycle Time[f] | $t_{AVAV}$ | $t_{cR}$ | 25 | | 35 | | 45 | | ns |
| 2 | Address Access Time to Data Valid[g] | $t_{AVQV}$ | $t_{a(A)}$ | | 25 | | 35 | | 45 | ns |
| 3 | Chip Enable Access Time to Data Valid | $t_{ELQV}$ | $t_{a(E)}$ | | 25 | | 35 | | 45 | ns |
| 4 | Output Enable Access Time to Data Valid | $t_{GLQV}$ | $t_{a(G)}$ | | 12 | | 20 | | 25 | ns |
| 5 | E HIGH to Output in High-Z[h] | $t_{EHQZ}$ | $t_{dis(E)}$ | | 13 | | 17 | | 20 | ns |
| 6 | G HIGH to Output in High-Z[h] | $t_{GHQZ}$ | $t_{dis(G)}$ | | 13 | | 17 | | 20 | ns |
| 7 | E LOW to Output in Low-Z | $t_{ELQX}$ | $t_{en(E)}$ | 5 | | 5 | | 5 | | ns |
| 8 | G LOW to Output in Low-Z | $t_{GLQX}$ | $t_{en(G)}$ | 0 | | 0 | | 0 | | ns |
| 9 | Output Hold Time after Address Change | $t_{AXQX}$ | $t_{v(A)}$ | 3 | | 3 | | 3 | | ns |
| 10 | Chip Enable to Power Active[e] | $t_{ELICCH}$ | $t_{PU}$ | 0 | | 0 | | 0 | | ns |
| 11 | Chip Disable to Power Standby[d, e] | $t_{EHICCL}$ | $t_{PD}$ | | 25 | | 35 | | 45 | ns |

e:  Parameter guaranteed but not tested.
f:  Device is continuously selected with E and G both LOW.
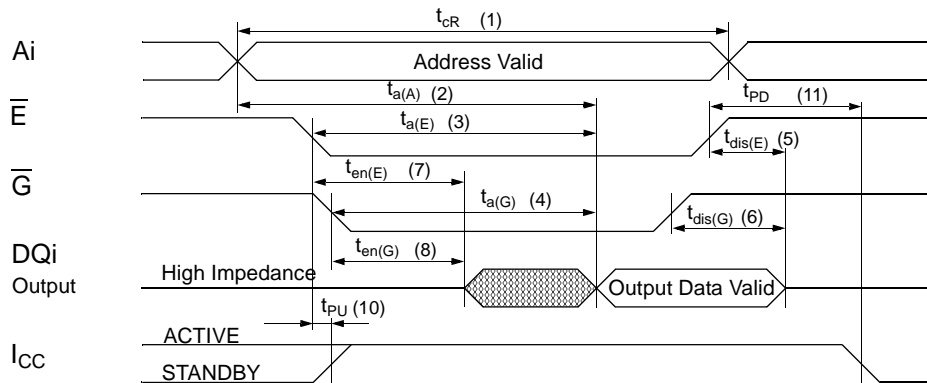g:  Address valid prior to or coincident with E transition LOW.
h:  Measured ± 200 mV from steady state output voltage.

**Read Cycle 1: Ai-controlled (during Read cycle: $\overline{E} = \overline{G} = V_{IL}$, $\overline{W} = V_{IH}$)[f]**



**Read Cycle 2: $\overline{G}$-, $\overline{E}$-controlled (during Read cycle: $\overline{W} = V_{IH}$)[g]**



| No. | Switching Characteristics Write Cycle | Symbol | | | 25 | | 35 | | 45 | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Alt. #1 | Alt. #2 | IEC | Min. | Max. | Min. | Max. | Min. | Max. | |
| 12 | Write Cycle Time | $t_{AVAV}$ | $t_{AVAV}$ | $t_{cW}$ | 25 | | 35 | | 45 | | ns |
| 13 | Write Pulse Width | $t_{WLWH}$ | | $t_{w(W)}$ | 20 | | 30 | | 35 | | ns |
| 14 | Write Pulse Width Setup Time | | $t_{WLEH}$ | $t_{su(W)}$ | 20 | | 30 | | 35 | | ns |
| 15 | Address Setup Time | $t_{AVWL}$ | $t_{AVEL}$ | $t_{su(A)}$ | 0 | | 0 | | 0 | | ns |
| 16 | Address Valid to End of Write | $t_{AVWH}$ | $t_{AVEH}$ | $t_{su(A\text{-}WH)}$ | 20 | | 30 | | 35 | | ns |
| 17 | Chip Enable Setup Time | $t_{ELWH}$ | | $t_{su(E)}$ | 20 | | 30 | | 35 | | ns |
| 18 | Chip Enable to End of Write | | $t_{ELEH}$ | $t_{w(E)}$ | 20 | | 30 | | 35 | | ns |
| 19 | Data Setup Time to End of Write | $t_{DVWH}$ | $t_{DVEH}$ | $t_{su(D)}$ | 12 | | 18 | | 20 | | ns |
| 20 | Data Hold Time after End of Write | $t_{WHDX}$ | $t_{EHDX}$ | $t_{h(D)}$ | 0 | | 0 | | 0 | | ns |
| 21 | Address Hold after End of Write | $t_{WHAX}$ | $t_{EHAX}$ | $t_{h(A)}$ | 0 | | 0 | | 0 | | ns |
| 22 | $\overline{W}$ LOW to Output in High-Z[h, i] | $t_{WLQZ}$ | | $t_{dis(W)}$ | | 10 | | 13 | | 15 | ns |
| 23 | $\overline{W}$ HIGH to Output in Low-Z | $t_{WHQX}$ | | $t_{en(W)}$ | 5 | | 5 | | 5 | | ns |

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**Write Cycle #1: $\overline{W}$-controlled[j]**
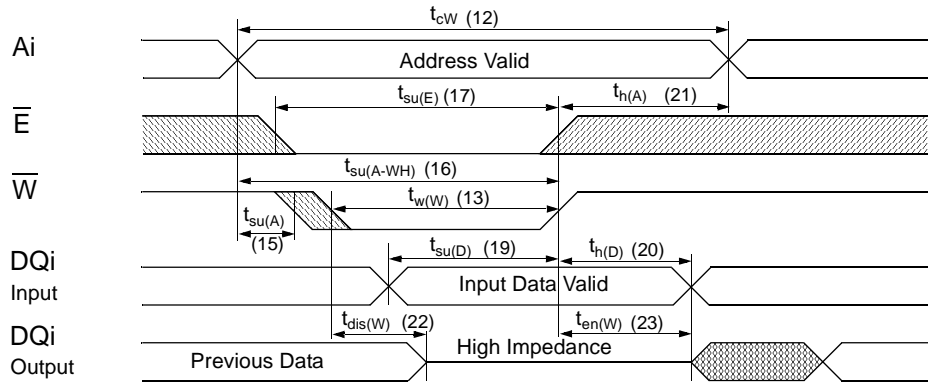


**Write Cycle #2: $\overline{E}$-controlled[j]**



undefined     L- to H-level     H- to L-level
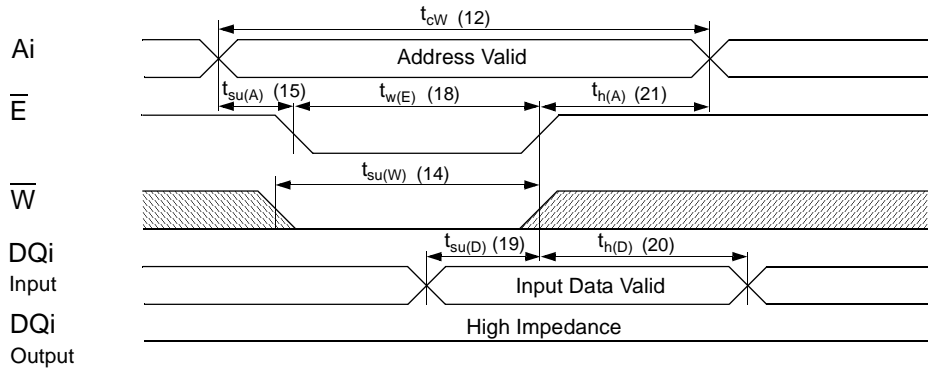
i: If $\overline{W}$ is LOW and when $\overline{E}$ goes LOW, the outputs remain in the high impedance state.

j: $\overline{E}$ or $\overline{W}$ must be $V_{IH}$ during address transition.

**Nonvolatile Memory Operations**

**Mode Selection**

| $\overline{E}$ | $\overline{W}$ | A10 - A0 (hex) | Mode | I/O | Power | Notes |
|---|---|---|---|---|---|---|
| H | X | X | Not Selected | Output High Z | Standby | |
| L | H | X | Read SRAM | Output Data | Active | m |
| L | L | X | Write SRAM | Input Data | Active | |
| L | H | 000 | Read SRAM | Output Data | Active | k, l |
| | | 555 | Read SRAM | Output Data | | k, l |
| | | 2AA | Read SRAM | Output Data | | k, l |
| | | 7FF | Read SRAM | Output Data | | k, l |
| | | 0F0 | Read SRAM | Output Data | | k, l |
| | | 70F | Nonvolatile STORE | Output High Z | | k |
| L | H | 000 | Read SRAM | Output Data | Active | k, l |
| | | 555 | Read SRAM | Output Data | | k, l |
| | | 2AA | Read SRAM | Output Data | | k, l |
| | | 7FF | Read SRAM | Output Data | | k, l |
| | | 0F0 | Read SRAM | Output Data | | k, l |
| | | 70E | Nonvolatile RECALL | Output High Z | | k |

k: The six consecutive addresses must be in order listed (000, 555, 2AA, 7FF, 0F0, 70F) for a Store cycle or (000, 555, 2AA, 7FF,0F0, 70E) for a RECALL cycle. $\overline{W}$ must be high during all six consecutive cycles.
See STORE cycle and RECALL cycle tables and diagrams for further details.
The following six-address sequence is used for testing purposes and should not be used: 000, 555, 2AA, 7FF, 0F0, 39C.
l: Activation of nonvolatile cycles does not depend on the state of $\overline{G}$.
m: I/O state assumes that $\overline{G} \leq V_{IL}$.

| No. | *PowerStore* Power Up RECALL | Symbol | | Conditions | Min. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| | | Alt. | IEC | | | | |
| 24 | Power Up RECALL Duration[n, e] | $t_{RESTORE}$ | | | | 650 | µs |
| 25 | STORE Cycle Duration[f] | $t_{PDSTORE}$ | | the power supply voltage must stay above 3.6 V at least 10 ms after the start of the STORE operation | | 10 | ms |
| 26 | time allowed to Complete SRAM Cycle[f, e] | $t_{DELAY}$ | | | 1 | | µs |
| | Low Voltage Trigger Level | $V_{SWITCH}$ | | | 4.0 | 4.5 | V |

n: $t_{RESTORE}$ starts from the time $V_{CC}$ rises above $V_{SWITCH}$.

*PowerStore* and automatic Power Up RECALL
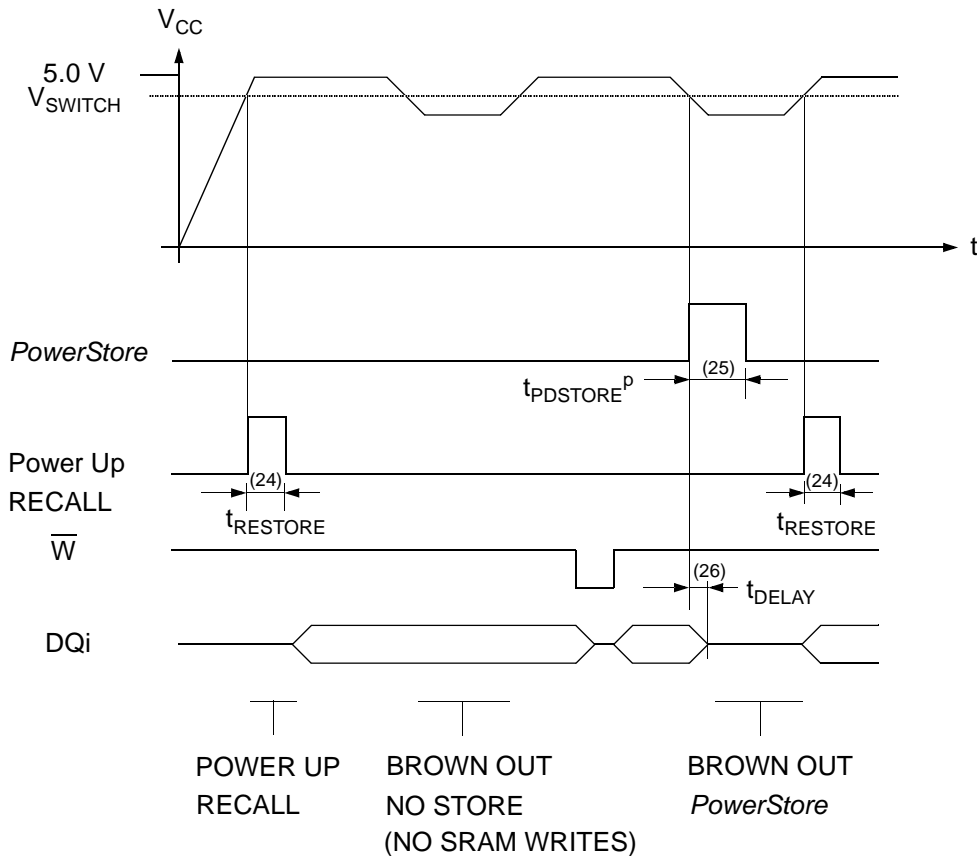


| No. | Software Controlled STORE/ RECALL Cycle[k, o] | Symbol | | 25 | | 35 | | 45 | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Alt. | IEC | Min. | Max. | Min. | Max. | Min. | Max. | |
| 27 | STORE/RECALL Initiation Time | $t_{AVAV}$ | $t_{cR}$ | 25 | | 35 | | 45 | | ns |
| 28 | Chip Enable to Output Inactive[p] | $t_{ELQZ}$ | $t_{dis(E)SR}$ | | 600 | | 600 | | 600 | ns |
| 29 | STORE Cycle Time[q] | $t_{ELQXS}$ | $t_{d(E)S}$ | | 10 | | 10 | | 10 | ms |
| 30 | RECALL Cycle Time[r] | $t_{ELQXR}$ | $t_{d(E)R}$ | | 20 | | 20 | | 20 | µs |
| 31 | Address Setup to Chip Enable[s] | $t_{AVELN}$ | $t_{su(A)SR}$ | 0 | | 0 | | 0 | | ns |
| 32 | Chip Enable Pulse Width[s, t] | $t_{ELEHN}$ | $t_{w(E)SR}$ | 20 | | 25 | | 35 | | ns |
| 33 | Chip Disable to Address Change[s] | $t_{EHAXN}$ | $t_{h(A)SR}$ | 0 | | 0 | | 0 | | ns |

o: The software sequence is clocked with $\overline{E}$ controlled READs.

p: Once the software controlled STORE or RECALL cycle is initiated, it completes automatically, ignoring all inputs.

q: Note that STORE cycles (but not RECALL) are aborted by $V_{CC} < V_{SWITCH}$ (STORE inhibit).

r: An automatic RECALL also takes place at power up, starting when $V_{CC}$ exceeds $V_{SWITCH}$ and takes $t_{RESTORE}$. $V_{CC}$ must not drop below $V_{SWITCH}$ once it has been exceeded for the RECALL to function properly.

s: Noise on the $\overline{E}$ pin may trigger multiple READ cycles from the same address and abort the address sequence.

t: If the Chip Enable Pulse Width is less than $t_{a(E)}$ (see Read Cycle) but greater than or equal $t_{w(E)SR}$, than the data may not be valid at the end of the low pulse, however the STORE or RECALL will still be initiated.

**Software Controlled STORE/RECALL Cycle**[s, t, u, v] **($\overline{E}$ = HIGH after STORE initiation)**
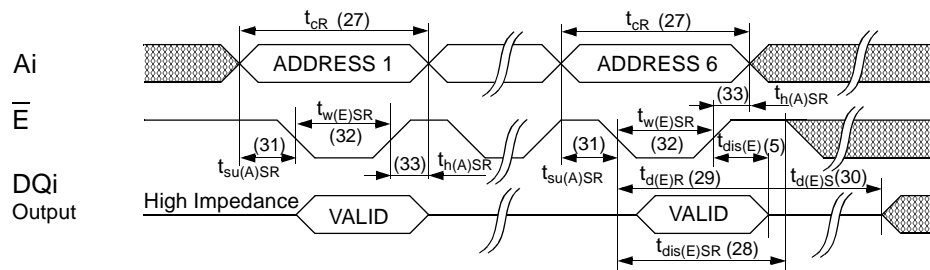


**Software Controlled STORE/RECALL Cycle**[s, t, u, v] **($\overline{E}$ = LOW after STORE initiation)**
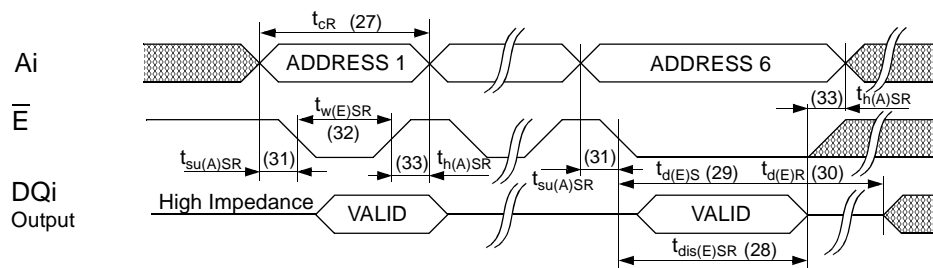


u: $\overline{W}$ must be HIGH when $\overline{E}$ is LOW during the address sequence in order to initiate a nonvolatile cycle. $\overline{G}$ may be either HIGH or LOW throughout. Addresses 1 through 6 are found in the mode selection table. Address 6 determines whether the U635H16 performs a STORE or RECALL.

v: $\overline{E}$ must be used to clock in the address sequence for the software controlled STORE and RECALL cycles.

**SIMTEK**

# U635H16

**Test Configuration for Functional Check**
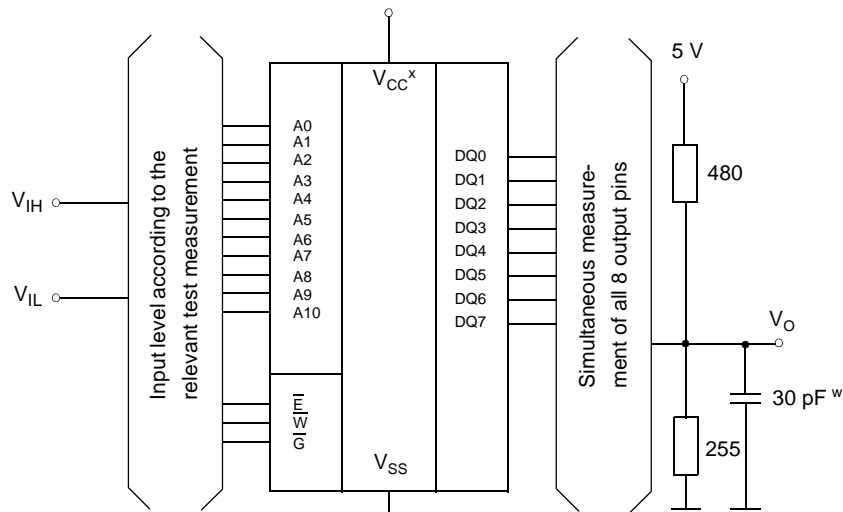
w: In measurement of $t_{dis}$-times and $t_{en}$-times the capacitance is 5 pF.

x: Between $V_{CC}$ and $V_{SS}$ must be connected a high frequency bypass capacitor 0.1 µF to avoid disturbances.

| Capacitance[e] | Conditions | | Symbol | Min. | Max. | Unit |
|---|---|---|---|---|---|---|
| Input Capacitance | $V_{CC}$ = 5.0 V $V_I$ = $V_{SS}$ | | $C_I$ | | 8 | pF |
| Output Capacitance | f = 1 MHz $T_a$ = 25 °C | | $C_O$ | | 7 | pF |

All pins not under test must be connected with ground by capacitors.

**Ordering Code**

Example    **U635H16  S  C  25  G1**

**Type**

**Package**
D = PDIP24 (600 mil)
S = SOP24 (300 mil)

**Leadfree Option**
blank = Standard Package
G1 = Leadfree Green Package [y]

**Access Time**
25 = 25 ns
35 = 35 ns [y]
45 = 45 ns [y]

**Operating Temperature Range**
C = 0 to 70 °C
K = -40 to 85 °C

y: on special request

**Device Marking** (example)

Product specification

ZMD
U635H16SC
25    Z  0425
G1
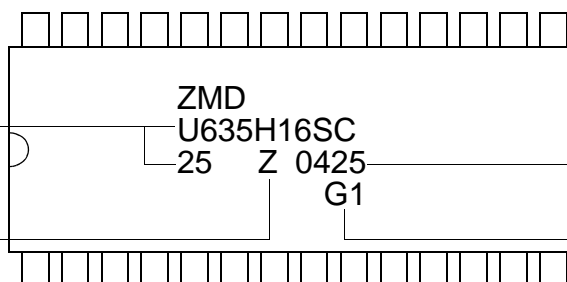
Date of manufacture
(The first 2 digits indicating
the year, and the last 2
digits the calendar week.)

Internal Code

Leadfree Green Package

**SIMTEK**

**Device Operation**

The U635H16 has two separate modes of operation: SRAM mode and nonvolatile mode. In SRAM mode, the memory operates as a standard fast static RAM. In nonvolatile mode, data is transferred from SRAM to EEPROM (the STORE operation) or from EEPROM to SRAM (the RECALL operation). In this mode SRAM functions are disabled.

STORE cycles may be initiated under user control via a software sequence and are also automatically initiated when the power supply voltage level of the chip falls below $V_{SWITCH}$. RECALL operations are automatically initiated upon power up and may also occur when the $V_{CC}$ rises above $V_{SWITCH}$, after a low power condition. RECALL cycles may also be initiated by a software sequence.

**SRAM READ**

The U635H16 performs a READ cycle whenever $\overline{E}$ and $\overline{G}$ are LOW and $\overline{W}$ are HIGH. The address specified on pins A0 - A10 determines which of the 2048 data bytes will be accessed. When the READ is initiated by an address transition, the outputs will be valid after a delay of $t_{cR}$. If the READ is initiated by $\overline{E}$ or $\overline{G}$, the outputs will be valid at $t_{a(E)}$ or at $t_{a(G)}$, whichever is later. The data outputs will repeatedly respond to address changes within the $t_{cR}$ access time without the need for transition on any control input pins, and will remain valid until another address change or until $\overline{E}$ or $\overline{G}$ is brought HIGH or $\overline{W}$ is brought LOW.

**SRAM WRITE**

A WRITE cycle is performed whenever $\overline{E}$ and $\overline{W}$ are LOW. The address inputs must be stable prior to entering the WRITE cycle and must remain stable until either $\overline{E}$ or $\overline{W}$ goes HIGH at the end of the cycle. The data on pins DQ0 - 7 will be written into the memory if it is valid $t_{su(D)}$ before the end of a $\overline{W}$ controlled WRITE or $t_{su(D)}$ before the end of an $\overline{E}$ controlled WRITE.

It is recommended that $\overline{G}$ is kept HIGH during the entire WRITE cycle to avoid data bus contention on the common I/O lines. If $\overline{G}$ is left LOW, internal circuitry will turn off the output buffers $t_{dis(W)}$ after $\overline{W}$ goes LOW.

**Automatic STORE**

The U635H16 uses the intrinsic system capacitance to perform an automatic STORE on power down. As long as the system power supply take at least $t_{PDSTORE}$ to decay from $V_{SWITCH}$ down to 3.6 V the U635H16 will safely and automatically STORE the SRAM data in EEPROM on power down.

In order to prevent unneeded STORE operations, automatic STORE will be ignored unless at least one WRITE operation has taken place since the most recent STORE or RECALL cycle. Software initiated STORE cycles are performed regardless of whether or not a WRITE operation has taken place.

**Automatic RECALL**

During power up an automatic RECALL takes place. After any low power condition ($V_{CC} < V_{SWITCH}$) an internal RECALL request may be latched. When $V_{CC}$ once again exceeds the sense voltage of $V_{SWITCH}$, a requested RECALL cycle will automatically be initiated and will take $t_{RESTORE}$ to complete.

If the U635H16 is in a WRITE state at the end of a power up RECALL, the SRAM data will be corrupted.

To help avoid this situation, a 10 KΩ resistor should be connected between $\overline{W}$ and system $V_{CC}$.

**Software Nonvolatile STORE**

The U635H16 software controlled STORE cycle is initiated by executing sequential READ cycles from six specific address locations. By relying on READ cycles only, the U635H16 implements nonvolatile operation while remaining compatible with standard 2K x 8 SRAMs. During the STORE cycle, an erase of the previous nonvolatile data is performed first, followed by a parallel programming of all nonvolatile elements. Once a STORE cycle is initiated, further inputs and outputs are disabled until the cycle is completed.

Because a sequence of addresses is used for STORE initiation, it is important that no other READ or WRITE accesses intervene in the sequence or the sequence will be aborted.

To initiate the STORE cycle the following READ sequence must be performed:

| | | | | |
|---|---|---|---|---|
| 1. | Read address | 000 | (hex) | Valid READ |
| 2. | Read address | 555 | (hex) | Valid READ |
| 3. | Read address | 2AA | (hex) | Valid READ |
| 4. | Read address | 7FF | (hex) | Valid READ |
| 5. | Read address | 0F0 | (hex) | Valid READ |
| 6. | Read address | 70F | (hex) | Initiate STORE |

Once the sixth address in the sequence has been entered, the STORE cycle will commence and the chip will be disabled. It is important that READ cycles and not WRITE cycles are used in the sequence, although it is not necessary that $\overline{G}$ is LOW for the sequence to be valid. After the $t_{STORE}$ cycle time has been fulfilled, the SRAM will again be activated for READ and WRITE operation.

# U635H16

**Software Nonvolatile RECALL**

A RECALL cycle of the EEPROM data into the SRAM is initiated with a sequence of READ operations in a manner similar to the STORE initiation. To initiate the RECALL cycle the following sequence of READ operations must be performed:

1.  Read address   000   (hex)  Valid READ
2.  Read address   555   (hex)  Valid READ
3.  Read address   2AA   (hex)  Valid READ
4.  Read address   7FF   (hex)  Valid READ
5.  Read address   0F0   (hex)  Valid READ
6.  Read address   70E   (hex)  Initiate RECALL

Internally, RECALL is a two step procedure. First, the SRAM data is cleared and second, the nonvolatile information is transferred into the SRAM cells. The RECALL operation in no way alters the data in the EEPROM cells. The nonvolatile data can be recalled an unlimited number of times.

**Hardware Protection**

The U635H16 offers hardware protection against inadvertent STORE operation through $V_{CC}$ Sense. When $V_{CC} < V_{SWITCH}$ all software controllod STORE operations will be inhibited.

**Low Average Active Power**

The U635H16 has been designed to draw significantly less power when $\overline{E}$ is LOW (chip enabled) but the access cycle time is longer than 55 ns.
When $\overline{E}$ is HIGH the chip consumes only standby current.
The overall average current drawn by the part depends on the following items:
1. CMOS or TTL input levels
2. the time during which the chip is disabled ($\overline{E}$ HIGH)
3. the cycle time for accesses ($\overline{E}$ LOW)
4. the ratio of READs to WRITEs
5. the operating temperature
6. the $V_{CC}$ level

The information describes the type of component and shall not be considered as assured characteristics. Terms of delivery and rights to change design reserved.

**LIFE SUPPORT POLICY**

**LIMITED WARRANTY**

# Change record

| Date/Rev | Name | Change |
|---|---|---|
| 01.11.2001 | Ivonne Steffens | format revision and release for „Memory CD 2002" |
| 20.04.2004 | Matthias Schniebel | adding „Leadfree Green Package" to ordering information<br>adding „Device Marking" |
| 7.4.2005 | Stefan Günther | edding RoHS compliance and Pb- free, $10^6$ endurance cycle and 100a data retention, ESD restrictions deleted, |
| 31.3.2006 | Troy Meester | changed to obsolete status |
| 1.0 | Simtek | Assigned Simtek Document Control Number |