TMC2192

10 Bit Encoder

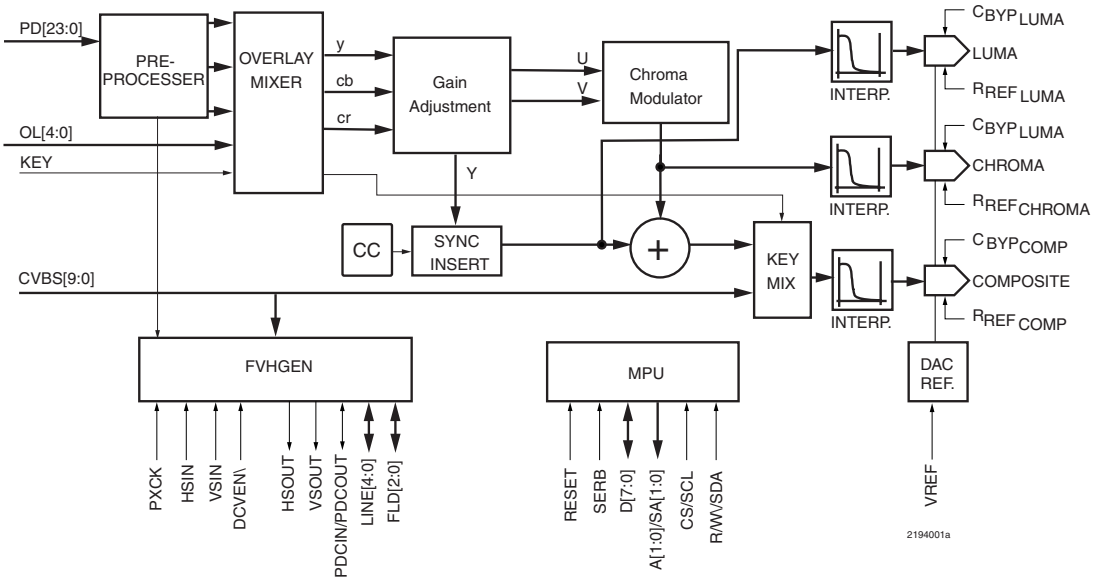
Features

- Multiple input formats
  - 20 bit CCIR601
  - 10 bit CCIR656
  - 10 bit Digital Composite
- Synchronization modes
  - Master
  - Slave
  - Genlock
  - CCIR656
- Subcarrier modes
  - Free-run
  - Subcarrier reset
  - Genlock
  - DRS-lock
- Ancillary Data Control (ANC)
- Pixel rates from 10 MHz to 15 MHz
- Programmable horizontal timing
- Programmable vertical blanking interval (VBI)
- Line-by-line pedestal enable
- Programmable pedestal height from -20 IRE to 20 IRE
- Programmable burst amplitude and phase
- Controlled edge rates for
  - Sync
  - Burst
  - Active video
- Programmable color space matrix
- 8:8:8 video reconstruction
- Three 10 bit D/A's with independent trim
- Individual power down modes for each D/A
- Multiple output formats
  - S-video
  - Composite
  - Digital composite output
- Pin-driven and data-driven, window keying
- Closed Caption waveform generation (13.5 MHz only)
- Sin(X)/X compensation filter
- 5 bit VBI line counter
- 3 bit field counter
- Internal test pattern generation
  - 100% Color Bars
  - 75% Color Bars
  - Modulated Ramp

Applications

- Broadcast Television
- Nonlinear Video Processing

Block Diagram



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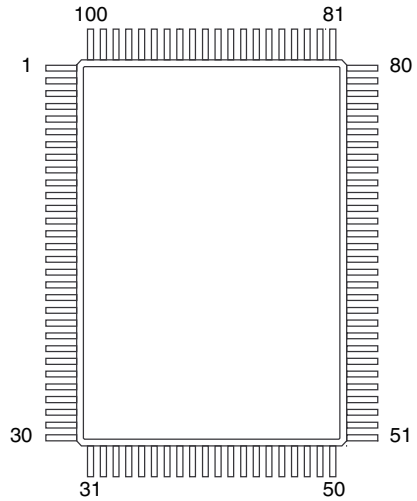

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Pin	Function	Pin	Function	Pin	Function	Pin	Function
1	V_{DDA}	31	PD_{19}	51	PD_1	81	FLD2
2	COMP	32	PD_{18}	52	PD_0	82	FLD1
3	$C_{BYPCOMP}$	33	PD_{17}	53	D_{GND}	83	FLD0
4	A_{GND}	34	PD_{16}	54	V_{DD}	84	CVBS9
5	CHROMA	35	PD_{15}	55	$\overline{VSIN}$	85	CVBS8
6	$C_{BYPCHROM}$	36	PD_{14}	56	$\overline{HSIN}$	86	CVBS7
7	V_{DDA}	37	PD_{13}	57	$\overline{DCVEN}$	87	CVBS6
8	$R_{REFCHROM}$	38	PD_{12}	58	$\overline{SER}$	88	CVBS5
9	A_{GND}	39	V_{DD}	59	CS\SCL	89	CVBS4
10	LUMA	40	D_{GND}	60	R/W\SDA	90	CVBS3
11	$C_{BYPLUMA}$	41	PD_{11}	61	A1/SA1	91	CVBS2
12	V_{DDA}	42	PD_{10}	62	A0/SA0	92	CVBS1
13	$R_{REFLUMA}$	43	PD_9	63	D_7	93	CVBS0
14	A_{GND}	44	PD_8	64	D_6	94	$\overline{RESET}$
15	A_{GND}	45	PD_7	65	D_5	95	PXCK
16	V_{DDA}	46	PD_6	66	D_4	96	V_{DD}
17	V_{DDA}	47	PD_5	67	D_3	97	D_{GND}
18	A_{GND}	48	PD_4	68	D_2	98	V_{REF}
19	A_{GND}	49	PD_3	69	D_1	99	$R_{REFCOMP}$
20	KEY	50	PD_2	70	D_0	100	AGND
21	OL_4			71	D_{GND}		
22	OL_3			72	V_{DD}		
23	OL_2			73	PDC		
24	OL_1			74	$\overline{HSOUT}$		
25	OL_0			75	$\overline{VSOUT}$		
26	D_{GND}			76	LINE4		
27	PD_{23}			77	LINE3		
28	PD_{22}			78	LINE2		
29	PD_{21}			79	LINE1		
30	PD_{20}			80	LINE0		

Pin Definitions

Pin Name	Pin Number	Value	Description
CLOCK, SYNC, & CONTROL INPUTS (6 pins)			
$\overline{DCVEN}$	57	TTL	**Digital CVBS Output Enable.** When $\overline{DCVEN}$ is LOW, the Comp2 output prior to the D/A is routed to D7-0, FLD2-1 providing a digital composite output. When $\overline{DCVEN}$ is HIGH, D7-0 and FLD2-1 operate in their normal mode.
$\overline{HSIN}$	56	TTL	**Horizontal Sync Input.** When operating in slave, Genlock, or DRS-Lock the TMC2192 will start a new horizontal line with each falling edge of $\overline{HSIN}$.
KEY	20	TTL	**Hard Key selection.** When the control register bit HKEN is set HIGH and the hardware KEY pin is high, the video data considered to be the foreground. is routed to the COMP2 output. This control signal is data aligned so that the pixel that is present on the PD port when KEY signal is latched is at the midpoint of the key transition. When HKEN is LOW, Key is ignored.

Pin Definitions (continued)

Pin Name	Pin Number	Value	Description
PXCK	95	TTL	**Pixel Clock Input.** PXCK is a clock signal that period is twice the sample rate of the pixel data. The operating range is 20 to 30 MHz. The clock is internally divided by 2 to generate the internal pixel clock, PCK. PXCK drives the entire TMC2192 except the asynchronous microprocessor interface.
$\overline{\text{RESET}}$	94	TTL	**Master Chip Reset.** When LOW, All outputs are tri-stated and the internal state machines and control registers are reset. At rising edge of $\overline{\text{RESET}}$, all outputs are active, the preset values will be loaded into the control registers and the internal states machines start to operate.
$\overline{\text{VSIN}}$	55	TTL	**Vertical Sync Input.** When operating in slave, Genlock, or DRS-Lock the TMC2192 will start a new vertical field with each falling edge of $\overline{\text{VSIN}}$ that is coincident with $\overline{\text{HSIN}}$.
SYNC & CONTROL OUTPUTS (11 pins)			
FLD[2:0]	81–83	TTL	**Field Identifier.** Field Identifier outputs the current field number. For all video standards the field identifier will cycle through the eight counts.
$\overline{\text{HSOUT}}$	74	TTL	**Horizontal Sync Output.** The alignment of $\overline{\text{HSOUT}}$ to the pixel data port or DCVBS port is controlled by control register TSOUT.
LINE[4:0]	76–80	TTL	**Vertical Blanking Interval Line Identifier.** LINE identifies the current line number for the first 31 lines. If the line count is greater than 31 then LINE is 11111b. The first line with a vertical serration is considered to be line 0.
PDC	73	TTL	**Pixel Data Control.** *When PDCDIR = LOW:* At a rising edge, The next pixel starts a controlled ramp of the PD data. At a falling edge, the pixel prior is the last PD used in the ramp. The rising edge is determined by the PDCCNT control register, the falling edge of PDC is determined by the horizontal timing registers. *When PDCDIR = HIGH:* PDCIN is used to override the internal PDC. When HIGH, the internal PDC controls the blank and unblank window. When LOW, the video remains blanked regardless of the internal PDC. All edges have the same ramp control as the internal PDC.
$\overline{\text{VSOUT}}$	75	TTL	**Vertical Sync Output.** The alignment of $\overline{\text{VSOUT}}$ to the pixel data port or DCVBS port is controlled by control register TSOUT.
DATA INPUTS (39 pins)			
CVBS[9:0]	84–93	TTL	Composite Data Input
OL[4:0]	21–25	TTL	Overlay Control
PD[23:0]	27–38, 41–52	TTL	Component Data Input
ANALOG INTERFACE – Video Out (5 pins)			
LUMA	10	1.35Vp-p	Luma
CHROMA	5	1.35Vp-p	Chroma
COMP	2	1.35Vp-p	Composite D/A with optional keying

Pin Definitions (continued)

Pin Name	Pin Number	Value	Description
ANALOG INTERFACE – Support (9 pins)			
$C_{BYPLUMA}$	11	0.1 µF	**Reference Bypass Capacitor for LUMA DAC.** Connection point for 0.1 µF Capacitor.
$C_{BYPCHROM}$	6	0.1 µF	**Reference Bypass Capacitor for CHROMA DAC.** Connection point for 0.1 µF Capacitor.
$C_{BYPCOMP}$	3	0.1 µF	**Reference Bypass Capacitor for COMPOSITE DAC.** Connection point for 0.1 µF Capacitor.
$R_{REFLUMA}$	13	1210 Ohm	**Current Setting Resistor.** Connection point for external current setting resistor for LUMA DAC. The resistor is connected between $R_{REFLUMA}$ and GND. Output video levels are inversely proportional to the value of R_{REF2}.
$R_{REFCHROM}$	8	1210 Ohm	**Current Setting Resistor.** Connection point for external current setting resistor for CHROMA DAC. The resistor is connected between $R_{REFCHROM}$ and GND. Output video levels are inversely proportional to the value of $R_{REFCHROM}$.
$R_{REFCOMP}$	99	1210 Ohm	**Current Setting Resistor.** Connection point for external current setting resistor for COMPOSITE DAC. The resistor is connected between $R_{REFCOMP}$ and GND. Output video levels are inversely proportional to the value of $R_{REFCOMP}$.
V_{REF}	98	1.235 V	**Voltage Reference Input.** External voltage reference input, internal voltage reference output, nominally 1.235V.
MPU INTERFACE (13 pins)			
A[1:0]/S_A[1:0]	61, 62	TTL	When $\overline{SER}$ (HIGH), OLUT/control/pointer address. When $\overline{SER}$ (LOW), SA[1:0] of serial chip address SA[6:0].
CS/SCL	59	TTL/R-BUS	When $\overline{SER}$ (HIGH), microprocessor port clock. When $\overline{SER}$ (LOW), serial bus clock.
D[7:0]	63–70	TTL	**Bi-directional Data Bus.**
RW/SDA	60	TTL/R-BUS	When $\overline{SER}$ (HIGH), read/write control. When $\overline{SER}$ (LOW), serial bus bi-directional data.
$\overline{SER}$	58	TTL	**Microprocessor Select.** When LOW, the serial interface is enabled. When HIGH, the parallel interface is enabled.
POWER & GROUND (17 pins)			
A_{GND}	4, 9, 14, 15, 18, 19, 100	0.0V	Analog ground
D_{GND}	26, 40, 53, 71, 97	0.0V	Digital ground
V_{DD}	39, 54, 72, 96	+5.0V	Digital positive power supply
V_{DDA}	1, 7, 12, 16, 17	+5.0V	Analog positive power supply

Functional Description

Input Formats

Control Registers for this section

Address	Bit(s)	Name
0x05	7	D1OFF
0x05	6-4	INMODE
0x06	0	TSOUT

The TMC2192 supports YC_BC_R component sources on the pixel data port. YC_BC_R input sources are supported in 10 bit 4:2:2, 20 bit 4:2:2, 20 bit 4:4:4, and 24 bit 4:4:4. In the 4:2:2 cases the color difference components are linearly interpolated to 4:4:4 internally.

Demuxing of multiplexed data streams depends on which synchronization mode the encoder is operating in. For slave and genlock modes the falling edge of $\overline{HSIN}$ must be LOW prior to the C_B data in order to demux the data correctly. For master mode synchronization the falling edge of $\overline{HSOUT}$ must be LOW prior to the Y data in order to demux the data correctly. Finally, in 656 mode the demuxing of the data stream is determined by the TRS codes, the first sample after the TRS is considered a C_B sample of the C_B Y C_R Y_I packet.

The control register D1OFF controls the formatting of the incoming luminance data at the pixel data port. When D1OFF is HIGH a blanking level of 64_{10} is subtracted from the luminance and when D1OFF is LOW the incoming the pixel data is passed through. The inversion of the MSB's on the C_B and C_R components is controlled by the INMODE control register.

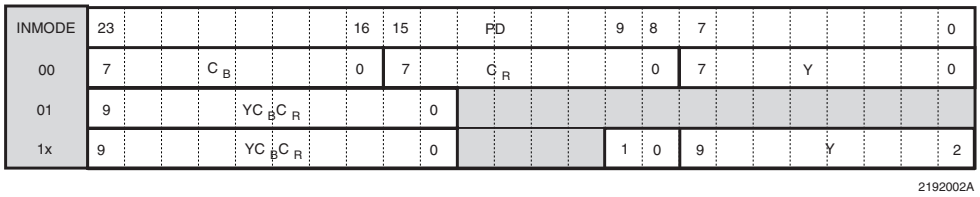


Figure 1. Input Formats

1. INMODE = 00, PD[7:0] = PD[23:16] = C_B, PD[15:8] = C_R

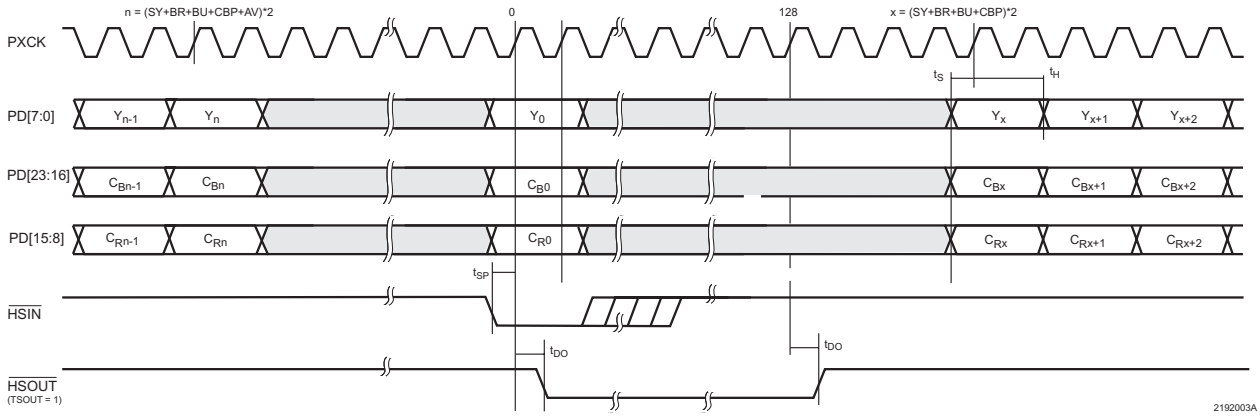


Figure 2. 24 Bit Input Format

2. INMODE = 01, PD[23:14] = YC_BC_R running at 27MHz.

The PD port is clocked at twice the pixel rate, with the data organized as C_B Y C_R Y, with the cosited Y's following the C_B's. In its CCIR-656 time base mode, the demuxed C_B, Y, and C_R data is synchronized to the SAV preamble. The first data value, after the SAV preamble, is treated as a C_B data point in the multiplexed C_B, Y, C_R Y , D1 data stream.

Note: Figure 3, pixel numbering, reflects the SMPTE-125M pixel numbering.

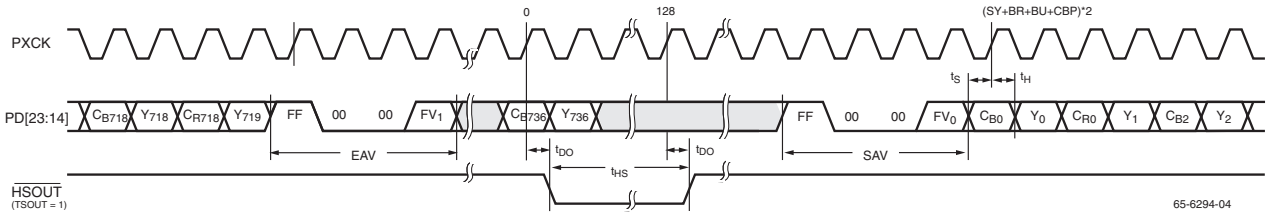


Figure 3. CCIR656 Input Format

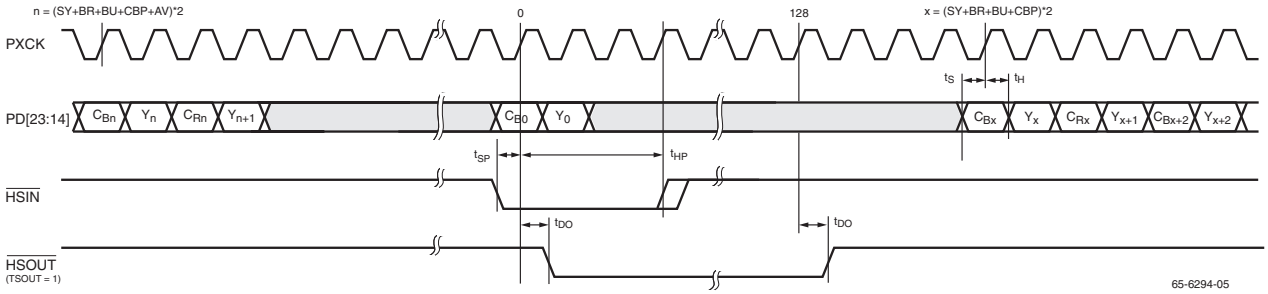


Figure 4. 10 bit Input Format

3. INMODE = 11, PD[9:0] = Y, PD[23:14] = C_B/C_R

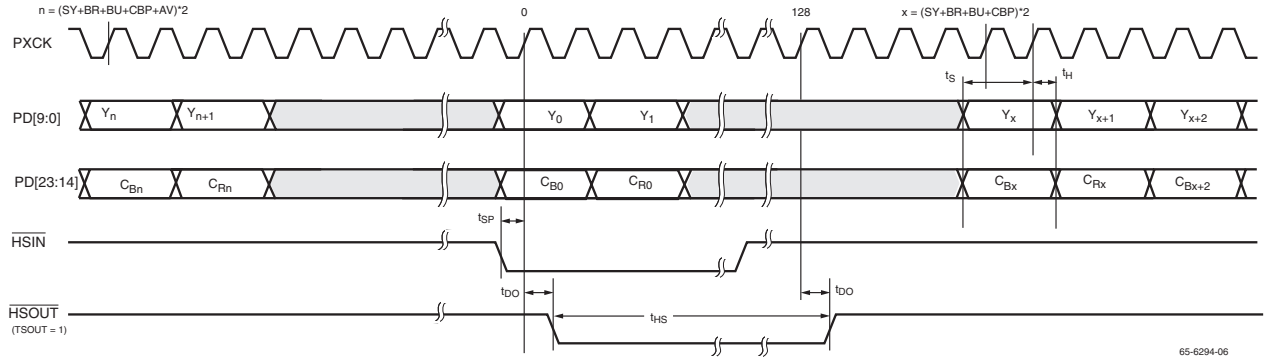


Figure 5. 20 bit 4:2:2 Input Format

4. INMODE = 10, PD[9:0] = Y at PCK, PD[23:14] = C_B-C_R at PXCK

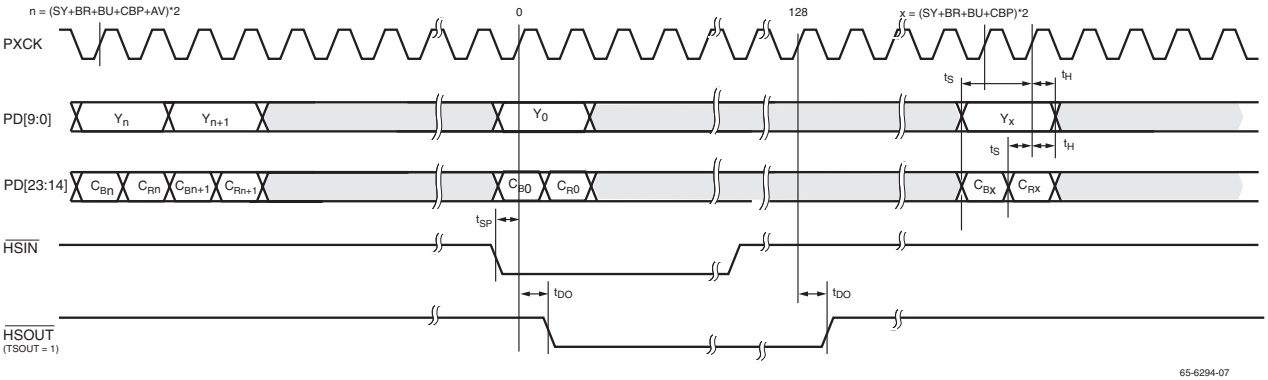


Figure 6. 20 bit 4:4:4 Input Format

Color Space Matrix

Control Registers for this section

Address	Bit(s)	Name
0x30	7-0	MCF1L
0x33	7-0	MCF2L
0x35	7-0	MCF3L
0x3A	7-4	MCF1M
0x3B	2-0	MCF2M
0x3C	2-0	MCF3M

Matrix configuration:

$Y_{composite} = MCF1 * Y_{in}$

$U = MCF2 * C_B$

$V = MCF3 * C_R$

The color space matrix consists of 3 multipliers with independently adjustable coefficients, and a resolution of 0.00049 (1/2048). The amount of gain varies among coefficients, Table 1 summarizes the gain for each coefficient.

Table 1. CSM Coefficient Range

Coefficient	Gain Range	Comment
MCF1	0 to 2	
MCF2	0 to 1	11 bit coefficient.
MCF3	0 to 1	11 bit coefficient.

To aid in the programming of the color space matrix Table 2 provides a set of default input and output values for 100% color bars. The component values given will be after the pre-processing block and prior to the sync and pedestal insertion. The blank, pedestal, and sync values are given as a reference. Table 4 gives the default coefficients values for the CSM.

Table 2. Expected Output Values for the CSM with YC_BC_R Inputs

	Inputs			5:2 Outputs			7:3 Outputs		
Color	Y	C_B	C_R	Y	U	V	Y	U	V
White	876	0	0	536	0	0	568	0	0
Yellow	776	-448	73	475	-235	54	503	-249	57
Cyan	614	151	448	376	79	-332	407	84	-351
Green	514	-297	-375	315	-156	-278	340	-165	-294
Magenta	362	297	375	222	156	278	240	165	294
Red	262	-151	448	160	-79	332	173	-84	351
Blue	100	448	-73	61	235	-54	66	249	-57
Black	0	0	0	0	0	0	0	0	0
Blank	64			240			256		
Pedestal				44			0		
Sync				8			12		

Synchronization Modes

Control Registers for this section

Address	Bit(s)	Name
0x06	5-3	MODE
0x06	1	TOUT
0x06	0	TSOUT

The TMC2192 offers a variety of synchronization modes; these are master, slave, genlock, 656 mode, and DRS-Lock. In master mode, the TMC2192 generates its own timing and the synchronization is supplied externally by $\overline{\text{HSOUT}}$ and $\overline{\text{VSOUT}}$ signals. In slave and genlock modes the TMC2192 derives its timing from the input pins $\overline{\text{HSIN}}$, $\overline{\text{VSIN}}$. In 656 mode the timing is driven by the synchronization codes embedded into the data stream.

Master

The TMC2192 drives the output pins $\overline{\text{HSOUT}}$ and $\overline{\text{VSOUT}}$ to synchronize the incoming video. A new color frame starts at the rising edge of $\overline{\text{RESET}}$. The encoder always starts at the 1st vertical serration in field 8 and will freerun the field and line sequence. The control register bit $\overline{\text{SRESET}}$ can be used to synchronize the start of the field and line sequence in master mode by resetting the FVHGEN state machine. Output synchronization signal $\overline{\text{VSOUT}}$ can operate in a traditional sync mode or in a MPEG style field toggle mode.

Slave

The TMC2192 is driven by the input synchronization pins $\overline{\text{HSIN}}$ and $\overline{\text{VSIN}}$. When the falling edge of $\overline{\text{HSIN}}$ and $\overline{\text{VSIN}}$ occurs at the same rising edge of PXCK the TMC2192 will start a new field.$\overline{\text{VSIN}}$ can be either a traditional pulse or the MPEG style field toggle. In both cases the TMC2192 will flywheel through fields 2, 4, 6, and 8 synchronizing only to fields 1, 3, 5, and 7.

CCIR656

The TMC2192 derives all synchronization from the embedded TRS (timing reference signals) information. Blanking of selected lines is determined by the v bit of the TRS. However the control registers VBIENx can override and blank the active video portion of VBI lines regardless of the state of the v-bit.

Genlock

The TMC2192 is driven by the input synchronization pins $\overline{\text{HSIN}}$ and $\overline{\text{VSIN}}$. When the falling edge of $\overline{\text{HSIN}}$ and $\overline{\text{VSIN}}$ occurs at the same rising edge of PXCK the TMC2192 will start a new field.$\overline{\text{VSIN}}$ can be either a traditional pulse or the MPEG style field toggle. In both cases the TMC2192 will flywheel through fields 2, 4, 6, and 8 synchronizing only to fields 1, 3, 5, and 7. The TMC2192 collects GRS data and resets its subcarrier phase and frequency to the data embedded in the GRS stream. The GRS detection occurs only on the CBVS port.

DRS

The TMC2192 is driven by the input synchronization pins $\overline{\text{HSIN}}$ and $\overline{\text{VSIN}}$. When the falling edge of $\overline{\text{HSIN}}$ and $\overline{\text{VSIN}}$ occurs at the same rising edge of PXCK the TMC2192 will start a new field.$\overline{\text{VSIN}}$ can be either a traditional pulse or the MPEG style field toggle. In both cases the TMC2192 will flywheel through fields 2, 4, 6, and 8 synchronizing only to fields 1, 3, 5, and 7. Subcarrier phase adjustment is determined by the DRS data. The DRS detection can occur on either the CBVS port or the pixel data port.

Propagation Delay

The propagation delay from the pixel data (PD) input to the D/A output is 64 PXCK's. Figure 8 shows the propagation delay for both master and slave synchronization modes. For CCIR656 data streams, pixel 736 (pixel 0 in Figure 8) is the midpoint of sync and is 32 PXCK's (24 PXCK's in PAL) after the EAV TRS.

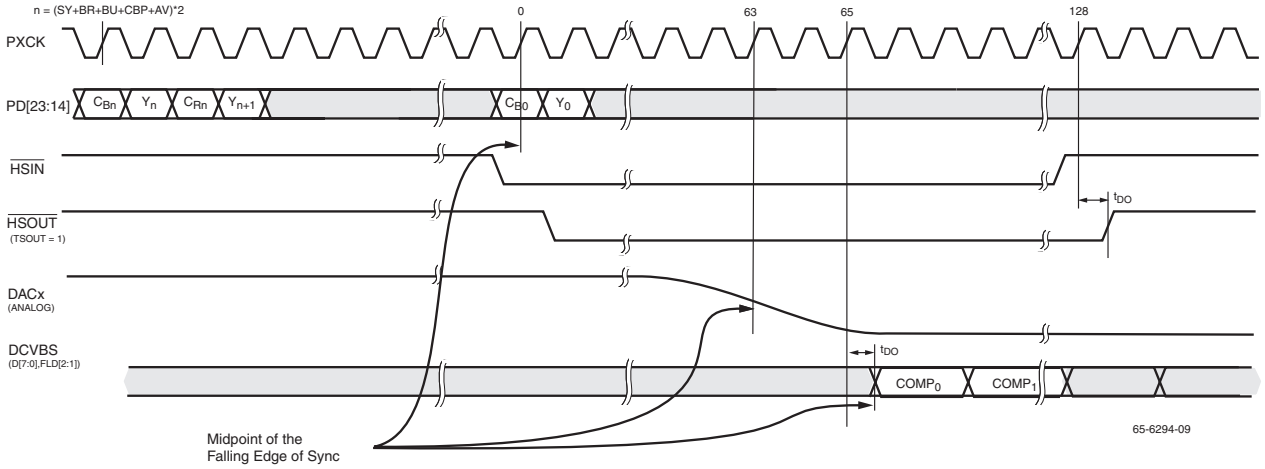


Figure 7. Propagation Delay through the Encoder

Blanking Control

Control Registers for this section

Address	Bit(s)	Name
0x04	1-0	PDRM
0x06	2	PDCDIR
0x18	4-0	VBIENF1
0x19	4-0	VBIENF2
0x1F	7-0	PDCCNT

The content of VBIENFx[4:0] selects the first line to contain an active video region in each field, all subsequent lines for the remainder of the field are active. To blank an entire field, the user zeroes the VBIENFx[4:0] control register. In CCIR656 slave mode, the user can selectively blank any enabled line by setting its TRS V bit HIGH. For 525-line systems, NTSC line numbering is employed, with the first vertical serration starting on line 4. PAL line numbering is used with 625-line systems, with each field's line 1 being the start of the first vertical serration.

Any line(s) enabled by the closed caption control are automatically unblanked for the closed caption waveform, irrespective of the corresponding values of VBIENF.

Pixel Data Control

The pixel data control has two modes of operation, as an input or as an output. The mode of operation is determined by the PDCDIR control register. When PDC is an input the internally generated PDC is ANDed with the PDC pin. This allows the user to blank any active video regions. When PDC is an output, the internally generated PDC is the output for the PDC pin.

The internal PDC control will toggle to a logic HIGH at the pixel specified by PDCNT and toggle to a logic LOW four pixels prior to the end of the active video region. The starting point and ending point of the active video region (VA) are determined by the control registers 10h to 1Fh. When PDC is used as an input, the sloped edge of the active video region will occur on the next four pixels following the toggle point.

Edge Shaping

The TMC2192 has three modes of sloped edges on the active video region and are controlled by PDRM control register.

Table 3. PDC Edge Control

PDRM[1:0]	Slope type at PDC (HIGH)	Slope type at PDC (LOW)
00	The following four pixels have the weighting of 1/8, 1/2, 7/8 and 1 for NTSC and 1/8, 3/8, 5/8, and 7/8 for PAL.	The following four pixels have the weighting of 1, 7/8, 1/2, and 1/8 for NTSC and 7/8, 5/8, 3/8, and 1/8 for PAL.
01	The fifth pixel is sampled and scaled 1/8, 1/2, 7/8 and 1 over the next four pixels for NTSC and 1/8, 3/8, 5/8, and 7/8 over the next four pixels for PAL.	The fifth pixel s sampled and scaled 1, 7/8, 1/2 and 1/8 over the next four pixels for NTSC and 7/8, 5/8, 3/8, and 1/8 over the next four pixels for PAL.
1x	Slope is off, edge control is dictated by the PD stream from active video start	Slope is off, edge control is dictated by the PD stream to active video end

Horizontal Programming

Control registers for this section

Address	Bit(s)	Name
0x06	7-6	FORMAT
0x19	7	SHORT
0x19	6	T512
0x19	5	$\overline{\text{HALFEN}}$
0x20	7-0	SY
0x21	7-0	BR
0x22	7-0	BU
0x23	7-0	CBP
0x24	7-0	XBP
0x25	7-0	VA
0x26	7-0	VC
0x27	7-0	VB
0x28	7-0	EL
0x29	7-0	EH
0x2A	7-0	SL
0x2B	7-0	SH
0x2C	7-0	FP
0x2D	7-6	XBP (MSB's)
0x2D	5-4	VA (MSB's)
0x2D	3-2	VB (MSB's)
0x2D	1-0	VC (MSB's)

Horizontal interval timing is fully programmable and is established by loading the timing registers with the duration of each horizontal element. The duration is expressed in PCK clock cycles. In this way, any pixel clock rate between 10 MHz and 15 MHz can be accommodated, and any desired standard or non-standard horizontal video timing may be produced.

Horizontal timing parameters can be calculated as follows:

t = N x (PCK period)
= N x (2 x PXCK period)

where N is the value loaded into the appropriate timing register, and PCK is the pixel clock period.

When programming horizontal timing, subtract 5 PCK periods from the calculated values of CBP and add 5 PCK periods to the calculated value for VA. The control register $\overline{\text{HALFEN}}$ enables the 1st half line (UBV) on line 283 for NTSC, PAL-M and line 23 for all other PAL standards when it is LOW.

Table 4. Horizontal Line Equations

Line Type	Line ID	Line Length Equals
EE	00	EL + EH + EL + EH
SE	02	SL + SH + EL + EH
SS	03	SL + SH + SL + SH
ES	01	EL + EH + SL + SH
EB	10	EL + EH + EL + EH
UBB, -BB	0D, 05	SY + BR + BU + CBP + VA + FP
UVV, -VV	0F, 07	SY + BR + BU + CBP + VA + FP
UVE, -VE	0C, 04	SY + BR + BU + CBP + VC + FP + EL + EH
UBV	0E	SY + BR + BU + XBP + VB + FP

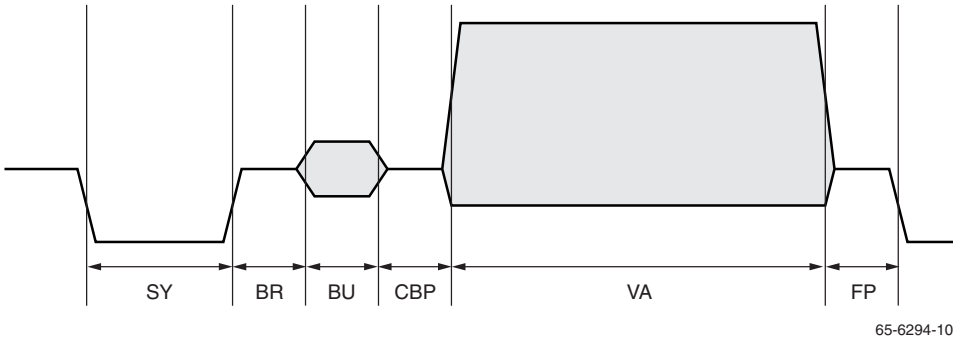


Figure 8. Horizontal Timing

Table 5. Horizontal Timing Specifications

Parameter	NTSC-M (µs)	PAL-I (µs)	PAL-M (µs)
FP	1.5	1.65	1.9
SY	4.7	4.7	4.95
BR	0.6	0.9	0.9
BU	2.5	2.25	2.25
CBP	1.6	2.55	1.8
VA	52.6556	51.95	51.692
H	63.5556	64.0	63.492

Vertical interval timing is also fully programmable, and is established by loading the timing registers with the duration's of each vertical timing element, the duration expressed in PCK clock cycles. In this way as with horizontal programming, any pixel rate between 10 and 15 Mpps can be accommodated, and any desired standard or non-standard vertical video timing may be produced.

Like horizontal timing parameters, vertical timing parameters are calculated as follows:

t = N x (PCK period)
= N x (2 x PXCK period)

where N is the value loaded into the appropriate timing register, and PCK is the pixel clock period.

The vertical interval comprises several different line types based upon H, the Horizontal line time.

H = (2 x SL) + (2 x SH) [Vertical sync pulses]
= (2 x EL) + (2 x EH) [Equalization pulses]

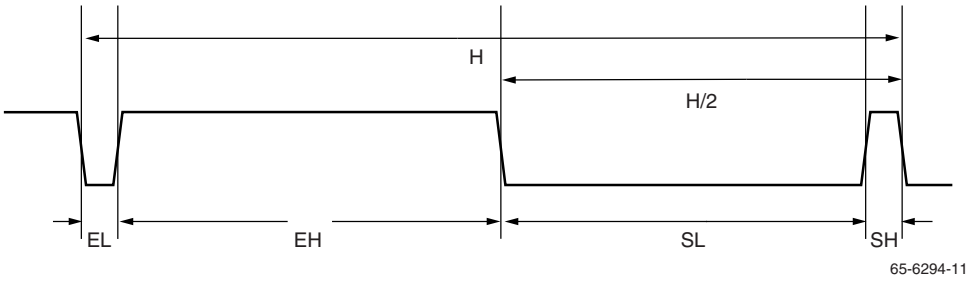


Figure 9. Horizontal Timing – Vertical Blanking

The VB and VC control registers are added to produce the half-lines needed in the vertical interval at the beginning and end of some fields. These must properly mate with components of the normal lines.

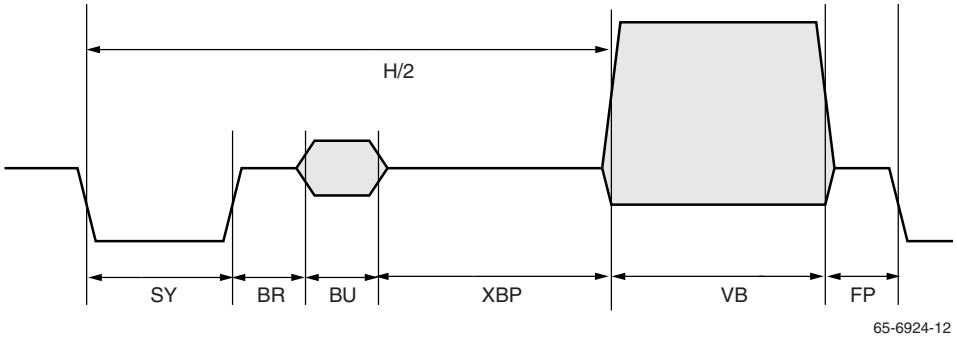


Figure 10. Horizontal Timing – 1st Half-line

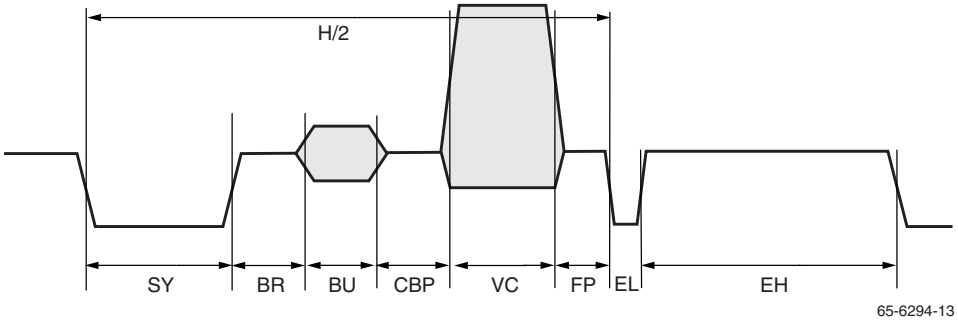


Figure 11. Horizontal Timing – 2nd Half-line

Table 6. Vertical Interval Timing Specifications

Parameter	NTSC-M (μs)	PAL-I (μs)	PAL-M (μs)
H	63.5556	64	63.492
EH	29.4778	29.65	29.45
EL	2.3	2.35	2.3
SH	4.7	4.7	4.65
SL	27.1	27.3	27.1

Table 7. Default Horizontal Timing Parameters

Standard	Field Rate (Hz)	Horizontal Freq. (KHz)	Pixel Rate (Mpps)	PXCK Freq. (MHz)	Timing Register (hex)														
					SY	BR	BU	CBP	XBP	VA	VC	VB	EL	EH[2]	SL[2]	SH	FP	Note	CBL
					20	21	22	23	24	25	26	27	28	29	2A	2B	2C	2D	2F
NTSC sqr. pixel	59.94	15.734266	12.27	24.54	3A	07	1F	0F	23	8B	05	77	1C	6A	4C	3A	12	65	52
NTSC CCIR-601	59.94	15.734266	13.50	27.00	40	08	22	11	44	CB	1E	98	1F	8E	6D	40	14	65	59
NTSC 4x F_{SC}	59.94	15.734266	14.32	28.64	43	09	24	12	54	F7	30	B5	21	A6	84	43	15	65	5F
PAL sqr. pixel	50.00	15.625000	14.75	29.50	45	0D	21	21	6D	03	2B	B7	23	B5	93	45	19	75	61
PAL CCIR-601	50.00	15.625000	13.50	27.00	40	0C	1E	22	4D	BE	0E	93	20	90	70	40	16	65	59
PAL 15 Mpps	50.00	15.625000	15.00	30.00	46	0D	22	21	73	11	31	BF	23	BD	9A	47	19	75	62
PAL-M sqr.pixel	60.00	15.750000	12.50	25.01	3E	0B	1C	13	26	86	FE	8B	1D	70	53	3A	18	61	52
PAL-M CCIR-601	60.00	15,750000	13.50	27.00	44	0C	1E	13	26	Bf	12	99	1F	8E	6E	3F	1A	65	57
PAL-M 4x F_{SC}	60.00	15,750000	14.30	28.60	47	0D	20	15	4C	E8	22	AC	21	A5	84	42	1B	65	5D

Notes:

1. XBP, VA, VC, and VB are 10 bit values. The 2 MSBs for these four variables are in Timing Register 2D.
2. EH and SL are 9 bit values. A most significant "1" is forced by the TMC2192 since EH and SL must range from 256 to 511. EH and SL may be extended to 767. Only the eight LSBs are stored in Timing Registers 29 and 2A.
3. Every calculated timing parameter has a minimum value of 5 except EH and SL which have minimum values of 256.

Vertical Timing

The vertical timing is controlled by the FORMAT control register, which dictates the field and line sequence.

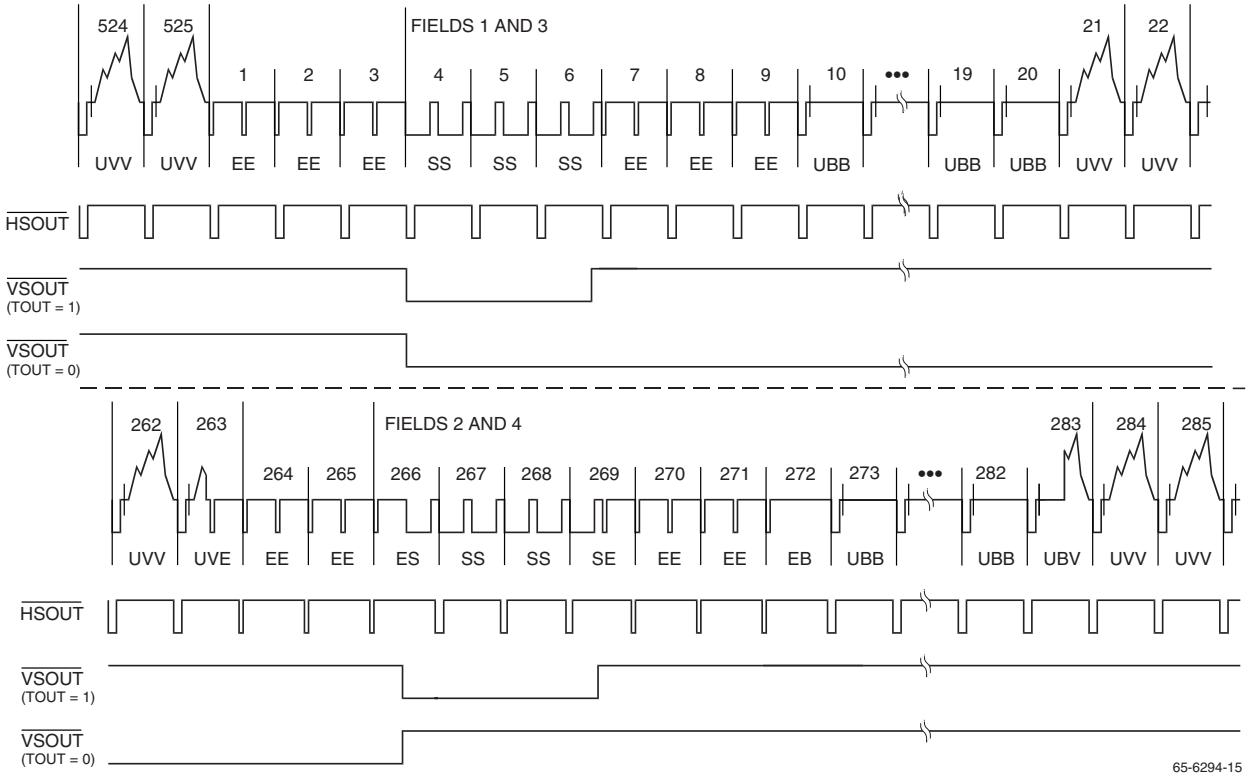


Figure 12. NTSC Vertical Interval

Table 8. NTSC Field/Line Sequence and Identification

Field 1 FIELD ID = x00			Field 2 FIELD ID = x01			Field 3 FIELD ID = x10			Field 4 FIELD ID = x11		
Line	**ID**	**LTYPE**	**Line**	**ID**	**LTYPE**	**Line**	**ID**	**LTYPE**	**Line**	**ID**	**LTYPE**
4	SS	03	266	ES	01	4	SS	03	266	ES	01
5	SS	03	267	SS	03	5	SS	03	267	SS	03
6	SS	03	268	SS	03	6	SS	03	268	SS	03
7	EE	00	269	SE	02	7	EE	00	269	SE	02
8	EE	00	270	EE	00	8	EE	00	270	EE	00
9	EE	00	271	EE	00	9	EE	00	271	EE	00
10	UBB	0D	272	EB	10	10	UBB	0D	272	EB	10
…	UBB	0D	273	UBB	0D	…	UBB	0D	273	UBB	0D
19	UBB	0D	…	UBB	0D	19	UBB	0D	…	UBB	0D
20	UBB	0D	282	UBB	0D	20	UBB	0D	282	UBB	0D
21	UVV	0F	283	UBV	0E	21	UVV	0F	283	UBV	0E
22	UVV	0F	284	UVV	0F	22	UVV	0F	284	UVV	0F
…	UVV	0F	…	UVV	0F	…	UVV	0F	…	UVV	0F
262	UVV	0F	524	UVV	0F	262	UVV	0F	524	UVV	0F.
263	UVE	0C	525	UVV	0F	263	UVE	0C	525	UVV	0F
264	EE	00	1	EE	00	264	EE	00	1	EE	00
265	EE	00	2	EE	00	265	EE	00	2	EE	00
			3	EE	00				3	EE	00

EE Equalization pulse
SE Half-line vertical sync pulse, half-line equalization pulse
SS Vertical sync pulse
ES Half-line equalization pulse, half-line vertical sync pulse
EB Equalization broad pulse
UBB Black burst
UVV Active video
UVE Half-line video, half-line equalization pulse
UBV half-line black, half-line video

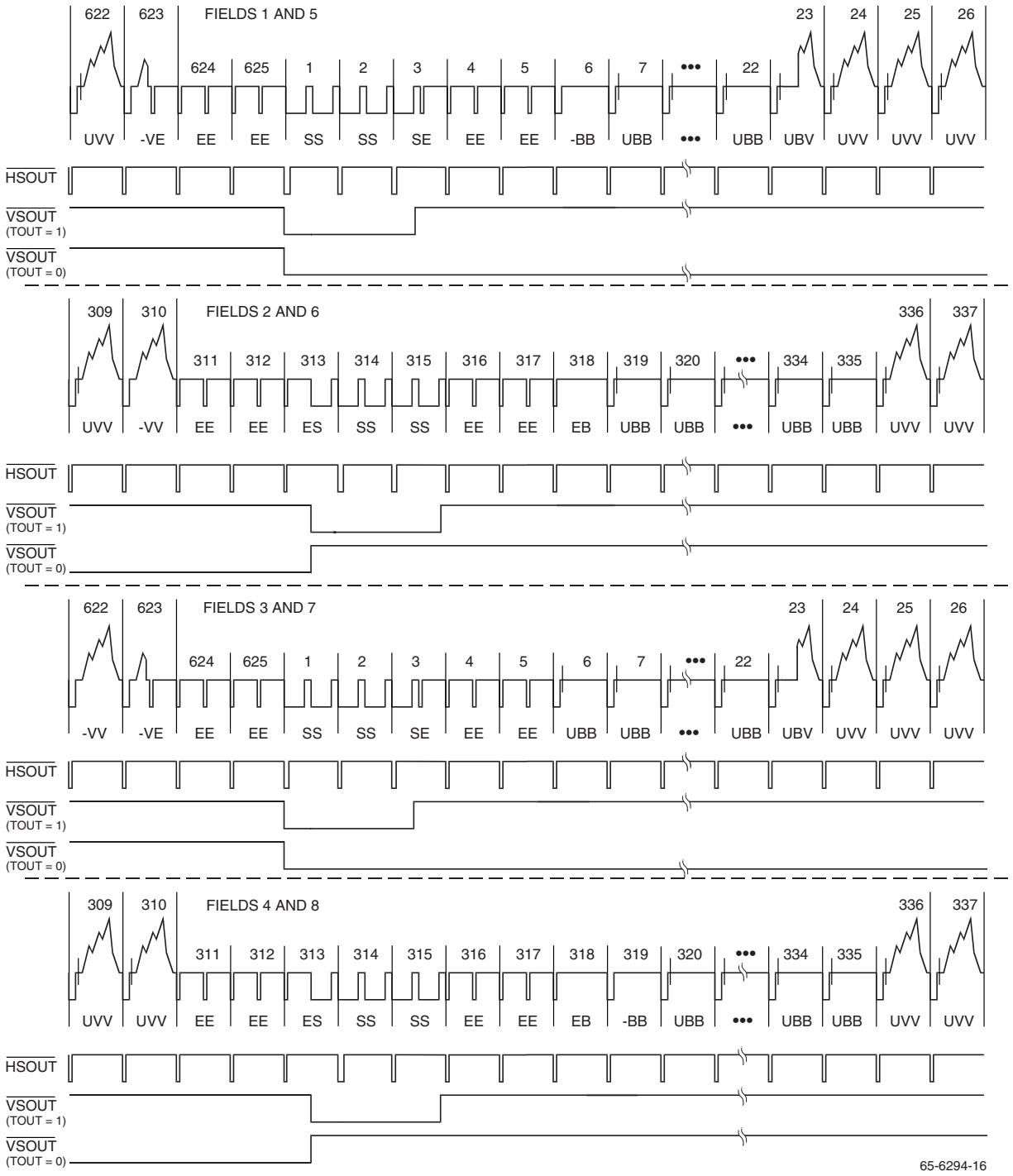


Figure 13. PAL Vertical Interval

Table 9. PAL Field/Line Sequence and Identification

Field 1 & 5 FIELD ID = 000, 100			Field 2 & 6 FIELD ID = 001, 111			Field 3 & 7 FIELD ID = 010, 110			Field 4 & 8 FIELD ID = 011, 111		
Line	**ID**	**LTYPE**	**Line**	**ID**	**LTYPE**	**Line**	**ID**	**LTYPE**	**Line**	**ID**	**LTYPE**
1	SS	03	313	ES	01	1	SS	03	313	ES	01
2	SS	03	314	SS	03	2	SS	03	314	SS	03
3	SE	02	315	SS	03	3	SE	02	315	SS	03
4	EE	00	316	EE	00	4	EE	00	316	EE	00
5	EE	00	317	EE	00	5	EE	00	317	EE	00
6	-BB	05	318	EB	10	6	UBB	0D	318	EB	10
7	UBB	0D	319	UBB	0D	7	UBB	0D	319	-BB	05
…	UBB	0D	320	UBB	0D	…	UBB	0D	320	UBB	0D
22	UBB	0D	…	UBB	0D	22	UBB	0D	…	UBB	0D
23	UBV	0E	334	UBB	0D	23	UBV	0E	334	UBB	0D
24	UVV	0F	335	UBB	0D	24	UVV	0F	335	UVV	0F.
25	UVV	0F	336	UVV	0F	25	UVV	0F	336	UVV	0F
26	UVV	0F	337	UVV	0F	26	UVV	0F	337	UVV	0F
…	UVV	0F	…	UVV	0F	…	UVV	0F	…	UVV	0F
309	UVV	0F	622	-VV	07	309	UVV	0F	622	UVV	0F
310	-VV	07	623	-VE	04	310	UVV	0F	623	-VE	04
311	EE	00	624	EE	00	311	EE	00	624	EE	00
312	EE	00	625	EE	00	312	EE	00	625	EE	00

EE Equalization pulse
SE Half-line vertical sync pulse, half-line equalization pulse
SS Vertical sync pulse
ES Half-line equalization pulse, half-line vertical sync pulse
EB Equalization broad pulse
UBB Black burst
-BB Black burst with color burst suppressed
UVV Active video
-VV Active video with color burst suppressed
UVE Half-line video, half-line equalization pulse
-VE Half-line video, half-line equalization pulse, color burst suppressed.
UBV half-line black, half-line video

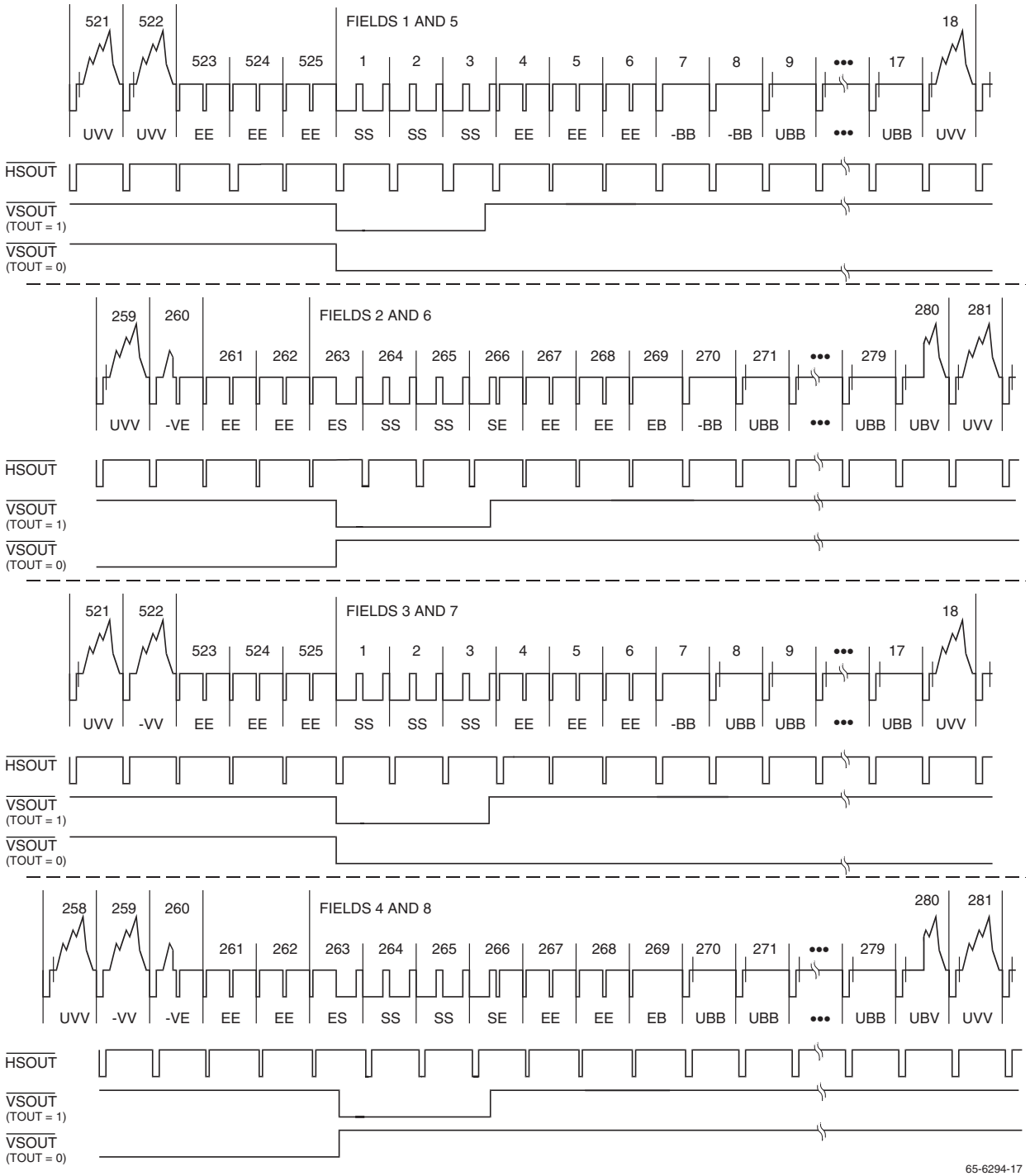


Figure 14. PAL-M Vertical Interval

Table 10. PAL-M Field/Line Sequence and Identification

Field 1 & 5 FIELD ID = 000, 100			Field 2 & 6 FIELD ID = 001, 111			Field 3 & 7 FIELD ID = 010, 110			Field 4 & 8 FIELD ID = 011, 111		
Line	**ID**	**LTYPE**	**Line**	**ID**	**LTYPE**	**Line**	**ID**	**LTYPE**	**Line**	**ID**	**LTYPE**
1	SS	03	263	ES	01	1	SS	03	263	ES	01
2	SS	03	264	SS	03	2	SS	03	264	SS	03
3	SS	03	265	SS	03	3	SS	03	265	SS	03
4	EE	00	266	SE	02	4	EE	00	266	SE	02
5	EE	00	267	EE	00	5	EE	00	267	EE	00
6	EE	00	268	EE	00	6	EE	00	268	EE	00
7	-BB	05	269	EB	10	7	-BB	05	269	EB	10
8	-BB	05	270	-BB	05	8	UBB	05	270	UBB	05
9	UBB	0D	271	UBB	1D	9	UBB	0D	271	UBB	1D
…	…	…	…	…	…	…	…	…	…	…	…
17	UBB	0D	279	UBB	0D	17	UBB	0D	279	UBB	0D
18	UVV	0F	280	UBV	0E.	18	UVV	0F	280	UBV	0E.
…	…	…	281	UVV	0F	…	UVV	0F	281	UVV	0F
259	UVV	0F	…	…	…	258	UVV	0F	…	…	…
260	-VE	04	521	UVV	0F	259	-VV	07	521	UVV	0F
261	EE	00	522	-VV	07	260	-VE	04	522	UVV	0F
262	EE	00	523	EE	00.	261	EE	00	523	EE	00
			524	EE	00	262	EE	00	524	EE	00
			525	EE	00				525	EE	00

EE Equalization pulse
SE Half-line vertical sync pulse, half-line equalization pulse
SS Vertical sync pulse
ES Half-line equalization pulse, half-line vertical sync pulse
EB Equalization broad pulse
UBB Black burst
-BB Black burst with color burst suppressed
UVV Active video
-VV Active video with color burst suppressed
UVE Half-line video, half-line equalization pulse
-VE Half-line video, half-line equalization pulse, color burst suppressed.
UBV half-line black, half-line video

Chrominance Processor

Control registers for this section:

Address	Bit(s)	Name
0x06	7-6	FORMAT
0x06	5-3	MODE
0x07	5	DDSRST
0x11	7	DRSSEL
0x18	6	GLKCTL1
0x18	5	GLKCTL0
0x3F	3	GAUSS_BYP
0x40	7-0	FREQL
0x41	7-0	FREQ3
0x42	7-0	FREQ2
0x43	7-0	FREQM
0x44	7-4	SYSPHL
0x45	3-0	SYSPHM
0x46	7-4	BURPHL
0x47	3-0	BURPHM
0x48	7-4	BRSTFULL
0x49	3-0	BRST1
0x4A	7-4	BRST2

Subcarrier Programming

The color subcarrier is produced by an internal 32 bit digital frequency synthesizer which is completely programmable in frequency and phase. Separate registers, FREQx, SYSPHx, BSTPHx, are provided for phase adjustment of the color burst and of the active video, permitting external delay compensation, color adjustment, etc. FREQx is the subcarrier phase step per pixel and SYSPHx is phase offset at field 1, line 1 (line 4 for NTSC), pixel 1.

NTSC Subcarrier

For NTSC encoding, the subcarrier synthesizer frequency has a simple relationship to the pixel clock period, repeating over 2 lines: The decimal value for the subcarrier phase step is:

$$\mathrm{FREQx} = \frac{455/2}{\mathrm{pixels/line}} \times 2^{32}$$

Where the number of pixels/line is:

$$\mathrm{pixels/line} = \frac{\mathrm{PXCK\ Frequency}}{\mathrm{H\ Period}}$$

This value must be converted to binary and split into four 8 bit registers, FREQM, FREQ2, FREQ3, and FREQL.

PAL Subcarrier

The PAL relationship is more complex, repeating only once in 8 fields (the well-known 25 Hz offset):

$$\mathrm{FREQx} = \frac{(1135/4) + (1/625)}{\mathrm{pixels/line}} \times 2^{32}$$

This value must be converted to binary and split as described previously for NTSC. The number of pixels/line is found as in NTSC.

PAL-M Subcarrier

$$\mathrm{FREQ} = \frac{909/4}{\mathrm{pixels/line}} \times 2^{32}$$

SYSPHx establishes the appropriate phase relationship between the internal synthesizer and the chroma modulator. The nominal value for SYSPHx is zero.

Other values for SYSPHx must be converted to binary and split into two 8 bit registers, SYSPHM and SYSPHL.

Burst Phase (BURPHx) sets up the correct relative NTSC modulation angle. The value for BURPH is:

BURPHx = SYSPHx

This value must be converted to binary and split into two 8 bit registers, BURPHM and BURPHL.

Table 11. Standard Subcarrier Parameters

Standard	Field Rate (Hz)	Horizontal Freq. (kHz)	Pixel Rate (Mpps)	PXCK Freq. (MHz)	Subcarrier Freq. (MHz)	Subcarrier Register (hex)							
						BURPHM	BURPHL	SYSPHM	SYSPHL	FREQM	FREQ2	FREQ3	FREQL
						47	46	45	44	43	42	41	40
NTSC sqr. pixel	59.94	15.734266	12.27	24.54	3.57954500	00	00	00	00	4A	AA	AA	AB
NTSC CCIR-601	59.94	15.734266	13.50	27.00	3.57954500	00	00	00	00	43	E0	F8	3E
NTSC 4x F_{SC}	59.94	15.734266	14.32	28.64	3.57954500	00	00	00	00	40	00	00	00
PAL sqr. pixel	50.00	15.625000	14.75	29.50	4.43361875	00	00	00	00	4C	F3	18	19
PAL CCIR-601	50.00	15.625000	13.50	27.00	4.43361875	00	00	00	00	54	13	15	96
PAL 15 Mpps	50.00	15.625000	15.00	30.00	4.43361875	00	00	00	00	4B	AA	C6	A1
PAL-M sqr.pixel	60.00	15.750000	12.50	25.01	3.57561149	00	00	00	00	49	45	00	51
PAL-M CCIR-601	60.00	15,750000	13.50	27.00	3.57561149	00	00	00	00	43	DF	3F	D7
PAL-M 4x F_{SC}	60.00	15,750000	14.30	28.60	3.57561149	00	00	00	00	40	10	66	F5

Subcarrier Synchronization

There are 5 modes of subcarrier synchronization in the TMC2192, freerun, subcarrier reset, Genlock, DRS-lock and Ancillary Data Control (ANC).

- Freerun

At the rising edge of $\overline{\text{RESET}}$ the DDS starts to generate the subcarrier reference and will continue to freerun the subcarrier. When setting the control register DDSRST is HIGH, the TMC2192 will reset the DDS to the SYSPH value on the next field 1, line 1 (line 4 for NTSC), pixel 1 occurrence and will reset this bit to be LOW. This allows the encoder to start with the correct SCH relationship. The phase of the subcarrier reference will drift over time since a 32 bit accumulator has a error of ±0.5 Hz when generating the subcarrier reference for NTSC 13.5 MHz.

- Subcarrier Reset

At the rising edge of $\overline{\text{RESET}}$ the DDS starts to generate the subcarrier reference and will reset the DDS to the SYSPH value every field 1, line 1 (line 4 for NTSC), pixel 1 occurrence. This enables the encoder to maintain the proper SCH relationship.

- Genlock

The Genlock mode allows the TMC2192 to lock to a composite reference when used in conjunction with the TMC22071A Genlocking Video Digitizer. The TMC22071A produces a genlock reference signal (GRS) which contains field identification, PALODD status, relative phase and relative frequency of the composite reference. The GRS is sampled on the CVBS bus 60 PXCK's after the falling edge of $\overline{\text{HSIN}}$. The phase and frequency values are used to update the DDS on a line to line basis, thus synchronizing the subcarrier to an external composite reference.

- DRS-Lock

The DRS-Lock mode allows the TMC2192 to lock its composite output to the decoded composite or S-video input of the TMC22x5y. The TMC22x5y produces a decoder reference signal (DRS) which contains field identification, PALODD status, relative phase and relative frequency of the composite or S-video input. The DRS is sampled on either the CVBS bus or the PD port, depending on DRSSEL, 60 PXCK's after the falling edge of $\overline{\text{HSIN}}$. The phase and frequency values are used to update the DDS on a line to line basis, thus synchronizing the subcarrier to an external composite reference.

- Ancillary Data Control (ANC)

Subcarrier synchronization in ANC mode is covered in the Ancillary Data Control section of this data sheet.

SCH Phase Error Correction

SCH refers to the timing relationship between the 50% point of the leading edge of horizontal sync and the positive or negative zero-crossing of the color burst subcarrier reference. SCH error is usually expressed in degrees of subcarrier phase. In PAL, SCH is defined for line 1 of field 1, but since there is no color burst on line 1, SCH is usually measured at line 7 of field 1. The need to specify SCH relative to a particular line in PAL is due to the 25 Hz offset of PAL subcarrier frequency. Since NTSC has no such 25 Hz offset, SCH applies to all lines.

The SCH relationship is important in the TMC2192 when two video sources are being combined or if the composite video output is externally combined with another video source. In these cases, improper SCH phasing will result in a noticeable horizontal jump of one image with respect to another and/or a change in hue proportional to the SCH error between the two sources.

SCH phasing can be adjusted by modifying BURPH and SYSPH values by equal amounts. SCH is advanced/delayed by one degree by increasing/decreasing the value of BURPH and SYSPH by approximately $B6_h$. An SCH error of 15^o is corrected with SYSPH and BURPH offsets of AAA_h.

Burst Envelope

The TMC2192 includes the ability to adjust the burst amplitude and the shape of the burst. The Control Registers BRSTFULL, BRST1 and BRST2 hold the magnitude of the burst vector. BRSTFULL is the maximum amplitude of the burst vector. BRST1 and BRST2 determine the intermediate values of the burst vector for the burst envelope shaping. A 5 pixel burst envelope shaping occurs at the rising and falling edges of burst. At the rising edge of burst the next 5 pixels have the following weighting; BRSTFULL – BRST1, BRSTFULL – BRST2, BRSTFULL/2, BRST2, and BRST1. At the falling edge of burst the next 5 pixels have the following weighting; BRST1, BRST2, BRSTFULL/2, BRSTFULL – BRST2, and BRSTFULL – BRST1. With this flexibility the user determine the shape, amplitude and width of the burst signal.

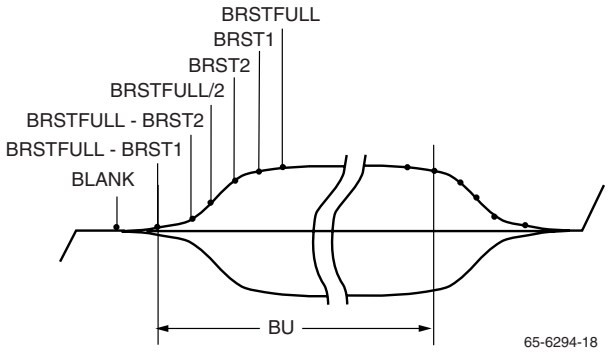


Figure 15. Burst Envelope

Color-Difference Low-Pass Filters

The chrominance portion of a composite video signal must be sufficiently bandlimited to avoid cross-color and cross-luminance distortion, and to preclude exceeding the allowable bandwidth of a video channel.

The color-difference low-pass filters on the TMC2192 establish chrominance bandwidths which meet the specifications outlined in CCIR Report 624-3, Table II, Item 2.6, for system I over a range of pixel rates from 12.27 Mpps to 14.75 Mpps. Equal bandwidth is established for both color-difference channels.

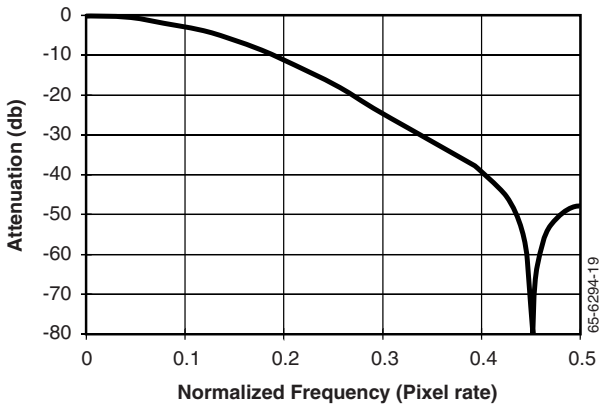


Figure 16. Gaussian Filter Response

Sync and Pedestal Insertion

Control Registers for this section

Address	Bit(s)	Name
0x06	7-6	MODE
0x11	5	COMP2DB
0x14	7-0	VBIPEDEM
0x15	7-0	VBIPEDEL
0x16	7-0	VBIPEDOM
0x17	7-0	VBIPENOL
0x1A	6-0	PEDHGT1
0x3F	3	C2DB_OFF

Pedestal Enable

The TMC2192 has the ability to independently select lines for pedestal insertion during the vertical blanking interval (VBI). For 525-line systems and using the NTSC line numbering convention, in which the first vertical serration is on line 4 for field 1 and line 266 for field 2, the vertical interval lines map to the control registers VBIPEDxy as shown in Table 15.

Table 12. Line by Line Pedestal Enable

Bit	7	6	5	4	3	2	1	0
VBIPEDEL	17	16	15	14	13	12	11	10
VBIPEDEM	25*	24	23	22	21	20	19	18
VBIPEDOL	279	278	277	276	275	274	273	
VBIPEDOM	287*	286	285	284	283	282	281	280

Enabling the pedestal on line 25 enables it for the remainder of field 1, to line 262. Likewise, enabling the pedestal on line 288 enables it for the remainder of field 2.

Pedestal Height

PEDHGT1 determines the height of the pedestal for the luminance channel on the composite path. The range of the pedestal height is from -22.1 to 21.74 IRE in .345 IRE increments.

Sync and Blank Insertion

The composite paths blank and sync D/A codes are determined by the FORMAT control register. For NTSC and PAL-M formats the blank D/A code is 240 (295 mV) and the sync D/A code is 8 (9 mV). For all other PAL formats the blank D/A code is 256 (314 mV) and the sync D/A code is 12 (14 mV).

In all cases the sync edges are sloped to insure the proper rise and fall times in all video standards.

Closed Caption Insertion

Control Registers for this section

Address	Bit(s)	Name
0x1C	7-6	CCD1
0x1D	1-0	CCD2
0x1E	7	CCON
0x1E	6	CCRTS
0x1E	5	CCPAR
0x1E	4	CCFLD
0x1E	3–0	CCLINE

The TMC2192 includes a flexible closed-caption processor. It may be programmed to insert a closed caption signal on any line within a range of 16 lines on ODD and/or EVEN fields. Closed Caption insertion overrides all other configurations of the encoder: if it is specified on an active video line, it takes precedence over the video data and removes NTSC setup if setup has been programmed for the active video lines. Closed Caption is only available when the TMC2192 is in a 13.5 MHz pixel rate.

Closed caption is turned on by setting CCON HIGH. Whenever the encoder begins producing a line specified by CCFLD and CCLINE, it will insert a closed caption line in its place. If CCRTS is HIGH, the data contained in CCDx will be sent. IF CCRTS is LOW, Null bytes (hex 00 with ODD parity) will be sent.

Line Selection

The line to contain CC data is selected by a combination of the CCFLD bit and the CCLINE bits. CCLINE is added to the offset shown in Table 16 to specify the line.

Table 13. Closed Caption Line Selection

Standard	Offset	Field	Lines
525	12	ODD	12-27
	274	EVEN	274-289
625	16	ODD	16-31
	328	EVEN	328-343

Parity Generation

Standard Closed-Caption signals employ ODD parity, which may be automatically generated by setting CCPAR HIGH. Alternatively, parity may be generated externally as part of the bytes to be transmitted, and, with CCPAR LOW, the entire 16 bits loaded into the CCDx registers will be sent unchanged.

Operating Sequence

A typical operational sequence for closed-caption insertion on line xx is:

Read Register 1E and check that bit 7 is LOW, indicating that the CCDx registers are ready to accept data.

If ready, write two bytes of CC data into registers 1C and 1D.

Write into register 1E the proper combination of CCFLD and CCLINE. CCPAR may be written as desired. Set CCRTS HIGH.

The CC data is transmitted during the specified line.

As soon as CCDx s transferred into the CC processor (and CCRTS goes LOW), new data may be loaded into registers 1C and 1D. This allows the user to transmit CC data on several consecutive lines by loading data for line n+1 while data is being sent on line n.

Interpolation Filters

Each video output on the TMC2192 is digitally filtered with sharp-cutoff low-pass interpolation filters. These filters ensure that the frequency band above base-band video and below the pixel frequency ($f_S/4$ to $3f_S/4$, where f_S is the PXCK frequency) are sufficiently suppressed.

Since these are fixed-coefficient digital filters, their filter characteristics depend upon clock rate.

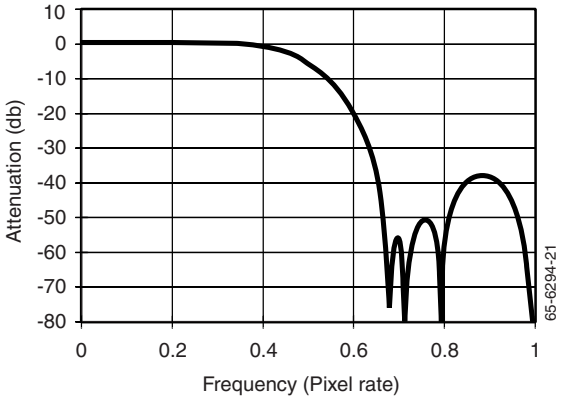


Figure 17. Interpolation Filter

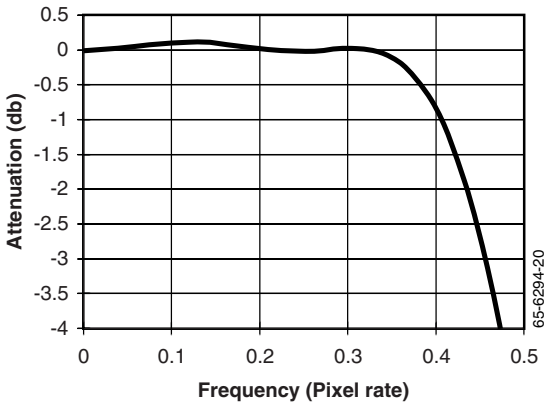


Figure 18. Interpolation Filter – Passband Detail

x/Sin(x) Filter

Control Registers for this section

Address	Bit(s)	Name
0x11	4	SINEN

The TMC2192 contains a selectable X/sin(X) filter prior to each DAC. The X/sin(X) filter boosts the high frequency data to negate the sin(X)/X roll-off associated with D/A converters.

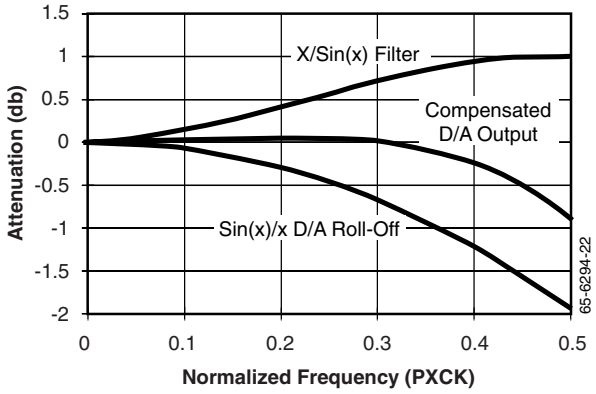


Figure 19. X/SIN(X) Filter

Output Data Formats

Control Registers for this section

Address	Bit(s)	Name
0x10	5	LUMADIS
0x10	6	CHROMADIS
0x10	7	COMPDIS
0x3F	7	SEL_CLK
0x3F	4	SEL_PIX

Analog outputs of the TMC2192 are driven by three 10 bit D/A converters, operating at twice the pixel rate. The outputs drive standard video levels into 37.5 or 75 Ohm loads. An internal voltage reference is used to provide reference current for the D/A converters. For more accurate levels, an external fixed or variable voltage reference source is accommodated. The video signal levels from the TMC2192 may be adjusted by varying the common Vref or the 3 independent Rrefs. Each video D/A converter has an independent reference resistor that can adjust the output gain. D/A Matching is achieved by trimming the each external reference resistor of each D/A.

Digital Composite Output

In addition, the TMC2192 supplies a 10 bit digital composite signal on pins D[7:0] and FLD[2:1]. The digital composite output can be either an interpolated signal on a non-interpolated signal, this controlled by the control register SEL_CLK.

Ancillary Data

Control Registers for this section

Address	Bit(s)	Name
0x07	2	ANCFREN
0x07	1	ANCPHEN
0x07	0	ANCTREN
0x08	7-0	ANCID

The TMC2192 is designed to accept 15 words of ancillary data after the active video pixels at the end of each horizontal line. Ancillary data may occur once per line, once per field, once per eight fields, on random lines, or not al all. The TMC2192 does not assume ancillary data is present on a regular basis.

Table 14. Ancillary Data Format

Word ID	Description	B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0
ANC2	Ancillary Data Header (Timing Reference Signal)	0	0	0	0	0	0	0	0
ANC1		1	1	1	1	1	1	1	1
ANC0		1	1	1	1	1	1	1	1
TT	Data Type	TT6	TT5	TT4	TT3	TT2	TT1	TT0	P
MM	Word	0	D11	D10	D9	D8	D7	D6	P
LL	Count	0	D5	D4	D3	D2	D1	D0	P
FIELD	Field ID/Synchronous Video Flag	x	x	x	$\overline{SVF}$	F2	F1	F0	P
	reserved	x	x	x	x	x	x	x	P
PH1	Subcarrier Phase	PHV	PH_{12}	PH_{11}	PH_{10}	PH_9	PH_8	PH_7	P
PH0		PH_6	PH_5	PH_4	PH_3	PH_2	PH_1	PH_0	P
FR4	Subcarrier Frequency	FRV	x	x	FR_{31}	FR_{30}	FR_{29}	FR_{28}	P
FR3		FR_{27}	FR_{26}	FR_{25}	FR_{24}	FR_{23}	FR_{22}	FR_{21}	P
FR2		FR_{20}	FR_{19}	FR_{18}	FR_{17}	FR_{16}	FR_{15}	FR_{14}	P
FR1		FR_{13}	FR_{12}	FR_{11}	FR_{10}	FR_9	FR_8	FR_7	P
FR0		FR_6	FR_5	FR_4	FR_3	FR_2	FR_1	FR_0	P

Note:

1. P = odd parity bit, x = reserved bit will be ignored

The first three words of ancillary data comprise the TRS signal (ANC2-0) which indicates the end of active video. Also known as the Ancillary data header, the TRS signal is a 00_h, FF_h, FF_h sequence. Except for the TRS words, ancillary data bit 0 (B_0, LSB) is odd parity for B_{7-1}.

The data type word (TT) is used to specify the ancillary data type. The TMC2192 compares this 7 bit value with the contents of the ANCID control register. If there is a match, the ancillary data will be processed. If there is no match, the TMC2192 ignores ancillary data.

The word count data (D_{11-0} in MM, LL) in the ancillary data packet indicate the number of words in ancillary data.

Ancillary phase data is used to program the MSBs of the PHASE register. ANCPHEN and PHV determine how ancillary phase data is used. When ancillary data is not present, the TMC2192 assumes PHV = LOW.

Table 15. Ancillary Data Control – Phase

ANCPHEN	PHV	Description
0	x	Ignore ancillary phase data, set PHASE = 0
1	0	Ignore ancillary phase data, no change to PHASE
1	1	Load ancillary phase data into PHASE registers

Ancillary frequency data is used to program the 32 bits of the FREQ3-0 registers. ANCFREN and FRV determine how ancillary frequency data is used. When ancillary data is not present, the TMC2192 assumes FRV = LOW.

Table 16. Ancillary Data Control Frequency

ANCFREN	FRV	Description
0	x	Ignore ancillary frequency data
1	0	Ignore ancillary frequency data
1	1	Load ancillary frequency data into FREQ3-0 registers

Table 17. Field Identification and Subcarrier Reset Modes

ANCTREN	$\overline{SVF}$	F_2	F_1	F_0	F (EAV)	Field ID / Subcarrier Reset Mode
Basic Mode						
0	x	x	x	x	0	Odd field, reset subcarrier every 8 fields
0	x	x	x	x	1	Even field
Genlocking Mode						
1	1	x	x	x	0	Odd field, subcarrier free run
1	1	x	x	x	1	Even field
Field Sequence Mode						
1	0	0	0	0	0	Field 1, reset subcarrier at field 1
1	0	0	0	1	1	Field 2
1	0	0	1	0	0	Field 3
1	0	0	1	1	1	Field 4
1	0	1	0	0	0	Field 5
1	0	1	0	1	1	Field 6
1	0	1	1	0	0	Field 7
1	0	1	1	1	1	Field 8

Note:
1. The F bit is part of the EAV timing reference code and tracks the F0 bit.

Operating Modes

The field number bits (F_{2-0}) from the ancillary data packet FIELD word, are used to program the encoder's field counter depending upon the state of the synchronous video flag ($\overline{SVF}$) and the ANCTREN bit in the control register.

In the basic operating mode (ANCTREN = LOW), all timing is found in the F bit of EAV. F_{2-0} and $\overline{SVF}$ are ignored and the encoder subcarrier synthesizer is reset to the PHASE value every eight fields (when the field counter transitions from 111 (field 8) to 000 (field 1).

In the basic mode, ANCFREN and ANCPHEN are typically set LOW, ignoring ancillary frequency and phase data. If ANCFREN and ANCPHEN are HIGH, the TMC2192 uses the incoming ancillary frequency and phase data on a line-by-line basis.

In genlocking mode (ANCTREN and $\overline{SVF}$ = HIGH), the subcarrier synthesizer is allowed to free run, with phase and frequency being set from the ancillary data packet PH_{12-0} and FR_{31-0} data. The field counter increments just like it does in basic mode.

Field sequence mode (ANCTREN = HIGH and $\overline{SVF}$ = LOW), is the same as basic mode except that the field counter is set by the F_{2-0} bits in the FIELD word of ancillary data. If ancillary data is not present on a line, the field counter will continue to count as it does in basic mode. When ancillary data is present, the contents of the field counter are loaded with field data (F_{2-0}). In this way, the TMC2192 may be synchronized with an external source by sending field data only once.

Layering Engine

Control Registers for this section

Address	Bit(s)	Name
0x04	2	SKEN
0x05	3-2	OMIX
0x07	6	SKFLIP
0x09	7	HKEN
0x09	6	BUKEN
0x09	5	SKEXT
0x09	4	DKDIS
0x09	3	EKDIS
0x09	2	FKDIS
0x09	1-0	LAYMODE

Address	Bit(s)	Name
0x0A	7-0	DKEYMAX
0x0B	7-0	DKEYMIN
0x0C	7-0	EKEYMAX
0x0D	7-0	EKEYMIN
0x0E	7-0	FKEYMAX
0x0F	7-0	FKEYMIN

The TMC2192 features a robust layering engine with three possible input layers controlled by two keying controls. The layer assignments are shown in Table 22, along with the keying control. The keying controls, KEY pin or OL4-0 are aligned with the incoming pixel data stream and are then delayed throughout the chip to be continuously aligned with the input video streams. A generic overview of the keying and layering features is shown in Figure 21.

Table 18. Layering and Keying Modes

LAYMODE	BACKGROUND	MIDGROUND		FOREGROUND	
	Image Source	Image Source	Keying Control	Image Source	Keying Control
0	PD	OVERLAY	OL4-0	CVBS	KEY or Data Key
1	PD	CVBS	KEY or Data Key	OVERLAY	OL4-0
2	CVBS	OVERLAY	OL4-0	PD	KEY or Data Key
3	CVBS	PD	KEY or Data Key	OVERLAY	OL4-0

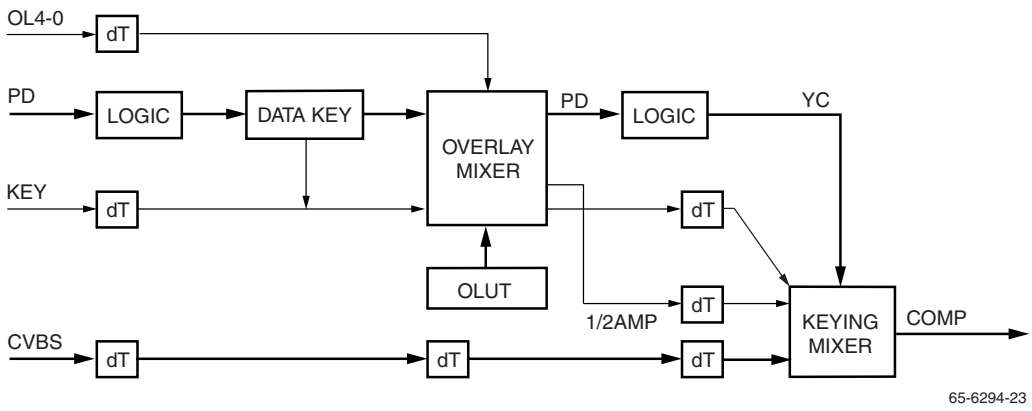


Figure 20. Layering Engine

Overlay Mixer

The OL[4:0] bus provides the ability to overlay 30 different 24 bit values onto the pixel data path. The 24 bit overlay colors must be the same format as the incoming Pixel data. For Y,Cb,Cr input formats the range of Y values spans the entire range of the format, 1 to 254, this enables super whites and super blacks in the overlay palette.

When OL[4:0] is equal to 00h the pixel data port to be the output of the overlay mixer. If OL[4:0] is in the range of 1 to 31 then the output source is one of 30 possible overlay colors, see Table 22. Overlay Address Map. When OL4-0 equal to 16, the overlay mixer produces a pixel data output with half the luminance magnitude and chrominance magnitude. Any OL4-0 value greater than 16 will result in a overlay mix with a full amplitude overlay and the pixel data with half amplitude pixel data (PD) or half amplitude CVBS data as its values. This allows for transparent overlays or produce shadow boxes around overlaid text.

The midpoint of the rising and falling edges on the mixed output is determined by the transition of the OL[4:0] pins in

relation to the PD port. Control register OMIX chooses among the following set of coefficients; either 0 1/8 1/2 7/8 1, 0 1/2 1 , or 0 1 to switch between the PD port and the overlay color. The timing diagram in Figure 22 identifies the three possible output formats that the mixer can produce.

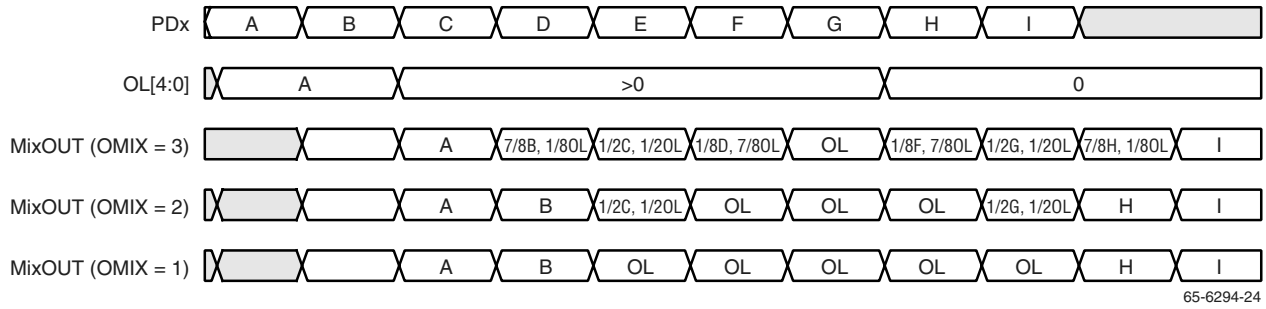


Figure 21. Overlay Outputs

Table 19. Overlay Address Map

OL4-0	Result
0	Pixel data is passed through overlay mixer.
1-15	Overlay is mixed with PD or CVBS at the transitions.
16	Half amplitude PD or half amplitude CVBS is the output of COMP2.
17-31	Overlay is mixed with half amplitude PD or half amplitude CVBS at the transitions.

Hardware Keying

The KEY input switches the input to the Comp data path between the composite video generated from the PD port and the CVBS data bus on a pixel-by-pixel basis. This is a “soft” switch is executed over 3 PCK periods to minimize out-of-band transients. Keying is accomplished in the digital composite video domain. The coefficients for the mix are 0, 1/8, 1/2, 7/8, and 1 . The COMP output is the final output for all overlay functions.

Hardware keying is enabled by the key Control Register HKEN. Normally, keying is only effective during the active video portion of the encoded video line (as determined by Control Register VA). That is, the horizontal blanking interval is generated by the encoder even if the KEY signal is held HIGH through horizontal blanking. However, it is possible to allow digital horizontal blanking to be passed through from the CVBS bus to the COMP output by setting key Control Register BUKEN HIGH. In this mode, KEY is always active, and may be exercised at will.

The KEY input is registered into the encoder just as Pixel data is clocked into the PD port. It is internally pipelined, so the midpoint of the KEY transition occurs at the output of the pixel that was input at the same time at the KEY signal.

Data Keying

Data keying for each channel Y, C_b, and C_r, is separately enabled or disabled by the control registers DKEYDIS, EKEYDIS, and FKEYDIS. On each channel the eight (8) MSBs of the pixel data are compared against a maximum key value and a minimum key value. If the pixel data is greater than xKEYMIN and less than or equal to xKEYMAX, then a key match is signaled for that channel.

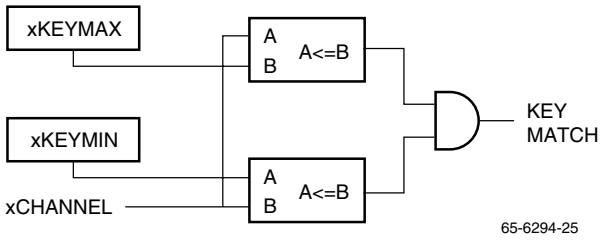


Figure 22. Data Keying

By allowing a window of possible key values on each channel the TMC2192 opens a key cube in the color space.

Parallel Microprocessor Interface

The parallel microprocessor interface is active when $\overline{SER}$ is HIGH and employs a 12-line interface; an 8 bit data bus and 2 bit address location, 1 bit read/write select, and a chip select controlling the timing. Two addresses are required for device programming, one to the pointer and one to the data location. When writing, the address is presented along with a LOW on the R/$\overline{W}$ pin during the falling edge of $\overline{CS}$. Eight bits of data are presented on D7-0 during the subsequent rising edge of $\overline{CS}$.

In read mode, the address is accompanied by a HIGH on the R/$\overline{W}$ pin during a falling edge of $\overline{CS}$. The data output pins go to a low-impedance state t_{DOZ} after $\overline{CS}$ falls. Valid data are present on D7-0 t_{DOM} after the falling edge of $\overline{CS}$. Because this port operates asynchronously with the pixel timing, there is an uncertainty in this data valid output delay of one PXCK period. This uncertainty does not apply to t_{DOZ}.

Writing data to specific control registers of the TMC2192 requires that the 8 bit address of the control register of interest be written prior to the data. This control register address is the base address for subsequent write operations. The base address auto increments by one for each byte of data written after the data byte intended for the base address. If more bytes are transferred than there are available addresses, the address will not increment and remain at its maximum value of 4Ch.

Writing data to specific OLUT location of the TMC2192 requires that the 8 bit address of the OLUT location of interest be written prior to the data sequence. This OLUT location address is the base address for subsequent write operations. The base address auto increments by one for each sequence of three (3) bytes of data written after the data byte intended for the base address. The sequence of data transfer is Y, C_b, C_r , after the C_r byte is transferred the base address will increment by one (1).

Table 20. Parallel Port Control

A_{1-0}	R/$\overline{W}$	Action
00	0	Load D_{7-0} into Control Register pointer (block 0)
00	1	Read Control Register pointer on D_{7-0}
01	0	Load D_{7-0} into addressed OLUT Location pointer (block 0)
01	1	Read addressed OLUT Location pointer on D_{7-0}.
10	0	Write D_{7-0} to addressed Control Register
10	1	Read addressed Control Register on D_{7-0}
11	0	Write D_{7-0} to addressed OLUT Location
11	1	Read addressed OLUT Location on D_{7-0}

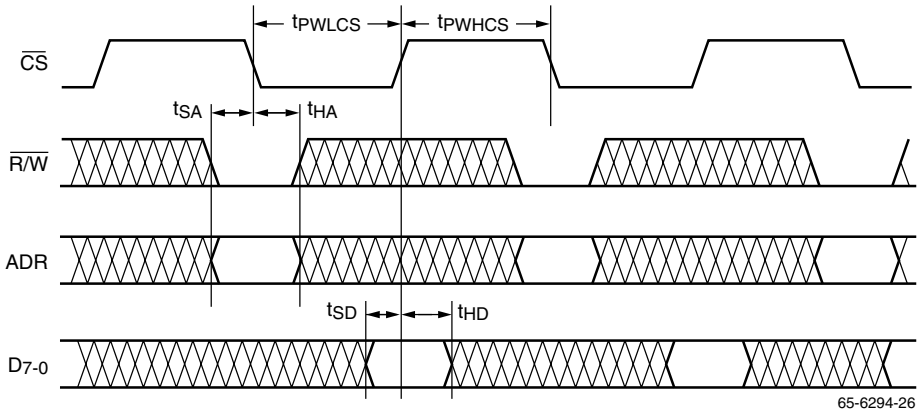


Figure 23. Microprocessor Parallel Port – Write Timing

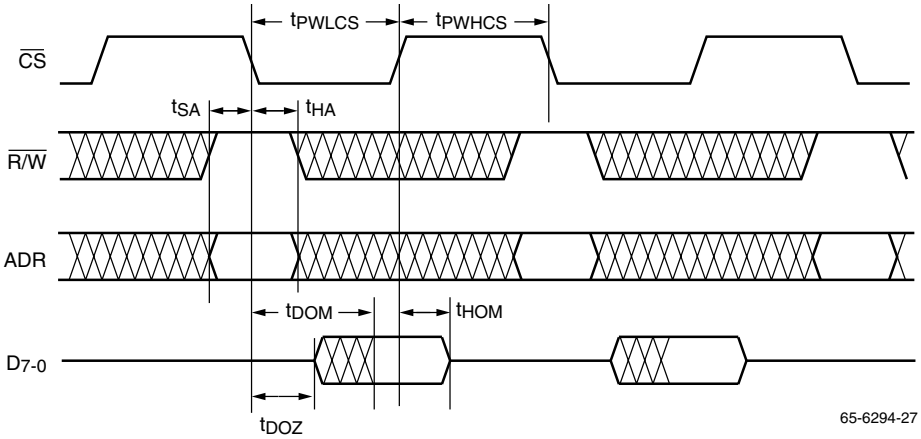


Figure 24. Microprocessor Parallel Port – Read Timing

Serial Control Port (R-Bus)

In addition to the 12-wire parallel port, a 2-wire serial control interface is provided, active when $\overline{SER}$ is LOW. Either port alone can control the entire chip. Up to four TMC2192 devices may be connected to the 2-wire serial interface with each device having a unique address.

The 2-wire interface comprises a clock (SCL) and a bi-directional data (SDA) pin. The encoder acts as a slave for receiving and transmitting data over the serial interface. When the serial interface is not active, the logic levels on SCL and SDA need to be pulled HIGH by external pull-up resistors.

Data received or transmitted on the SDA line must be stable for the duration of the positive-going SCL pulse. Data on SDA must change only when SCL is LOW. If SDA changes state while SCL is HIGH, the serial interface interprets that action as a start or stop sequence.

There are six components to serial bus operation:

- Start signal
- Slave address byte
- Block Pointer
- Offset Pointer
- Data byte to read or write
- Stop signal

When the serial interface is inactive (SCL and SDA are HIGH) communications are initiated by sending a start signal. The start signal is a HIGH-to-LOW transition on SDA while SCL is HIGH. This signal alerts all slaved devices that a data transfer sequence is coming.

The first eight bits of data transferred after a start signal comprise a seven bit slave address and a single R/W bit. The R/W bit indicates the direction of data transfer, read from or write to the slave device. If the transmitted slave address matches the address of the device (set by the state of the SA1-0 input pins in Table 24), the TMC2192 acknowledges by bringing SDA LOW on the 9th SCL pulse. If the addresses do not match, the TMC2192 will not acknowledge.

Table 21. Serial Port Addresses

A6	A5	A4	A3	A2	A1 (SA1)	A0 (SA0)
1	0	1	0	1	0	0
1	0	1	0	1	0	1
1	0	1	0	1	1	0
1	0	1	0	1	1	1

Data Transfer via Serial Interface

For each byte of data read or written, the MSB is the first bit of the sequence.

If the TMC2192 does not acknowledge the master device during a write sequence, the SDA remains HIGH so the master can generate a stop signal. If the master device does not acknowledge the TMC2192 during a read sequence, the encoder interprets this as “end of data”.

Writing data to specific control registers of the TMC2192 requires that the 8 bit address of the control register of interest be written after the slave address has been established. This control register address is the base address for subsequent write operations. The base address auto increments by one for each byte of data written after the data byte intended for the base address.

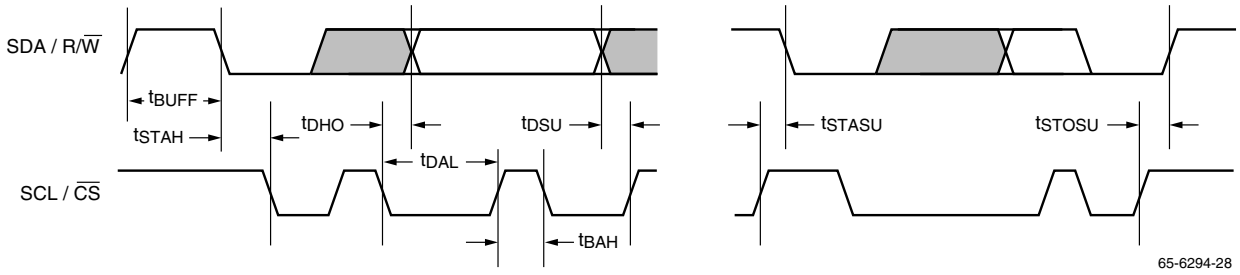


Figure 25. Serial Port Read/Write Timing

Data are read from the control registers of the TMC2192 in a similar manner. Reading requires two data transfer operations:

The base address must be written with the R/W bit of the slave address byte LOW to set up a sequential read operation.

Reading (the R/W bit of the slave address byte HIGH) begins at the previously established base address. The address of the read register auto increments after each byte is transferred.

To terminate a write sequence to the TMC2192, a stop signal must be sent. A stop signal comprises a LOW-to-HIGH transition of SDA while SCL is HIGH. To terminate a read

sequence simply do not acknowledge (NOACK) the last byte received and the TMC2192 will terminate the sequence.

A repeated start signal occurs when the master device driving the serial interface generates a start signal without first generating a stop signal to terminate the current communication. This is used to change the mode of communication (read, write) between the slave and master without releasing the serial interface lines.

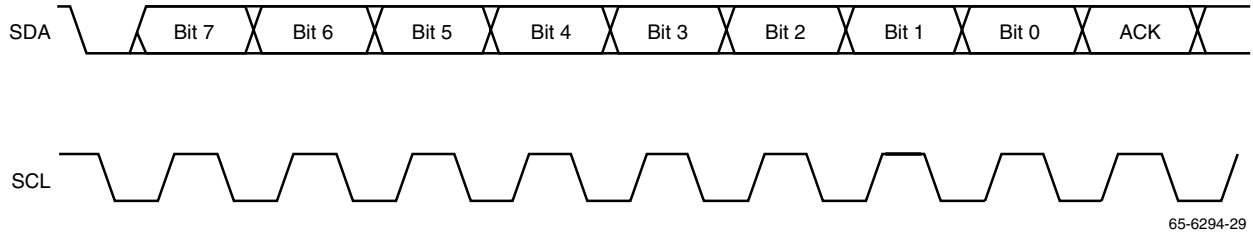


Figure 26. Serial Interface – Typical Byte Transfer

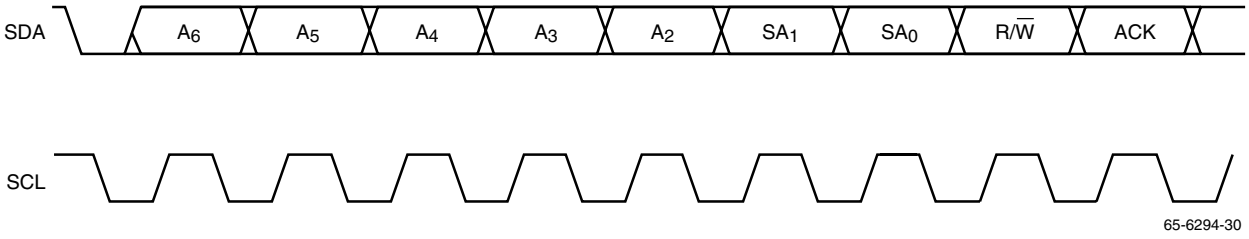


Figure 27. Serial Interface – Chip Address

Serial Interface Read/Write Examples

Write to one control register
- Start signal
- Slave Address byte (R/W bit = LOW)
- Block Pointer (00)
- Offset Pointer
- Data byte to base address
- Stop signal

Write to four consecutive control registers
- Start signal
- Slave Address byte (R/W bit = LOW)
- Block Pointer (00)
- Offset Pointer
- Data byte to base address
- Data byte to (base address + 1)
- Data byte to (base address + 2)
- Data byte to (base address + 3)
- Stop signal

Write to one OLUT location
- Start signal
- Slave Address byte (R/W bit = LOW)
- Block Pointer (01)
- Offset Pointer (base address)
- Data byte to base address (Y)
- Data byte to base address (Cb)
- Data byte to base address (Cr)
- Stop signal

Write to four consecutive OLUT locations
- Start signal
- Slave Address byte (R/W bit = LOW)
- Block Pointer (01)
- Offset Pointer (base address)
- Data byte to base address (Y)
- Data byte to base address (Cb)
- Data byte to base address (Cr)
- Data byte to base address +1 (Y)
- Data byte to base address +1 (Cb)
- Data byte to base address +1 (Cr)
- Data byte to base address +2 (Y)
- Data byte to base address +2 (Cb)
- Data byte to base address +2 (Cr)
- Data byte to base address +3 (Y)
- Data byte to base address +3 (Cb)
- Data byte to base address +3 (Cr)
- Stop signal

Read from one control register
- Start signal
- Slave Address byte (R/W bit = LOW)
- Block Pointer (00)
- Offset Pointer
- Stop signal
- Start signal
- Slave Address byte (R/W bit = HIGH)
- Data byte from base address
- NOACK

Read from four consecutive control registers
- Start signal
- Slave Address byte (R/W bit = LOW)
- Block Pointer (00)
- Offset Pointer
- Stop signal
- Start signal
- Slave Address byte (R/W bit = HIGH)
- Data byte from base address
- Data byte from (base address + 1)
- Data byte from (base address + 2)
- Data byte from (base address + 3)
- NOACK

Control Register Map

Table 22. Control Register Map

Reg	Bit	Mnemonic	Function
TMC2192 Identification Registers (Read only)			
00	7-0	PARTID2	Reads back 97h
01	7-0	PARTID1	Reads back 21h
02	7-0	PARTID0	Reads back 92h
03	7-0	REVID	Silicon revision #
Gamma Filters Register			
04	7-4	Reserved	Set to Low
04	3	$\overline{\text{SRESET}}$	Software RESET
04	2	SKEN	Data KEY Enable
04	1-0	PDRM	Pixel Data Ramping Mode
Input Format Register			
05	7	D1OFF	YCBCR Input Formatting
05	6	Reserved	Program Low
05	5-4	INMODE	Input Mode Select
05	3-2	OMIX	Overlay Mixer Select
05	1-0	SOURCE	Video Input Select
General Control Register			
06	7-6	FORMAT	Video Format
06	5-3	MODE	Video Mode
06	2	PDCDIR	PDC Directional Control
06	1	TOUT	External Sync Output Control
06	0	TSOUT	External Sync Delay Control
Horizontal Ancillary Data Control Register			
07	7	LDFID	Field Lock Select
07	6	SKFLIP	Soft Key Inversion
07	5	DDSRST	DDS Reset
07	4-3	Reserved	
07	2	ANCFREN	Ancillary Frequency Enable
07	1	ANCPHEN	Ancillary Phase Enable
07	0	ANCTREN	Ancillary Timing Enable
Ancillary Data ID Register			
08	7-0	ANCID	Ancillary Data Identification
Keying/Overlay Engine			
09	7	HKEN	Hardware KEY Enable
09	6	BUKEN	Burst KEY Enable
09	5	SKEXT	Data KEY Operation Select
09	4	DKDIS	Green/Y Data KEY Disable
09	3	EKDIS	Blue/C_B Data KEY Disable
09	2	FKDIS	Red/C_R Data KEY Disable
09	1-0	LAYMODE	Layer Assignment Select
Key Value Registers			
0A	7-0	DKEYMAX	Green/Y Maximum Data Key Value
0B	7-0	DKEYMIN	Green/Y Minimum Data Key Value
0C	7-0	EKEYMAX	Blue/C_B Maximum Data Key Value
0D	7-0	EKEYMIN	Blue/C_B Minimum Data Key Value
0E	7-0	FKEYMAX	Red/C_R Maximum Data Key Value
0F	7-0	FKEYMIN	Red/C_R Minimum Data Key Value
DAC Control Registers			
10	7	COMPDIS	D/A #4 Disable
10	6	CHROMADIS	D/A #3 Disable
10	5	LUMADIS	D/A #2 Disable
10	4-3	Reserved	Set to 0.
10	2	OLUTDIS	Overlay LUT Disable
10	1-0	Reserved	Program Low
11	7	DRSSEL	DRS Selection
11	6	Reserved	Program Low
11	5	COMP2DB	Composite 2 Overflow Control
11	4	SINEN	X/Sin(x) Filter Enable
11	3	Reserved	Program Low
11	2	LUMDIS	Luma Disable
11	1	CHRMDIS	Chroma Disable
11	0	BURSTDIS	Burst Disable

Table 22. Control Register Map (continued)

Reg	Bit	Mnemonic	Function
VBI Ped Enable Registers			
14	7-0	VBIPEDEM	VBI Pedestal Enable, Even Fields
15	7-0	VBIPEDEL	VBI Pedestal Enable, Even Fields
16	7-0	VBIPEDOM	VBI Pedestal Enable, Odd Fields
17	7-1	VBIPEDOL	VBI Pedestal Enable, Odd Fields
17	0	HVA	Horizontal and Vertical Sync Alignment
Vertical Blanking Interval Enable Registers			
18	7	Reserved	Program Low
18	6	GLKCTL1	Genlock Control Register 1
18	5	GLKCTL0	Genlock Control Register 0
18	4-0	VBIENF1	VBI Active Video Enable, Field 1
19	7	SHORT	Test Register
19	6	T512	EH/SL Offset Control Bit
19	5	$\overline{\text{HALFEN}}$	Half Line Enable
19	4-0	VBIENF2	VBI Active Video Enable, Field 2
Pedestal Height Register			
1A	7	Reserved	Program Low
1A	6-0	PEDHGT1	Composite Pedestal Height
Closed Caption Registers			
1C	7-0	CCD1	First Byte of CC Data
1D	7-0	CCD2	Second Byte of CC Data
1E	7	CCON	Enable CC Data Packet
1E	6	CCRTS	Request to Send Data
1E	5	CCPAR	Auto Parity Generation
1E	4	CCFLD	CC Field Select
1E	3-0	CCLINE	CC Line Select
Timing Registers			
1F	7-0	PDCNT	Pixel Data Control Start
20	7-0	SY	Horizontal Sync Tip Duration
21	7-0	BR	Breezeway Duration
22	7-0	BU	Burst Duration
23	7-0	CBP	Color Back Porch Duration
24	7-0	XBP	Extended Color Back Porch Duration
25	7-0	VA	Active Video Region Duration
26	7-0	VC	Active Video Region 2nd Half Line Duration
27	7-0	VB	Active Video Region 1st Half Line Duration
28	7-0	EL	Equalization Pulse Low Duration
29	7-0	EH	Equalization Pulse High Duration
2A	7-0	SL	Vertical Sync Pulse Low Duration
2B	7-0	SH	Vertical Sync Pulse High Duration
2C	7-0	FP	Front Proch Duration
2D	7-6	XBP	Extended Color Back Porch Duration
2D	5-4	VA	Active Video Duration
2D	3-2	VB	Active Video Region 1st Half Line Duration
2D	1-0	VC	Active Video Region 2nd Half Line Duration
2E	7-5	FIELD	Field Identification (read only)
2E	4-0	LTYPE	Line Type Identification (read only)
2F	7-0	CBL	Color Bar Duration
Color Space Matrix Registers			
30	7-0	MCF1L	Matrix Coefficient #1
31	7-0	Reserved	Program Low
32	7-0	Reserved	Program Low
33	7-0	MCF2L	Matrix Coefficient #2
34	7-0	Reserved	Program Low
35	7-0	MCF3L	Matrix Coefficient #3
36	7-0	Reserved	Program Low
37	7-0	Reserved	Program Low

Table 22. Control Register Map (continued)

Reg	Bit	Mnemonic	Function
38	7-0	Reserved	Program Low
39	7-0	Reserved	Program Low
3A	7-4	MCF1M	Matrix Coefficient #1
3A	3-0	Reserved	Program Low
3B	7-3	Reserved	Set to 0.
3B	2-0	MCF4M	Matrix Coefficient #4
3C	7-3	Reserved	Set to 0.
3C	2-0	MCF6M	Matrix Coefficient #6
3D	7-4	Reserved	Program Low
3D	3-0	Reserved	Program Low
3E	7-4	Reserved	Program Low
3E	3-0	Reserved	Program Low
3F	7	SEL_CLK	DCVBS Clock Select
3F	6	Reserved	Program Low
3F	5	GAUSS_BVP	Gaussian Bypass Select
3F	4	SEL_PIX	DCVBS Output Selection
3F	3	C2DB_OFF	COMP2DB Offset Selection
3F	2-0	Reserved	Program Low

Reg	Bit	Mnemonic	Function
Subcarrier Registers			
40	7-0	FREQL	Subcarrier Frequency
41	7-0	FREQ3	Subcarrier Frequency
42	7-0	FREQ2	Subcarrier Frequency
43	7-0	FREQM	Subcarrier Frequency
44	7-0	SYSPHL	System Phase
45	7-0	SYSPHM	System Phase
46	7-0	BURPHL	Burst Phase
47	7-0	BURPHM	Burst Phase
48	7-0	BRSTFULL	Burst Height – Maximum Amplitude
49	7-0	BRST1	Burst Height – 1st Intermediate Value
4A	7-0	BRST2	Burst Height – 2nd Intermediate Value

Note:

1. For each register listed above, all bits not specified are reserved and should be set to logic LOW to ensure proper operation.

Control Register Definitions

Part Identification Register (0x00)

7	6	5	4	3	2	1	0
PARTID2							

Reg	Bit	Name	Description
00	7-0	PARTID2	**(Read Only)** 0x97

Part Identification Register (0x01)

7	6	5	4	3	2	1	0
PARTID1							

Reg	Bit	Name	Description
01	7-0	PARTID1	**(Read Only)** 0x21

Control Register Definitions (continued)

Part Identification Register (0x02)

7	6	5	4	3	2	1	0
PARTID0							

Reg	Bit	Name	Description
02	7-0	PARTID0	**(Read Only)** 0x92

Revision Identification Register (0x03)

7	6	5	4	3	2	1	0
REVID0							

Reg	Bit	Name	Description
03	7-0	REVID0	Reads back the revision number of the part.

Gamma Filters Register (0x04)

7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	RESERVED	$\overline{\text{SRESET}}$	SKEN	PDRM	

Reg	Bit	Name	Description
04	7-4	RESERVED	Set to Low
04	3	$\overline{\text{SRESET}}$	**Software RESET.** When LOW, resets internal state machines and disables outputs. When HIGH, state machines are active and outputs are enabled.
04	2	SKEN	**Data KEY Enable.** When SKEN is LOW, Data keying is disabled. When SKEN is HIGH, Data keying is enabled.
04	1-0	PDRM	**Pixel Data Ramping Mode.** Pixel Data weighting for the rising edge of active video. NTSC: 0 0 1/8 1/2 7/8 1 1 PAL: 0 1/8 3/8 5/8 7/8 1 1 00 Pixels are weighted on the edge. 01 Sample and hold the 5th pixel for the slope weighting 1X Hard switch 0 0 0 1 1 1

Control Register Definitions (continued)

Input Format Register (0x05)

7	6	5	4	3	2	1	0
D10FF	INMODE			OMIX		SOURCE	

Reg	Bit	Name	Description
05	7	D1OFF	**YCBCR Input Formatting.** When D1OFF is HIGH, 64 is subtracted from Y data path of the PD port. When D1OFF is LOW, pixel data is passed through.
05	6	Reserved	Program Low
05	5-4	INMODE	**Input Mode Select.** 00 24 bit YC_BC_R (4:4:4) PD[7:0] = Y PD[23:16] = C_B PD[15:8] = C_R 01 10 bit D1 (YC_BC_R) PD[23:14] = YC_BC_R at 27MHz 10 20 bit YC_BC_R (4:4:4) PD[9:0] = Y PD[23:14] = C_BC_R (at 27MHz) 11 20 bit YC_BC_R (4:2:2) PD[9:0] = Y PD[23:14] = C_BC_R
05	3-2	OMIX	**Overlay Mixer Select.** 00 No mix – PD data is always passed 01 Hard mix – mixer performs a hard switch between PD and Overlay 10 Set1 mix – the pixel data has the following weighting on the transition; 0, 1/2, 1 11 Set2 mix – the pixel data has the following weighting on the transition; 0, 1/8, 1/2, 7/8, 1
05	1-0	SOURCE	**Video Input Select.** Chooses from internal test patterns or pixel data port. 00 PD PORT 01 Modulated Ramp 10 INTERNAL COLOR BAR (75%) 11 INTERNAL COLOR BAR (100%)

Control Register Definitions (continued)

General Control Register (0x06)

7	6	5	4	3	2	1	0
FORMAT		MODE			PDCDIR	TOUT	TSOUT

Reg	Bit	Name	Description
06	7-6	FORMAT	**Video Format.** 00 NTSC 01 PAL – B,G,H,I,N 10 PAL – M 11 Reserved
06	5-3	MODE	**Video Mode.** 000 MASTER with free-running subcarrier 001 SLAVE with free-running subcarrier 010 CCIR656 with free-running subcarrier 011 GENLOCK with subcarrier phase and frequency locked to the GRS information. 100 MASTER with subcarrier phase reset every 8 fields 101 SLAVE with subcarrier phase reset every 8 fields 110 CCIR656 with subcarrier phase reset every 8 fields. 111 DRS-Lock with subcarrier phase and frequency locked to the DRS information.
06	2	PDCDIR	**PDC Directional Control.** When PDC is LOW, the PDC pin is an output. When PDCDIR is HIGH, the PDC pin is an input that can override the internally generated PDC and blank the active video of a line.
06	1	TOUT	**External Sync Output Control.** When TOUT = LOW, a MPEG style field toggle is the output on pin $\overline{\text{VSOUT}}$. When TOUT = HIGH, a traditional vertical sync is the output on pin $\overline{\text{VSOUT}}$.
06	0	TSOUT	**External Sync Delay Control.** When the TSOUT is LOW, $\overline{\text{HSOUT}}$, $\overline{\text{VSOUT}}$ are delayed to match propagation delay through the chip. When TSOUT is HIGH, $\overline{\text{HSOUT}}$, $\overline{\text{VSOUT}}$ are aligned with the incoming data on the PD port.

Control Register Definitions (continued)

Horizontal Ancillary Data Control Register (0x07)

7	6	5	4	3	2	1	0
LDFID	SKFLIP	DDSRST	RESERVED		ANCFREN	ANCPHEN	ANCTREN

Reg	Bit	Name	Description
07	7	LDFID	**Field Lock Select.** When LDFID is HIGH, the FLD[2:0] pins are used as inputs to lock the field the that the TMC2192 is encoding. 5 PXCK's after the falling edge of HSIN the FLD[2:0] pins are sampled. When LDFID is LOW, the FLD[2:0] pins output the current field that is being encoded.
07	6	SKFLIP	**Soft Key Inversion.** When SKFLP is LOW, the key generated by the data keying is a normal state. When SKFLP is HIGH, the key generated by the data keying is a inverted state.
07	5	DDSRST	**DDS Reset.** By inserting a logic HIGH into this register the DDS accumulator is reset to SYSPH value at the start of the next field 1 and DDSRST is reset LOW. This enables the DDS to be reset when the encoder is operating with a free running subcarrier.
07	4-3	RESERVED	
07	2	ANCFREN	**Ancillary Frequency Enable.** When HIGH, the encoder gets subcarrier frequency data (FREQ3-0) from incoming ancillary data (in accordance with FRV bit). When LOW, FREQ3-0 registers contain the subcarrier frequency data.
07	1	ANCPHEN	**Ancillary Phase Enable.** When HIGH, the encoder gets subcarrier phase offset data (SCHPHL and SCHPHM) from incoming ancillary data (in accordance with PHV bit). When LOW, a default value of 0000h is used for subcarrier phase.
07	0	ANCTREN	**Ancillary Timing Enable.** When HIGH, the encoder decodes incoming ancillary data to determine video timing (FIELD and SVF). When LOW, the ancillary timing reference data is ignored.

Ancillary Data ID Register (0x08)

7	6	5	4	3	2	1	0
ANCID							

Reg	Bit	Name	Description
08	7-0	ANCID	**Ancillary Data Identification.** Bits 7-0 determine the ancillary data identification. Bit 0 is an odd parity bit. The value in this register must match that of the incoming ancillary data.

Control Register Definitions (continued)

Keying/Overlay Engine Register (0x09)

7	6	5	4	3	2	1	0
HKEN	BUKEN	SKEXT	DKDIS	EKDIS	FKDIS	LAYMODE	

Reg	Bit	Name	Description
09	7	HKEN	**Hardware KEY Enable.** When LOW, the KEY pin is ignored. When HIGH, the KEY pin is enabled.
09	6	BUKEN	**Burst KEY Enable.** When LOW, the output video burst is generated internally. When HIGH, the output video burst is taken from the CVBS port.
09	5	SKEXT	**Data KEY Operation Select.** When LOW, data keying is allowed only during active video window. When HIGH, data keying is allowed during frame.
09	4	DKDIS	**Y Data KEY Disable.** When LOW, Y input data is enabled for data keying. When HIGH, Y input data is ignored for data keying.
09	3	EKDIS	**C_B Data KEY Disable.** When LOW, C_B input data is enabled for data keying. When HIGH, C_B input data is ignored for data keying.
09	2	FKDIS	**C_R Data KEY Disable.** When LOW, C_R input data is enabled for data keying. When HIGH, C_R input data is ignored for data keying.
09	1-0	LAYMODE	**Layer Assignment Select.**

Mode	BACKGND Source	MIDGND Source	Key	FOREGND Source	Key
0	PD	OVERLAY	0L4-0	CVBS	KEY
1	PD	CVBS	KEY	OVERLAY	OL4-0
2	CVBS	OVERLAY	OL4-0	PD	KEY
3	CVBS	PD	KEY	OVERLAY	OL4-0

Control Register Definitions (continued)

Key Value Register (0x0A)

7	6	5	4	3	2	1	0
DKEYMAX							

Reg	Bit	Name	Description
0A	7-0	DKEYMAX	**Y Maximum Data Key Value.** DKEYMAX is compared against the 8 MSB's of Y channel. If DKEYMAX is greater or equal to Y and DKEYMIN less than Y then a match is signaled.

Key Value Register (0x0B)

7	6	5	4	3	2	1	0
DKEYMIN							

Reg	Bit	Name	Description
0B	7-0	DKEYMIN	**Y Minimum Data Key Value.** DKEYMIN is compared against the 8 MSB's of Y channel. If DKEYMAX is greater or equal to Y and DKEYMIN less than Y then a match is signaled.

Key Value Register (0x0C)

7	6	5	4	3	2	1	0
EKEYMAX							

Reg	Bit	Name	Description
0C	7-0	EKEYMAX	**C_B Maximum Data Key Value.** EKEYMAX is compared against the 8 MSB's of C_B channel. If EKEYMAX is greater or equal to C_B and EKEYMIN less than C_B then a match is signaled.

Key Value Register (0x0D)

7	6	5	4	3	2	1	0
EKEYMIN							

Reg	Bit	Name	Description
0D	7-0	DKEYMIN	**C_B Minimum Data Key Value.** EKEYMIN is compared against the 8 MSB's of C_B channel. If EKEYMAX is greater or equal to C_B and EKEYMIN less than C_B then a match is signaled

Control Register Definitions (continued)

Key Value Register (0x0E)

7	6	5	4	3	2	1	0
FKEYMAX							

Reg	Bit	Name	Description
0E	7-0	FKEYMAX	**C_R Maximum Data Key Value.** FKEYMAX is compared against the 8 MSB's of C_R channel. If FKEYMAX is greater or equal to C_R and FKEYMIN less than C_R then a match is signaled.

Key Value Register (0x0F)

7	6	5	4	3	2	1	0
FKEYMIN							

Reg	Bit	Name	Description
0F	7-0	FKEYMIN	**C_R Minimum Data Key Value.** FKEYMIN is compared against the 8 MSB's of C_R channel. If FKEYMAX is greater or equal to C_R and FKEYMIN less than C_R then a match is signaled.

Control Register Definitions (continued)

DAC Control Register (0x10)

7	6	5	4	3	2	1	0
COMPDIS	CHROMADIS	LUMADIS	RESERVED	RESERVED	OLUTDIS	RESERVED	

Reg	Bit	Name	Description
10	7	COMPDIS	**Composite D/A Disable.** When COMPDIS is LOW, the COMPOSITE D/A is enabled. When COMPDIS is HIGH, the COMPOSITE D/A is disabled.
10	6	CHROMADIS	**Chroma D/A Disable.** When CHROMADIS is LOW, the CHROMA D/A is enabled. When CHROMADIS is HIGH, the CHROMA D/A is disabled.
10	5	LUMADIS	**LUMA D/A Disable.** When LUMADIS is LOW, the LUMA D/A is enabled. When LUMADIS is HIGH, the LUMA D/A is disabled.
10	4-3	RESERVED	Set to 0.
10	2	OLUTDIS	**Overlay LUT Disable.** When OLUTDIS is LOW, the olut is enabled. When OLUTDIS is HIGH, the olut is disabled.
10	1-0	RESERVED	Program Low

Control Register Definitions (continued)

DAC Control Register (0x11)

7	6	5	4	3	2	1	0
DRSSEL	RESERVED	COMP2DB	SINEN	REFSEL	LUMDIS	CHRMDIS	BURSTDIS

Reg	Bit	Name	Description
11	7	DRSSEL	**DRS Selection.** When DRSSEL is HIGH, PD[7:0] is routed to the DRS detection block. When DRSSEL is LOW, CVBS[9:2] is routed to the DRS detection block.
11	6	RESERVED	Program Low
11	5	COMP2DB.	**Composite 2 Overflow Control.** When COMP2DB is HIGH, the digital range of the composite sumer is 0 to 2047 with half the digital resolution. When COMP2DB is LOW, the digital output of the composite summer is 0 to 1023, all values exceeding 1023 or below 0 are clipped.
11	4	SINEN	**X/Sine(X) Filter Enable.** When SINEN is LOW, the X/Sin(X) filter is bypassed. When SINEN is HIGH, the X/Sin(X) filter is used to compensate for the DAC roll-off at high frequencies.
11	3	RESERVED	Program Low
11	2	LUMDIS	**Luma Disable.** When LUMDIS is LOW, the luminance data on the composite data path is enabled. When LUMDIS is HIGH, the luminance data on the composite data path is disabled.
11	1	CHRMDIS	**Chroma Disable.** When CHRMDIS is LOW, the chrominance data on the composite data path is enabled. When CHRMDIS is HIGH, the chrominance data on the composite data path is disabled.
11	0	BURSTDIS	**Burst Disable.** When BURSTDIS is LOW, the burst is enabled. When BURSTDIS is HIGH, the burst is disabled.

Control Register Definitions (continued)

VBI Ped Enable Register (0x14)

7	6	5	4	3	2	1	0
VBIPEDEM							

Reg	Bit	Name	Description
14	7-0	VBIPEDEM	**VBI Pedestal Enable, Even Fields.** VBIPEDEM is the bits 15-8 of VBIPEDE[15:0]. VBIPEDE controls the addition of pedestal on a line by line basis from line 10 in NTSC (VBIPEDE[0] = HIGH) to line 24 (VBIPEDE[14] = HIGH) in the EVEN field of NTSC. VBIPEDE[15] controls the pedestal from line 25 to line 263 inclusive.

VBI Ped Enable Register (0x15)

7	6	5	4	3	2	1	0
VBIPEDEL							

Reg	Bit	Name	Description
15	7-0	VBIPEDEL	**VBI Pedestal Enable, Even Fields.** VBIPEDEL is the bits 7-0 of VBIPEDE[15:0]. VBIPEDE controls the addition of pedestal on a line by line basis from line 10 in NTSC (VBIPEDE[0] = HIGH) to line 24 (VBIPEDE[14] = HIGH) in the EVEN field of NTSC. VBIPEDE[15] controls the pedestal from line 25 to line 263 inclusive.

VBI Ped Enable Register (0x16)

7	6	5	4	3	2	1	0
VBIPEDOM							

Reg	Bit	Name	Description
16	7-0	VBIPEDOM	**VBI Pedestal Enable, Odd Fields.** VBIPEDOM is the bits 14-7 of VBIPEDO[14:0]. VBIPEDO controls the addition of pedestal on a line by line basis from line 273 (VBIPEDE[0] = HIGH) to line 286 (VBIPEDE[13] = HIGH) in the ODD field of NTSC. VBIPEDO[14] controls the pedestal from line 287 to line 525 inclusive.

Control Register Definitions (continued)

VBI Ped Enable Register (0x17)

7	6	5	4	3	2	1	0
VBIPEDOL							HVA

Reg	Bit	Name	Description
17	7-1	VBIPEDOM	**VBI Pedestal Enable, Odd Fields.** VBIPEDOL is the bits 6-0 of VBIPEDO[14:0]. VBIPEDO controls the addition of pedestal on a line by line basis from line 273 (VBIPEDE[0] = HIGH) to line 286 (VBIPEDE[13] = HIGH) in the ODD field of NTSC. VBIPEDO[14] controls the pedestal from line 287 to line 525 inclusive.
17	0	HVA	**Horizontal and Vertical Sync Alignment.** When HVA is LOW, the falling edge of $\overline{\text{HSIN}}$ and $\overline{\text{VSIN}}$ must occur just prior to the rising edge of PXCK to start an field 1. When HVA is HIGH, $\overline{\text{VSIN}}$ is allowed to vary from $\overline{\text{HSIN}}$ by ±32 pixels.

Vertical Blanking Interval Enable Register (0x18)

7	6	5	4	3	2	1	0
Reserved	GLKCTL1	GLKCTL0	VBIENF1				

Reg	Bit	Name	Description
18	7	Reserved	
18	6	GLKCTL1	**Genlock Control Register 1.** When GLKCTL1 is LOW, the PALODD bit of the GRS stream is ignored. When GLKCTL1 is HIGH, the PALODD bit of the GRS stream controls the PALODD flip of the subcarrier.
18	5	GLKCTL0	**Genlock Control Register 0.** When GLKCTL0 is LOW, the Color Frame bit of the GRS stream is ignored. When GLKCTL0 is HIGH, the Color Frame bit of the GRS stream controls the field sequence in the FVHGEN.
18	4-0	VBIENF	**VBI Active Video Enable, Field 1.** The value of VBIENF1 determines which line blanking stops and active line for EVEN fields in NTSC starting from line 4 to line 35 or an ODD fields for PAL starting from line 1 to line 32.

Control Register Definitions (continued)

Vertical Blanking Interval Enable Register (0x19)

7	6	5	4	3	2	1	0
SHORT	T512	$\overline{\text{HALFEN}}$	VBIENF2				

Reg	Bit	Name	Description
19	7	SHORT	**Test Register.** Program LOW.
19	6	T512	**EH/SL Offset Control Bit.** When LOW, the true value of EH and SL is offset by 256. When HIGH, the true value of EH and SL is offset by 512.
19	5	$\overline{\text{HALFEN}}$	**Half Line Enable.** When LOW, half-line blanking occurs on line 283 (NTSC) or line 23 (PAL). When HIGH, line 283 (NTSC) or line 23 (PAL) is treated as a full line of active video.
19	4-0	VBIENF2	**VBI Active Video Enable, Field 2.** The value of VBIENF2 determines which line blanking stops and active line for ODD fields in NTSC starting from line 4 to line 35 or an EVEN fields for PAL starting from line 1 to line 32.

Pedestal Height Register (0x1A)

7	6	5	4	3	2	1	0
Reserved	PEDHGT1						

Reg	Bit	Name	Description
1A	7	Reserved	
1A	6-0	PEDHGT1	**Composite Pedestal Height.** PEDHGT1 is a 2's comp value producing a pedestal height from -22.1 IRE to 21.7 IRE with .345 IRE steps on the composite data path. The default 7.5 IRE pedestal for NTSC-M results from a hex code of 0010110b.

Closed Caption Register (0x1C)

7	6	5	4	3	2	1	0
CCD1							

Reg	Bit	Name	Description
1C	7-0	CCD1	**First Byte of CC Data.** Bit 0 is the LSB. The MSB will be overwritten by an ODD Parity Bit if CCPAR is HIGH.

Control Register Definitions (continued)

Closed Caption Register (0x1D)

7	6	5	4	3	2	1	0
CCD2							

Reg	Bit	Name	Description
1D	7-0	CCD2	**Second Byte of CC Data.** Bit 0 is the LSB. The MSB will be overwritten by an ODD Parity Bit if CCPAR is HIGH

Closed Caption Register (0x1E)

7	6	5	4	3	2	1	0
CCON	CCRTS	CCPAR	CCFLD	CCLINE			

Reg	Bit	Name	Description
1E	7	CCON	**Enable CC Data Packet.** Command the CC data generator to send either CC data or a NULL byte whenever the specified line is transmitted.
1E	6	CCRTS	**Request To Send Data.** This bit is set HIGH by the user when bytes 0x1C and 0x1D have been loaded with the next two bytes to be sent. When the encoder's line count reaches preceding the line specified in bits 4-0 of this register the data will be transferred from registers 0x1C and 0x1D, and RTS will be RESET LOW. A new pair of bytes may then be loaded into registers 0x1C and 0x1D. If CCON = 1 and CCRTS = 0 when the CC line is to be sent, NULL bytes will be sent.
1E	5	CCPAR	**Auto Parity Generation.** When set HIGH, the encoder replaces the MSB of bytes 0x1C and 0x1D with a calculated ODD parity. When set LOW, the CC processor transmits the 16 bits exactly as loaded into registers 0x1C and 0x1D.
1E	4	CCFLD	**CC Field Select.** When LOW, CC data is transmitted on the selected line of ODD fields. When HIGH, it is sent on EVEN fields.
1E	3-0	CCLINE	**CC Line Select.** Defines (with an offset) the line on which CC data are transmitted.

Timing Register (0x1F)

7	6	5	4	3	2	1	0
PDCNT							

Reg	Bit	Name	Description
1F	7-0	PDCNT	**Pixel Data Control Start.** PDCNT determines the number of pixels (PCK's) from the midpoint of the falling edge of horizontal sync to the rising edge of PDC on active video lines.

Control Register Definitions (continued)

Timing Register (0x20)

7	6	5	4	3	2	1	0
SY							

Reg	Bit	Name	Description
20	7-0	SY	**Horizontal Sync Tip Duration.** This 8 bit register holds a value extending from 0 to 255 PCK cycles.

Timing Register (0x21)

7	6	5	4	3	2	1	0
BR							

Reg	Bit	Name	Description
21	7-0	BR	**Breezeway Duration.** This 8 bit register holds a value extending from 0 to 255 PCK cycles.

Timing Register (0x22)

7	6	5	4	3	2	1	0
BU							

Reg	Bit	Name	Description
22	7-0	BU	**Burst Duration.** This 8 bit register holds a value extending from 0 to 255 PCK cycles.

Timing Register (0x23)

7	6	5	4	3	2	1	0
CBP							

Reg	Bit	Name	Description
23	7-0	CBP	**Color Back Porch Duration.** This 8 bit register holds a value extending from 0 to 255 PCK cycles.

Timing Register (0x24)

7	6	5	4	3	2	1	0
XBP							

Reg	Bit	Name	Description
24	7-0	CBP	**Extended Color Back Porch Duration.** This 8 bit register holds the LSB's of a 10 bit value extending from 0 to 1023 PCK cycles.

Control Register Definitions (continued)

Timing Register (0x25)

7	6	5	4	3	2	1	0
VA							

Reg	Bit	Name	Description
25	7-0	VA	**Active Video Region Duration.** This 8 bit register holds the LSB's of a 10 bit value extending from 0 to 1023 PCK cycles.

Timing Register (0x26)

7	6	5	4	3	2	1	0
VC							

Reg	Bit	Name	Description
26	7-0	VC	**Active Video Region 2nd Half Line Duration.** This 8 bit register holds the LSB's of a 10 bit value extending from 0 to 1023 PCK cycles.

Timing Register (0x27)

7	6	5	4	3	2	1	0
VB							

Reg	Bit	Name	Description
27	7-0	VB	**Active Video Region 1st Half Line Duration.** This 8 bit register holds the LSB's of a 10 bit value extending from 0 to 1023 PCK cycles.

Timing Register (0x28)

7	6	5	4	3	2	1	0
VB							

Reg	Bit	Name	Description
28	7-0	EL	**Equalization Pulse Low Duration.** This 8 bit register holds a value extending from 0 to 255 PCK cycles.

Control Register Definitions (continued)

Timing Register (0x29)

7	6	5	4	3	2	1	0
EH							

Reg	Bit	Name	Description
29	7-0	EH	**Equalization Pulse High Duration.** This 8 bit register holds 8 LSB's of EH, The addition of 256 or 512 is controlled by T512. The range is either 256 to 511 PCK cycles or 512 to 767 PCK cycles.

Timing Register (0x2A)

7	6	5	4	3	2	1	0
SL							

Reg	Bit	Name	Description
2A	7-0	SL	**Vertical Sync Pulse Low Duration.** This 8 bit register holds 8 LSB's of SL, The addition of 256 or 512 is controlled by T512. The range is either 256 to 511 PCK cycles or 512 to 767 PCK cycles.

Timing Register (0x2B)

7	6	5	4	3	2	1	0
SH							

Reg	Bit	Name	Description
2B	7-0	SH	**Vertical Sync Pulse High Duration.** This 8 bit register holds a value extending from 0 to 255 PCK cycles.

Timing Register (0x2C)

7	6	5	4	3	2	1	0
FP							

Reg	Bit	Name	Description
2C	7-0	FP	**Front Porch Duration.** This 8 bit register holds a value extending from 0 to 255 PCK cycles.

Control Register Definitions (continued)

Timing Register (0x2D)

7	6	5	4	3	2	1	0
XBP		VA		VB		VC	

Reg	Bit	Name	Description
2D	7-6	XBP	**Extended Color Back Porch Duration.** 2 MSB's of the 10 bit XBP, extending from 0 to 1023 PCK cycles.
2D	5-4	VA	**Active Video Duration.** 2 MSB's of the 10 bit VA, extending from 0 to 1023 PCK cycles.
2D	3-2	VB	**Active Video Region 1st Half Line Duration.** 2 MSB's of a 10 bit VB, extending from 0 to 1023 PCK cycles.
2D	1-0	VC	**Active Video Region 2nd Half Line Duration.** 2 MSB's of a 10 bit VC, extending from 0 to 1023 PCK cycles.

Timing Register (0x2E)

7	6	5	4	3	2	1	0
FIELD			LTYPE				

Reg	Bit	Name	Description
2E	7-5	FIELD	**Field Identification. (READ ONLY)** These three bits are updated 12 PXCK periods after each vertical sync. They allow the user to determine field type on a continuous basis
2E	4-0	LTYPE	**LineType Identification (READ ONLY)** These three bits are updated 5 PXCK periods after each horizontal sync. They allow the user to determine line type on a continuous basis.

Timing Register (0x2F)

7	6	5	4	3	2	1	0
CBL							

Reg	Bit	Name	Description
2F	7-0	CBL	**Color Bar Duration.** This 8 bit register holds a value extending from 0 to 255 PCK cycles.

Color Space Matrix Register (0x30)

7	6	5	4	3	2	1	0
MCF1L							

Reg	Bit	Name	Description
30	7-0	MCF1L	**Matrix Coefficient #1.** Bits 7-0 of MCF1.

Control Register Definitions (continued)

Color Space Matrix Register (0x31)

7	6	5	4	3	2	1	0
RESERVED							

Reg	Bit	Name	Description
31	7-0	RESERVED	Program Low

Color Space Matrix Register (0x32)

7	6	5	4	3	2	1	0
RESERVED							

Reg	Bit	Name	Description
32	7-0	RESERVED	Program Low

Color Space Matrix Register (0x33)

7	6	5	4	3	2	1	0
MCF2L							

Reg	Bit	Name	Description
33	7-0	MCF2L	**Matrix Coefficient #2.** Bits 7-0 of MCF4.

Color Space Matrix Register (0x34)

7	6	5	4	3	2	1	0
RESERVED							

Reg	Bit	Name	Description
34	7-0	RESERVED	Program Low

Color Space Matrix Register (0x35)

7	6	5	4	3	2	1	0
MCF3L							

Reg	Bit	Name	Description
35	7-0	MCF3L	**Matrix Coefficient #3.** Bits 7-0 of MCF6.

Control Register Definitions (continued)

Color Space Matrix Register (0x36)

7	6	5	4	3	2	1	0
RESERVED							

Reg	Bit	Name	Description
36	7-0	RESERVED	Program Low

Color Space Matrix Register (0x37)

7	6	5	4	3	2	1	0
RESERVED							

Reg	Bit	Name	Description
37	7-0	RESERVED	Program Low

Color Space Matrix Register (0x38)

7	6	5	4	3	2	1	0
RESERVED							

Reg	Bit	Name	Description
38	7-0	RESERVED	Program Low

Color Space Matrix Register (0x39)

7	6	5	4	3	2	1	0
RESERVED							

Reg	Bit	Name	Description
39	7-0	RESERVED	Program Low

Color Space Matrix Register (0x3A)

7	6	5	4	3	2	1	0
MCF1M				MCF2M			

Reg	Bit	Name	Description
3A	7-4	MCF1M	**Matrix Coefficient #1.** Bits 11-8 of MCF1.
3A	3-0	RESERVED	Program Low

Control Register Definitions (continued)

Color Space Matrix Register (0x3B)

7	6	5	4	3	2	1	0
MCF3M				RESERVED	MCF4M		

Reg	Bit	Name	Description
3B	7-3	RESERVED	Set to 0.
3B	2-0	MCF4M	**Matrix Coefficient #4.** Bits 10-8 of MCF4.

Color Space Matrix Register (0x3C)

7	6	5	4	3	2	1	0
MCF5M				RESERVED	MCF6M		

Reg	Bit	Name	Description
3C	7-3	RESERVED	Set to 0.
3C	2-0	MCF6M	**Matrix Coefficient #6.** Bits 10-8 of MCF6.

Color Space Matrix Register (0x3D)

7	6	5	4	3	2	1	0
RESERVED				RESERVED			

Reg	Bit	Name	Description
3D	7-4	RESERVED	Program Low
3D	3-0	RESERVED	Program Low

Color Space Matrix Register (0x3E)

7	6	5	4	3	2	1	0
RESERVED				RESERVED			

Reg	Bit	Name	Description
3E	7-4	RESERVED	Program Low
3E	3-0	RESERVED	Program Low

Control Register Definitions (continued)

Color Space Matrix Register (0x3F)

7	6	5	4	3	2	1	0
SEL_CLK	RESERVED	GAUSS_BYP	SEL_PIX	C2DB_OFF	NMEH	CSMFMT	

Reg	Bit	Name	Description
3F	7	SEL_PIX	**DCVBS Output Selection.** When SEL_PIX is HIGH, the interpolated pixel data is selected as the output for the DCVBS port. When SEL_PIX is LOW, the non-interpolated pixel data is selected as the output for the DCVBS port.
3F	6	RESERVED	Program Low
3F	5	GAUSS_BYP	**Gaussian Bypass Select.** When GAUSS_BYP is LOW, the gaussian filter is enabled. When GAUSS_BYP is HIGH, the gaussian filter is bypassed.
3F	4	SEL_CLK	**DCVBS Clock Select.** When SEL_CLK is LOW, the DCVBS output is clocked at the PXCK. When SEL_CLK is HIGH, the DCVBS output is clocked at the PCK.
3F	3	C2DB_OFF	**COMP2DB Offset Selection.** When C2DB_OFF is HIGH an offset of 256 is added to the COMP2 output allowing the chrominance data that extends below the sync level to be passed through the outputs.
3F	2-0	RESERVED	Program Low

Subcarrier Register (0x40)

7	6	5	4	3	2	1	0
FREQL							

Reg	Bit	Name	Description
40	7-0	FREQL	**Subcarrier Frequency.** Bits 7-0 of the subcarrier frequency FREQL[31:0].

Control Register Definitions (continued)

Subcarrier Register (0x41)

7	6	5	4	3	2	1	0
FREQ3							

Reg	Bit	Name	Description
41	7-0	FREQ3	**Subcarrier Frequency.** Bits 15-8 of the subcarrier frequency FREQL[31:0].

Subcarrier Register (0x42)

7	6	5	4	3	2	1	0
FREQ2							

Reg	Bit	Name	Description
42	7-0	FREQ2	**Subcarrier Frequency.** Bits 23-16 of the subcarrier frequency FREQL[31:0].

Subcarrier Register (0x43)

7	6	5	4	3	2	1	0
FREQM							

Reg	Bit	Name	Description
43	7-0	FREQM	**Subcarrier Frequency.** Bits 31-24 of the subcarrier frequency FREQL[31:0].

Subcarrier Register (0x44)

7	6	5	4	3	2	1	0
SYSPHL							

Reg	Bit	Name	Description
44	7-0	SYSPHL	**System Phase.** Bits 7-0 of the video phase offset SYSPH[15:0].

Subcarrier Register (0x45)

7	6	5	4	3	2	1	0
SYSPHM							

Reg	Bit	Name	Description
45	7-0	SYSPHM	**System Phase.** Bits 15-8 of the video phase offset SYSPH[15:0].

Control Register Definitions (continued)

Subcarrier Register (0x46)

7	6	5	4	3	2	1	0
BURPHL							

Reg	Bit	Name	Description
46	7-0	BURPHL	**Burst Phase.** Bits 7-0 of the burst phase offset BURPH[15:0].

Subcarrier Register (0x47)

7	6	5	4	3	2	1	0
BURPHM							

Reg	Bit	Name	Description
47	7-0	BURPHM	**Burst Phase.** Bits 15-8 of the burst phase offset BURPH[15:0].

Burst Height Register (0x48)

7	6	5	4	3	2	1	0
BRSTFULL							

Reg	Bit	Name	Description
48	7-0	BRSTFULL	**Burst Height – Maximum Amplitude.** The 8 bit value assigned to U burst component in NTSC and to the U and V components in PAL for the maximum burst amplitude. The burst envelopes midpoint is derived from BRSTFULL. The value programmed into BRSTFULL needs to be .707 of the magnitude of the burst vector.

Burst Height Register (0x49)

7	6	5	4	3	2	1	0
BRST1							

Reg	Bit	Name	Description
49	7-0	BRST1	**Burst Height – 1st Intermediate Value.** The 8 bit value assigned to U burst component in NTSC and to the U and V components in PAL for the first intermediate value of the burst envelope. The value programmed into BRST1 needs to be .707 of the magnitude of the burst vector.

Control Register Definitions (continued)

Subcarrier Register (0x4A)

7	6	5	4	3	2	1	0
BRST2							

Reg	Bit	Name	Description
4A	7-0	BRST2	**Burst Height – 2nd Intermediate Value.** The 8 bit value assigned to U burst component in NTSC and to the U and V components in PAL for the second intermediate value of the burst envelope. The value programmed into BRST2 needs to be .707 of the magnitude of the burst vector.

Absolute Maximum Ratings (beyond which the device may be damaged)

Parameter	Min.	Max.	Unit
Power Supply Voltage	-0.5	7.0	V
Digital Inputs			
Applied Voltage[2]	-0.5	V_{DD} + 0.5	V
Forced Current[3,4]	-20.0	20.0	mA
Digital Outputs			
Applied Voltage[2]	-0.5	V_{DD} + 0.5	V
Forced Current[3,4]	-20.0	20.0	mA
Short Circuit Duration (Single Output in HIGH state to GND)		1	second
Analog Output Short Circuit Duration (Single output to GND)	Infinite		
Temperature			
Operating, Ambient	-20	+110	°C
Operating, Junction, Plastic package		+150	°C
Lead, Soldering (10 seconds)		+300	°C
Vapor Phase Soldering (1 minute)		+220	°C
Storage	-65	+150	°C

Notes:

1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied.
2. Applied voltage must be current limited to specified range, and measured with respect to GND.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current, flowing into the device.

Operating Conditions

Parameter			Min.	Nom.	Max.	Units
V_{DD}	Power Supply Voltage		4.75	5.0	5.25	V
V_{IH}	Input Voltage, Logic HIGH	TTL Compatible Inputs	2.0		V_{DD}	V
		CMOS Compatible Inputs	$0.7V_{DD}$		V_{DD}	V
V_{IL}	Input Voltage, Logic LOW	TTL Compatible Inputs	GND		0.8	V
		CMOS Compatible Inputs	GND		$0.3V_{DD}$	V
I_{OH}	Output Current, Logic HIGH				-2.0	mA
I_{OL}	Output Current, Logic LOW				4.0	mA
V_{REF}	External Reference Voltage			1.235		V
I_{REF}	D/A Converter Reference Current (I_{REF} = V_{REF} / R_{REF}, flowing out of the R_{REF} pin)			1.020		mA
R_{REF}	Reference Resistor, V_{REF} = Nom.			1210		Ω
R_{OUT}	Total Output Load Resistance			37.5		Ω
T_A	Ambient Temperature, Still Air		0		70	°C
Pixel Interface						
f_{PXL}	Pixel Rate		10		15	Mpps
f_{PXCK}	Master Clock Rate, 2x pixel rate		20		30	MHz
t_{PWHPX}	PXCK Pulse Width, HIGH		15			ns
t_{PWLPX}	PXCK Pulse Width, LOW		17.5			ns

Operating Conditions (continued)

Parameter		Min.	Nom.	Max.	Units
t_{SP}	Setup Time	16			ns
t_{HP}	Hold Time	0			ns
Parallel Microprocessor Interface					
t_{PWLCS}	$\overline{CS}$ Pulse Width, LOW	4			PXCK
t_{PWHCS}	$\overline{CS}$ Pulse Width, HIGH	6			PXCK
t_{SA}	Address Setup Time	17			ns
t_{HA}	Address Hold Time	0			ns
t_{SD}	Data Setup Time (write)	16			ns
t_{HD}	Data Hold Time (write)	0			ns
t_{SR}	$\overline{RESET}$ Setup Time	12			ns
t_{HR}	$\overline{RESET}$ Hold Time	2			ns
Serial Interface					
t_{DAL}	SCL Pulse Width, LOW		1.3		µs
t_{DAH}	SCL Pulse Width, HIGH		0.6		µs
t_{STAH}	SDA Start Hold Time		0.6		µs
t_{STASU}	SCL to SDA Setup Time (Stop)		0.6		µs
t_{STOSU}	SCL to SDA Setup Time (Start)		0.6		µs
t_{BUFF}	SDA Stop Hold Time Setup		1.3		µs
t_{DSU}	SDA to SCL Data Setup Time		300		ns
t_{DHO}	SDA to SCL Data Hold Time		300		ns

Electrical Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
I_{DD}	Power Supply Current	V_{DD} = Max., f_{PXCK} = 27MHz		335	375	mA
I_{DDQ}	Power Supply Current (D/A disabled)	V_{DD} = Max., f_{PXCK} = 27MHz		15	25	mA
V_{RO}	Voltage Reference Output			1.235		V
I_{BR}	Input Bias Current, V_{REF}	V_{REF} = Nom.		50		µA
I_{IH}	Input Current, Logic HIGH	V_{DD} = Max., V_{IN} = V_{DD}			10	µA
I_{IL}	Input Current, Logic LOW	V_{DD} = Max., V_{IN} = GND			-10	µA
V_{OH}	Output Voltage, Logic HIGH	I_{OH} = Max.	2.4			V
V_{OL}	Output Voltage, Logic LOW	I_{OL} = Max.			0.4	V
I_{OZH}	Hi-Z Leakage current, HIGH	V_{DD} = Max., V_{IN} = V_{DD}			10	µA
I_{OZL}	Hi-Z Leakage current, LOW	V_{DD} = Max., V_{IN} = GND			-10	µA
C_I	Digital Input Capacitance	T_A = 25°C, f = 1MHz		4	10	pF
C_O	Digital Output Capacitance	T_A = 25°C, f = 1MHz		10		pF
V_{OC}	Video Output Compliance Voltage		-0.3		2.0	V
R_{OUT}	Video Output Resistance			15		kΩ
C_{OUT}	Video Output Capacitance	I_{OUT} = 0 mA, f = 1 MHz		15	25	pF

Notes:

1. Typical I_{DD} with V_{DD} = +5.0 Volts and T_A = 25°C.
2. Timing reference points are at the 50% level.

Switching Characteristics

Parameter		Conditions	Min.	Typ.	Max.	Units
PIPES	Pipeline Delay	PD to Analog Out PD to DCVBS			64 66	PXCK Periods
t_{DOZ}	Output Delay, $\overline{CS}$ to low-Z		4		15	ns
t_{DOM}	Output Delay, $\overline{CS}$ to Data Valid				15	ns
t_{HOM}	Output Hold Time, $\overline{CS}$ to hi-Z		10			ns
t_{DO}	Output Delay	PXCK to HSOUT, VSOUT, PDC, LINE, FLD			15	ns
t_R	D/A Output Current Risetime	10% to 90% of full-scale		2		ns
t_F	D/A Output Current Falltime	90% to 10% of full-scale		2		ns
t_{DOV}	Analog Output Delay			10		ns

Notes:

1. Timing reference points are at the 50% level.
2. Analog C_{LOAD} <10 pF, D_{7-0} load <40 pF.
3. Pipeline delay, with respect to PXCK, is a function of the phase relationship between the internally generated PCK (PXCK/2) and PXCK, as established by the hardware $\overline{RESET}$.

System Performance Characteristics

Parameter		Conditions	Min.	Typ.	Max.	Units
RES	D/A Converter Resolution		10	10	10	Bits
E_{LI}	Integral Linearity Error				0.25	%
E_{LD}	Differential Linearity Error (monotonic)				0.10	%
E_G	Gain Error				±7.5	%FS
dp	Differential Phase	PXCK = 27.00 MHz,40 IRE Ramp		0.5		degree
dg	Differential Gain	PXCK = 27.00 MHz,40 IRE Ramp		0.9		%
SKEW	CHROMA to LUMA Output Skew			0	1	ns
PSRR	Power Supply Rejection Ratio	f=1kHz		0.5		%/%V_{DD}

Notes:

1. TTL input levels are 0.0 and 3.0 Volts, 10%-90% rise and fall times <3 ns.
2. Analog CLOAD <10 pF, D7-0 load <40 pF.

Applications Discussion

The suggested output reconstruction filter is shown in Figure 29. The phase and frequency response for the encoder and the reconstruction filter is shown in Figure 30.

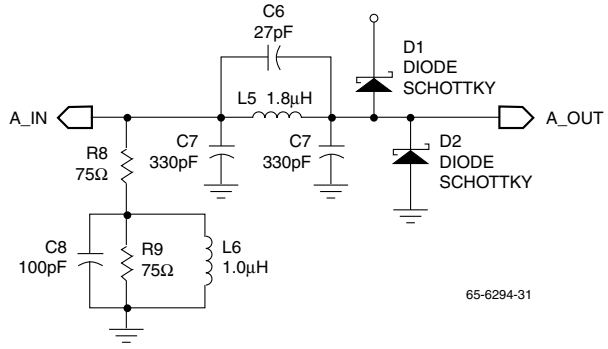


Figure 28. Typical Analog Reconstruction Filter

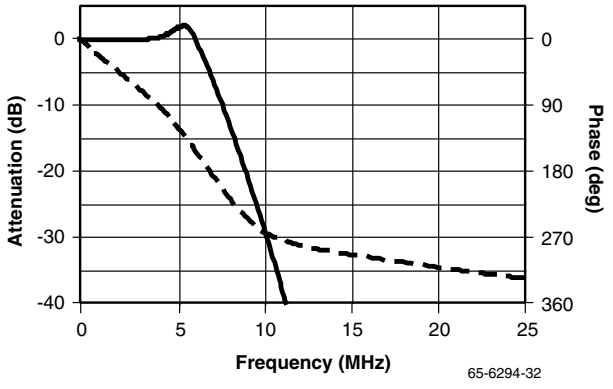


Figure 29. Overall Response

The circuit in Figure 31 shows the connection of power supply voltages, output reconstruction filters and the external voltage reference. All V_{DD} pins should be connected to the same power source.

The full-scale output voltage level for each D/A:

$$V_{OUTx} = I_{OUTx} \times R_{Lx} = K \times I_{REFx} \times R_{Lx}$$
$$= K \times (V_{REF}/R_{REFx}) \times R_{Lx}$$

where:

- I_{OUTx} is the full-scale output current sourced by the D/A converter.
- R_{Lx} is the resistive load on the D/A output pin.
- K is a constant for the TMC2192 D/A converters (approximately equal to 34).
- I_{REFx} is the reference current flowing out of the R_{REFx} pin to ground.
- V_{REF} is the voltage measured on the V_{REF} pin.
- R_{REFx} is the total resistance connected between the R_{REFx} pin and ground.

The reference voltage in Figure 31 is from an LM185 1.2 Volt band-gap reference. The suggested trim is designed to give ±10% of trim around 5K Ohms. This R_{REFx} sets the "gain" for that D/A converter. Varying R_{REFx} ±10% will cause the full-scale output voltage on the D/A to vary by ±10%.

An alternative output reconstruction filter is the Microelectronic Modules Corp. ST-163E, which contains 4 independent reconstruction filter. The phase and frequency response of this filter is shown in the Output Low-Pass Filters Section of this data sheet.

Layout Considerations

Designing with high-performance mixed-signal circuits demands printed circuits with ground planes. Wire-wrap is not an option. Overall system performance is strongly influenced by the board layout. Capacitive coupling from digital to analog circuits may result in poor picture quality. Consider the following suggestions when doing the layout:

- Keep analog traces (C_{BYPx}, V_{REF}, R_{REF}, DACx) as short and far from all digital signals as possible. The TMC2192 should be located near the board edge, close to the analog output connectors.
- The power plane for the TMC2192 should be separate from that which supplies other digital circuitry. A single power plane should be used for all of the V_{DD} pins. If the power supply for the TMC2192 is the same for the system's digital circuitry, power to the TMC2192 should be filtered with ferrite beads and 0.1µF capacitors to reduce noise.
- The ground plane should be solid, not cross-hatched. Connections to the ground plane should be very short.
- Decoupling capacitors should be applied liberally to pins. For best results, use 0.1µF capacitors. Lead lengths should be minimized. Ceramic chip capacitors are the best choice.
- If there is dedicated digital power plane, it should not overlap the TMC2192 footprint, the voltage reference, or the analog outputs. Capacitive coupling of digital power supply noise from this layer to the TMC2192 and its related analog circuitry can have an adverse effect on performance.
- The PXCK should be handled carefully. Jitter and noise on this clock or its ground reference will translate to noise on the video outputs. Terminate the clock line carefully to eliminate overshoot and ringing.
- Connect all unused inputs to the TMC2192 to either ground or V_{DD}. Do not leave them unconnected.

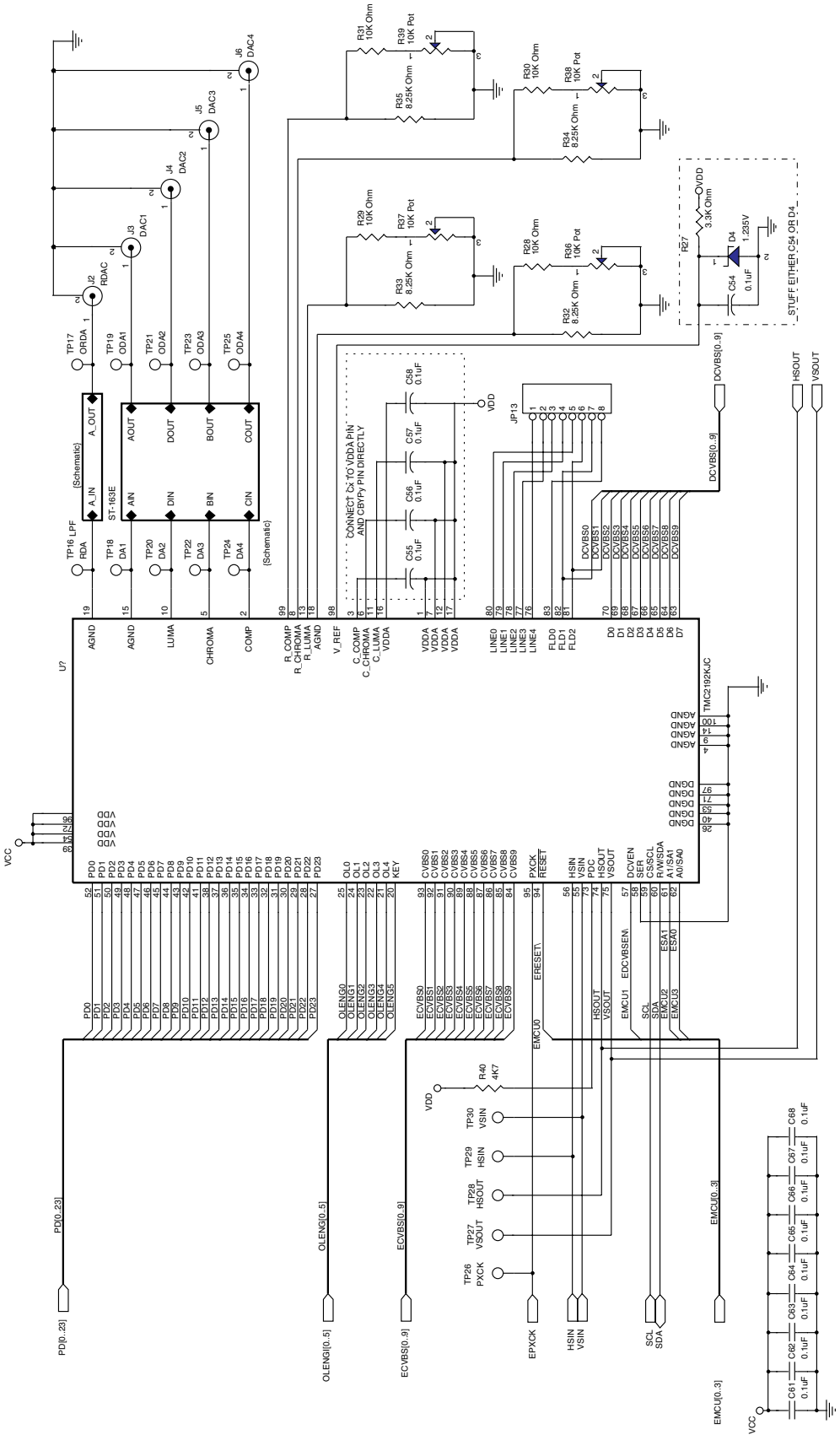


Figure 30. Typical Layout

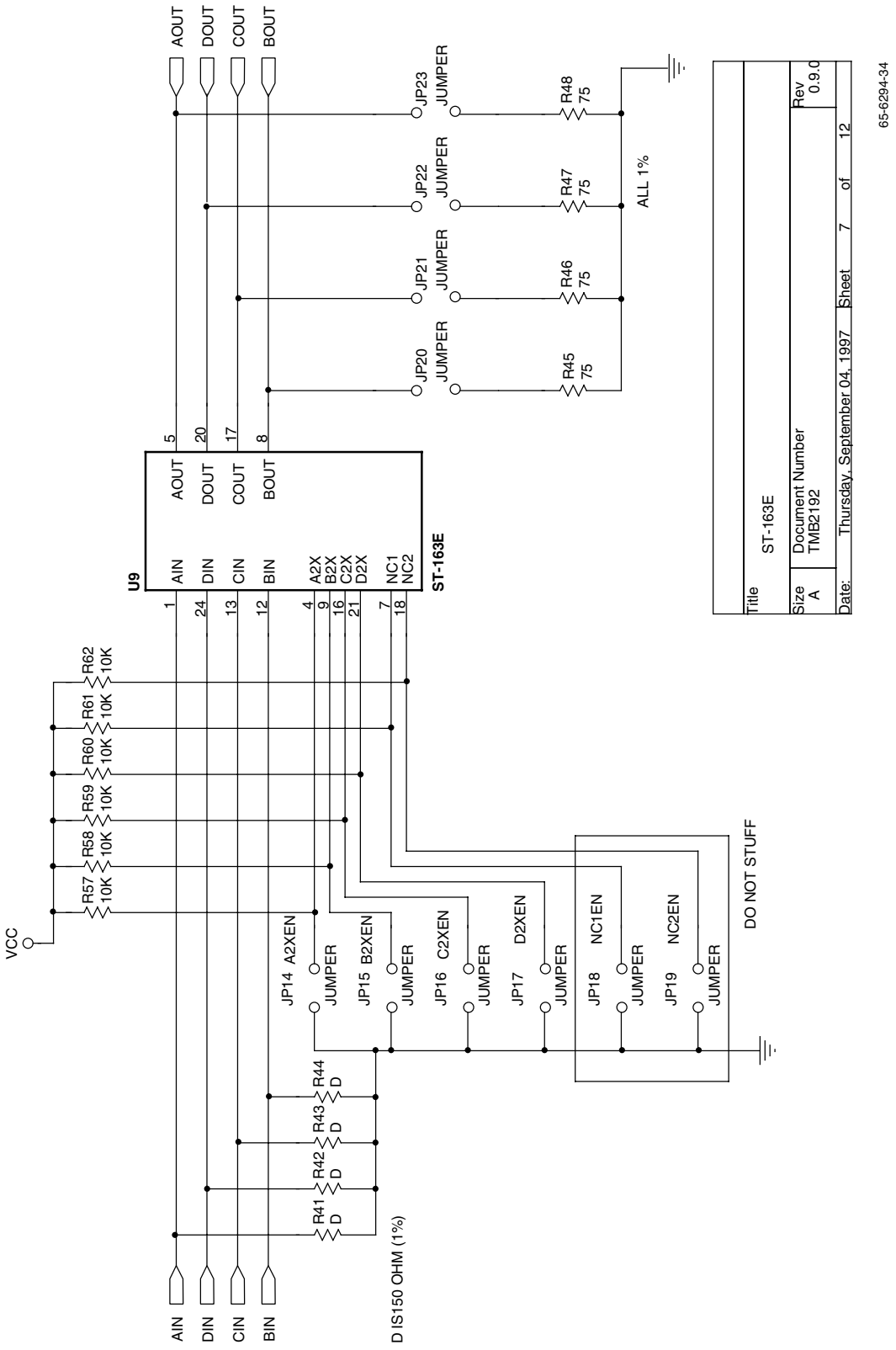


Figure 31. ST-163E Layout

Output Low-Pass Filters

The response at 5.0MHz typically varies < ±0.25dB with supplies of ±5V to ±8V. When operating in the 0dB gain mode, pin 6 must be well isolated from ground planes. When operating in the +6dB gain mode, pin 6 must have a low resistance path to ground.

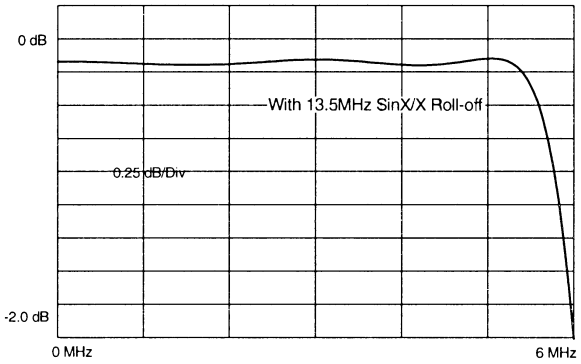


Figure 32. Pass Band

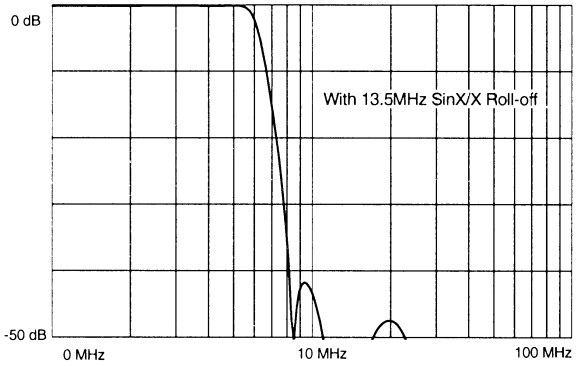


Figure 33. Stop Band

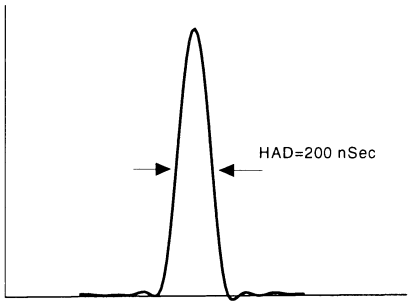


Figure 34. 2T Pulse

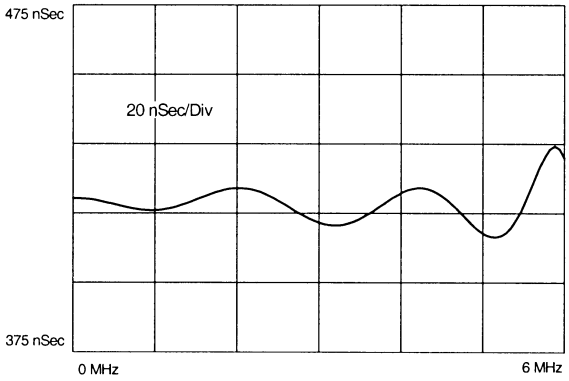


Figure 35. Group Delay

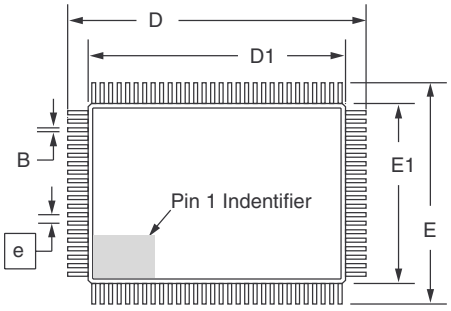
Mechanical Dimensions

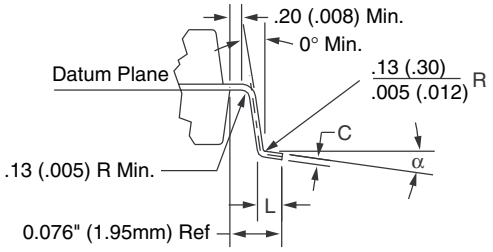
100-Lead MQFP

Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	—	.134	—	3.40	
A1	.010	—	.25	—	
A2	.100	.120	2.55	3.05	
B	.008	.015	.22	.38	3, 5
C	.005	.009	.13	.23	5
D	.904	.923	22.95	23.45	
D1	.783	.791	19.90	20.10	
E	.667	.687	16.95	17.45	
E1	.547	.555	13.90	14.10	
e	.0256 BSC		.65 BSC		
L	.028	.040	.73	1.03	4
N	100		100		
ND	30		30		
NE	20		20		
α	0°	7°	0°	7°	
ccc	—	.004	—	.12	

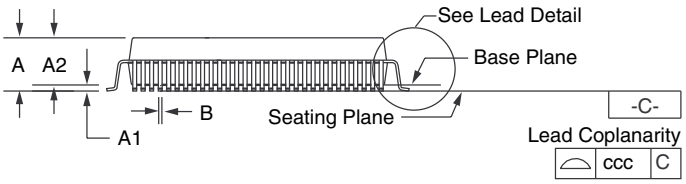
Notes:

1. All dimensions and tolerances conform to ANSI Y14.5M-1982.
2. Controlling dimension is millimeters.
3. Dimension "B" does not include dambar protrusion. Allowable dambar protrusion shall be .08mm (.003in.) maximum in excess of the "B" dimension. Dambar cannot be located on the lower radius or the foot.
4. "L" is the length of terminal for soldering to a substrate.
5. "B" & "C" includes lead finish thickness.





Lead Detail



Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
TMC2192KHC	T_A = 0°C to 70°C	Commercial	100-pin MQFP	TMC2192KHC