TMC2011A/2111A

Variable-Length Shift Register

Features

- Low power CMOS
- TMC2011A is a pin compatible replacement for the TDC1011 and TMC2011
- TMC2211A is a pin compatible replacement for the TMC2111
- Inputs and outputs are TTL compatible
- DC–40MHz clock rate
- Selectable delay lengths (TMC2011A: 3 to 18 stages, TMC2111A: 1 to 16 stages)
- Special 4-bit wide mixed-delay mode (TMC2011A)
- Available in 24-pin CERDIP and plastic DIP and 28-lead Plastic Leadless Chip Carrier

Applications

- Video filtering
- High speed data registers
- Local storage registers
- Digital delay lines
- Television special effects
- Pipeline register

Description

The TMC2011A and TMC2111A are high-speed, byte-wide shift registers with programmable delay lengths.

The TMC2011A can be programmed to any length between 3 and 18 stages. It offers a special split-word mode which allows for mixed delay lengths. The TMC2011A, constructed in low-power CMOS, is pin and function compatible with the bipolar TDC1011.

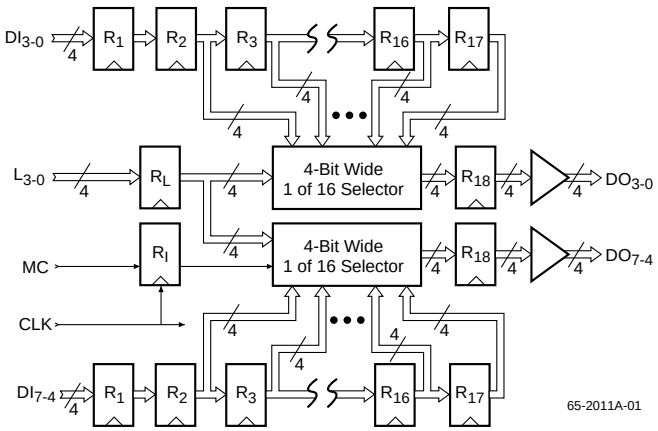
The TMC2111A is a byte-wide shift register that can be programmed to lengths of 1 to 16 stages.

The TMC2011A and TMC2111A are fully synchronous, with all operations controlled by a single master clock. Input and output registers are positive-edge triggered D-type flip-flops. The length and mode controls are also registered. Both devices operate with a maximum clock rate of 40 MHz.

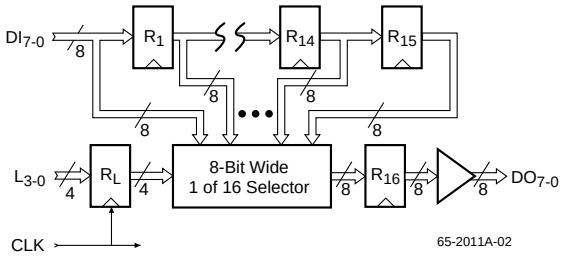
Fabricated in a submicron CMOS process, the TMC2011A and TMC2111A are TTL-compatible, and are available in 24-pin CERDIP and Plastic DIP packages as well as a 28-lead Plastic Leadless Chip Carrier.

Block Diagrams

TMC2011A



TMC2111A

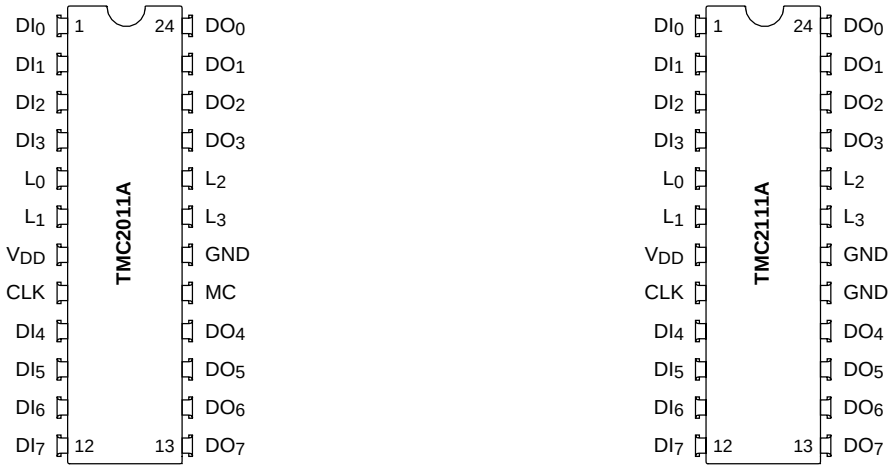


Functional Description

The TMC2011A consists of two 4-bit wide, programmable length shift registers. The TMC2111A consists of a single 8-bit wide, programmable length shift register. The internal registers of each device share control signals and a common clock.

Pin Assignments

24 Lead DIP (B2, N2) Packages



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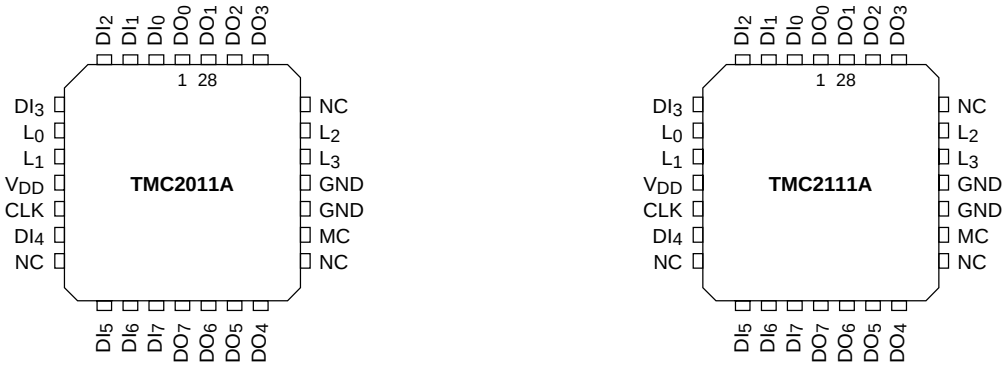
28 Lead PLCC (R3) Package



65-2011A-04

Pin Descriptions – TMC2011A

Pin Name	Pin Number DIP	Pin Number PLCC	Pin Function Description
Power			
V_{DD}	7	8	**Supply Voltage.** The TMC2011A and operates from a single +5V supply. All power and ground lines must be connected.
GND	18	21,22	**Ground.** The TMC2011A operates from a single +5V supply. All power and ground lines must be connected.
Data Inputs			
DI_{7-0}	12,11,10, 9,4,3,2,1	14,13,12, 10,5,4,3,2	**Data Input.** Eight inputs are provided for the data, which pass through the shift register unchanged. The eight inputs on the TMC2011A are divided into two groups of four bits to allow mixed delay operation. The lengths of these two groups are different when the Mode Control (MC) is HIGH (see Table 1). When MC is LOW both groups have equal delays.
Data Outputs			
DO_{7-0}	13,14,15, 16,21,22, 23,24	15,16,17, 18,26,27, 28,1	**Data Output.** The outputs of the shift register are delayed relative to the input signals. The amount of the delay is programmable (see Table 1). The outputs remain valid for a minimum of t_{HO} nanoseconds after the leading edge of CLK. This allow the data to be latched into circuits with non-zero hold time requirements.
Controls			
CLK	8	9	**Master Clock.** All inputs and outputs are synchronous and operate from a single master clock. All operations occur on the rising edge of the master clock.
L_{3-0}	19,20,6,5	23,24,7,6	**Length Select.** The length select input is used to determine the register delay of the TMC2011A. This input is registered and affects the output t_{DO} after the clock edge after it is input to the device (see Timing Diagram). Delay lengths are specified in Table 1.
MC	17	20	**Mode Control.** The Mode Control is used to select the special 4-bit wide split mode. When HIGH, the delay on DO_{7-4} is fixed at 18 stages, while DO_{3-0} have the delay specified by the length select. When MC is LOW, all eight bits have equal delays as specified by the length select.

Pin Descriptions – TMC2111A

Pin Name	Pin Number DIP	Pin Number PLCC	Pin Function Description
Power			
V_{DD}	7	8	**Supply Voltage.** The TMC2111A operates from a single +5V supply. All power and ground lines must be connected.
GND	17,18	20,21,22	**Ground.** The TMC2111A operates from a single +5V supply. All power and ground lines must be connected.
Data Inputs			
DI_{7-0}	12,11,10, 9,4,3,2,1	14,13,12, 10,5,4,3,2	**Data Input.** Eight inputs are provided for the data, which pass through the shift register unchanged. The TMC2111A consists of a single group of eight bits with all data bits having equal delays.
Data Outputs			
DO_{7-0}	13,14,15, 16,21,22, 23,24	15,16,17, 18,26,27, 28,1	**Data Output.** The outputs of the shift register are delayed relative to the input signals. The amount of the delay is programmable (see Table 1). The outputs remain valid for a minimum of t_{HO} nanoseconds after the leading edge of CLK. This allow the data to be latched into circuits with non-zero hold time requirements.
Controls			
CLK	8	9	**Master Clock.** All inputs and outputs are synchronous and operate from a single master clock. All operations occur on the rising edge of the master clock.
L_{3-0}	19,20,6,5	23,24,7,6	**Length Select.** The length select input is used to determine the register delay of the TMC2111A. This input is registered and affects the output t_{DO} after the clock edge after it is input to the device (see Timing Diagram). Delay lengths are specified in Table 1.

Table 1. Programming Length Controls

Input Code				TMC2011A				TMC2111A
				Mode (MC) =0		Mode (MC) =1		
L_3	L_2	L_1	L_0	DO_{3-0} Length	DO_{7-4} Length	DO_{3-0} Length	DO_{7-4} Length	DO_{7-0} Length
0	0	0	0	3	3	3	18	1
0	0	0	1	4	4	4	18	2
0	0	1	0	5	5	5	18	3
0	0	1	1	6	6	6	18	4
0	1	0	0	7	7	7	18	5
0	1	0	1	8	8	8	18	6
0	1	1	0	9	9	9	18	7
0	1	1	1	10	10	10	18	8
1	0	0	0	11	11	11	18	9
1	0	0	1	12	12	12	18	10
1	0	1	0	13	13	13	18	11
1	0	1	1	14	14	14	18	12
1	1	0	0	15	15	15	18	13
1	1	0	1	16	16	16	18	14
1	1	1	0	17	17	17	18	15
1	1	1	1	18	18	18	18	16

Absolute Maximum Ratings

(beyond which the device may be damaged)[1]

Parameter	Min	Typ	Max	Unit
Supply Voltage	-0.5		7.0	V
Input Voltage	-0.5		V_{DD} + 0.5	V
Output, Applied Voltage[2]	-0.5		V_{DD} + 0.5	V
Output, Externally Forced Current[3,4]	-3.0		6.0	mA
Output, Short Circuit Duration (single output in HIGH state to ground)			1	sec
Operating, Ambient Temperature	-20		110	°C
Junction Temperature			140	°C
Storage Temperature	-65		150	°C
Lead Soldering (10 seconds)			300	°C

Notes:

1. Functional operation under any of these conditions is NOT implied. Performance and reliability are guaranteed only if Operating Conditions are not exceeded.
2. Applied voltage must be current limited to specified range.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current flowing into the device.

Operating Conditions

Parameter			Min	Nom	Max	Units
V_{DD}	Power Supply Voltage		4.75	5.0	5.25	V
f_{CLK}	Clock frequency	TMC2011A, 2111A			30	MHz
		TMC2011A-1, 2111A-1			40	
t_{PWH}	CLK pulse width, HIGH		12			ns
t_{PWL}	CLK pulse width, LOW		12			ns
t_S	Input Data Set-up Time		6			ns
t_H	Input Data Hold Time		1			ns
V_{IH}	Input Voltage, Logic HIGH	DI_{7-0}, L_{3-0}, MC	2.0			V
		CLK	2.6			
V_{IL}	Input Voltage, Logic LOW				0.8	V
I_{OH}	Output Current, Logic HIGH				-2.0	mA
I_{OL}	Output Current, Logic LOW				4.0	mA
T_A	Ambient Temperature, Still Air		0		70	°C

Electrical Characteristics

Parameter		Conditions	Min	Typ	Max	Units
I_{DDU}	Power Supply Current, Unloaded	V_{DD} = Max, f_{CLK}=30 MHz V_{DD} = Max, f_{CLK}=40 MHz			30 40	mA mA
I_{DDQ}	Power Supply Current, Quiescent	V_{DD} = Max, CLK = LOW			0.5	mA
C_{PIN}	I/O Pin Capacitance			5		pF
I_{IH}	Input Current, HIGH	V_{DD} = Max, V_{IN} = V_{DD}			±10	μA
I_{IL}	Input Current, LOW	V_{DD} = Max, V_{IN} = 0 V			±10	μA
I_{OS}	Short-Circuit Current				-100	mA
V_{OH}	Output Voltage, HIGH	DO_{7-0}, I_{OH} = Max	2.4			V
V_{OL}	Output Voltage, LOW	DO_{7-0}, I_{OL} = Max			0.4	V

Switching Characteristics

Parameter		Conditions	Min	Typ	Max	Units
t_{DO}	Output Delay Time	C_{LOAD} = 25 pF			15	ns
t_{HO}	Output Hold Time	C_{LOAD} = 25 pF	3			ns

Timing Diagrams

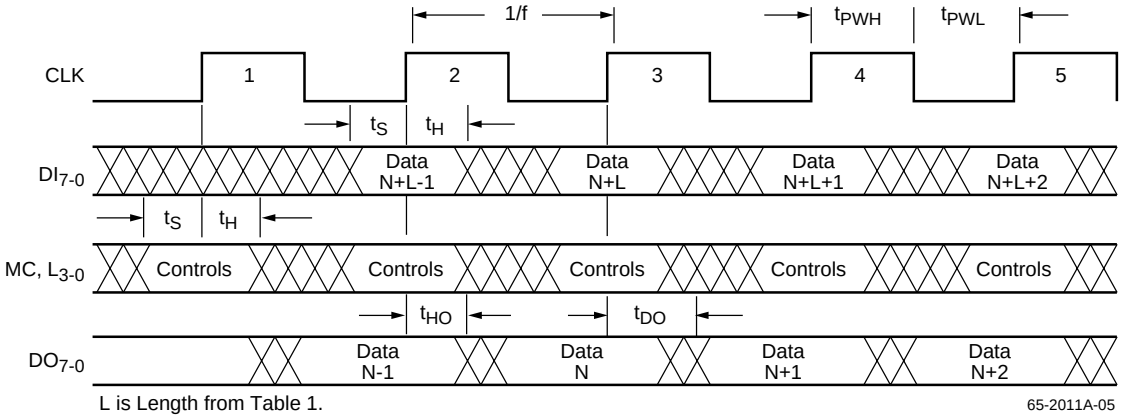


Figure 1. Preset Length Controls

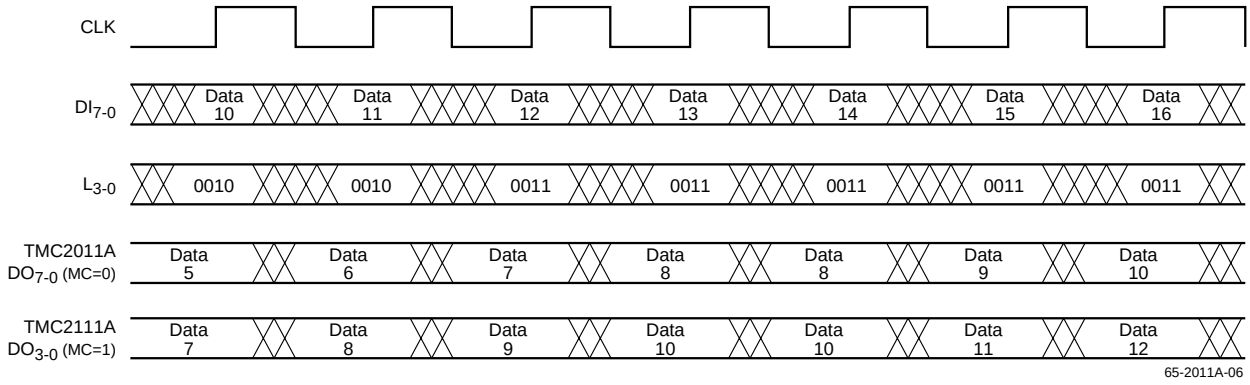


Figure 2. Length Control Operation

Equivalent Circuits

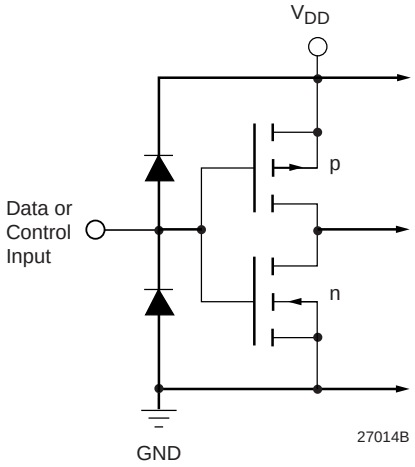


Figure 3. Equivalent Digital Input Circuit

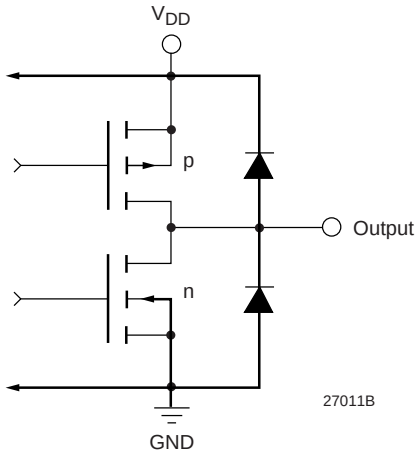


Figure 4. Equivalent Digital Output Circuit

Notes:

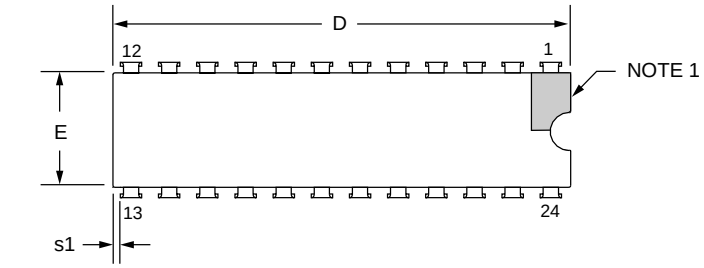
Mechanical Dimensions

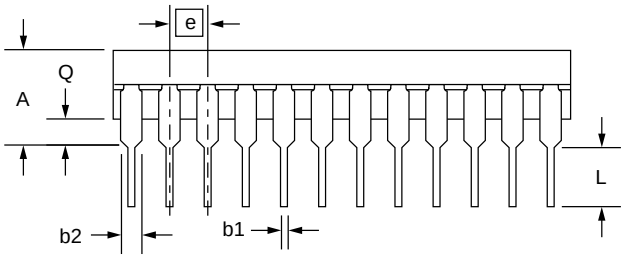
24-Lead Ceramic DIP Package

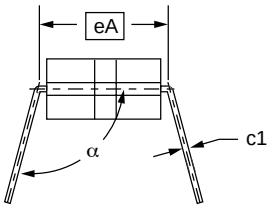
Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	—	.200	—	5.08	
b1	.014	.023	.36	.58	8
b2	.045	.065	1.14	1.65	2, 8
c1	.008	.015	.20	.38	8
D	—	1.280	—	32.51	4
E	.220	.310	5.59	7.87	4
e	.100 BSC		2.54 BSC		5
eA	.300 BSC		7.62 BSC		7
L	.125	.200	3.18	5.08	
Q	.015	.060	.38	1.52	3
s1	.005	—	.13	—	6
α	90°	105°	90°	105°	

Notes:

1. Index area: a notch or a pin one identification mark shall be located adjacent to pin one. The manufacturer's identification shall not be used as pin one identification mark.
2. The minimum limit for dimension "b2" may be .023 (.58mm) for leads number 1, 12, 13 and 24 only.
3. Dimension "Q" shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. The basic pin spacing is .100 (2.54mm) between centerlines. Each pin centerline shall be located within ±.010 (.25mm) of its exact longitudinal position relative to pins 1 and 24.
6. Applies to all four corners (leads number 1, 12, 13, and 24).
7. "eA" shall be measured at the center of the lead bends or at the centerline of the leads when "α" is 90°.
8. All leads – Increase maximum limit by .003 (.08mm) measured at the center of the flat, when lead finish applied.
9. Twenty-two spaces.







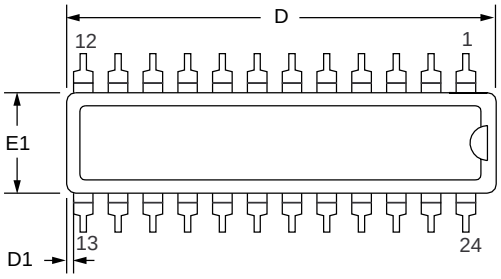
Mechanical Dimensions (continued)

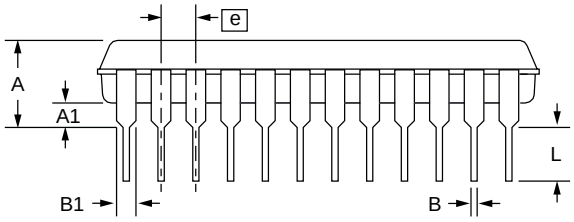
24-Lead Plastic DIP Package

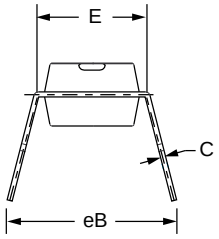
Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	—	.210	—	5.33	
A1	.015	—	.38	—	
A2	.115	.195	2.53	4.95	
B	.014	.022	.36	.56	
B1	.045	.070	1.14	1.78	
C	.008	.015	.20	.38	4
D	1.125	1.275	28.58	32.39	2
D1	.005	—	.13	—	
E	.300	.325	7.62	8.26	
E1	.240	.280	6.10	7.11	2
e	.100 BSC		2.54 BSC		
eB	—	.430	—	10.92	
L	.115	.160	2.92	4.06	
N	24		24		5

Notes:

1. Dimensioning and tolerancing per ANSI Y14.5M-1982.
2. "D" and "E1" do not include mold flashing. Mold flash or protrusions shall not exceed .010 inch (0.25mm).
3. Terminal numbers are shown for reference only.
4. "C" dimension does not include solder finish thickness.
5. Symbol "N" is the maximum number of terminals.







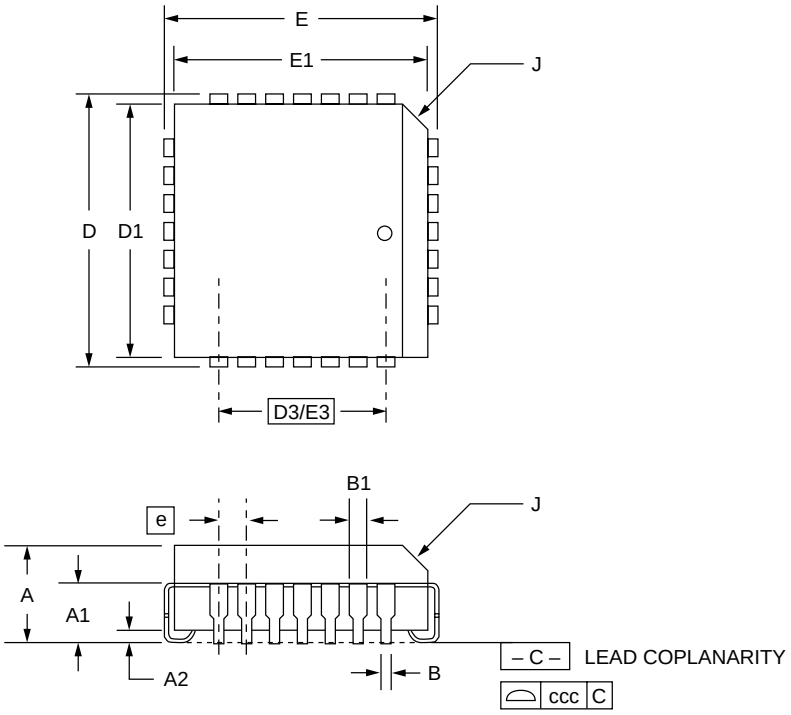
Mechanical Dimensions (continued)

28-Lead PLCC Package

Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.165	.180	4.19	4.57	
A1	.090	.120	2.29	3.05	
A2	.020	—	.51	—	
B	.013	.021	.33	.53	
B1	.026	.032	.66	.81	
D/E	.485	.495	12.32	12.57	
D1/E1	.450	.456	11.43	11.58	3
D3/E3	.300 BSC		7.62 BSC		
e	.050 BSC		1.27 BSC		
J	.042	.048	1.07	1.22	2
ND/NE	7		7		
N	28		28		
ccc	—	.004	—	0.10	

Notes:

1. All dimensions and tolerances conform to ANSI Y14.5M-1982
2. Corner and edge chamfer (J) = 45°
3. Dimension D1 and E1 do not include mold protrusion. Allowable protrusion is .101" (.25mm)



Ordering Information

Product Number	Temperature Range	Speed Grade	Screening	Package	Package Marking
TMC2011AB2C	0°C to 70°C	30 MHz	Commercial	24 Pin 0.3" CerDIP	2011AB2C
TMC2011AB2C1	0°C to 70°C	40 MHz	Commercial	24 Pin 0.3" CerDIP	2011AB2C1
TMC2011AN2C	0°C to 70°C	30 MHz	Commercial	24 Pin 0.3" Plastic DIP	2011AN2C
TMC2011AN2C1	0°C to 70°C	40 MHz	Commercial	24 Pin 0.3" Plastic DIP	2011AN2C1
TMC2011AR3C	0°C to 70°C	30 MHz	Commercial	28 Lead PLCC	2011AR3C
TMC2011AR3C1	0°C to 70°C	40 MHz	Commercial	28 Lead PLCC	2011AR3C1
TMC2111AB2C	0°C to 70°C	30 MHz	Commercial	24 Pin 0.3" CerDIP	2111AB2C
TMC2111AB2C1	0°C to 70°C	40 MHz	Commercial	24 Pin 0.3" CerDIP	2111AB2C1
TMC2111AN2C	0°C to 70°C	30 MHz	Commercial	24 Pin 0.3" Plastic DIP	2111AN2C
TMC2111AN2C1	0°C to 70°C	40 MHz	Commercial	24 Pin 0.3" Plastic DIP	2111AN2C1
TMC2111AR3C	0°C to 70°C	30 MHz	Commercial	28 Lead PLCC	2111AR3C
TMC2111AR3C1	0°C to 70°C	40 MHz	Commercial	28 Lead PLCC	2111AR3C1