

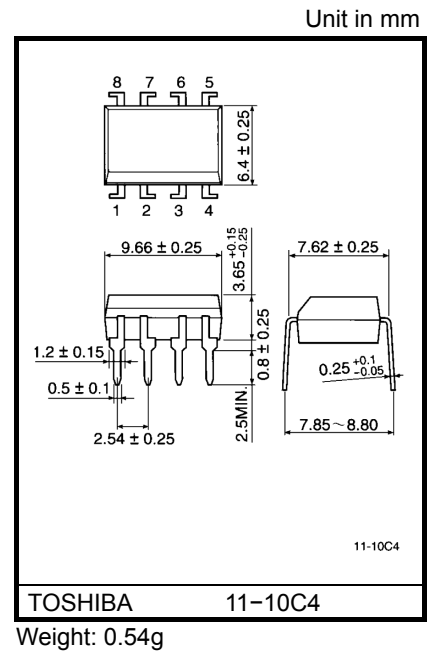
# TLP651

- Digital Logic Ground Isolation
- Line Receiver
- Microprocessor System Interfaces
- Switching Power Supply Feedback Control
- Analog Signal Isolation

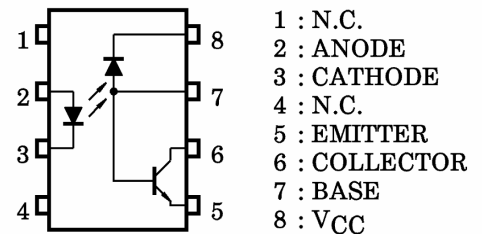
The TOSHIBA TLP651 consists of a GaAlAs high-output light emitting diode and a high speed detector of one chip photo diode-transistor. This unit is 8-lead DIP.

TLP651 has internal base connection. This base pin should be used for analog application or enable operation. If base pin is open, output signal will be noisy by environmental condition. For this case, TLP650 is suitable.

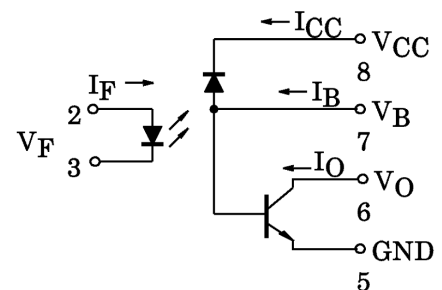
- Isolation voltage: 5000V<sub>rms</sub> (min.)
- Switching speed:  $t_{pHL} = 0.3\mu s$  (typ.)  
 $t_{pLH} = 0.5\mu s$  (typ.) ( $R_L = 1.9k\Omega$ )
- TTL compatible
- UL recognized: UL1577, file no. E67349
- BSI approved: BS EN60065: 2002  
Certificate no. 7613  
BS EN60950-1: 2002  
Certificate no. 7614



### Pin Configuration (top view)



### Schematic



## Absolute Maximum Ratings (Ta = 25°C)

Characteristic		Symbol	Rating	Unit
LED	Forward current (Note 1)	I <sub>F</sub>	25	mA
	Pulse forward current (Note 2)	I <sub>FP</sub>	50	mA
	Peak transient forward current (Note 3)	I <sub>FPT</sub>	1	A
	Reverse voltage	V <sub>R</sub>	5	V
	Diode power dissipation (Note 4)	P <sub>D</sub>	45	mW
Detector	Output current	I <sub>O</sub>	8	mA
	Peak output current	I <sub>OP</sub>	16	mA
	Output voltage	V <sub>O</sub>	-0.5~15	V
	Supply voltage	V <sub>CC</sub>	-0.5~15	V
	Base current	I <sub>B</sub>	5	mA
	Emitter-base reverse voltage	V <sub>EB</sub>	5	V
	Output power dissipation (Note 5)	P <sub>O</sub>	100	mW
Operating temperature range		T <sub>opr</sub>	-55~100	°C
Storage temperature range		T <sub>stg</sub>	-55~125	°C
Lead solder temperature (10s) (Note 6)		T <sub>sol</sub>	260	°C
Isolation voltage (AC, 1min., R.H.≤ 60%) (Note 7)		BV <sub>S</sub>	5000	V <sub>rms</sub>

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

(Note 1) Derate 0.8mA above 70°C.

(Note 2) 50% duty cycle, 1ms pulse width.  
Derate 1.6mA / °C above 70°C.

(Note 3) Pulse width ≤ 1μs, 300pps.

(Note 4) Derate 0.9mW / °C above 70°C.

(Note 5) Derate 2mW / °C above 70°C.

(Note 6) Soldering portion of lead: Up to 2mm from the body of the device.

(Note 7) Device considered a two terminal device: Pins 1, 2, 3 and 4 shorted together and pins 5, 6, 7 and 8 shorted together.

## Electrical Characteristics (Ta = 25°C)

Characteristic		Symbol	Test Condition	Min.	Typ.	Max.	Unit	
LED	Forward voltage	$V_F$	$I_F = 16\text{mA}$	—	1.65	1.85	V	
	Forward voltage temperature coefficient	$\Delta V_F / \Delta T_a$	$I_F = 16\text{mA}$	—	-2	—	mV / °C	
	Reverse current	$I_R$	$V_R = 5\text{V}$	—	—	10	$\mu\text{A}$	
	Capacitance between terminal	$C_T$	$V_F = 0, f = 1\text{MHz}$	—	45	—	pF	
Detector	High level output current	$I_{OH(1)}$	$I_F = 0\text{mA}, V_{CC} = V_O = 5.5\text{V}$	—	3	500	nA	
		$I_{OH(2)}$	$I_F = 0\text{mA}, V_{CC} = V_O = 15\text{V}$	—	—	5	$\mu\text{A}$	
		$I_{OH}$	$I_F = 0\text{mA}, V_{CC} = V_O = 15\text{V}$ $T_a = 70^\circ\text{C}$	—	—	250	$\mu\text{A}$	
	High level supply voltage	$I_{CCH}$	$I_F = 0\text{mA}, V_{CC} = 15\text{V}$	—	0.01	1	$\mu\text{A}$	
Coupled	Current transfer ratio	$I_O / I_F$	$I_F = 16\text{mA}$ $V_{CC} = 4.5\text{V}$ $V_O = 0.4\text{V}$	$T_a = 25^\circ\text{C}$	10	30	—	%
				Rank: O	19	30	—	
				$T_a = 0\sim 70^\circ\text{C}$	5	—	—	
	Low level output voltage	$V_{OL}$	$I_F = 16\text{mA}, V_{CC} = 4.5\text{V},$ $I_O = 1.1\text{mA}$ (Rank 0: $I_O = 2.4\text{mA}$ )	—	—	0.4	V	
				—	—	—	—	
Isolation resistance	$R_S$	$R.H. \leq 60\%, V_S = 500\text{V}_{DC}$ (Note 7)	$5 \times 10^{10}$	$10^{14}$	—	$\Omega$		
Capacitance between input to output	$C_S$	$V_S = 0, f = 1\text{MHz}$ (Note 7)	—	0.8	—	pF		

## Switching Characteristics (Ta = 25°C, VCC = 5V)

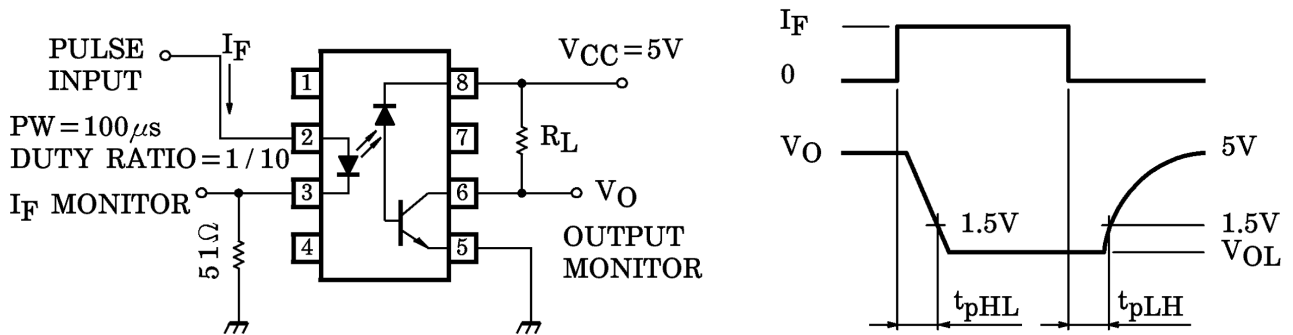
Characteristic	Symbol	Test Circuit	Test Condition	Min.	Typ.	Max.	Unit
Propagation delay time (H→L)	$t_{pHL}$	1	$I_F = 0 \rightarrow 16\text{mA}, V_{CC} = 5\text{V},$ $R_L = 4.1\text{k}\Omega$	—	0.2	0.8	$\mu\text{s}$
			Rank O: $R_L = 1.9\text{k}\Omega$	—	0.3	0.8	
Propagation delay time (L→H)	$t_{pLH}$	1	$I_F = 16 \rightarrow 0\text{mA}, V_{CC} = 5\text{V},$ $R_L = 4.1\text{k}\Omega$	—	1.0	2.0	$\mu\text{s}$
			Rank O: $R_L = 1.9\text{k}\Omega$	—	0.5	1.2	
Common mode transient immunity at logic high output (Note 8)	$C_{MH}$	2	$I_F = 0\text{mA}, V_{CM} = 200\text{V}_{p-p}$ $R_L = 4.1\text{k}\Omega$ (Rank O: $R_L = 1.9\text{k}\Omega$ )	—	400	—	V / $\mu\text{s}$
Common mode transient immunity at logic low output (Note 8)	$C_{ML}$		$I_F = 16\text{mA}, V_{CM} = 200\text{V}_{p-p}$ $R_L = 4.1\text{k}\Omega$ (Rank O: $R_L = 1.9\text{k}\Omega$ )	—	-1000	—	V / $\mu\text{s}$

(Note 8)  $CM_L$  is the maximum rate of fall of the common mode voltage that can be sustained with the output voltage in the logic low state ( $V_O < 0.8V$ ).

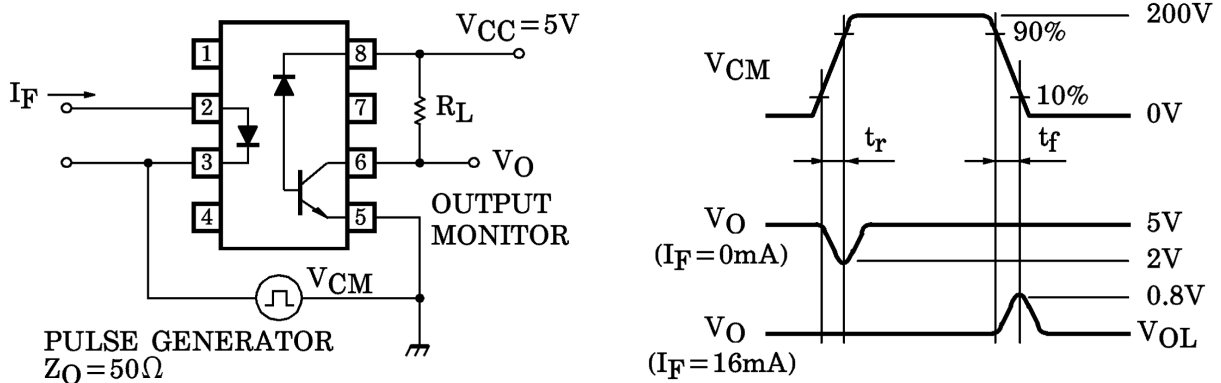
$CM_H$  is the maximum rate of rise of the common mode voltage that can be sustained with the output voltage in the logic high state ( $V_O > 2.0V$ ).

(Note 9) Maximum electrostatic discharge voltage for any pins: 100V (C = 200pF, R = 0).

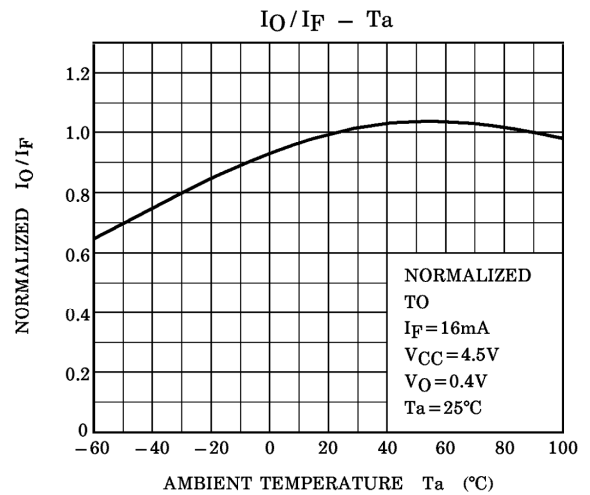
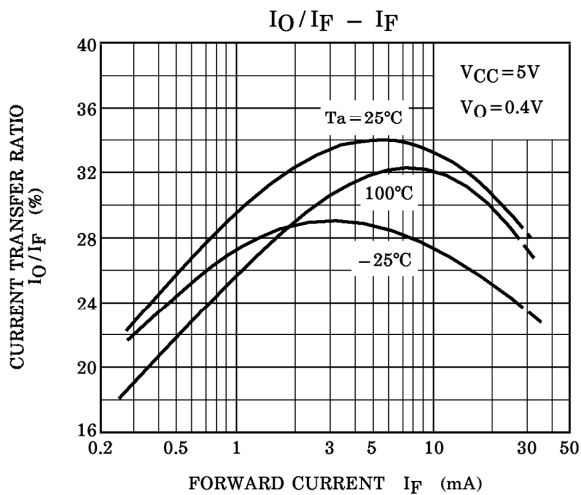
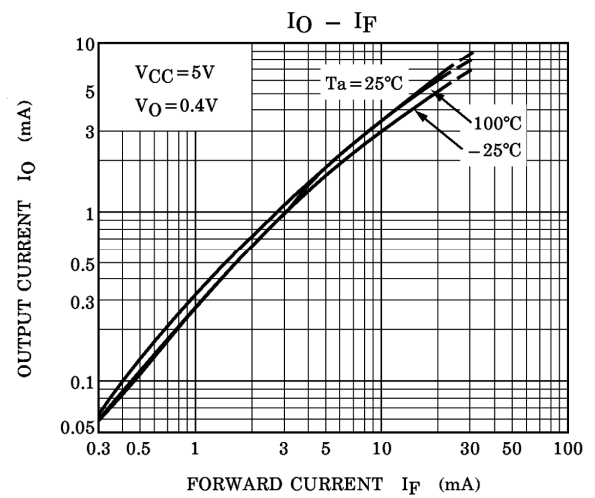
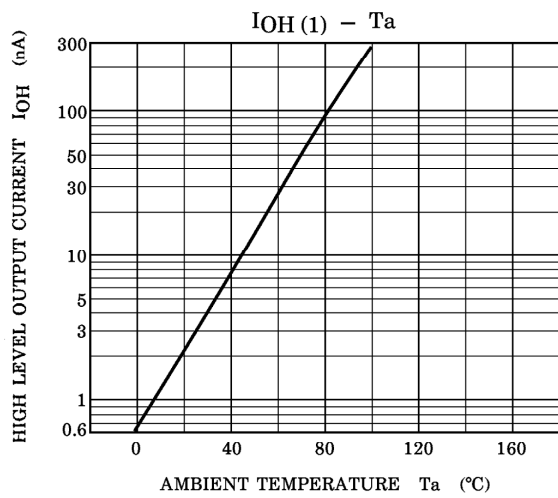
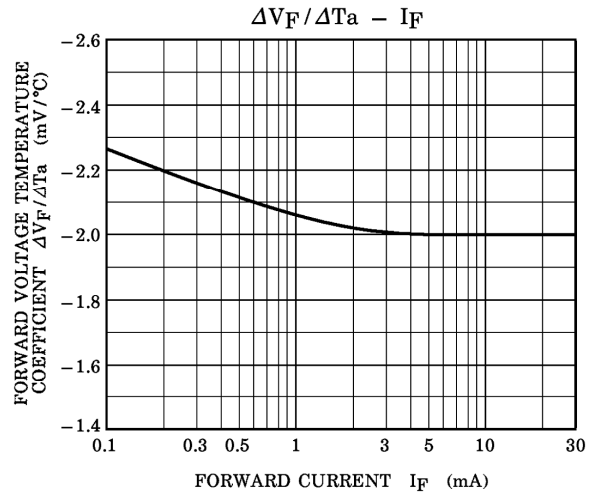
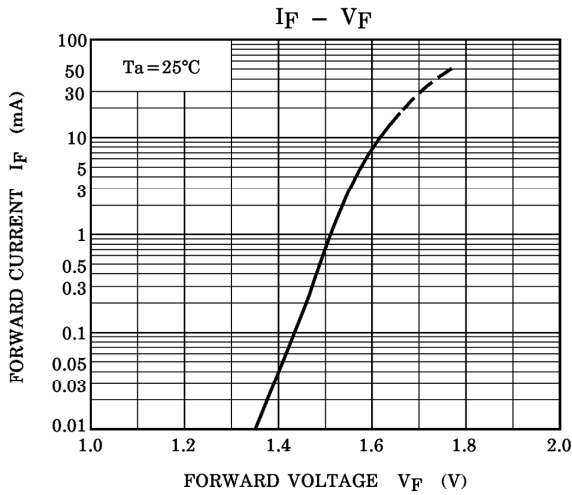
## Test Circuit 1: Switching Time Test Circuit

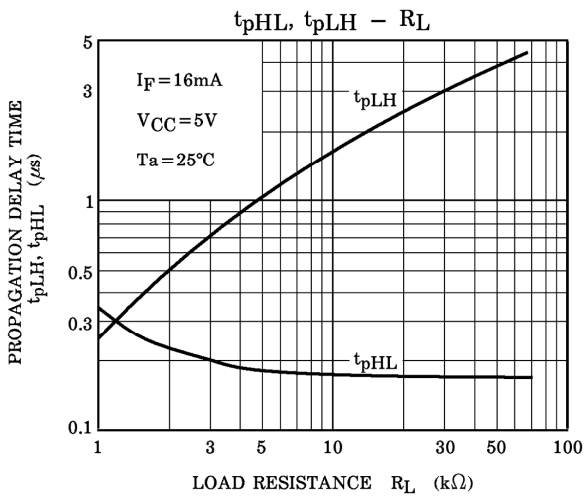
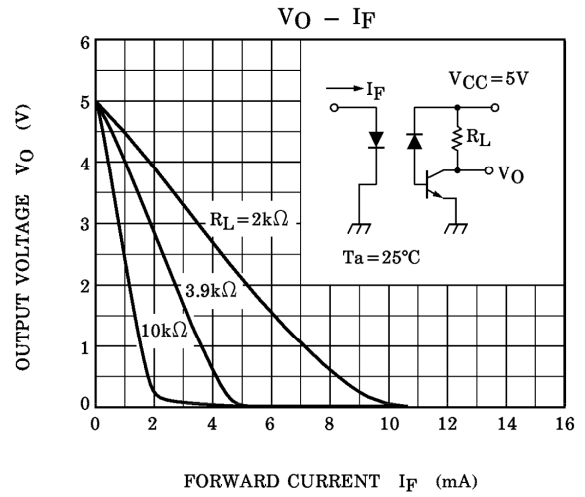
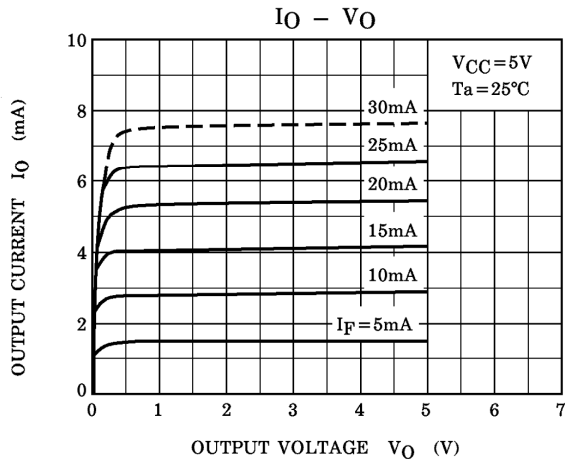


## Test Circuit 2: Common Mode Noise Immunity Test Circuit



$$CM_H = \frac{160(V)}{t_r(\mu s)}, \quad CM_L = \frac{160(V)}{t_f(\mu s)}$$





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