SMART MOSFET DRIVER

FEATURES

- **20 ns Rise and Fall Times into 1000 pF**
- **550 μA Standby Current Consumption**
- **Undervoltage Lockout Combined with First Pulse Wake-Up Feature ***
- **Cycle-by-Cycle Current Limiting**
- **Current Sense Voltage Spike Cancellation when Used with Gate Charge Recovery Circuit ***
- **Thermal Overload Protection**
- **TTL/CMOS Compatible Input**

APPLICATIONS

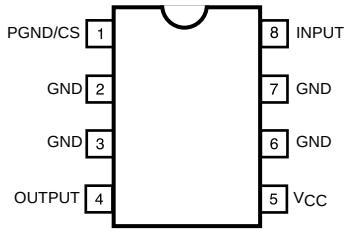
- **Driving of Power MOSFETs and IGBTs**
- **Switch Mode Power Supplies**
- **Step Motor Drivers**
- **Solenoid Drivers**

DESCRIPTION

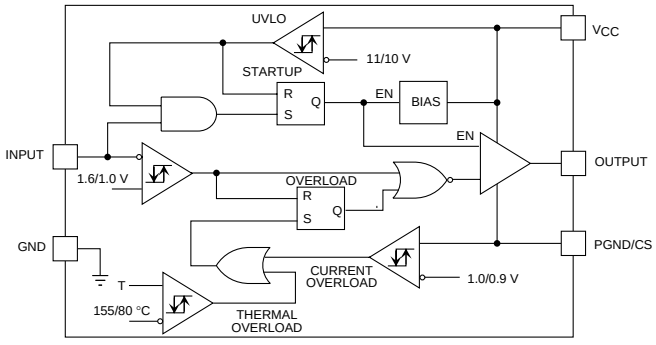
The TK75050 is a non-inverting buffer to drive high power insulated gate transistors (e.g., MOSFETs and IGBTs). The output can source or sink 2 A into a 10,000 pF equivalent load. The IC features built-in cycle-by-cycle current limiting. Its Undervoltage Lockout (UVLO) circuit is combined with a First Pulse Wake-up Feature*. The chip has thermal overload protection. Using the IC in the Gate Charge Recovery* application, the switching spike developed across the current sense resistor practically becomes negligible. Due to its low standby current and first-pulse wake-up feature, the device can be used in self-biased power supplies. The IC's high-speed cycle-by-cycle current limiting capability eliminates the short circuit runaway problem which characterizes most current-controlled converters. The IC is well suited to provide supplementary overload protection in voltage-controlled converters, too. The TK75050 is available in the widely used 8-pin DIP package.

*Toko proprietary feature: See "Application Information" section.

TK75050



BLOCK DIAGRAM



ORDERING INFORMATION

TK75050D□ □□

- Tape/Reel Code
- Temperature Code

PACKAGE CODE	EXTENDED TEMP. RANGE	TAPE/REEL CODE
D: DIP-8	I: -40 TO +85 °C	TL: Tape Left

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (Low Impedance Source) ..... 14 V
Power Dissipation TK75050D (Note 1) ..... 825 mW
Storage Temperature Range ..... -55 to +150 °C
Operating Temperature Range .....-20 to +70 °C
Extended Temperature Range ..... -40 to +85 °C
Junction Temperature ..... 150 °C
Lead Soldering Temperature (10 s) ..... 235 °C

TK75050 ELECTRICAL CHARACTERISTICS

Test conditions: V_{CC} = 12 V, $T_A = T_j$ = Full Operating Temperature Range, DC Test Setup 1, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNITS
POWER SUPPLY SECTION							
$I_{CC(STBY)}$	Supply Current (Standby), (Note 2)	V_{IN} = 0 V Before Wake-Up			550	1000	µA
$I_{CC(L)}$	Supply Current (Output LOW)	V_{IN} = 0 V After Wake-Up			17	26	mA
$I_{CC(H)}$	Supply Current (Output HIGH)	V_{IN} = 2.4 V After Wake-up			14	18	mA
$I_{CC(SD)}$	Suppy Current (Output SHUTDOWN)	Current or Thermal Overload			19	24	mA
$I_{PGND/CS}$	PGND/CS Current (Output LOW)	V_{IN} = 0 V After Wake-up			4	10	mA
UNDERVOLTAGE LOCKOUT SECTION							
$V_{CC(ON)}$	Suppy Voltage (UVLO HIGH Threshold)	V_{CC} Sweeps Upward		10.4	11.0	11.4	V
$V_{CC(OFF)}$	Suppy Voltage (UVLO LOW Threshold)	V_{CC} Sweeps Downward		9.3	10.0	10.4	V
INPUT SECTION							
$V_{IN(L)}$	Input Voltage (LOW Threshold)			0.6	1.0		V
$V_{IN(H)}$	Input Voltage (HIGH Threshold)				1.6	2.1	V
$I_{IN(L)}$	Input Current (LOW)	V_{IN} = 0 V		-250	-100		µA
$I_{IN(H)}$	Input Current (HIGH)	V_{IN} = 2.4 V			10	25	µA
$V_{IN(WU)}$	Input Voltage (Wake-up Threshold)			0.5	1.25	2.25	V
OUTPUT SECTION							
$V_{OUT(L)}$	Output Voltage (LOW)	I_{SINK} = 50 mA			0.25	0.5	V
		I_{SINK} = 1.0 A			3.0	3.8	V
$V_{OUT(H)}$	Output Voltage (HIGH)	I_{SOURCE} = 50 mA		9.7	10.5		V
		I_{SOURCE} = 1.0 A		8.0	9.5		V
$I_{OUT(MAX)}$	Maximum Output Sink or Source Current, (Note 3)	C_L = 10,000 pF			2.0		A
$I_{OUT(STBY)}$	Standby Output Pull-down Current	V_{CC} = 9 V	V_{OUT} = 8 V	1	2.5		mA
			V_{OUT} = 2 V	0.3	0.7		mA

TK75050 ELECTRICAL CHARACTERISTICS (CONT.)

Test conditions: V_{CC} = 12 V, $T_A = T_j$ = Full Operating Temperature Range, DC Test Setup 1, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
THERMAL OVERLOAD PROTECTION SECTION						
$T_{j(OFF)}$	Junction Temperature, Thermal Overload Shutdown Threshold, (Note 3)	Temperature Sweeps Upward in Normal Mode		150		° C
$T_{j(ON)}$	Junction Temperature, Turn Back to Normal Mode Threshold, (Note 3)	Temperature Sweeps Downward in Thermal Shutdown Mode		80		° C
CURRENT OVERLOAD PROTECTION SECTION						
V_{CL}	Current Sense Voltage, Current Limit Threshold	V_{CS} Sweeps Upward, T_A = 25 ° C, DC Test Setup 2	0.8	0.95	1.1	V
$V_{CL(HYST)}$	Current Sense Voltage, Current Limit Hysteresis, (Note 3)	DC Test Setup 2		100		mV
SWITCHING CHARACTERISTICS						
t_{DR}	Delay Time (RISE)	C_L = 1000 pF, AC Test Setup 3		20	45	ns
t_R	Rise Time	C_L = 1000 pF, AC Test Setup 3		20	40	ns
t_{DF}	Delay Time (FALL)	C_L = 1000 pF, AC Test Setup 3		20	45	ns
t_F	Fall Time	C_L = 1000 pF, AC Test Setup 3		20	40	ns
$t_{D(COS)}$	Delay Time, Current Overload Shutdown, (Note 3)	C_L = 1000 pF, ΔV_{CS} = 200 mV, AC Test Setup 3		120		ns

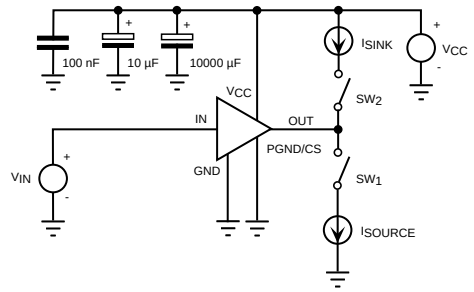
Note 1: Power dissipation is 825 mW when mounted. Derate at 6.6 mW/°C for operation above 25°C.

Note 2: Conditions for "wake-up": either 1) V_{IN} exceeds $V_{IN(H)}$, stays above $V_{IN(L)}$, and V_{CC} passes $V_{CC(ON)}$
or 2) V_{CC} exceeds $V_{CC(ON)}$, stays above $V_{CC(OFF)}$, and V_{IN} exceeds $V_{IN(H)}$.
Conditions for "standby": either 1) V_{CC} never exceeds $V_{CC(ON)}$
or 2) V_{CC} drops below $V_{CC(OFF)}$
or 3) V_{IN} never exceeds $V_{IN(H)}$.

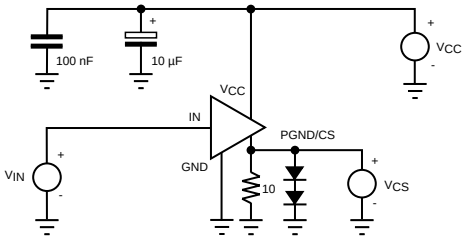
Note 3: Guaranteed by design; not 100% tested.

TEST CIRCUITS

DC TEST SETUP 1

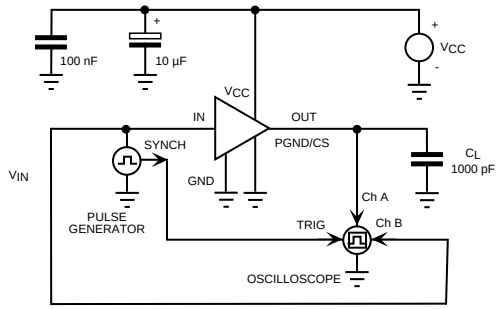


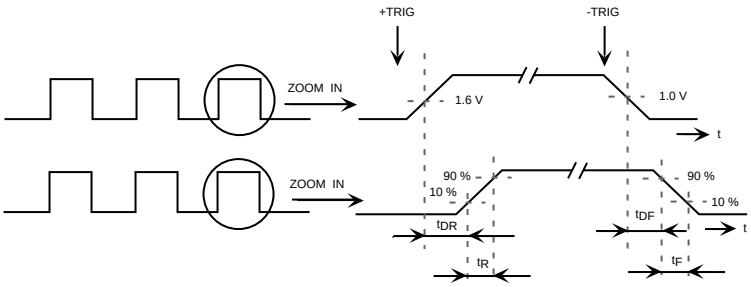
DC TEST SETUP 2



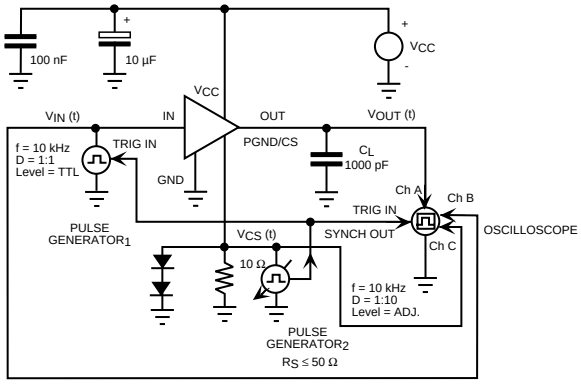
Note: SW_1 and SW_2 are open by default. To avoid excessive dissipation, they are exclusively closed only for less than 100 ms to measure the appropriate output voltages $V_{OUT(H)}$ and $V_{OUT(L)}$ at specified currents I_{SOURCE} and I_{SINK}, respectively.

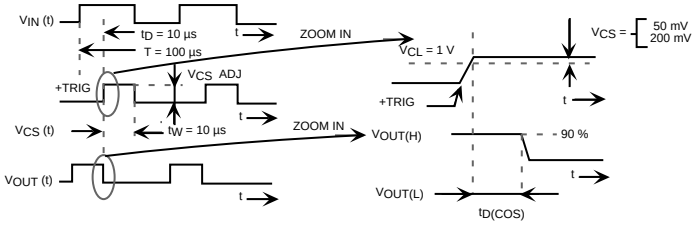
AC TEST SETUP 3





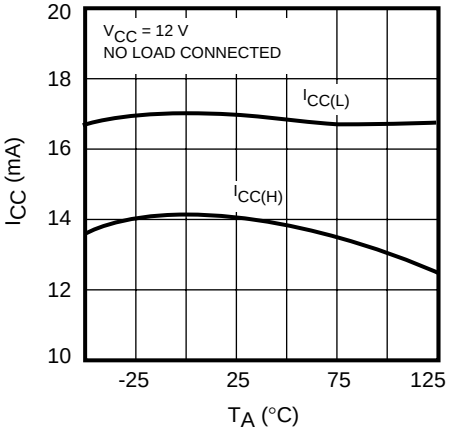
AC TEST SETUP 4



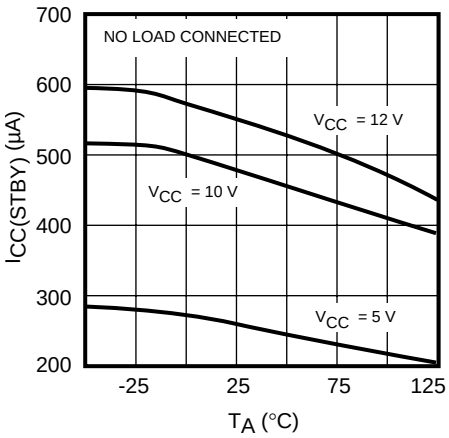


TYPICAL PERFORMANCE CHARACTERISTICS

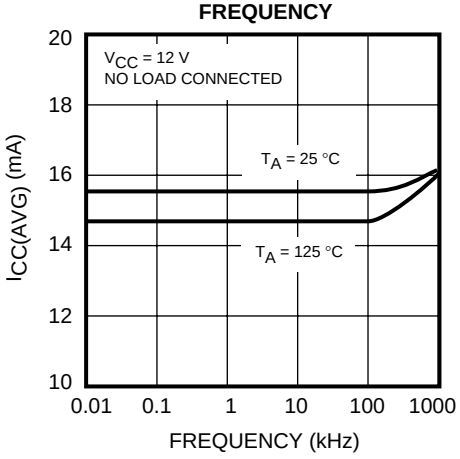
SUPPLY CURRENT vs. TEMPERATURE



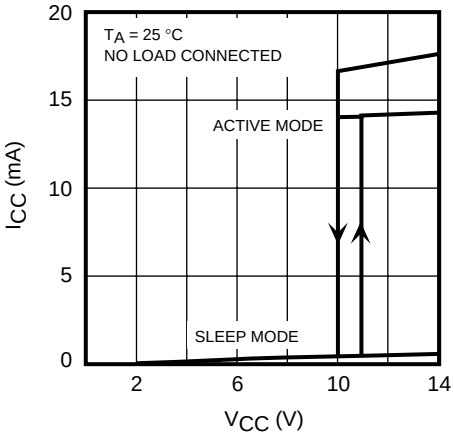
STANDBY CURRENT vs. TEMPERATURE



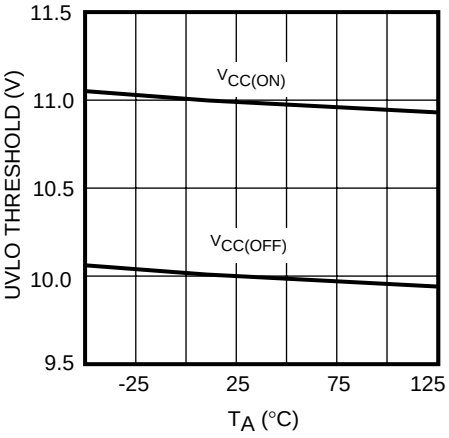
AVERAGE SUPPLY CURRENT vs. FREQUENCY



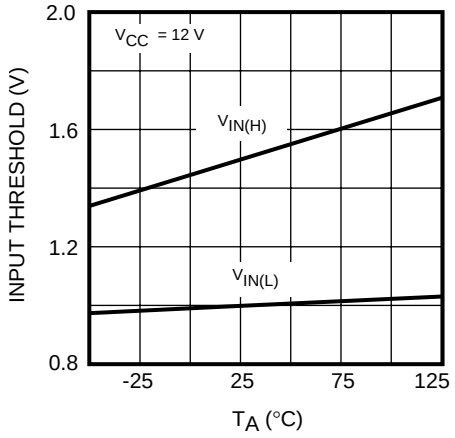
SUPPLY CURRENT vs. SUPPLY VOLTAGE



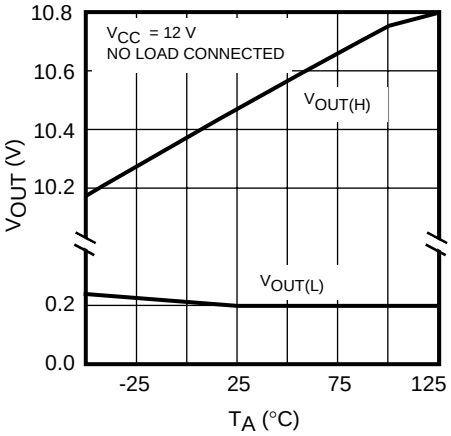
UVLO THRESHOLD vs. TEMPERATURE



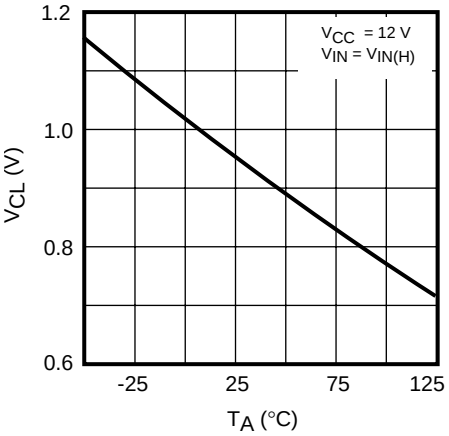
INPUT THRESHOLD vs. TEMPERATURE



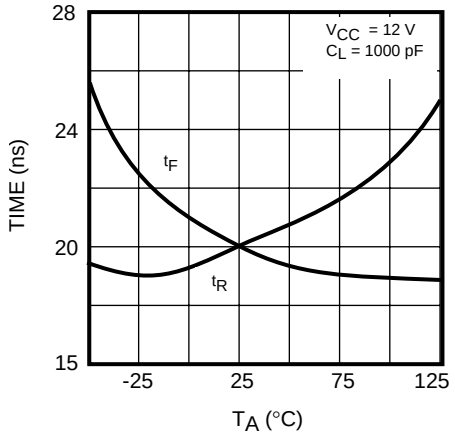
OUTPUT VOLTAGE vs. TEMPERATURE



CURRENT LIMIT THRESHOLD vs. TEMPERATURE

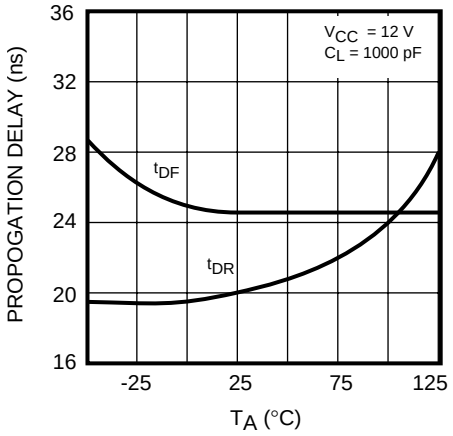


RISE AND FALL TIME vs. TEMPERATURE

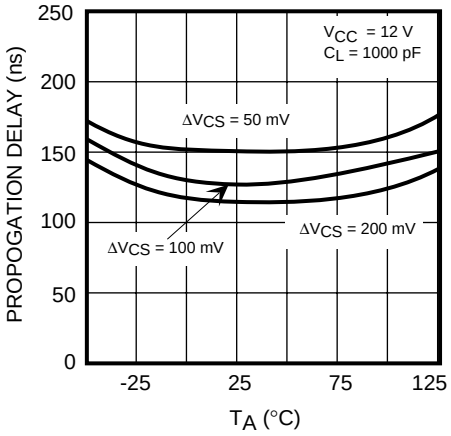


TYPICAL PERFORMANCE CHARACTERISTICS (CONT.)

PROPOGATION DELAY vs. TEMPERATURE



CURRENT OVERLOAD SHUTDOWN DELAY vs. TEMPERATURE



PIN DESCRIPTION

SUPPLY VOLTAGE PIN (V_{CC})

This pin is connected to the supply voltage. Regardless of the state of the other pins, the IC is always in a low-current standby mode when the supply voltage is below the lower threshold of the undervoltage lockout circuit. The IC enters normal mode when two conditions are met simultaneously: 1) the supply voltage exceeds the upper threshold of the undervoltage lockout circuit, and 2) a "first" pulse arrives at the input.

That first pulse "wakes up" the IC (i.e., it enables the high-speed internal circuitry). The First Pulse Wake-Up is a proprietary feature of theTK75050. The feature is proprietary, but use is granted for use with the IC. That feature is indispensable in off-line self-biased power-supply applications where the start-up current is provided by a large-value resistor connected between the rectified line and the IC (see Figure 1). Without the First Pulse Wake-up, the starting current would be equal to the normal supply current, which is prohibitively large for a self-biased start.

GROUND PIN (GND)

This pin provides ground return connection for the small-signal portion of the IC. The return of the output stage is not connected here, but to the floating power GND pin.

OUTPUT PIN

This pin drives the external MOSFET using a totem pole output stage. The peak drive source or sink current is typically 2 A into a 10,000 pF equivalent load. The UVLO circuity ensures that the high-level output voltage will never be less than about 7 V. In standby mode, the output stage is equivalent to a pull-down resistor of about 3 kΩ value, eliminating the need for an external gate to source resistor. Normally, there is no need to add a Schottky diode between the output and ground. In applications, however, with heavy capacitive load located far from the IC or when the IC drives a transformer, the Schottky diode may become necessary.

INPUT PIN

The input pin receives the signal to be buffered. The incoming signal is processed by a comparator with a 600 mV hysteresis centered around a threshold of about 1.3 V. The hysteresis ensures that noise riding on the input signal does not cause spurious response at the output.

POWER GROUND/CURRENT SENSE PIN (PGND/CS)

This pin has two distinct functions: 1) it provides a separate, fully floating return path for the turnoff drive current of the output stage and, thus, reduces the internal noise of the IC; 2) by connecting the pin to a current-sense resistor, the IC acts as a fast cycle-by-cycle current limiter.

When the voltage between the power-ground pin (PGND/CS) and the signal-ground pin (GND) exceeds the 0.95 V current-limit threshold, the drive signal is terminated for the remainder of the time while the input signal is high. Once the input signal returned to zero, the latch that stored the information about the presence of the overcurrent is reset, and the IC is ready to acquire another overcurrent event in the next cycle.

APPLICATION INFORMATION

START-UP

Figure 1 shows the application of the TK75050 smart MOSFET driver in a self-biased power supply.

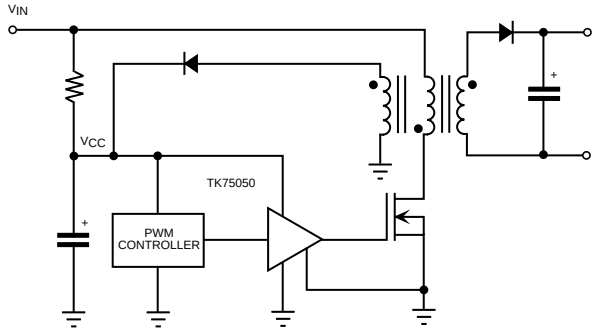


FIGURE 1: TK75050 IN A SELF-BIASED POWER SUPPLY

Figure 2 shows the typical waveforms during start-up.

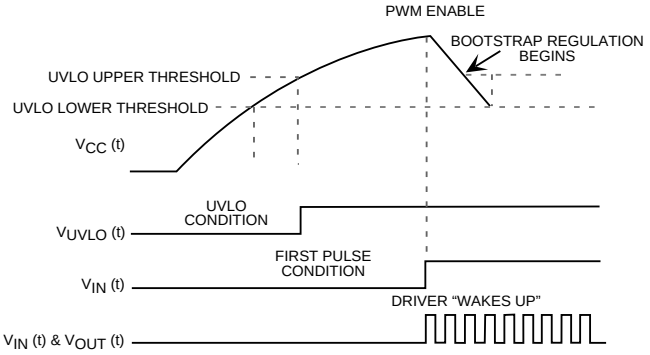
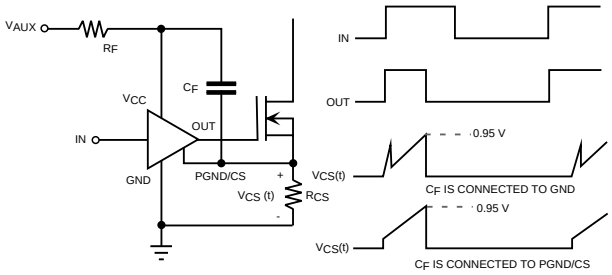


FIGURE 2: WAVEFORMS DURING START-UP

CYCLE-BY-CYCLE CURRENT LIMIT

Figure 3(a) shows how to use the TK75050 as a high-speed cycle-by-cycle current limiter. Figure 3(b) shows the waveforms. Note that the preferred connection for the bottom terminal of the filter capacitor C_F is to the PGND/CS pin and not to the GND pin. By connecting C_F to the PGND/CS pin, the capacitive feedthrough of the drive signal that would appear as a leading-edge spike in the current-sense waveform is completely eliminated. This technique, called "Gate Charge Recovery" is patented by Toko, Inc., but is granted for use with the TK75050. For a detailed description and application information of the Gate Charge Recovery technique, see the Toko application note "Application Considerations for a Smart Five-Pin MOSFET/IGBT Driver with High-Speed Current-Limit Capability."



(a) (b)

FIGURE 3: CYCLE-BY-CYCLE CURRENT LIMIT WITH THE TK75050
(a) SCHEMATIC (b) WAVEFORMS

MAIN OVERLOAD PROTECTION IN VOLTAGE-MODE-CONTROLLED CONVERTERS

Figure 4 shows the TK75050 in a voltage-mode-controlled flyback converter. In this application example, the IC provides the main overload protection.

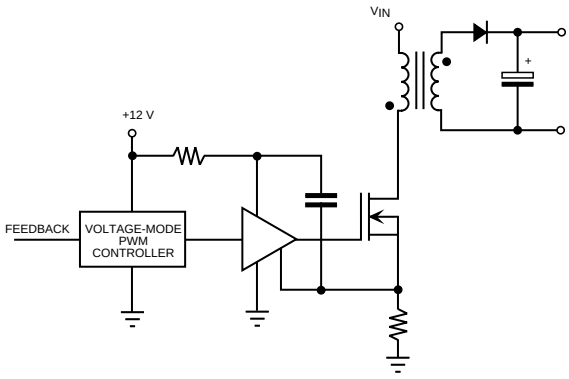


FIGURE 4: TK75050 IN A VOLTAGE-MODE-CONTROLLED CONVERTER

APPLICATION INFORMATION (CONT.)

ADDITIONAL OVERLOAD PROTECTION IN PEAK-CURRENT-CONTROLLED CONVERTERS

Figure 5 shows the TK75050 in a current-mode-controlled forward converter, with optically isolated feedback. In this application the TK75050 helps to achieve a tightly controlled current-limit-characteristic. A tight current limit cannot usually be achieved with only current-mode control due to the presence of the stabilizing ramp. The lack of the stabilizing ensures that the knee current (i.e., the output current where the limiting begins) is only slightly lower than the short-circuit current. The difference between the knee current and the short-circuit current is about one-half of the ripple current in the filter inductor. If a stabilizing ramp were added to the current-sense signal, the difference would be significantly higher.

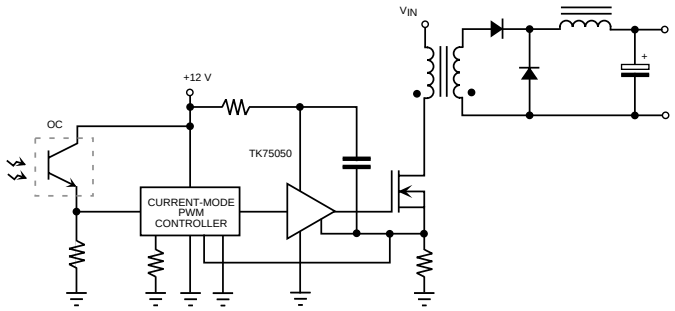


FIGURE 5: TK75050 IN A PEAK-CURRENT-CONTROLLED CONVERTER

ADDITIONAL OVERLOAD PROTECTION IN AVERAGE-CURRENT-CONTROLLED CONVERTERS

In converters with average current control the peak current information is lost and the response of the current-control loop slows down. The speed of the current-control loop may not be sufficient to provide effective protection against sudden overload or saturation of an inductor or transformer. Figure 6 shows an average-current-controlled boost converter where the TK75050 provides additional fast overload protection.

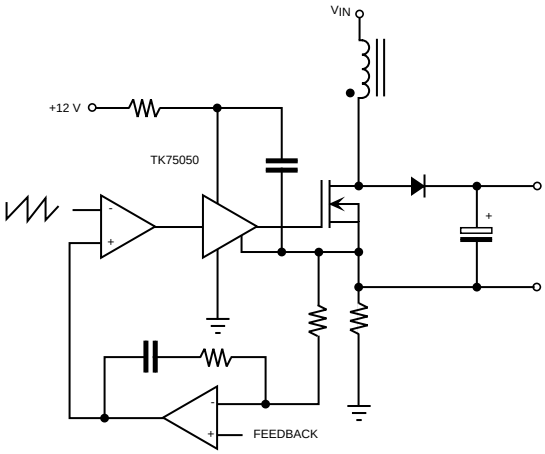


FIGURE 6: TK75050 IN A CONVERTER WITH AVERAGE CURRENT CONTROL

FLOATING DRIVE WITH OVERLOAD PROTECTION

The TK75050 can be used as a driver and current limiter for a floating power switch. Figure 7 shows the IC in a buck converter with transformer-isolated drive.

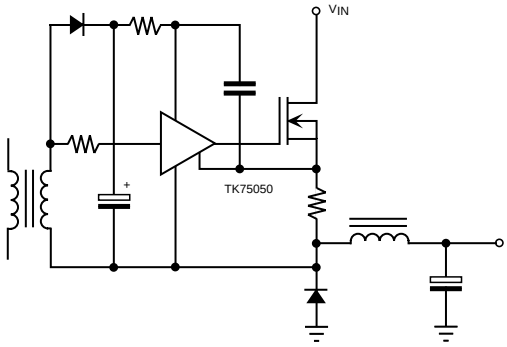


FIGURE 7: TK75050 AS A FLOATING DRIVER IN A BUCK CONVERTER

DEMO BOARD

The purpose of the board is to demonstrate the high-speed current-limit capability of Toko's TK75050 smart MOSFET driver. In the board a 2-A/500 V MOSFET switch is turned on directly (i.e., without any series impedance) into a DC-bus with up to 400 V, at a frequency of 30 kHz. By removing the short across a 3.3 µH inductor in series with the MOSFET, it is also possible to investigate the effect of the wiring inductance between the switch and the load. In

APPLICATION INFORMATION (CONT.)

addition to the short-circuit protection, the board also illustrates how to use the IC for driving and protecting a floating switch.

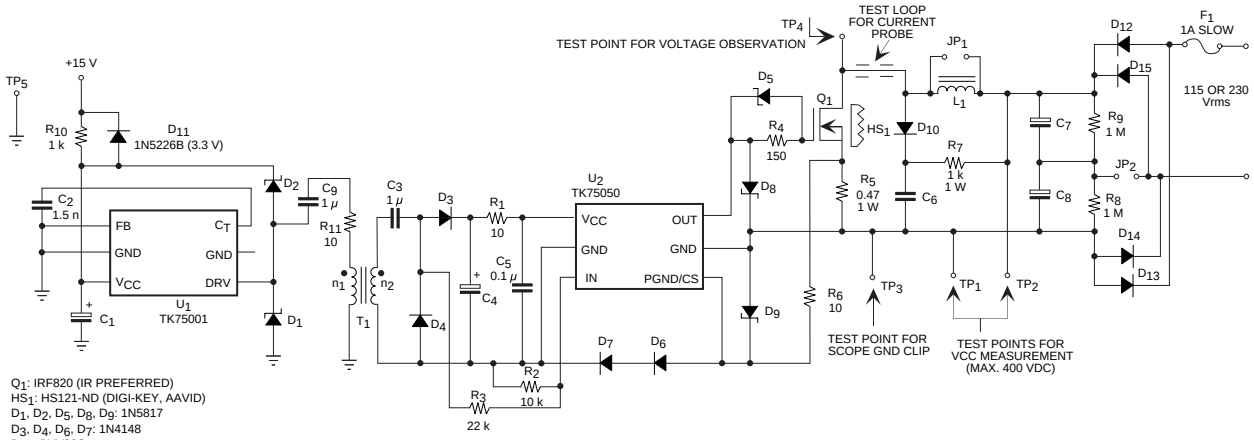
CIRCUIT SCHEMATIC

Figure 8 shows the circuit schematic. The operation is as follows: U_1, a 5-pin PWM IC (TK75001) generates a 30 kHz square-wave signal, with about 15 V peak-to-peak magnitude and 44% duty ratio. That square-wave signal is connected to the primary winding of a pulse transformer T_1 through a coupling capacitor C_9 and a small series resistor R_{11}. A voltage-doubler comprising C_3, C_4, D_3 and D_4 rectifies the transformed square wave appearing across the secondary winding of the transformer, generating a floating supply voltage of about 12 V for the MOSFET driver IC U_2 (TK75050). A drive signal is derived for U_2 from the voltage across the diode D_4 with the help of the resistive divider R_3 and R_2. The output of U_2 (pin 3) is connected to the gate of the MOSFET Q_1 through a 150 ohm resistor R_4 and a parallel diode D_5. The current of the MOSFET switch is sensed by resistor R_5. D_6 and D_7 protect the PGND/CS pin (pin 1) of U_2 from excessive voltage; D_8 and D_9 prevent the voltages of pins 3 and 1 from swinging below ground by more than 0.3 V. The MOSFET Q_1 is connected to a DC-bus through a small inductor L_1. That inductor represents the inductance of a wire connection to a load, which is at a distance of approximately 1 meter from the MOSFET. By placing a short across jumper JP_1, we can emulate the case when the free-wheeling diode in a buck or boost converter fails. If the inductor L_1 is not shorted, a clamp comprising D_{10}, C_6 and R_7 limits the drain voltage excursion of Q_1 to about 60 V above the bus voltage.

A test loop is provided for clamp-on type current probes to monitor the current in the MOSFET Q_1. Test points TP_1 through TP_4 are available for measuring the dc bus voltage and the voltage across Q_1.

The DC-bus is generated by rectifying the line voltage with a bridge rectifier (in the case of 230 V_{RMS} line) or with a voltage doubler (in the case of 115 V_{RMS} line, when jumper JP_2 is shorted). Alternatively, a DC source of not more than 400 V can be connected to the line terminals.

Notes: (1) Leave JP_2 open if you connect more than 250 V dc voltage to the line terminals, otherwise the excess voltage across C_7 or C_8 can lead to failure of the capacitor. (2) Never operate the circuit from 230 V_{RMS} line with the jumper JP_2 shorted. In such a case excess bus voltage will develop that will destroy capacitor C_7 and C_8 and transistor Q_1.



Q_1: IRF820 (IR PREFERRED)
HS_1: HS121-ND (DIGI-KEY, AAVID)
D_1, D_2, D_5, D_8, D_9: 1N5817
D_3, D_4, D_6, D_7: 1N4148
D_{10}: BYV26C
$D_{12\text{-}15}$: 1N4005
C_1, C_4: 10 μ, 25 V
C_6: 15 n, 630 V(e.g. ECQ-E6153KF, PANASONIC)
C_7, C_8: 2.2 μ, 250 V (PANASONIC SU SERIES, RADIAL, ECE-A2EU2R2)
L_1: 3.3. μ, 4 A (e.g. R622LY-3R3M, TOKO)
T_1: RM5/I, 3E1 (PHILIPS), n_1 = 40, n_2 = 46, SINGLE LAYER WINDINGS, WIRE SIZE TO FILL THE BOBBIN
MYLAR INSULATION BETWEEN LAYERS, FOR 1 kV BETWEEN PRIMARY AND SECONDARY
JP_2: OPEN AT 230 V, SHORTED AT 115 V.

FIGURE 8: CIRCUIT SCHEMATIC

APPLICATION INFORMATION (CONT.)

Figures 9 and 10 show the measured voltages across Q_1 (top trace) and the currents in Q_1 (bottom trace). Figure 9 shows the wave forms when there is no inductor in series with Q_1 (i.e., L_1 is shorted). Figure 10 shows the waveforms when there is an inductor in series with Q_1 (i.e., L_1 is not shorted). The vertical scales are 100 V/div. (top trace) and 1 A/div (bottom trace). The horizontal scales are 25 ns/div.

As can be seen, the peak currents stay below 2.5 A (Figure 9) or 2.8 A (Figure 10). Those numbers correspond to 25% or 40% overshoots above the nominal current-limit threshold of 2 A. Both figures show that the IC shuts off the MOSFET completely in less than 50 ns after the current passed the 2 A threshold. The measured average DC current consumption at a bus voltage of 400 V and a switching frequency of 30 kHz is 4.3 mA when L1 is shorted (Figure 9) and 5.3 mA when L_1 is not shorted (Figure 10).

SAFETY CONSIDERATIONS/LIABILITY DISCLAIMER

Dangerous voltages are present in the demo board. Extreme caution must be used when using and testing the circuit. Only trained personnel, experienced in working with high voltages and power, should operate it. Use an isolating transformer between the line and the circuit if any grounded instrument (including the 20 V auxiliary supply for the square-wave generator at the primary side of transformer T_1) is to be connected to the board. Note: Although the two windings of transformer T_1 are isolated from each other, the transformer is not designed to provide safety isolation between those windings.

Toko, Inc. disclaims any and all liability arising from use or misuse of the demo board described herein.

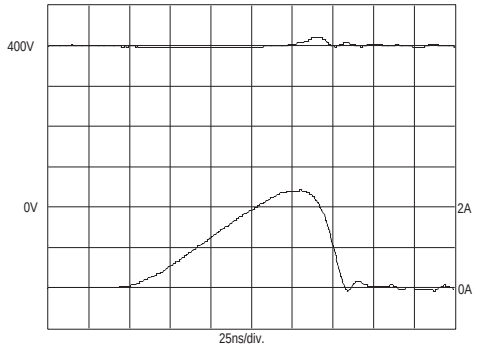


FIGURE 9

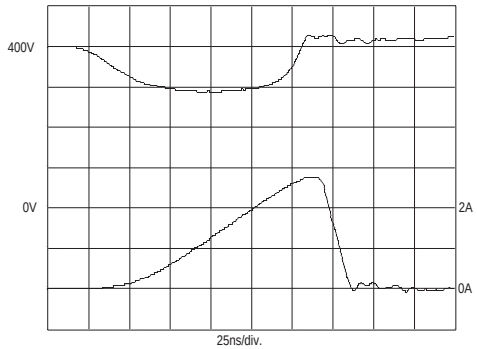
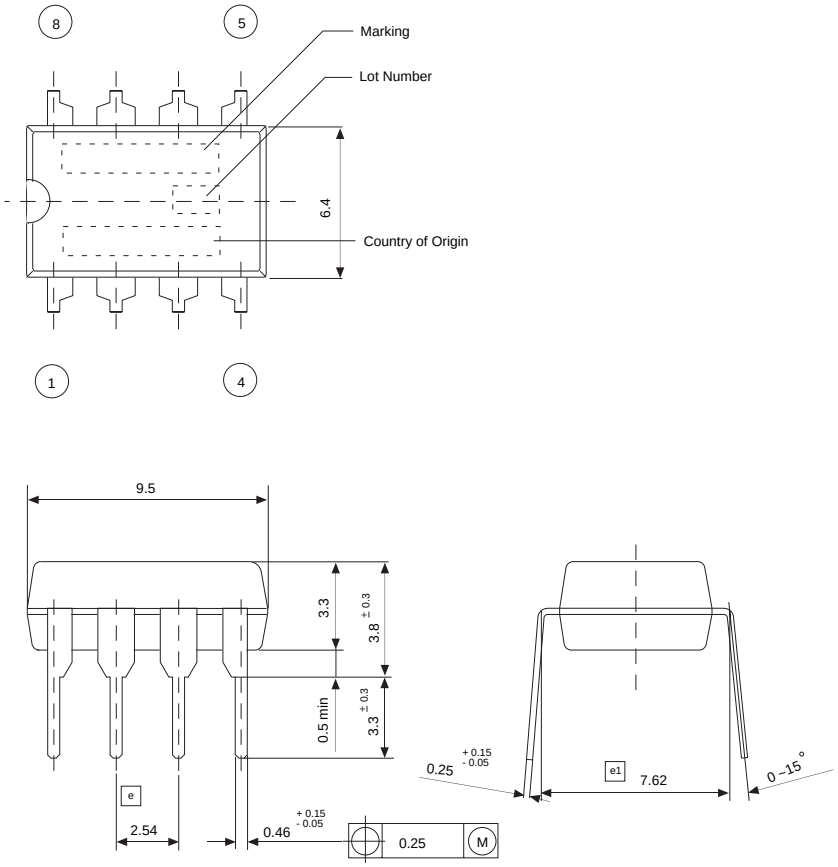


FIGURE 10

PACKAGE OUTLINE

DIP-8



Dimensions are shown in millimeters
Tolerance: x.x = ± 0.2 mm (unless otherwise specified)

Marking Information

	Marking
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