TH7108

868/915MHz
FSK/FM/ASK Transmitter

Features

- ❑ Fully integrated, PLL-stabilized VCO
- ❑ Frequency range from 850 MHz to 920 MHz
- ❑ FSK through crystal pulling allows modulation from DC to 40 kbit/s
- ❑ High FSK deviation possible for wideband data transmission
- ❑ ASK achieved by on/off keying of internal power amplifier
- ❑ FM possible with external varactor
- ❑ Wide power supply range from 2.2 V to 5.5 V
- ❑ High over-all frequency accuracy
- ❑ Very low standby current
- ❑ Adjustable output power range from -15 dBm to +1 dBm
- ❑ Adjustable current consumption from 6.2 mA to 12.5 mA
- ❑ FSK deviation and center frequency independently adjustable
- ❑ Differential output well-suited for loop antenna
- ❑ External clock available for µC drive, down to 1.9 V supply
- ❑ ”Clock only” mode
- ❑ Conforms to EN 300 220 and similar standards

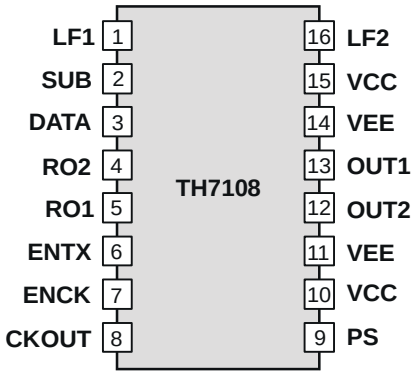
Ordering Information

Part No.	*Temperature Code*	*Package Code*
TH7108	E (-40 C° to 85 °C)	FC (QSOP16)

Application Examples

- ❑ Keyless car and central locking
- ❑ Low-power telemetry
- ❑ Alarm and security systems
- ❑ General digital data transmission
- ❑ General analog audio signal transmission

Pin Description



General Description

The TH7108 FSK/ASK/FM transmitter IC is designed for applications in the European 868MHz industrial-scientific-medical (ISM) band, according to the EN 300 220 telecommunications standard. It can also be used for any other system with carrier frequencies ranging from 850 MHz to 920 MHz (e.g. for applications in the US 915MHz ISM band).
The transmitter's carrier frequency f_c is determined by the frequency of the reference crystal f_{ref} that is used. The integrated PLL synthesizer ensures that each RF value, ranging from 850 MHz to 920 MHz, can be achieved by using a crystal with reference frequency according to: $f_{ref} = f_c/N$, where N = 32 is the PLL feedback divider ratio.

Document Content

1 Theory of Operation

1.1 General

As depicted in Fig.1, the TH7108 transmitter consists of a fully integrated voltage-controlled oscillator (VCO), a divide-by-32 divider (div32), a phase-frequency detector (PFD) and a charge pump. An external loop filter at pin LF determines the dynamic behavior of the PLL and suppresses reference spurious signals. The VCO's output signal feeds the power amplifier (PA). RF signal power P_o can be adjusted in six steps from P_o = –15 dBm to +1 dBm either by changing the value of resistor RPS or by varying the voltage V_{PS} at pin PS. The open-collector differential output (OUT1, OUT2) can be used to either directly drive a loop antenna or to be converted to a single-ended impedance by means of a balanced-to-unbalanced (balun) transformer. For maximum available output power, the differential output should be matched to a load of about 1 kΩ. Bandgap biasing ensures stable operation of the IC at a power supply range of 2.2 V to 5.5 V.

1.2 Block Diagram

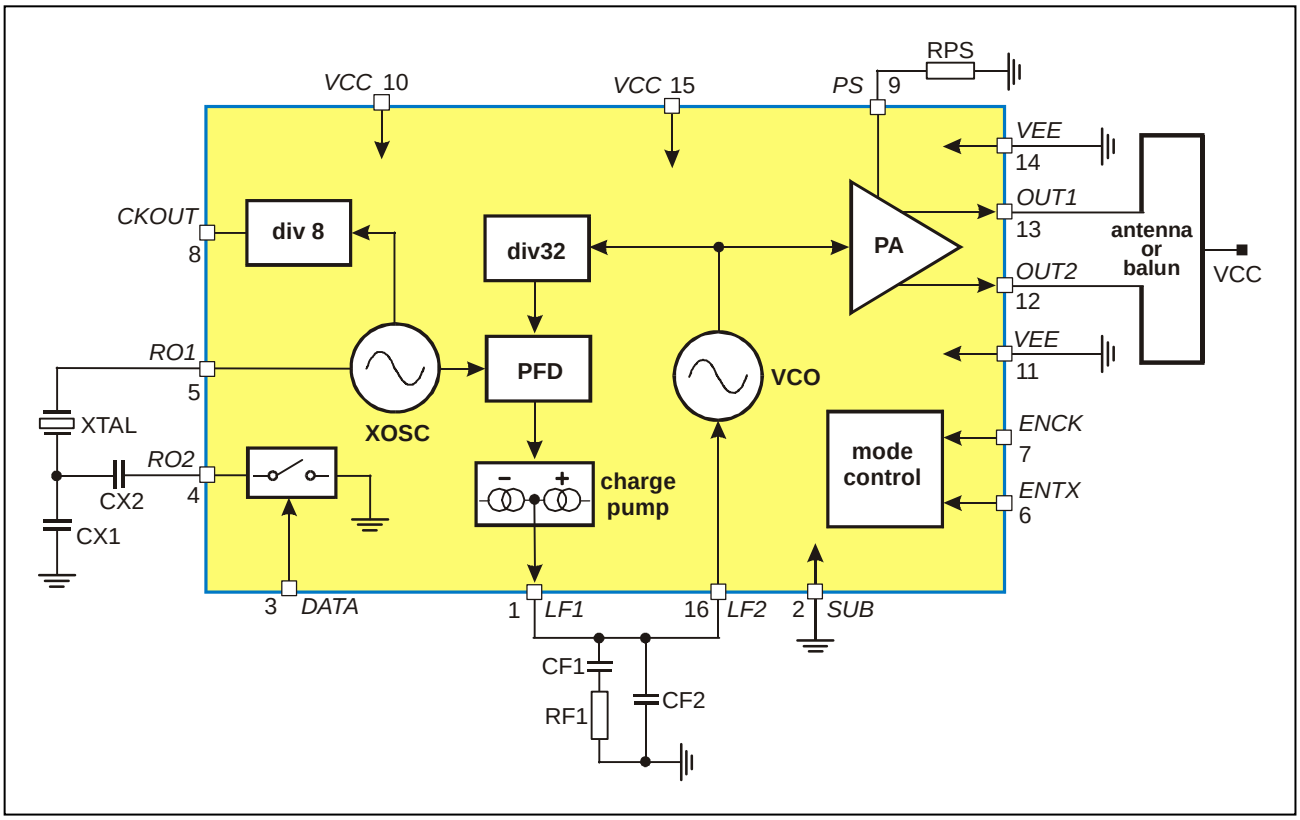


Fig. 1: Block diagram with external components

2 Functional Description

2.1 FSK Modulation

A Colpitts crystal oscillator (XOSC) is used as the reference oscillator of a phase-locked loop (PLL) synthesizer. FSK modulation is achieved by pulling the crystal (XTAL) through the data. So a CMOS-compatible data stream applied at input DATA digitally modulates the XOSC. Two external pulling capacitors CX1 and CX2 allow the FSK deviation and center frequency to be adjusted independently. At DATA = LOW CX2 is connected in parallel to CX1 leading to the low-frequency component of the FSK spectrum (f_{min}); while at DATA = HIGH CX2 is deactivated and the XOSC is set to its high frequency, leading to f_{max}.
An external reference signal can be directly AC-coupled to pin RO1. Then the TH7108 is used without an XTAL. The reference signal has to contain the FSK (or FM) and sets the carrier frequency.

2.2 Frequency Modulation

For FM operation an external varactor is required. It simply acts as a pulling capacitor connected in series to the crystal. Then the analog modulation signal, applied through a series resistor, directly modulates the XOSC.

2.3 ASK Modulation

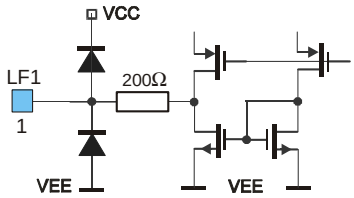
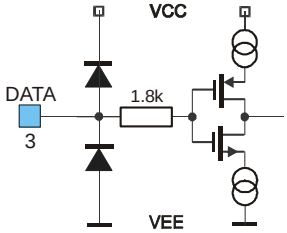
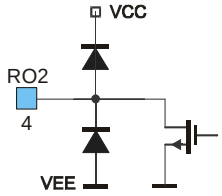
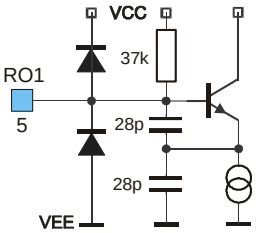
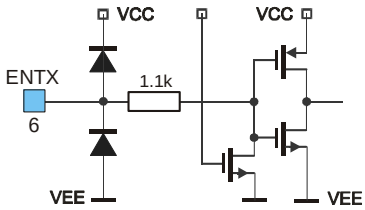
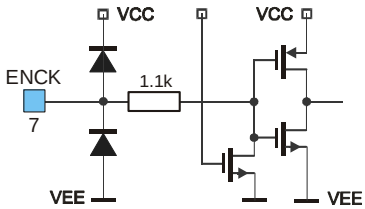
The TH7108 can be ASK-modulated by applying data directly at pin PS. This turns the PA on and off and therefore leads to an ASK signal at the output.

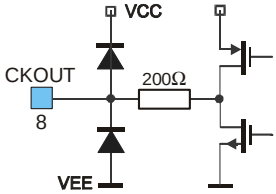
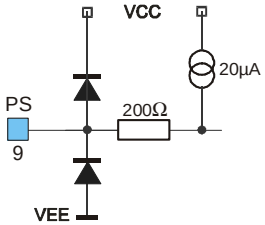
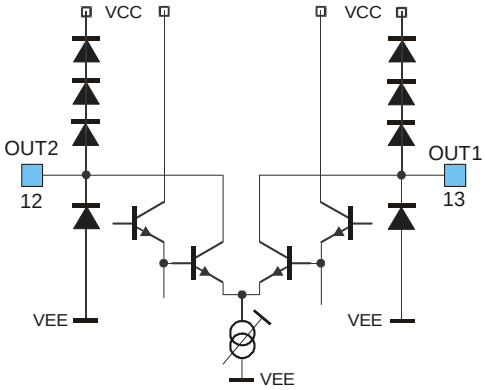
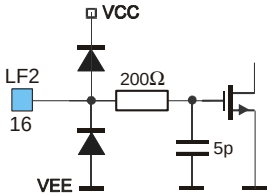
2.4 Mode Control Logic

The mode control logic allows four different modes of operation as listed in the following table. The mode control pins ENCK and ENTX are pulled-down internally. This guarantees that the whole circuit is shut down if these pins are left floating.
The clock output CKOUT can be used to drive a µC. This output can be activated by the ENCK pin as required for any specific application. Clock frequency is 1/8 of the reference crystal frequency.

ENCK	ENTX	Mode	Description
0	0	all OFF	whole circuit in standby
0	1	TX only	TX active, no clock available
1	0	clock only	TX standby and clock available
1	1	all ON	TX active and clock available

3 Pin Definition and Description

Pin No.	Name	I/O Type	Functional Schematic	Description
1	LF1	output		charge pump output, connection to loop filter
2	SUB	ground		negative power supply, substrate connection
3	DATA	input		FSK data input, CMOS-compatible
4	RO2	analog I/O		XOSC FSK pulling pin, MOS switch
5	RO1	analog I/O		XOSC connection to XTAL, Colpitts type crystal oscillator
6	ENTX	input		mode control input, CMOS-compatible with internal pull-down
7	ENCK	input		mode control input, CMOS-compatible with internal pull-down

Pin No.	Name	I/O Type	Functional Schematic	Description
8	CKOUT	output		clock output, CMOS-compatible
9	PS	analog I/O		power-select and ASK input, high-impedance comparator logic TX standby: I_{PS} = 0 TX active: I_{PS} = 20µA
10	VCC	supply		positive power supply
11	VEE	ground		negative power supply
12	OUT2	output		differential power amplifier output, open collector
13	OUT1	output		differential power amplifier output, open collector
14	VEE	ground		negative power supply
15	VCC	supply		positive power supply
16	LF2	input		VCO tuning input, connection from loop filter

4 Electrical Characteristics

4.1 Absolute Maximum Ratings

Parameter	Symbol	Condition	Min	Max	Unit
Supply voltage	V_{CC}		0	7.0	V
Input voltage	V_{IN}		-0.3	V_{CC}+0.3	V
Storage temperature	T_{STG}		-65	150	°C
Junction temperature	T_J			150	°C
Thermal Resistance	R_{thJA}			112	K/W
Power dissipation	P_{diss}			0.12	W
Electrostatic discharge	V_{ESD1}	human body model, 1)	-1.0	+1.0	kV
	V_{ESD2}	human body model, 2)	-0.75	+0.75	

1) all pins except OUT1, OUT2 2) pins OUT1, OUT2

4.2 Normal Operating Conditions

Parameter	Symbol	Condition		Min	Max	Unit
Supply voltage	V_{CC}			2.2	5.5	V
Operating temperature	T_A			-40	85	°C
Input low voltage CMOS	V_{IL}	ENTX, ENCK, DATA pins			0.3*V_{CC}	V
Input high voltage CMOS	V_{IH}	ENTX, ENCK, DATA pins		0.7*V_{CC}		V
XOSC frequency	f_{ref}	set by the crystal		26.5	28.75	MHz
VCO frequency	f_c	$f_c = 32 \bullet f_{ref}$		850	890	MHz
			$T_A < 70°C$, $V_{CC} \geq 2.5V$		920	
Clock frequency	f_{clk}	$f_c = f_{ref} / 8$		3.3	3.6	MHz
FSK deviation	Δf_{FSK}	depends on CX1, CX2 and crystal parameter		±5	±100	kHz
Data rate FSK	R_{FSK}	NRZ			40	kbit/s
FM deviation	Δf_{FM}	adjustable with V1 and CX3			±6	kHz
Modulation frequency FM	f_{mod}				5	kHz
Data rate ASK	R_{ASK}	NRZ			40	kbit/s

4.3 Crystal Parameters

Parameter	Symbol	Condition	Min	Max	Unit
Crystal frequency	f_0	fundamental mode, AT	26.5	28.75	MHz
Load capacitance	C_L		10	15	pF
Static capacitance	C_0			7	pF
Resonance resistance	R_1			40	Ω
Spurious response	a_{spur}	only required for FSK		-10	dB

4.4 DC Characteristics

all parameters under normal operating conditions, unless otherwise stated;
typical values at T_A = 23 °C and V_{CC} = 3 V

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Standby current	I_{SBY}	ENCK=0, ENTX=0		0.05	0.1	µA
Clock only current	I_{CLK}	ENCK=1, ENTX=0	0.7	0.9	1.6	mA
Operating current	I_{CC}	ENCK=x, ENTX=1, RPS=56kΩ	7	9.5	14	mA
Input current	I_{IN}	DATA=x, ENCK=0, ENTX=0	-1		1	µA
Pull down current	I_{PD}	ENCK=1, ENTX=1	3	8	30	µA
Pull up current	I_{PS}	ENCK=1, ENTX=1	14	20	24	µA
MOS switch On resistance	R_{ON}	DATA=0, ENTX=1	10	25	80	Ω

4.5 AC Characteristics

all parameters under normal operating conditions, unless otherwise stated;
typical values at T_A = 23 °C and V_{CC} = 3 V;
ENCK = 1, ENTX = 1, RPS = 56 kΩ, f_c = 868.3 MHz, test circuit shown in Fig. 2

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Output power	P_o			-2		dBm
Reference spurs	P_{ref}	@ $f_c \pm f_{ref}$		-44		dBm
Clock spurs	P_{clk}	@ $f_c \pm f_{clk}$		-44		dBm
Harmonic content	P_{harm}	@ $2f_c$, $3f_c$, $4f_c$		-40		dBm
Spurious output signal	P_{off}	$V_{PS} \leq 0.1V$		-60		dBm
Phase noise	PN	@ $f_c \pm 200kHz$		-82	-78	dBc/Hz
VCO gain	K_{VCO}			300		MHz/V
Charge pump current	I_{CP}			±260		µA
Clock voltage swing	V_{CKOUT}	C_{load} = 5pF		2		V_{pp}
Start-up time	t_{on}	from ”all OFF” to any other mode		1.0	1.2	ms

4.6 Output Power Selection

typical values at T_A = 23 °C and V_{CC} = 3 V:
ENCK = 1, ENTX = 1, f_c = 868.3 MHz, test circuit shown in Fig. 2

RPS / kΩ	≥ 68	56	47	39	27	15
V_{PS}/ V	**≥ 2**	**1.1**	**0.9**	**0.7**	**0.5**	**0.3**
I_{cc} / mA	12.5	9.5	8.5	7.8	7.0	6.2
P_o / dBm	1	-2	-5	-8	-10	-15
P_{harm} / dBm	≤-40	≤-40	≤-40	≤-45	≤-45	≤-50

5 Test Circuit

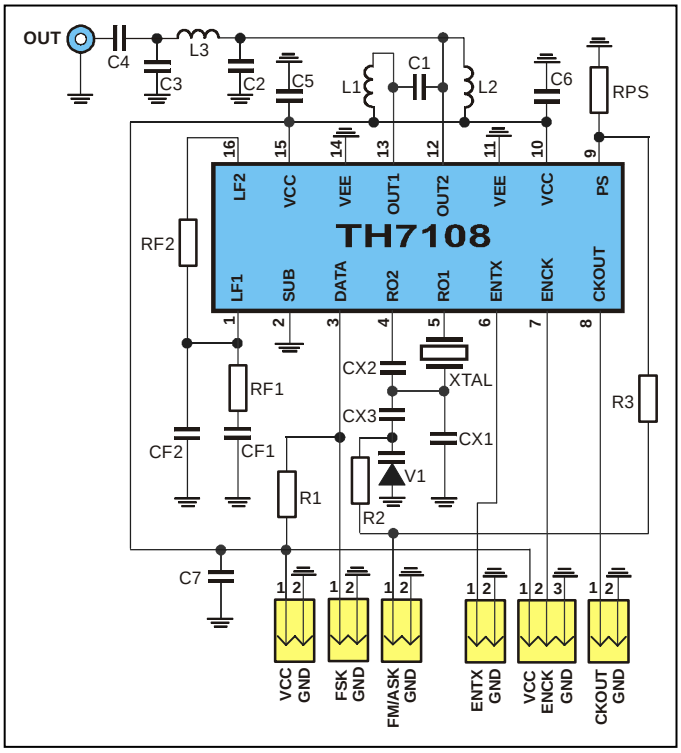


Fig. 2: Test circuit for FSK, ASK and FM; with 50Ω matching network

5.1 Test circuit component list (Fig. 2)

Part	Size	Value	Tolerance	Description
CF1	0603	5.6 nF	±10%	loop filter capacitor
CF2	0603	27 pF	±10%	loop filter capacitor
$CX1_{\_FSK}$	0603	56 pF	±5%	XOSC capacitor for FSK (Δf = ±30 kHz), **note 1**
$CX1_{\_ASK}$	0603	18 pF	±5%	XOSC capacitor for ASK, trimmed to f_C, **note 1**
CX2	0603	1 nF	±5%	XOSC capacitor (for FSK only), **note 1**
CX3	0603	1 nF	±10%	XOSC capacitor (for FM only)
C1	0603	0.47 pF	±5%	impedance matching capacitor
C2	0805	1.0 pF	±5%	impedance matching capacitor
C3	0805	1.8 pF	±5%	impedance matching capacitor
C4	0603	150 pF	±5%	impedance matching capacitor
C5	0603	330 pF	±10%	blocking capacitor
C6	0603	330 pF	±10%	blocking capacitor
C7	1206	220 nF	±20%	blocking capacitor
L1	0603	10 nH	±5%	impedance matching inductor
L2	0603	15 nH	±5%	impedance matching inductor
L3	0805	15 nH	±5%	impedance matching inductor
RF1	0805	1.6 kΩ	±10%	loop filter resistor
RF2	0805	2.0 kΩ	±10%	loop filter resistor
RPS	0805	56 kΩ	±10%	power-select resistor
R1	0805	470 kΩ	±10%	optional pull-up resistor
R2	0805	30 kΩ	±10%	varactor bias resistor, (for FM only)
R3	0805	0 Ω	±10%	ASK jumper, (for ASK only)
V1	SOD323	BB535		varactor diode (for FM only)
XTAL	HC49/S	27.1344 MHz fundamental wave	±30ppm calibr. ±30ppm temp.	crystal, C_{load} = 12 pF to 15 pF, $C_{0,\,max}$ = 7 pF, $R_{m,\,max}$ = 40 Ω

Note 1: value depends on crystal parameters

6 Spectrum Plots

All plots depict TH7108's typical performance at V_{CC} = 3.0 V and T_A = 23 °C, derived with the test circuit shown in Fig. 2.

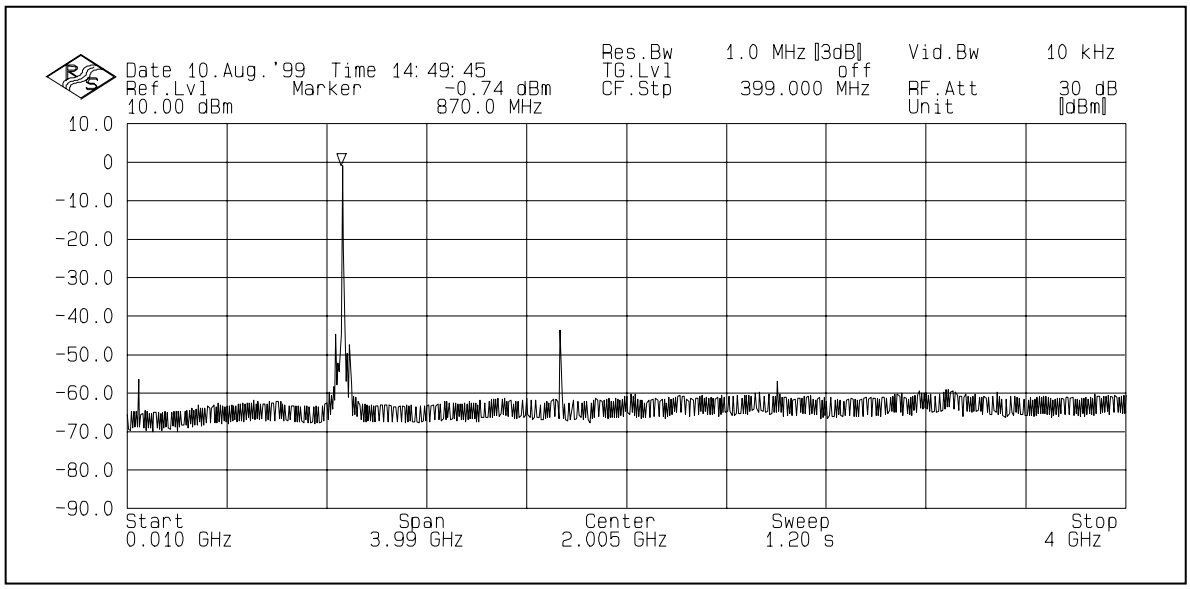


Fig. 3: RF output signal and spurious emissions, CW mode (DATA = HIGH)

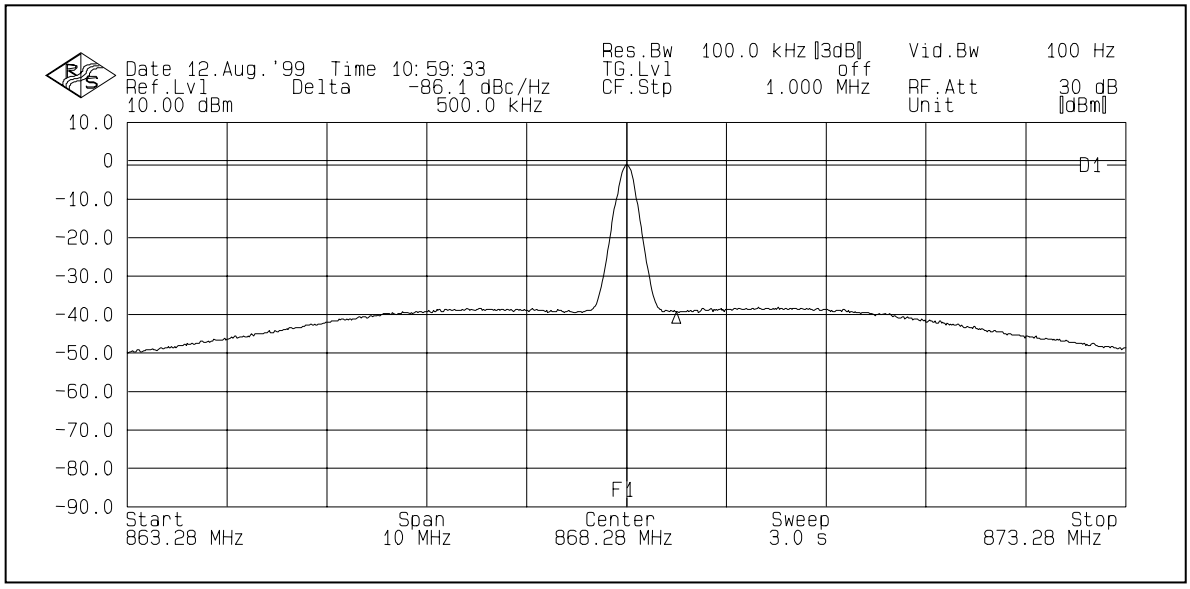


Fig. 4: Single-sideband phase noise at 500 kHz offset, CW mode (DATA = HIGH)

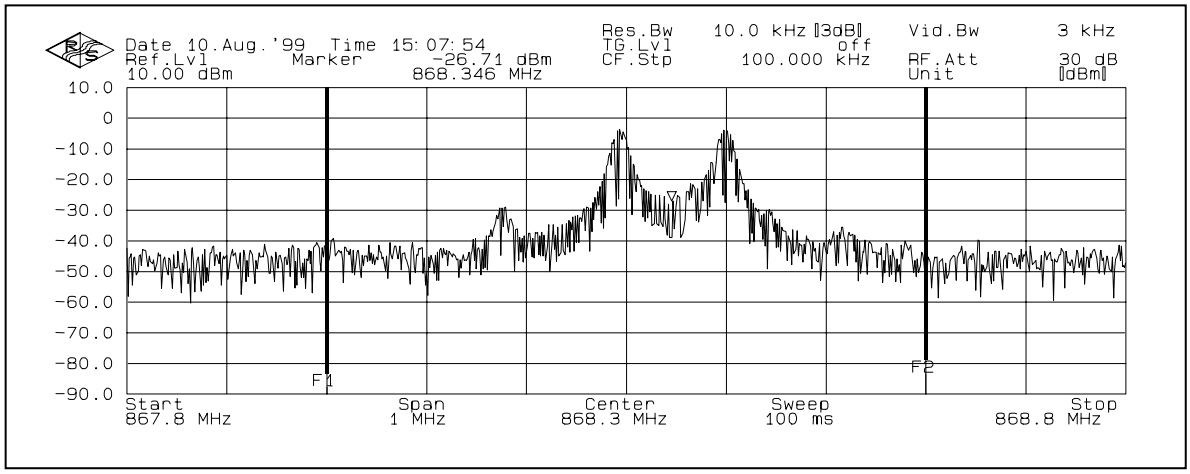


Fig.5: FSK modulation with R_{FSK} = 6.6 kbit/s NRZ

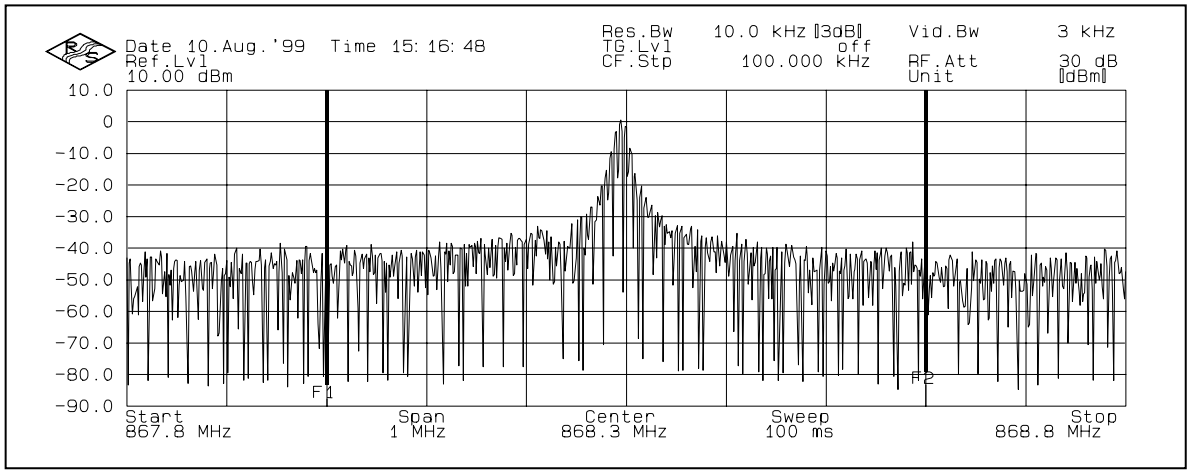


Fig. 6: ASK modulation with R_{ASK} = 4 kbit/s NRZ

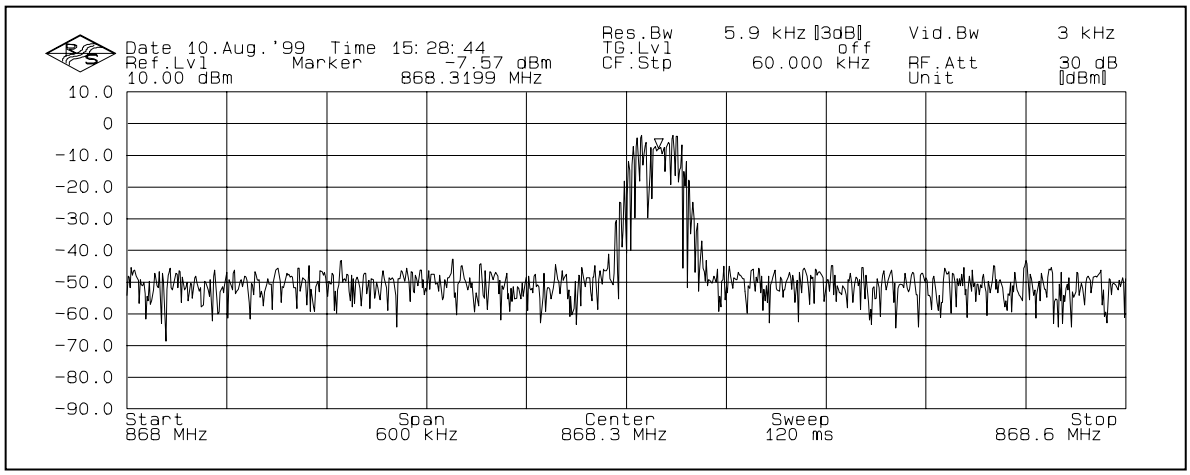


Fig. 7: FM with f_{mod} = 2 kHz, FM input signal with 1 V_{pp} around 1.5 V_{DC}, DATA = HIGH

7 Package Information

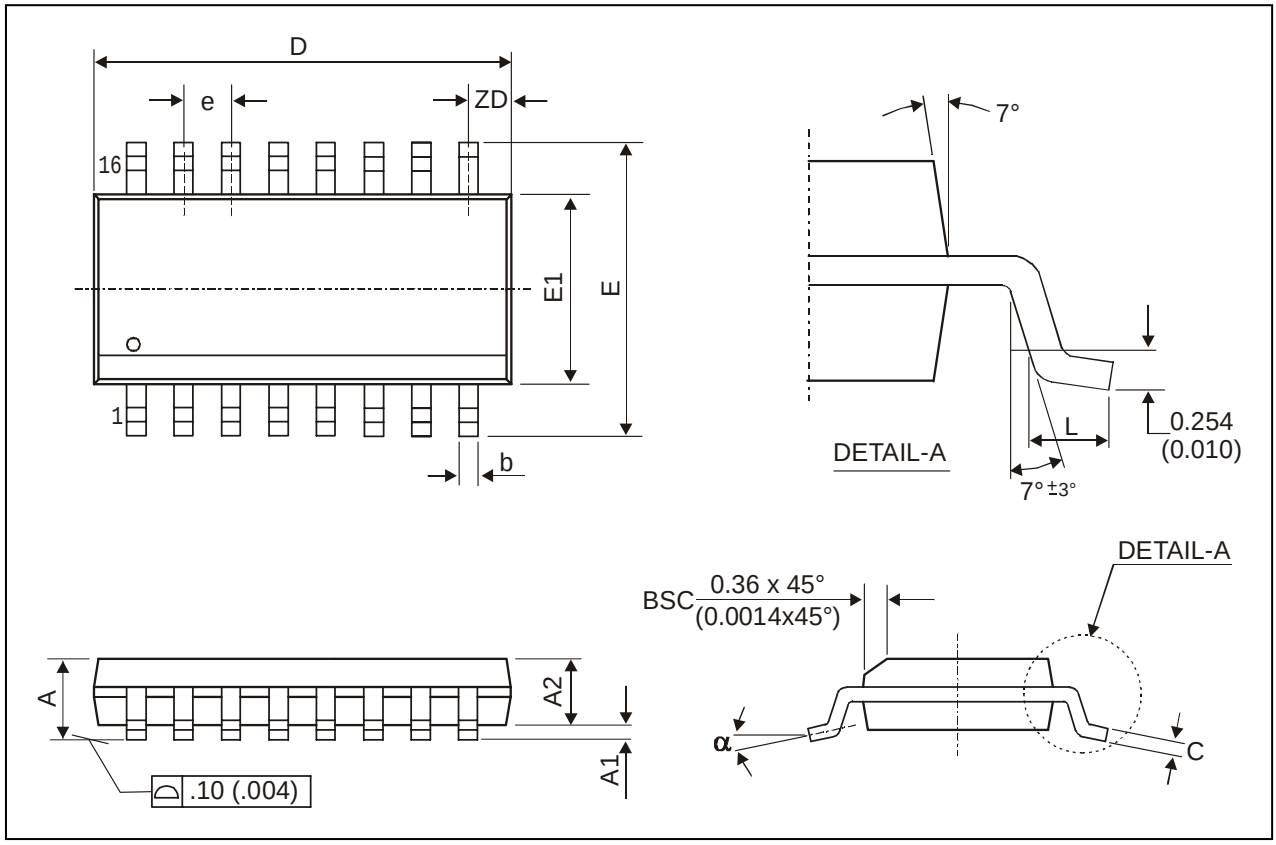


Fig. 8: QSOP16 (Quarter size Small Outline Package)

all Dimension in mm, coplanarity < 0.1mm												
	D	**E1**	**E**	**A**	**A1**	**A2**	**e**	**b**	**ZD**	**C**	**L**	**α**
min	4.80	3.81	5.79	1.35	0.10	1.37	0.635	0.20	0.230	0.19	0.40	0°
max	4.98	3.99	6.20	1.75	0.25	1.50		0.30		0.25	1.27	8°
all Dimension in inch, coplanarity < 0.004”												
min	0.189	0.150	0.228	0.0532	0.0040	0.054	0.025	0.008	0.009	0.075	0.016	0°
max	0.196	0.157	0.244	0.0688	0.0098	0.059		0.012		0.098	0.050	8°

8 Reliability Information

Melexis devices are classified and qualified regarding suitability for infrared, vapor phase and wave soldering with usual (63/37 SnPb-) solder (melting point at 183degC).
The following test methods are applied:

- IPC/JEDEC J-STD-020A (issue April 1999)
  Moisture/Reflow Sensitivity Classification For Nonhermetic Solid State Surface Mount Devices
- CECC00802 (issue 1994)
  Standard Method For The Specification of Surface Mounting Components (SMDs) of Assessed Quality
- MIL 883 Method 2003 / JEDEC-STD-22 Test Method B102
  Solderability

For all soldering technologies deviating from above mentioned standard conditions (regarding peak temperature, temperature gradient, temperature profile etc) additional classification and qualification tests have to be agreed upon with Melexis.

The application of Wave Soldering for SMD's is allowed only after consulting Melexis regarding assurance of adhesive strength between device and board.

For more information on manufacturability/solderability see quality page at our website:
http://www.melexis.com/

9 ESD Precautions

Electronic semiconductor products are sensitive to Electro Static Discharge (ESD).
Always observe Electro Static Discharge control procedures whenever handling semiconductor products.

Your Notes

10 Disclaimer

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