TH7108

868/915MHz FSK/ASK/FM Transmitter

Description

The TH7108 FSK/ASK/FM transmitter IC is designed for applications in the European 868MHz short range devices (SRD) band, according to the EN 300 220 telecommunications standard. It can also be used for any other system with carrier frequencies ranging from 700 to 1000 MHz (e.g. for applications in the US 915MHz ISM band). The transmitter's carrier frequency f_c is determined by the frequency of the reference crystal f_{ref} that is used. The integrated PLL synthesizer ensures that each RF value, ranging from 700 to 1000 MHz, can be achieved by using a crystal with reference frequency according to: $f_{ref} = f_c/N$, where N = 32 is the PLL feedback divider ratio.

Features

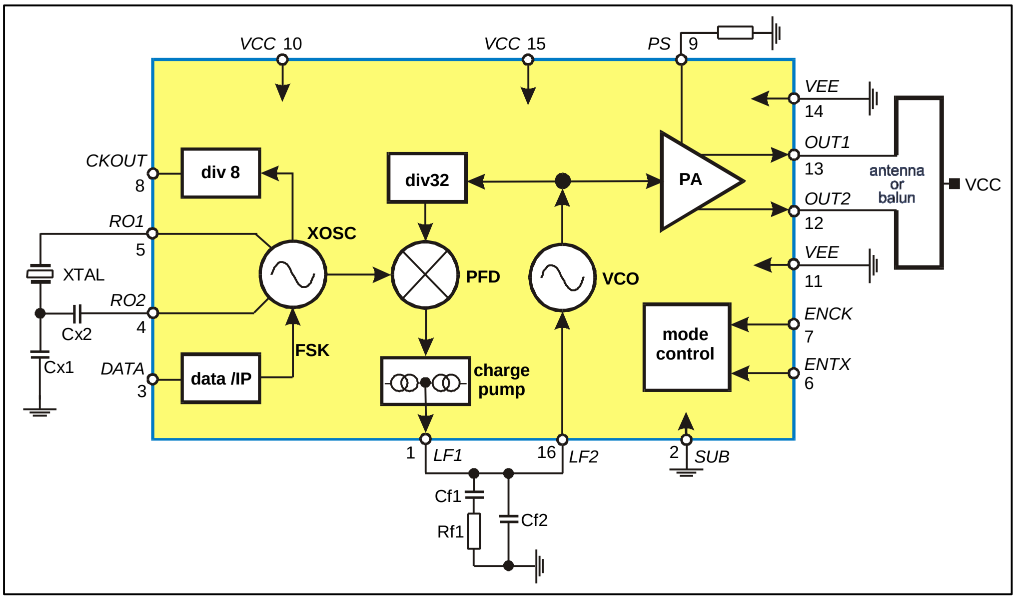
- ❑ fully integrated, PLL-stabilized VCO
- ❑ FSK through crystal pulling allows modulation from DC to 20 kbit/s
- ❑ high deviation possible for wideband data transmission
- ❑ ASK achieved by on/off keying of internal power amplifier
- ❑ FM possible with external varactor
- ❑ wide power supply range from 2.1 to 5.5 V
- ❑ flexible frequency range from 700 to 1000 MHz
- ❑ high over-all frequency accuracy
- ❑ adjustable output power range from -12 to +3 dBm
- ❑ adjustable current consumption from 6 to 12.5 mA
- ❑ deviation and center frequency independently adjustable
- ❑ very low standby current
- ❑ differential output well-suited for loop antenna
- ❑ external clock available for µC drive, down to 1.9 V supply
- ❑ "clock only" mode
- ❑ conforms to EN 300 220 standard

Applications

- ❑ keyless car security and central locking
- ❑ low power telemetry
- ❑ alarm systems
- ❑ general digital data transmission
- ❑ general analog audio signal transmission

Block Diagram with External Components

Fig. 1: TH7108 block diagram



Theory of Operation

FSK Modulation

A Colpitts crystal oscillator (XOSC) is used as the reference oscillator of a phase-locked loop (PLL) synthesizer. FSK modulation is achieved by pulling the crystal (XTAL) through the data. So a CMOS-compatible data stream applied at input DATA digitally modulates the XOSC. Two external pulling capacitors C_{x1} and C_{x2} allow the FSK deviation and center frequency to be adjusted independently. At DATA = LOW C_{x2} is connected in parallel to C_{x1} leading to the low-frequency component of the FSK spectrum (f_{min}); while at DATA = HIGH C_{x2} is deactivated and the XOSC is set to its high frequency, leading to f_{max}.

An external reference signal can be directly AC-coupled to pin RO1. Then the TH7108 is used without an XTAL. The reference signal has to contain the FSK (or FM) and sets the carrier frequency.

ASK Modulation

The TH7108 can be ASK-modulated by applying data directly at pin PS. This turns the PA on and off and therefore leads to an ASK signal at the output.

Frequency Modulation (FM)

For FM operation an external varactor is required. It simply acts as a pulling capacitor connected in series to the crystal. Then the analog modulation signal, applied through a series resistor, directly modulates the XOSC.

General

Other parts of the TH7108 transmitter are the fully integrated voltage-controlled oscillator (VCO), the divide-by-32 divider (div32), the phase-frequency detector (PFD) and the charge pump. An external loop filter between pins LF1 and LF2 determines the dynamic behaviour of the PLL and suppresses reference spurious signals. The VCO's output signal feeds the power amplifier (PA). RF signal power P_o can be adjusted in six steps from P_o = –12 to +3 dBm either by changing the value of resistor R_{ps} or by varying the voltage V_{ps} at pin PS. The open-collector differential output (OUT1, OUT2) can be used to either directly drive a loop antenna or to be converted to a single-ended impedance by means of a balanced-to-unbalanced (balun) transformer. For maximum available output power, the differential output should be matched to a load of approx. 0.5 to 1.5 kΩ.

Bandgap biasing ensures stable operation of the IC at a power supply range of 2.1 to 5.5 V. The mode control logic allows four different modes of operation as listed in the following table. The mode control pins ENCK and ENTX are internally terminated to pull-down and pull-up resistors, respectively. This guarantees that the whole circuit is shut down if these pins are left floating.

ENCK	ENTX	Mode	Description
0	0	all OFF	whole circuit in standby
0	1	TX only	TX functionality only, no clock available
1	0	clock only	TX in standby and clock available
1	1	all ON	TX functional and clock available

The clock output CKOUT can be used to drive a µC. This output can be activated by the ENCK pin as required for any specific application. Clock frequency is 1/8 of the reference crystal frequency.

Electrical Characteristics

Absolute Maximum Ratings

Parameter	Symbol	Condition	Min	Max	Unit
supply voltage	V_{cc}		-0.3	7.0	V
input voltage	V_{in}	@ DATA, ENCK, ENTX	-0.3	VCC+0.3	V
input current	I_{in}	@ DATA, ENCK, ENTX	-1.0	1.0	mA
storage temperature	T_{str}		-40	150	°C

Operating Conditions

Parameter	Symbol	Min	Max	Unit
supply voltage	V_{cc}	2.1	5.5	V
ambient temperature	T_a	-40	85	°C
VCO frequency	f_c	700	1000	MHz
XOSC frequency	f_{ref}	25	32	MHz
clock frequency	f_{clk}	3	4	MHz

DC Characteristics

T_a = -40 to +85 °C,
V_{cc} = 2.1 to 5.5 V,
typical values at T_a = 23 °C and V_{cc} = 3 V

Parameter	Symbol	Condition	Min	Typ	Max	Unit
standby current	I_{stb}	ENCK=0, ENTX=0		< 0.1	0.1	µA
clock only current	I_{clk}	ENCK=1, ENTX=0	0.7	0.9	1.1	mA
operating current	I_{cc}	ENCK=1, ENTX=1, R_{ps}=47kΩ	7	9	10	mA
input HIGH voltage	V_{HIGH}	@ DATA, ENCK, ENTX	0.7*V_{cc}		V_{cc}+0.3	V
input LOW voltage	V_{LOW}	@ DATA, ENCK, ENTX	-0.3		0.3*V_{cc}	V
input current @ V_{LOW}<V_{In}<V_{HIGH}	I_{in}	@ DATA, ENCK, ENTX	-10		10	µA

AC Characteristics

T_a = -40 to +85 °C,
V_{cc} = 2.1 to 5.5 V,
typical values at T_a = 23 °C and V_{cc} = 3 V

(ENCK = 1 ENTX = 1, R_{ps}=47 kΩ, f_c = 868.35 MHz, test circuit shown in **Fig. 2**)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
output power	P_o	DATA = HIGH		-1		dBm
max. data rate at FSK	R_{FSK}			25		kbit/s
FSK deviation	Δf_{FSK}	adjustable with C_{x1}, C_{x2},, ref. to Fig. 2		±30		kHz
max. data rate at ASK	R_{ASK}	DATA = LOW		40		kbit/s
max. modulation frequency at FM	f_{mod}	DATA = HIGH		20		kHz
FM deviation	Δf_{FM}	adjustable with varactor and V_{FM}		±12		kHz
reference spurs	P_{ref}	@ $f_c \pm f_{ref}$		-40		dBm
clock spurs	P_{clk}	@ $f_c \pm f_{clk}$		-40		dBm
harmonic content	P_{harm}			-55		dBm
phase noise	L	DATA = HIGH @ $f_c \pm$ 500kHz		-87		dBc/Hz
VCO gain	k_{VCO}			300		MHz/V
charge pump current	I_{CP}			±260		µA
clock volt. swing	V_{CKOUT}	C_{load} = 5pF		1.8		V_{pp}
start-up time	t_{on}	from "all OFF" to any other mode		0.7		ms

Output Power Selection

typical values at T_a = 23 °C and V_{cc} = 3 V,

(ENCK = 1, ENTX = 1, f_c = 868.35 MHz, test circuit shown in **Fig. 2**, C2 and C3 to adjust for P_o and P_{harm})

R_{ps} / kW	**^{3} 68**	**56**	**47**	**39**	**27**	**15**
V_{ps} / V	**^{3} 2**	**1.2**	**0.9**	**0.7**	**0.5**	**0.3**
I_{cc} / mA	12.5	9.5	8.5	6.5	5.8	5.0
P_o / dBm	3.0	0.5	-1.0	-4.0	-8.0	-12.0
P_{harm}/dBm	≤-36	≤-40	≤-40	≤-45	≤-45	≤-50
C2 / pF	TBD	TBD	TBD	TBD	TBD	TBD
C3 / pF	TBD	TBD	TBD	TBD	TBD	TBD

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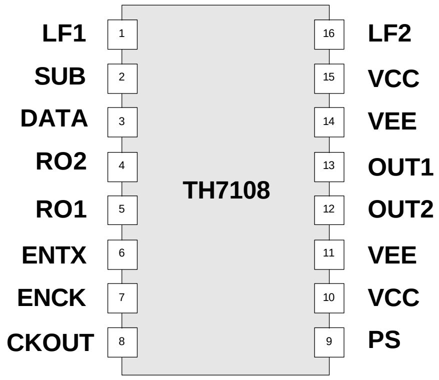
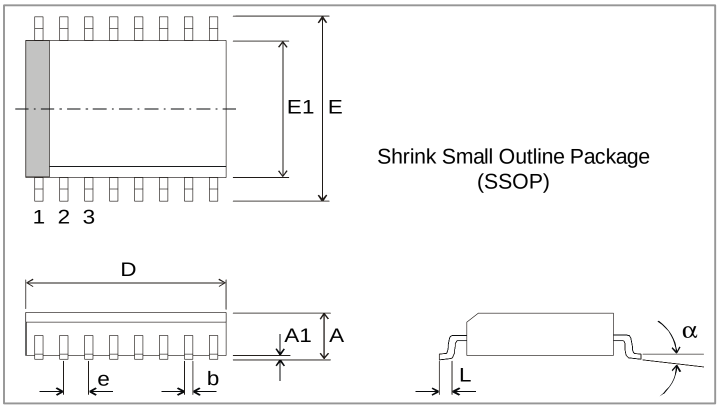
Pin Description



Pin #	Pin Name	Description
1	LF1	charge pump output, input to loopfilter
2	SUB	negative power supply, substrate connection
3	DATA	FSK data input, CMOS-compatible
4	RO2	XOSC FSK pulling pin, switch to GND or OPEN
5	RO1	XOSC connection to XTAL, base of bipolar transistor
6	ENTX	mode control input, CMOS-compatible with internal pull-up res.
7	ENCK	mode control input, CMOS-compatible with internal pull-down res.
8	CKOUT	clock output
9	PS	power-select and ASK input, high-impedance comparator logic
10	VCC	positive power supply
11	VEE	negative power supply
12	OUT2	differential power amp output, open collector
13	OUT1	differential power amp output, open collector
14	VEE	negative power supply
15	VCC	positive power supply
16	LF2	VCO tuning input, output from loopfilter

Package Information



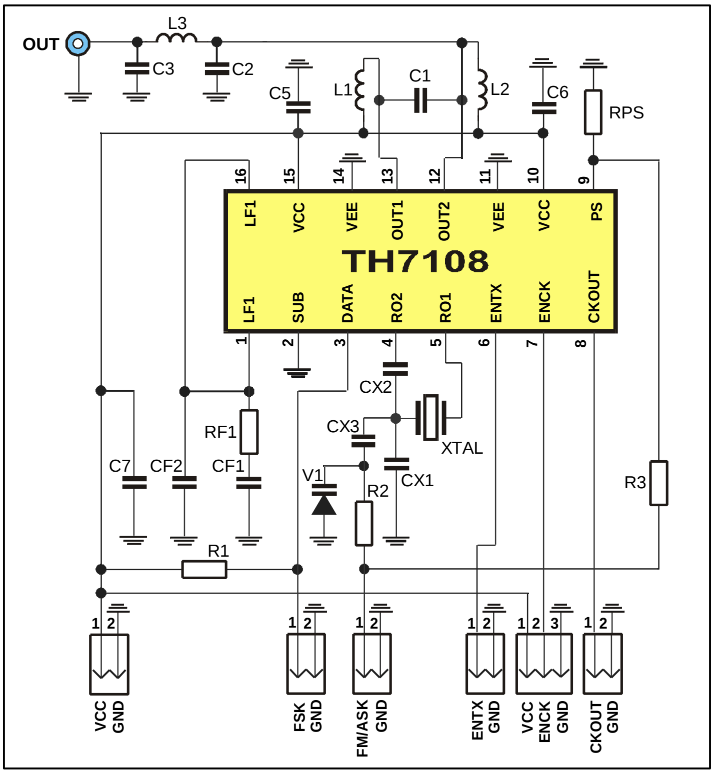
SSOP 16 150 mil

Dimension : mm

	D	E1	E	A	A1	e	b	L	Copl	α
min	4.80	3.81	5.79	1.35	0.10	0.635	0.20	0.41		0°
max	5.00	3.99	6.20	1.75	0.25		0.30	1.27	0.10	8°

Test Circuit

Fig. 2: test circuit for FSK, ASK and FM; with 50Ω matching network



test circuit component list

Part	Size	Value	Tolerance	Description
CF1	0603	5.6 nF	±10%	loopfilter capacitor
CF2	0603	4.7 pF	±10%	loopfilter capacitor
CX1	0603	15 pF	±5%	XOSC capacitor, **for FSK only**
CX2	0603	12 pF	±5%	XOSC capacitor, **for FSK only**
CX3	0603	1 nF	±10%	XOSC capacitor, **for FM only**
C1	0603	0.47 pF	±5%	impedance matching capacitor
C2	0805	1.2 pF	±5%	impedance matching capacitor
C3	0805	5.5 pF	±5%	impedance matching capacitor
C4	0603	10 pF	±5%	impedance matching capacitor
C5	0603	330 pF	±10%	blocking capacitor
C6	0603	330 pF	±10%	blocking capacitor
C7	1206	220 nF	±20%	blocking capacitor
L1	0603	10 nH	±5%	impedance matching inductor
L2	0603	15 nH	±5%	impedance matching inductor
L3	0805	15 nH	±5%	impedance matching inductor
RF1	0805	3.6 kΩ	±10%	loopfilter resistor
RF2	0805	2.2 kΩ	±10%	loopfilter resistor
RPS	0805	47 kΩ	±10%	power-select resistor
R1	0805	470 kΩ	±10%	pull-up resistor, **optional**
R2	0805	30 kΩ	±10%	varactor bias resistor, **for FM only**
R3	0805	0 Ω	±10%	ASK jumper, **for ASK only**
V1	SOD323	BB535		varactor diode, **for FM only**
XTAL	HC49/S	27.1344 MHz fundamental wave	±30ppm calibration ±30ppm temp.	crystal, C_{load} = 12pF, $C_{0,max}$ = 4pF, C_m = 20fF, R_m= 10 -20Ω

Spectrum Plots

All plots depict TH7108's typical performance at V_{cc} = 3.0 V and T_a = 23 °C, derived with the test circuit shown **Fig. 2**.

Fig. 3: RF output signal and spurious emissions, CW mode (DATA = HIGH)

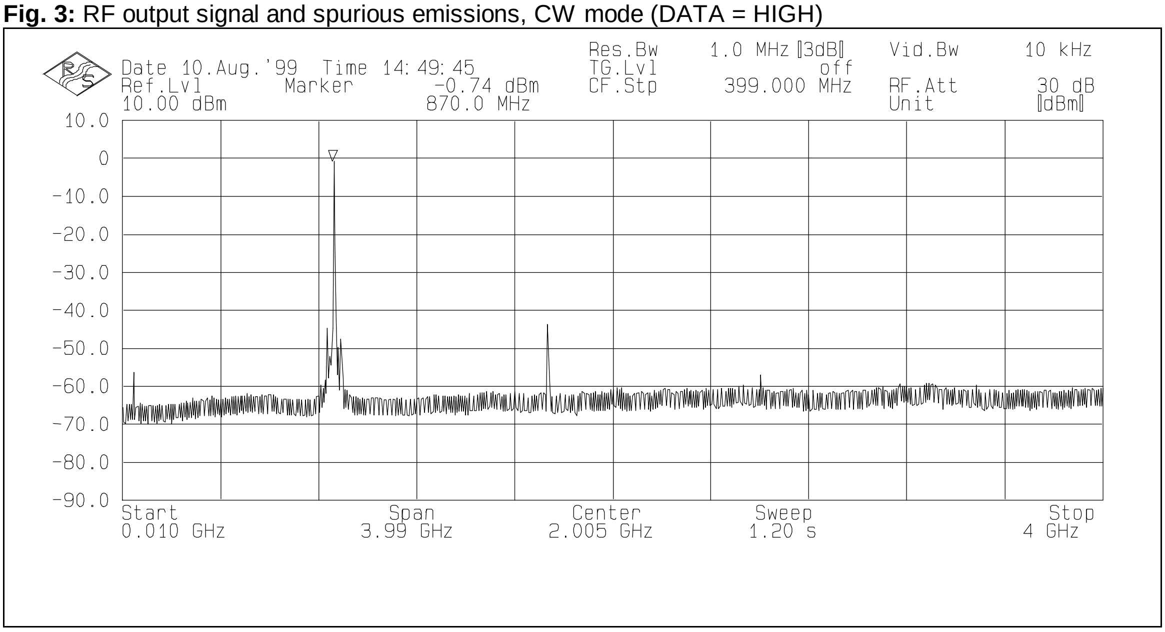


Fig. 4: Single-sideband phase noise at 500 kHz offset, CW mode (DATA = HIGH)

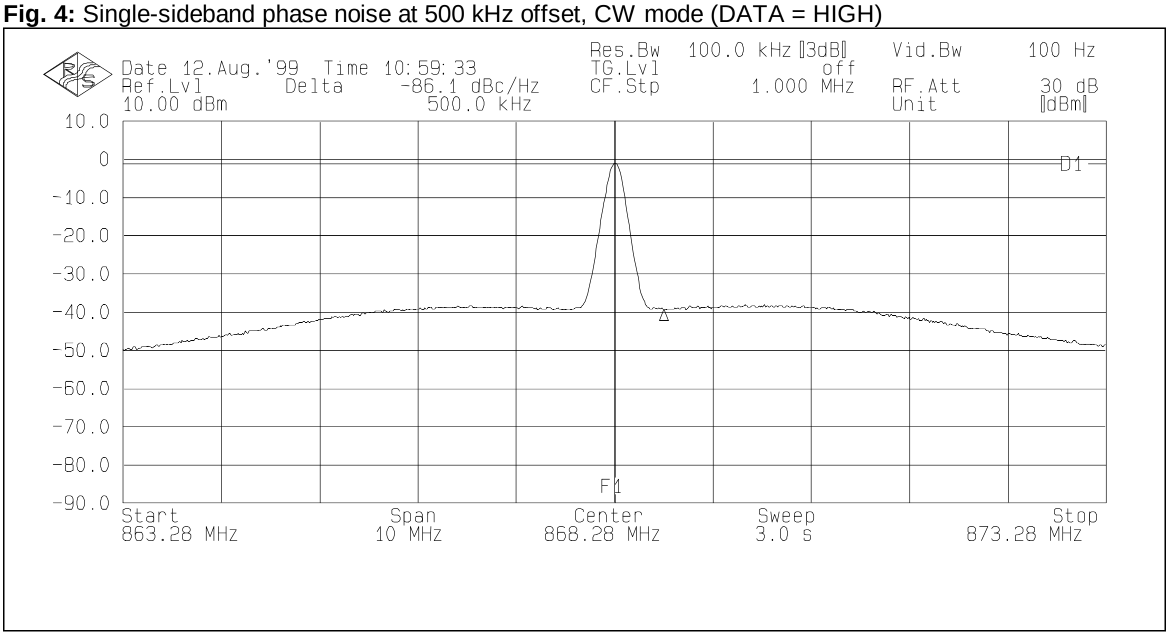


Fig. 5: FSK modulation with R_{FSK} = 7.6 kbit/s, frequency lines indicate SRD band from 868.0 to 868.6 MHz

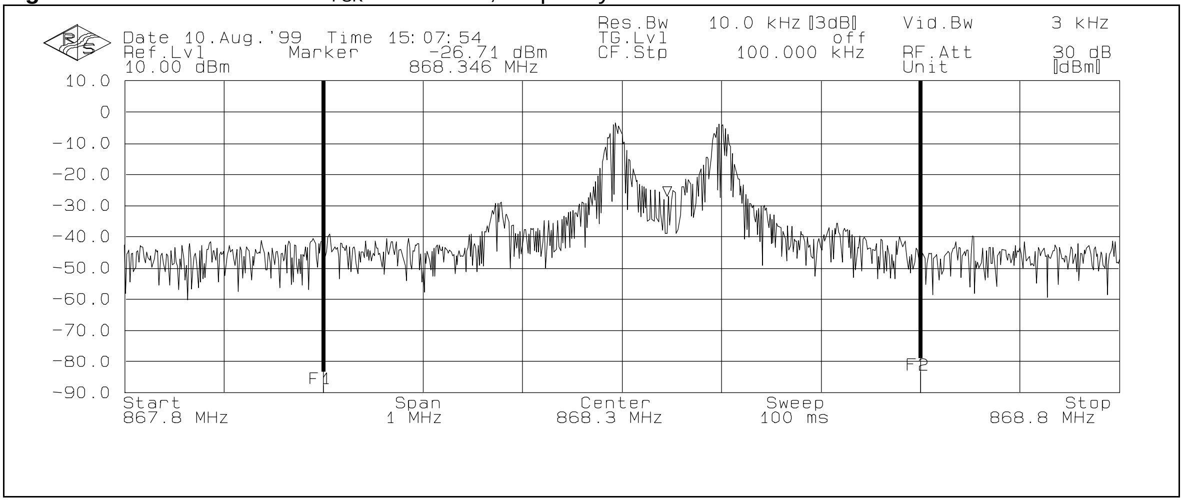


Fig. 6: ASK modulation with R_{ASK} = 4 kbit/s, frequency lines indicate SRD band from 868.0 to 868.6 MHz

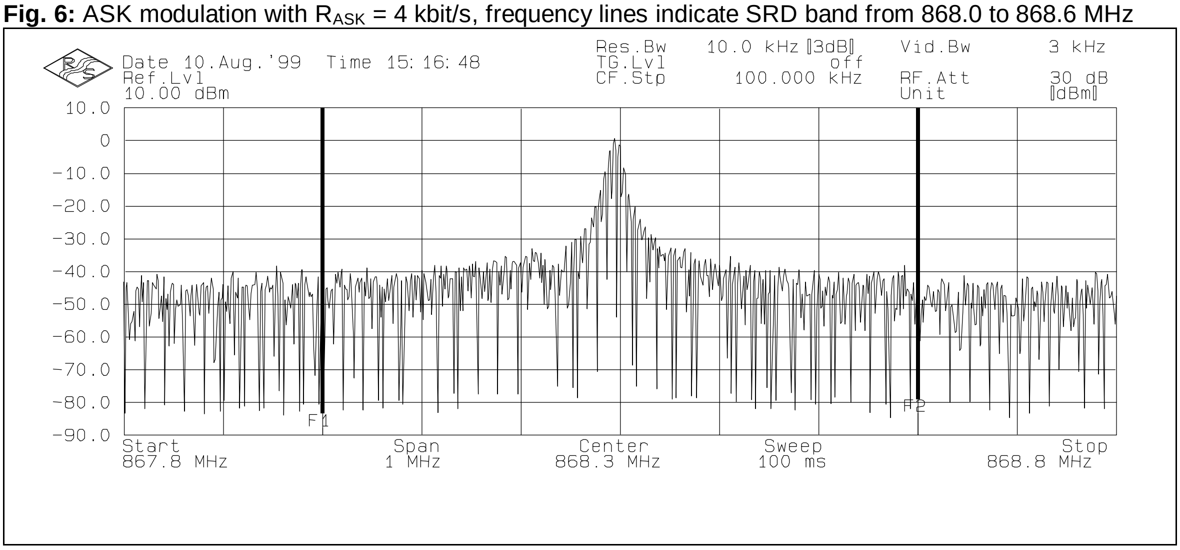


Fig. 7: FM with f_{mod} = 2 kHz, FM input signal with 1 V_{pp} around 1.5 V_{DC}