



# TDA7463D

## LOW VOLTAGE TONE CONTROL DIGITALLY CONTROLLED AUDIO PROCESSOR

### 1 FEATURES

- 1 STEREO INPUT
- 1 STEREO OUTPUT
- TREBLE BOOST
- BASS CONTROL
- BASS AUTOMATIC LEVEL CONTROL
- VOLUME CONTROL IN 1dB STEPS
- MUTE
- STAND-BY FUNCTION SOFTWARE CONTROLLED
- ALL FUNCTIONS ARE PROGRAMMABLE VIA SERIAL BUS

### 2 DESCRIPTION

The TDA7463 is a volume tone (bass and treble) processor for quality audio applications in Low voltage supply portable systems.

Bass ALC (Automatic Level Control) function can be adjusted by a dedicated pin. The control of all

Figure 1. Package

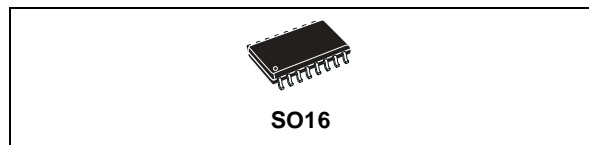


Table 1. Order Codes

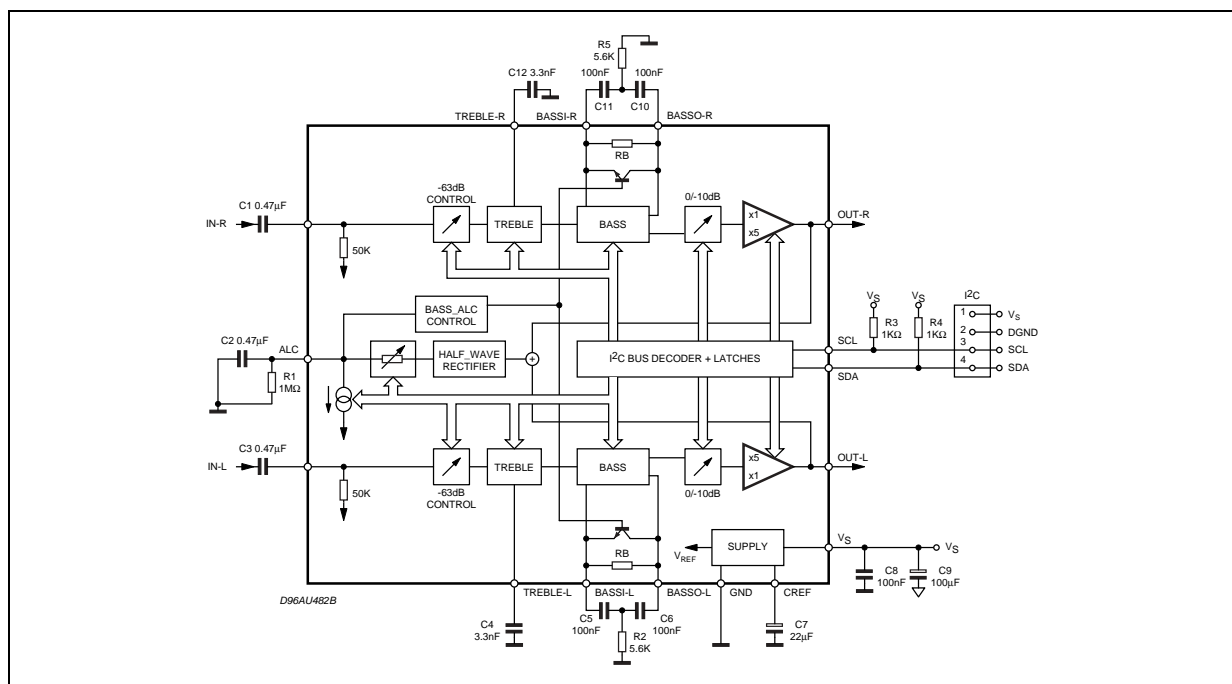
Part Number	Package
TDA7463D	SO16
TDA7463D013TR	Tape & Reel

the functions is accomplished by serial bus.

The AC signal setting is obtained by resistor networks and switches combined with operational amplifiers. Thanks to the used BIPOLAR/CMOS Technology,

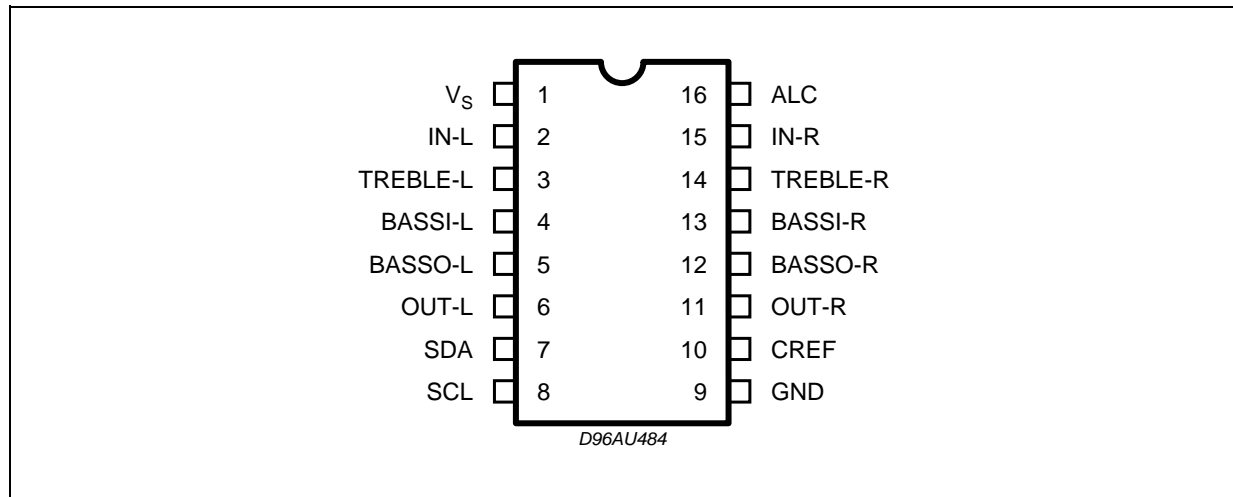
Low Distortion, Low Noise and DC stepping are obtained.

Figure 2. Block Diagram



**Table 2. Absolute Maximum Ratings**

Symbol	Parameter	Value	Unit
$V_S$	Operating Supply Voltage	5	V
$T_{amb}$	Operating Ambient Temperature	0 to 70	°C
$T_{stg}$	Storage Temperature Range	-55 to 150	°C

**Figure 3. Pin Connection****Table 3. Thermal Data**

Symbol	Parameter	Value	Unit
$R_{th\ j-pin}$	Thermal Resistance Junction-pins	85	°C/W

**Table 4. Quick Reference Data**

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
$V_S$	Supply voltage		1.8	2.4	3	V
$V_{CL}$	Max. input signal handling		0.2			V <sub>rms</sub>
THD	Total Harmonic Distortion	$V = 0.1V_{rms}$ ; $f = 1KHz$			0.1	%
S/N	Signal to Noise Ratio	$V_{out} = 0.1V_{rms}$ (mode = OFF)		80		dB
$Sc$	Channel Separation	$f = 1KHz$		80		dB
	Volume control	(1dB step)	-63		0	dB
		-10dB damping	-10		0	dB
		-14dB	0		14	dB
		Treble Control	0		8	dB
		Bass Control	0		14	dB
		mute attenuation		100	8	dB

**Table 5. Electrical Characteristics (refer to the test circuit  $T_{amb} = 25^{\circ}\text{C}$ ,  $V_S = 2.4\text{V}$ ,  $R_L = 10\text{K}\Omega$ ,  $R_G = 600\Omega$ , all controls flat, unless otherwise specified)**

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
<b>SUPPLY</b>						
V <sub>S</sub>	Supply Voltage		1.8	2.4	3	V
I <sub>S</sub>	Supply Current			4		mA
I <sub>ST-BY</sub>	Stand-By Current			50		μA
SVR	Ripple Rejection			70		dB
<b>INPUT STAGE</b>						
R <sub>IN</sub>	Input Resistance		35	50	65	KΩ
V <sub>CL</sub>	Clipping Level	THD = 0.3%	0.2			V <sub>rms</sub>
<b>VOLUME CONTROL</b>						
C <sub>RANGE</sub>	Control Range			63		dB
A <sub>V MIN</sub>	Min Attenuation		-1	0	1	dB
A <sub>V MAX</sub>	Max. Attenuation		62	63	64	dB
A <sub>STEP</sub>	Step Resolution			1		dB
A <sub>mute</sub>	Mute Attenuation		80	100		dB
A-10dB	-10dB damping			10		dB
G14dB	14dB gain			14		dB
<b>BASS CONTROL (1)</b>						
G <sub>b</sub>	Control Range	Max. Boost/on		14		dB
R <sub>B</sub>	Internal Feedback Resistance		33.75	45	56.25	KΩ
<b>TREBLE CONTROL (1)</b>						
G <sub>t</sub>	Control Range	Max. Boost on		8		dB
<b>AUDIO OUTPUTS</b>						
V <sub>CLIP</sub>	Clipping Level	d = 0.3%	0.2			V <sub>RMS</sub>
R <sub>L</sub>	Output Load Resistance		10			KΩ
V <sub>DC</sub>	DC Voltage Level			0.8		V
<b>GENERAL</b>						
E <sub>NO</sub>	Output Noise	Output Muted All gains = 0dB; BW = 20Hz to 20KHz flat		5 8		μV μV
E <sub>t</sub>	Total Tracking Error			0	1	dB
S/N	Signal to Noise Ratio	All gains 0dB; V <sub>O</sub> = 0.1V <sub>RMS</sub> ;		80		dB
SC	Channel Separation Left/Right			80		dB
d	Distortion	A <sub>V</sub> = 0; V <sub>I</sub> = 0.1V <sub>RMS</sub> ;			0.1	%
<b>BUS INPUT</b>						
V <sub>IL</sub>	Input Low Voltage				0.5	V
V <sub>IH</sub>	Input High Voltage		1.9			V
I <sub>IN</sub>	Input Current	V <sub>IN</sub> = 0.4V	-5		5	μA
V <sub>O</sub>	Output Voltage SDA Acknowledge	I <sub>O</sub> = 1.6mA			0.4	V

Note: 1. BASS and TREBLE response: The center frequency and the response quality can be chosen by the external circuitry.

### 3 DATA BYTES

Address = (HEX) 10001000

**Table 6. FUNCTION SELECTION:**

The first byte (subaddress)58

MSB							LSB	SUBADDRESS
D7	D6	D5	D4	D3	D2	D1	D0	
	X	X	B	0	0	0	0	STAND-BY & TREBLE & OTHERS
	X	X	B	0	0	0	1	BASS
	X	X	B	0	0	1	0	VOLUME

B = 1 incremental bus; active

B = 0 no incremental bus;

X = indifferent 0,1

**Table 7. STAND\_BY & TREBLE & OTHERS**

MSB							LSB	
D7	D6	D5	D4	D3	D2	D1	D0	
								<b>STAND-BY</b>
							1	ALL CIRCUITS STOP
								<b>TREBLE</b>
						1		STAND-BY (Treble block stops)
					1	0		BOOST OFF
					0	0		BOOST ON
				1	0	0		High Boost (+8dB)
				0	0	0		Low Boost (+4dB)
								<b>MUTE</b>
			1					Input Mute ON
			0					Input Mute OFF
		1						Output Mute ON
		0						Output Mute OFF
								<b>BASS</b>
	1							Release Current Circuit ON
	0							Release Current Circuit OFF
								<b>INPUT Select</b>
1								INPUT 1
0								INPUT 2

Table 8. BASS

MSB							LSB	BASS
D7	D6	D5	D4	D3	D2	D1	D0	
							1	STAND-BY (Bass block stops)
						1		BASS (boost OFF)
						0		BASS (boost ON)
					1	0		High boost (Ex. + 14dB)
					0	0		Low boost (Ex. + 6dB)
				1				ALC mode OFF (ALC block stops)
				0				ALC mode ON
		0	0					Attack time resistor (12.5K $\Omega$ ) Release current (0.4 $\mu$ A)
		0	1					Attack time resistor (25K $\Omega$ ) Release current (0.2 $\mu$ A)
		1	0					Attack time resistor (50K $\Omega$ ) Release current (0.1 $\mu$ A)
		1	1					Attack time resistor (100K $\Omega$ ) Release current (0.05 $\mu$ A)
0	0							Threshold1 (0.2Vrms)
0	1							Threshold2 (0.14Vrms)
1	0							Threshold3 (0.1Vrms)
1	1							Threshold4 (0.07Vrms)

Table 9. VOLUME

MSB							LSB	VOLUME
D7	D6	D5	D4	D3	D2	D1	D0	1 dB STEPS
					0	0	0	0
					0	0	1	-1
					0	1	0	-2
					0	1	1	-3
					1	0	0	-4
					1	0	1	-5
					1	1	0	-6
					1	1	1	-7
								<b>8 dB STEPS</b>
		0	0	0				0
		0	0	1				-8
		0	1	0				-16
		0	1	1				-24
		1	0	0				-32
		1	0	1				-40
		1	1	0				-48
		1	1	1				-56
								<b>OUTPUT GAIN</b>
	1							0dB
	0							+14dB
								<b>OUTPUT ATTENUATION</b>
1								0dB
0								-10dB

VOLUME : 0 ~ -63dB

## 3.1 ALC IN general:

Table 10. VOLUME setting with ALC

Target Volume [dB]	Volume [dB]	Output Gain 0/+14dB0/-10dB [dB]	Output Attenuation 0/-10dB [dB]
0	-14	+14	0
-1	-15		
-2	-16		
-3	-17		
-4	-18		
-5	-19		
-6	-20		
-7	-21		
-8	-22		
-9	-23		
-10	-24		
-11	-25		
-12	-26		
-13	-27		
-14	-14	0	0
-15	-15		
-16	-16		
-17	-17		
-18	-18		
-19	-19		
-20	-20		
-21	-21		
-22	-22		
-23	-23		
-24	-14	0	-10
-25	-15		
-26	-16		
-27	-17		
:	:		
:	:		
-70	-60		
-71	-61		
-72	-62		
-73	-63		

Figure 4. PIN: IN-L, IN-R

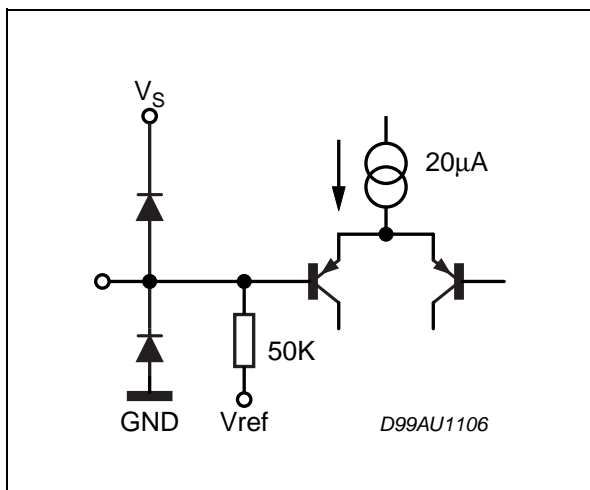


Figure 7. OUT-L, OUT-R

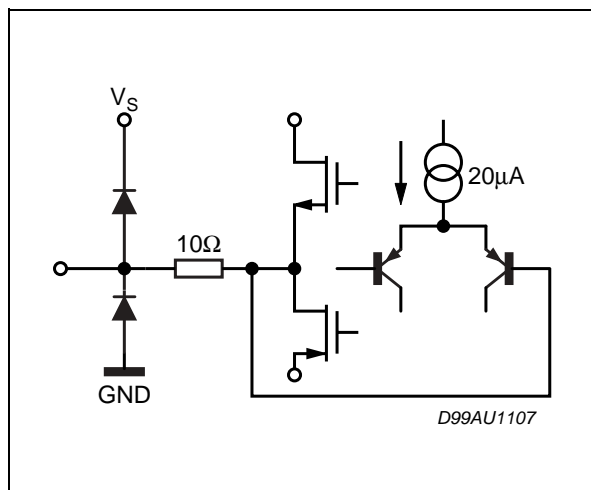


Figure 5. PIN: TREBLE-L, TREBLE-R

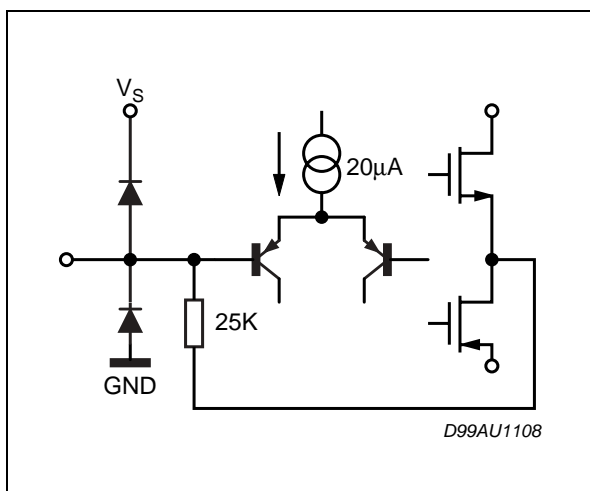


Figure 8. SCL, SDA

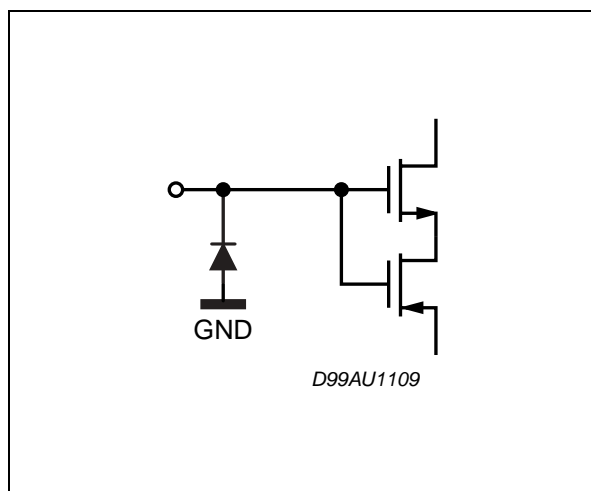


Figure 6. PIN: BASSI-L, BASSI-R

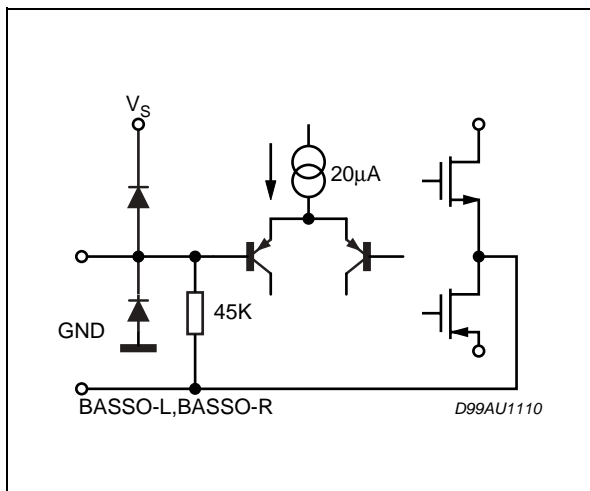


Figure 9. BASSO-L, BASSO-R

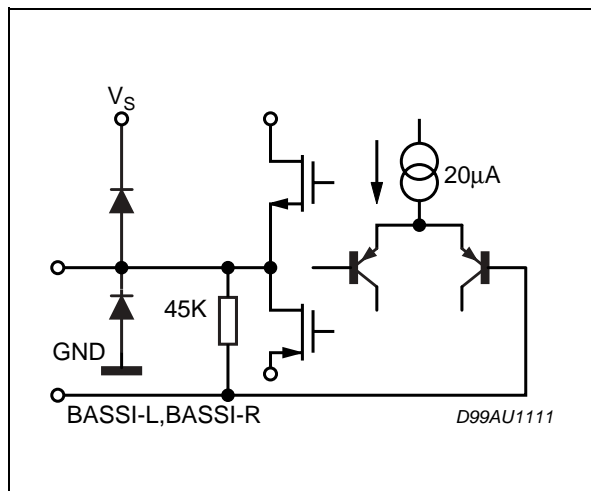


Figure 10. PIN: ALC

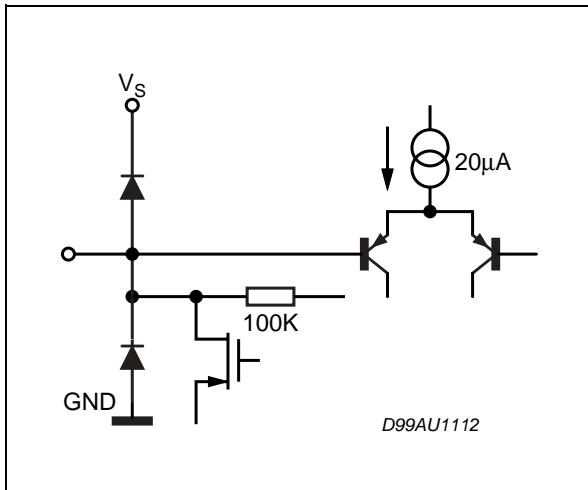


Figure 12. BASS ALC: Threshold curve

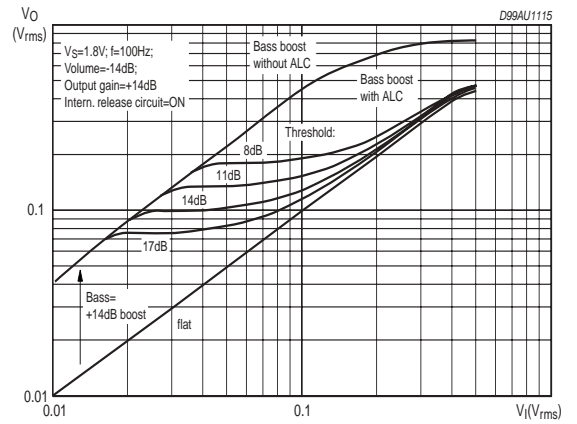


Figure 11. PIN CREF

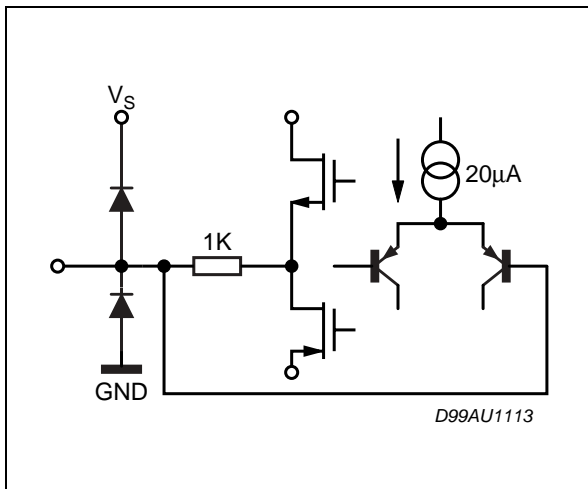


Figure 13. BASS ALC: THD

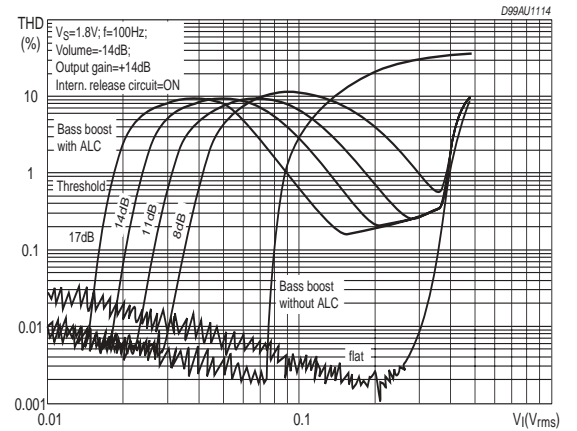




Figure 14. board and Components Layout of the Application &amp; Test Circuit.

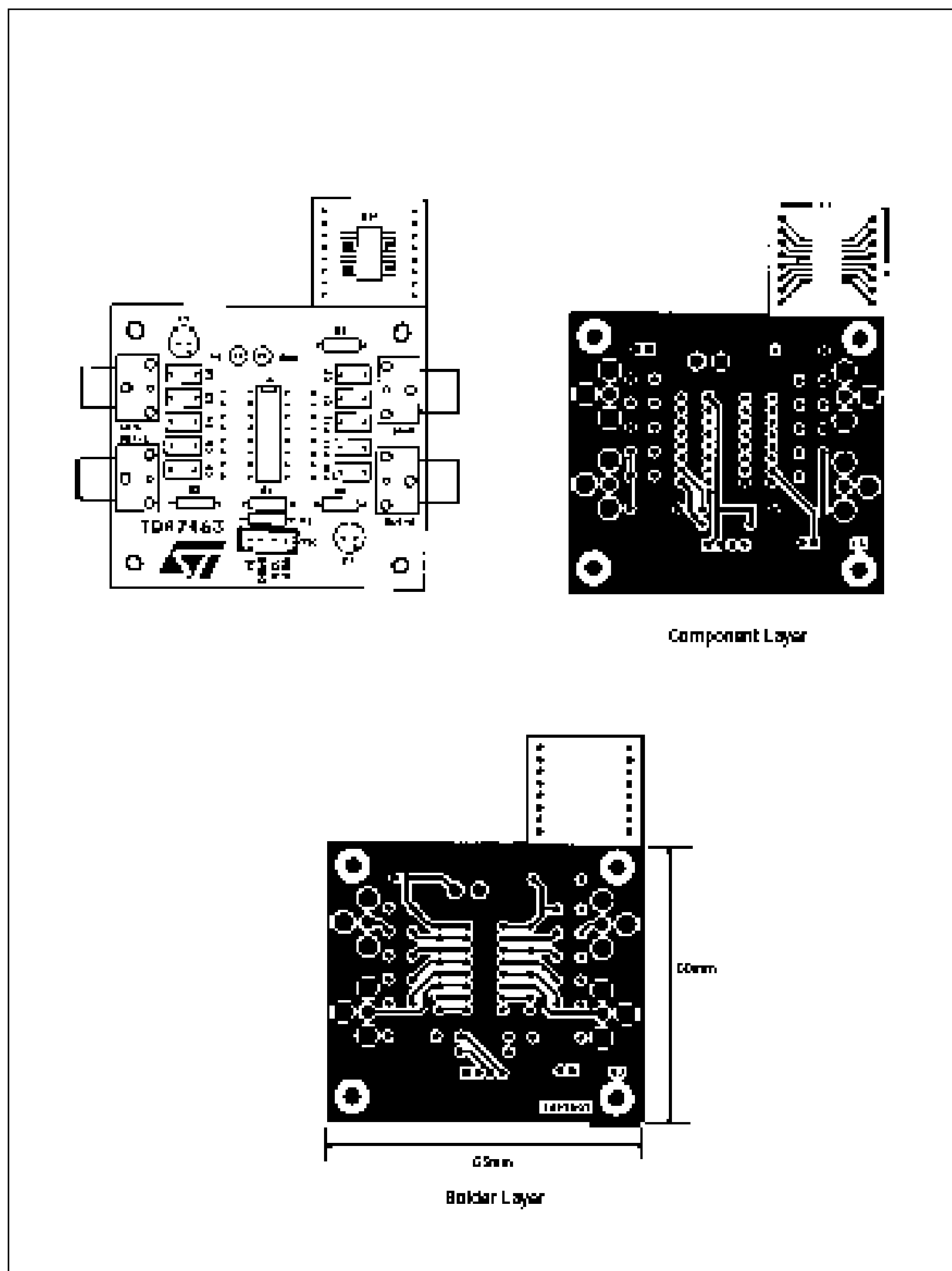
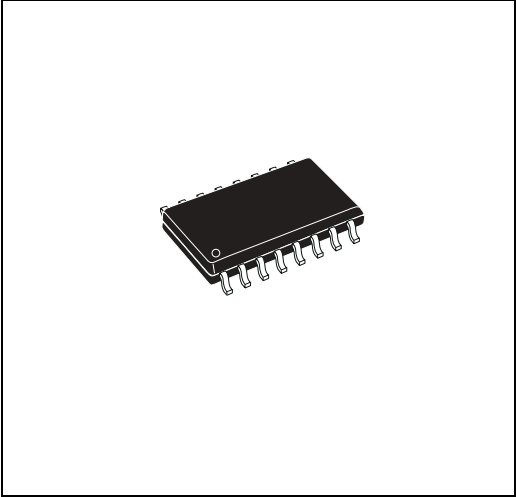


Figure 15. SO16 Wide Mechanical Data & Package Dimensions

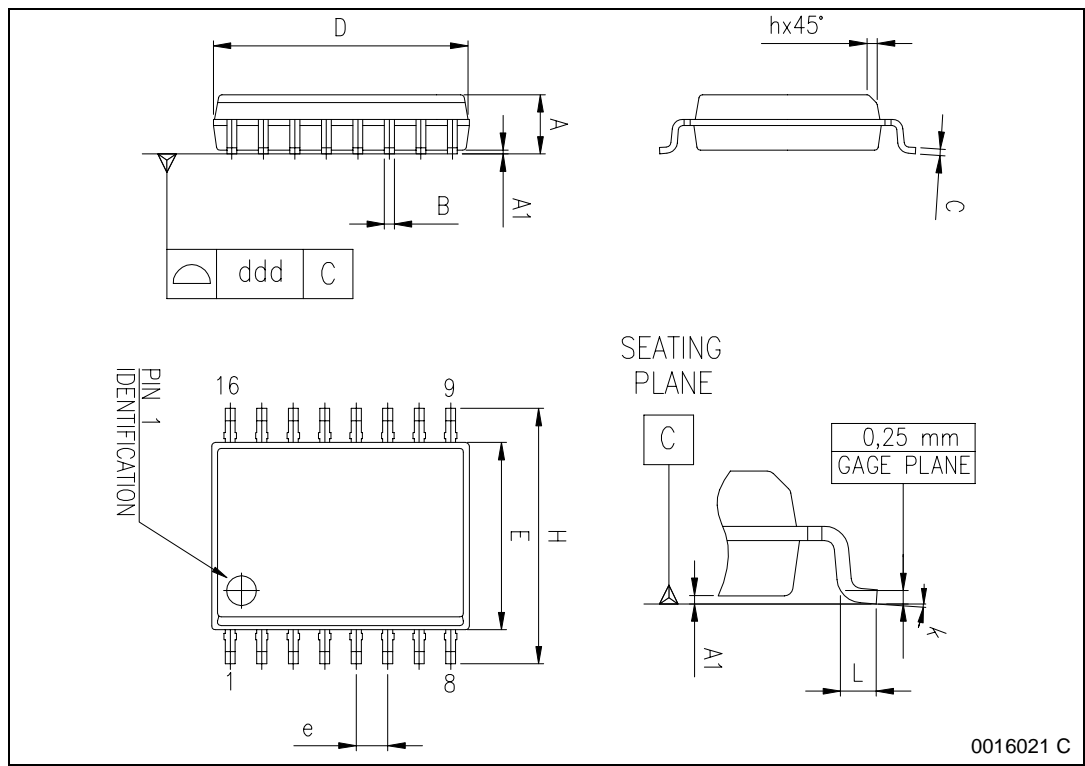
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.35		2.65	0.093		0.104
A1	0.10		0.30	0.004		0.012
B	0.33		0.51	0.013		0.200
C	0.23		0.32	0.009		0.013
D (1)	10.10		10.50	0.398		0.413
E	7.40		7.60	0.291		0.299
e		1.27			0.050	
H	10.0		10.65	0.394		0.419
h	0.25		0.75	0.010		0.030
L	0.40		1.27	0.016		0.050
k	0° (min.), 8° (max.)					
ddd			0.10			0.004

(1) "D" dimension does not include mold flash, protusions or gate burrs. Mold flash, protusions or gate burrs shall not exceed 0.15mm per side.

**OUTLINE AND MECHANICAL DATA**



**SO16 (Wide)**



0016021 C

**Table 11. Revision History**

<b>Date</b>	<b>Revision</b>	<b>Description of Changes</b>
May 2002	3	Third issue
June 2004	3	Changed the Style-sheet in compliance to the new "Corporate Technical Publications Design Guide"

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