

TOSHIBA Digital Integrated Circuit Silicon Monolithic

TC7MPH3245FTG

Low Voltage/Low Power 4-Bit × 2 Dual Supply Bus Transceiver with Bushold

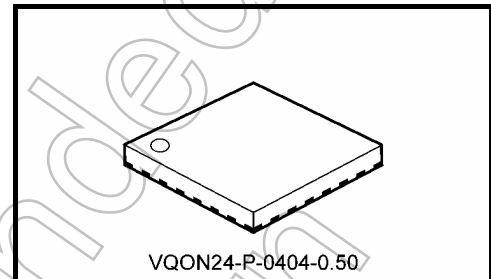
The TC7MP3245FTG is a dual supply, advanced high-speed CMOS 8-bit dual supply voltage interface bus transceiver fabricated with silicon gate CMOS technology.

Designed for use as an interface between a 1.2-V, 1.5-V, 1.8-V, or 2.5-V bus and a 1.8-V, 2.5-V or 3.6-V bus in mixed 1.2-V, 1.5-V, 1.8-V or 2.5-V/1.8-V, 2.5-V or 3.6-V supply systems.

The A-port interfaces with the 1.2-V, 1.5-V, 1.8-V or 2.5-V bus, the B-port with the 1.8-V, 2.5-V, 3.3-V bus.

The direction of data transmission is determined by the level of the DIR input. The enable input (\overline{OE}) can be used to disable the device so that the buses are effectively isolated. The bus of a B bus side at floating state is maintained in an appropriate logic level due to a bushold circuit to a B bus. Moreover, the bushold circuit which is added to a B bus is off when \overline{OE} is low.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.



Weight: 0.03 g (typ.)

Features

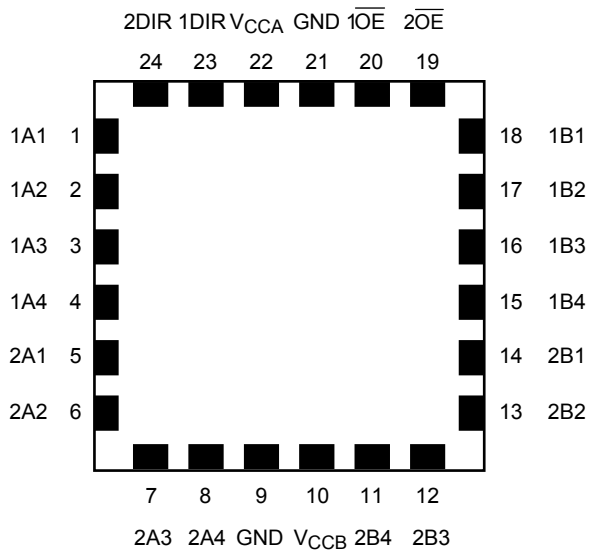
- Bidirectional interface between 1.2-V and 1.8-V, 1.2-V and 2.5-V, 1.2-V and 3.3-V, 1.5-V and 2.5-V, 1.5-V and 3.3-V, 1.8-V and 2.5-V, 1.8-V and 3.3-V or 2.5-V and 3.3-V buses.
- High-speed operation: $t_{pd} = 6.8 \text{ ns (max)}$ ($V_{CCA} = 2.5 \pm 0.2 \text{ V}$, $V_{CCB} = 3.3 \pm 0.3 \text{ V}$)
 $t_{pd} = 8.9 \text{ ns (max)}$ ($V_{CCA} = 1.8 \pm 0.15 \text{ V}$, $V_{CCB} = 3.3 \pm 0.3 \text{ V}$)
 $t_{pd} = 10.3 \text{ ns (max)}$ ($V_{CCA} = 1.5 \pm 0.1 \text{ V}$, $V_{CCB} = 3.3 \pm 0.3 \text{ V}$)
 $t_{pd} = 61 \text{ ns (max)}$ ($V_{CCA} = 1.2 \pm 0.1 \text{ V}$, $V_{CCB} = 3.3 \pm 0.3 \text{ V}$)
 $t_{pd} = 9.5 \text{ ns (max)}$ ($V_{CCA} = 1.8 \pm 0.15 \text{ V}$, $V_{CCB} = 2.5 \pm 0.2 \text{ V}$)
 $t_{pd} = 10.8 \text{ ns (max)}$ ($V_{CCA} = 1.5 \pm 0.1 \text{ V}$, $V_{CCB} = 2.5 \pm 0.2 \text{ V}$)
 $t_{pd} = 60 \text{ ns (max)}$ ($V_{CCA} = 1.2 \pm 0.1 \text{ V}$, $V_{CCB} = 2.5 \pm 0.2 \text{ V}$)
 $t_{pd} = 58 \text{ ns (max)}$ ($V_{CCA} = 1.2 \pm 0.1 \text{ V}$, $V_{CCB} = 1.5 \pm 0.1 \text{ V}$)
- Output current: $I_{OH}/I_{OL} = \pm 12 \text{ mA (min)}$ ($V_{CC} = 3.0 \text{ V}$)
 $I_{OH}/I_{OL} = \pm 9 \text{ mA (min)}$ ($V_{CC} = 2.3 \text{ V}$)
 $I_{OH}/I_{OL} = \pm 3 \text{ mA (min)}$ ($V_{CC} = 1.65 \text{ V}$)
 $I_{OH}/I_{OL} = \pm 1 \text{ mA (min)}$ ($V_{CC} = 1.4 \text{ V}$)
- Latch-up performance: $\pm 300 \text{ mA}$
- ESD performance: Machine model $\geq \pm 200 \text{ V}$
Human body model $\geq \pm 2000 \text{ V}$
- Ultra-small package: VQON24
- Bushold circuit is build in only the B bus side. (Only in $\overline{OE} = \text{“H”}$, a former state is maintained.)
- Low current consumption: Using the new circuit significantly reduces current consumption when $\overline{OE} = \text{“H”}$.
Suitable for battery-driven applications such as PDAs and cellular phones.
- Floating A-bus and B-bus are permitted. (when $\overline{OE} = \text{“H”}$)
- 3.6-V tolerant function provided on A-bus terminal, DIR and \overline{OE} terminal.

Note 1: Do not apply a signal to any bus pins when it is in the output mode. Damage may result.

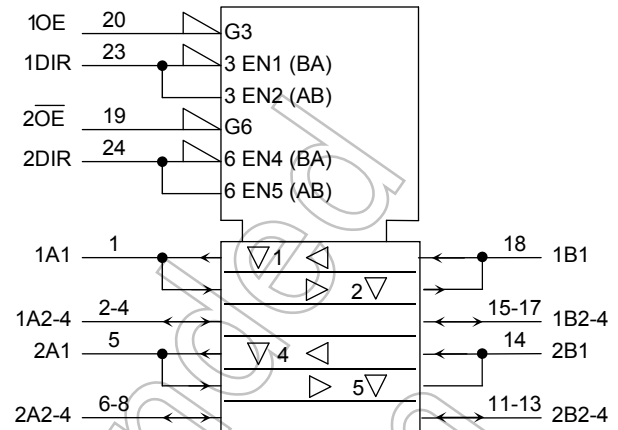
Note: When mounting VQON package, the type of recommended flux is RA or RMA.

Start of commercial production
2004-12

Pin Assignment (top view)



IEC Logic Symbol



Truth Table

Inputs		Function		Outputs	Bushold Circuit (B bus)
1OE	1DIR	Bus 1A1-1A4	Bus 1B1-1B4		
L	L	Output	Input	A = B	OFF
L	H	Input	Output	B = A	OFF
H	X	Z		Z	ON*

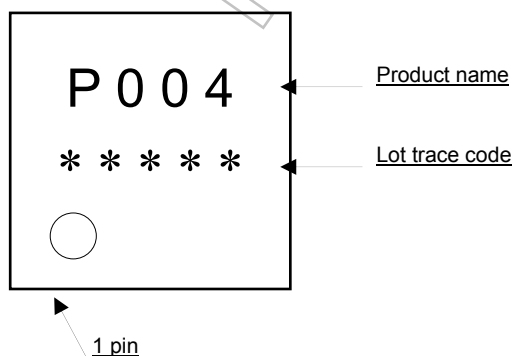
Inputs		Function		Outputs	Bushold Circuit (B bus)
2OE	2DIR	Bus 2A1-2A4	Bus 2B1-2B4		
L	L	Output	Input	A = B	OFF
L	H	Input	Output	B = A	OFF
H	X	Z		Z	ON*

X: Don't care

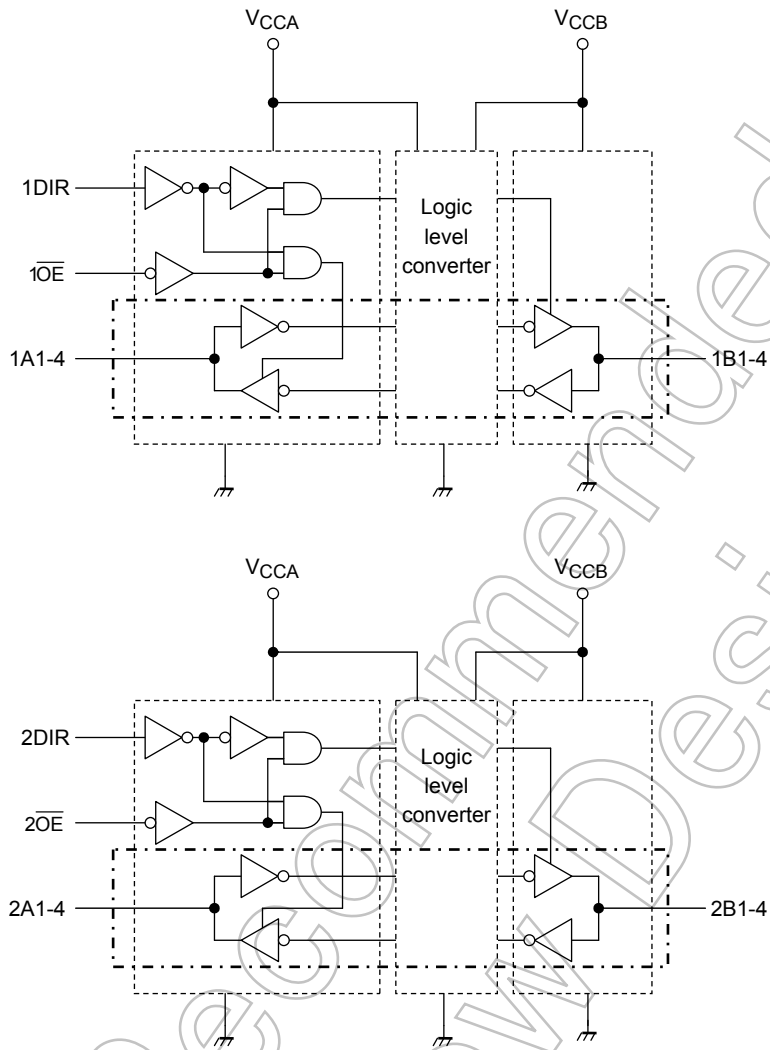
Z: High impedance

*: Logic state just before becoming disable is maintained.

Marking



Block Diagram



Not Recommended for New Design

Absolute Maximum Ratings (Note 1)

Characteristics	Symbol	Rating	Unit
Power supply voltage (Note 2)	V_{CCA}	-0.5 to 4.6	V
	V_{CCB}	-0.5 to 4.6	
DC input voltage (DIR, \overline{OE})	V_{IN}	-0.5 to 4.6	V
DC bus I/O voltage	V_{IOA}	-0.5 to 4.6 (Note 3)	V
		-0.5 to $V_{CCA} + 0.5$ (Note 4)	
	V_{IOB}	-0.5 to $V_{CCB} + 0.5$ (Note 4)	
Input diode current	I_{IK}	-50	mA
Output diode current	$I_{I/OK}$	± 50 (Note 5)	mA
DC output current	I_{OUTA}	± 25	mA
	I_{OUTB}	± 25	
DC V_{CC} /ground current per supply pin	I_{CCA}	± 50	mA
	I_{CCB}	± 50	
Power dissipation	P_D	180	mW
Storage temperature	T_{stg}	-65 to 150	$^{\circ}\text{C}$

Note 1: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc.).

Note 2: Don't supply a voltage to V_{CCB} pin when V_{CCA} is in the OFF state.

Note 3: Output in OFF state

Note 4: High or Low stats. I_{OUT} absolute maximum rating must be observed.

Note 5: $V_{OUT} < \text{GND}$, $V_{OUT} > V_{CC}$

Operating Ranges (Note 1)

Characteristics	Symbol	Rating	Unit
Power supply voltage (Note 2)	V_{CCA}	1.1 to 2.7	V
	V_{CCB}	1.65 to 3.6	
Input voltage (DIR, \overline{OE})	V_{IN}	0 to 3.6	V
Bus I/O voltage	V_{IOA}	0 to 3.6 (Note 3)	V
		0 to V_{CCA} (Note 4)	
	V_{IOB}	0 to V_{CCB} (Note 4)	
Output current	I_{OUTA}	± 9 (Note 5)	mA
		± 3 (Note 6)	
		± 1 (Note 7)	
	I_{OUTB}	± 12 (Note 8)	
		± 9 (Note 9)	
		± 3 (Note 10)	
Operating temperature	T_{opr}	-40 to 85	°C
Input rise and fall time	dt/dv	0 to 10 (Note 11)	ns/V

Note 1: The operating ranges must be maintained to ensure the normal operation of the device. Unused inputs and bus inputs must be tied to either V_{CC} or GND. Please connect both bus inputs and the bus outputs with V_{CC} or GND when the I/O of the bus terminal changes by the function. In this case, please note that the output is not short-circuited.

Note 2: Don't use in $V_{CCA} > V_{CCB}$

Note 3: Output in OFF state

Note 4: High or low state

Note 5: $V_{CCB} = 2.3$ to 2.7 V

Note 6: $V_{CCB} = 1.65$ to 1.95 V

Note 7: $V_{CCB} = 1.4$ to 1.6 V

Note 8: $V_{CCA} = 3.0$ to 3.6 V

Note 9: $V_{CCA} = 2.3$ to 2.7 V

Note 10: $V_{CCA} = 1.65$ to 1.95 V

Note 11: $V_{IN} = 0.8$ to 2.0 V, $V_{CCA} = 2.5$ V, $V_{CCB} = 3.0$ V

Electrical Characteristics

DC Characteristics (2.3 V ≤ V_{CCA} ≤ 2.7 V, 2.7 V < V_{CCB} ≤ 3.6 V)

Characteristics	Symbol	Test Condition	V _{CCA} (V)	V _{CCB} (V)	Ta = -40 to 85°C		Unit	
					Min	Max		
H-level input voltage	V _{IHA}	DIR, \overline{OE} , An	2.3 to 2.7	2.7 to 3.6	1.6	—	V	
	V _{IHB}	Bn	2.3 to 2.7	2.7 to 3.6	2.0	—		
L-level input voltage	V _{ILA}	DIR, \overline{OE} , An	2.3 to 2.7	2.7 to 3.6	—	0.7	V	
	V _{ILB}	Bn	2.3 to 2.7	2.7 to 3.6	—	0.8		
H-level output voltage	V _{OHA}	V _{IN} = V _{IH} or V _{IL}	I _{OHA} = -100 μA	2.3 to 2.7	2.7 to 3.6	V _{CCA} - 0.2	—	V
			I _{OHA} = -9 mA	2.3	2.7 to 3.6	1.7	—	
	V _{OHB}		I _{OHB} = -100 μA	2.3 to 2.7	2.7 to 3.6	V _{CCB} - 0.2	—	
			I _{OHB} = -12 mA	2.3 to 2.7	3.0	2.2	—	
L-level output voltage	V _{OLA}	V _{IN} = V _{IH} or V _{IL}	I _{OLA} = 100 μA	2.3 to 2.7	2.7 to 3.6	—	0.2	V
			I _{OLA} = 9 mA	2.3	2.7 to 3.6	—	0.6	
	V _{OLB}		I _{OLB} = 100 μA	2.3 to 2.7	2.7 to 3.6	—	0.2	
			I _{OLB} = 12 mA	2.3 to 2.7	3.0	—	0.55	
3-state output OFF state current	I _{OZA}	V _{IN} = V _{IH} or V _{IL} V _{OUT} = 0 to 3.6 V	2.3 to 2.7	2.7 to 3.6	—	±5.0	μA	
	I _{OZB}	V _{IN} = V _{IH} or V _{IL} V _{OUT} = 0 to 3.6 V	2.3 to 2.7	2.7 to 3.6	—	±5.0		
Input leakage current	I _{IN}	V _{IN} (DIR, \overline{OE}) = 0 to 3.6 V	2.3 to 2.7	2.7 to 3.6	—	±5.0	μA	
Bushold input minimum drive hold current	I _{IHOLD}	V _{IN} = 0.8 V	2.3 to 2.7	3.0	75	—	μA	
		V _{IN} = 2.0 V	2.3 to 2.7	3.0	-75	—		
Bushold input over-drive current to change state (Note)	I _{IOD}	V _{IN} = "L" → "H"	2.3 to 2.7	3.6	—	550	μA	
		V _{IN} = "H" → "L"	2.3 to 2.7	3.6	—	-550		
Power-off leakage current	I _{OFF1}	V _{IN} , V _{OUT} = 0 to 3.6 V	0	0	—	5.0	μA	
	I _{OFF2}		2.3 to 2.7	0	—	5.0		
	I _{OFF3}		2.3 to 2.7	Open	—	5.0		
Quiescent supply current	I _{CCA}	V _{INA} = V _{CCA} or GND V _{INB} = V _{CCB} or GND	2.3 to 2.7	2.7 to 3.6	—	5.0	μA	
	I _{CCB}	V _{INA} = V _{CCA} or GND V _{INB} = V _{CCB} or GND	2.3 to 2.7	2.7 to 3.6	—	5.0		
	I _{CCA}	V _{CCA} ≤ (V _{IN} , V _{OUT}) ≤ 3.6 V	2.3 to 2.7	2.7 to 3.6	—	±5.0	μA	
	I _{CCB}	V _{CCB} ≤ (V _{IN} , V _{OUT}) ≤ 3.6 V	2.3 to 2.7	2.7 to 3.6	—	±5.0		
	I _{CCTB}	V _{INA} = V _{CCB} - 0.6 V per input	2.3 to 2.7	2.7 to 3.6	—	750.0	μA	

Note: It is a necessary electric current to change the input in "L" or "H".

DC Characteristics (1.65 V ≤ V_{CCA} < 2.3 V, 2.7 V < V_{CCB} ≤ 3.6 V)

Characteristics	Symbol	Test Condition	V _{CCA} (V)	V _{CCB} (V)	Ta = -40 to 85°C		Unit	
					Min	Max		
H-level input voltage	V _{IHA}	DIR, \overline{OE} , An	1.65 to 2.3	2.7 to 3.6	$0.65 \times V_{CCA}$	—	V	
	V _{IHB}	Bn	1.65 to 2.3	2.7 to 3.6	2.0	—		
L-level input voltage	V _{ILA}	DIR, \overline{OE} , An	1.65 to 2.3	2.7 to 3.6	—	$0.35 \times V_{CCA}$	V	
	V _{ILB}	Bn	1.65 to 2.3	2.7 to 3.6	—	0.8		
H-level output voltage	V _{OHA}	V _{IN} = V _{IH} or V _{IL}	I _{OHA} = -100 μA	1.65 to 2.3	2.7 to 3.6	V _{CCA} - 0.2	—	V
			I _{OHA} = -3 mA	1.65	2.7 to 3.6	1.25	—	
	V _{OHB}		I _{OHB} = -100 μA	1.65 to 2.3	2.7 to 3.6	V _{CCB} - 0.2	—	
			I _{OHB} = -12 mA	1.65 to 2.3	3.0	2.2	—	
L-level output voltage	V _{OLA}	V _{IN} = V _{IH} or V _{IL}	I _{OLA} = 100 μA	1.65 to 2.3	2.7 to 3.6	—	0.2	V
			I _{OLA} = 3 mA	1.65	2.7 to 3.6	—	0.3	
	V _{OLB}		I _{OLB} = 100 μA	1.65 to 2.3	2.7 to 3.6	—	0.2	
			I _{OLB} = 12 mA	1.65 to 2.3	3.0	—	0.55	
3-state output OFF state current	I _{OZA}	V _{IN} = V _{IH} or V _{IL} V _{OUT} = 0 to 3.6 V	1.65 to 2.3	2.7 to 3.6	—	±5.0	μA	
	I _{OZB}	V _{IN} = V _{IH} or V _{IL} V _{OUT} = 0 to 3.6 V	1.65 to 2.3	2.7 to 3.6	—	±5.0		
Input leakage current	I _{IN}	V _{IN} (DIR, \overline{OE}) = 0 to 3.6 V	1.65 to 2.3	2.7 to 3.6	—	±2.0	μA	
Bushold input minimum drive hold current	I _{IHOLD}	V _{IN} = 0.8 V	1.65 to 2.3	3.0	75	—	μA	
		V _{IN} = 2.0 V	1.65 to 2.3	3.0	-75	—		
Bushold input over-drive current to change state (Note)	I _{IOD}	V _{IN} = "L" → "H"	1.65 to 2.3	3.6	—	550	μA	
		V _{IN} = "H" → "L"	1.65 to 2.3	3.6	—	-550		
Power-off leakage current	I _{OFF1}	V _{IN} , V _{OUT} = 0 to 3.6 V	0	0	—	5.0	μA	
	I _{OFF2}		1.65 to 2.3	0	—	5.0		
	I _{OFF3}		1.65 to 2.3	Open	—	5.0		
Quiescent supply current	I _{CCA}	V _{INA} = V _{CCA} or GND V _{INB} = V _{CCB} or GND	1.65 to 2.3	2.7 to 3.6	—	5.0	μA	
	I _{CCB}	V _{INA} = V _{CCA} or GND V _{INB} = V _{CCB} or GND	1.65 to 2.3	2.7 to 3.6	—	5.0		
	I _{CCA}	V _{CCA} ≤ (V _{IN} , V _{OUT}) ≤ 3.6 V	1.65 to 2.3	2.7 to 3.6	—	±5.0	μA	
	I _{CCB}	V _{CCB} ≤ (V _{IN} , V _{OUT}) ≤ 3.6 V	1.65 to 2.3	2.7 to 3.6	—	±5.0		
	I _{CCTB}	V _{INB} = V _{CCB} - 0.6 V per input	1.65 to 2.3	2.7 to 3.6	—	750.0		

Note: It is a necessary electric current to change the input in "L" or "H".

DC Characteristics (1.4 V ≤ V_{CCA} < 1.65 V, 2.7 V < V_{CCB} ≤ 3.6 V)

Characteristics	Symbol	Test Condition	V _{CCA} (V)	V _{CCB} (V)	Ta = -40 to 85°C		Unit	
					Min	Max		
H-level input voltage	V _{IHA}	DIR, \overline{OE} , An	1.4 to 1.65	2.7 to 3.6	$0.65 \times V_{CCA}$	—	V	
	V _{IHB}	Bn	1.4 to 1.65	2.7 to 3.6	2.0	—		
L-level input voltage	V _{ILA}	DIR, \overline{OE} , An	1.4 to 1.65	2.7 to 3.6	—	$0.30 \times V_{CCA}$	V	
	V _{ILB}	Bn	1.4 to 1.65	2.7 to 3.6	—	0.8		
H-level output voltage	V _{OHA}	V _{IN} = V _{IH} or V _{IL}	I _{OHA} = -100 μA	1.4 to 1.65	2.7 to 3.6	V _{CCA} - 0.2	—	V
			I _{OHA} = -1 mA	1.4	2.7 to 3.6	1.05	—	
	V _{OHB}		I _{OHB} = -100 μA	1.4 to 1.65	2.7 to 3.6	V _{CCB} - 0.2	—	
			I _{OHB} = -12 mA	1.4 to 1.65	3.0	2.2	—	
L-level output voltage	V _{OLA}	V _{IN} = V _{IH} or V _{IL}	I _{OLA} = 100 μA	1.4 to 1.65	2.7 to 3.6	—	0.2	V
			I _{OLA} = 1 mA	1.4	2.7 to 3.6	—	0.35	
	V _{OLB}		I _{OLB} = 100 μA	1.4 to 1.65	2.7 to 3.6	—	0.2	
			I _{OLB} = 12 mA	1.4 to 1.65	3.0	—	0.55	
3-state output OFF state current	I _{OZA}	V _{IN} = V _{IH} or V _{IL} V _{OUT} = 0 to 3.6 V	1.4 to 1.65	2.7 to 3.6	—	±5.0	μA	
	I _{OZB}	V _{IN} = V _{IH} or V _{IL} V _{OUT} = 0 to 3.6 V	1.4 to 1.65	2.7 to 3.6	—	±5.0		
Input leakage current	I _{IN}	V _{IN} (DIR, \overline{OE}) = 0 to 3.6 V	1.4 to 1.65	2.7 to 3.6	—	±2.0	μA	
Bushold input minimum drive hold current	I _{IHOLD}	V _{IN} = 0.8 V	1.4 to 1.65	3.0	75	—	μA	
		V _{IN} = 2.0 V	1.4 to 1.65	3.0	-75	—		
Bushold input over-drive current to change state (Note)	I _{IOD}	V _{IN} = "L" → "H"	1.4 to 1.65	3.6	—	550	μA	
		V _{IN} = "H" → "L"	1.4 to 1.65	3.6	—	-550		
Power-off leakage current	I _{OFF1}	V _{IN} , V _{OUT} = 0 to 3.6 V	0	0	—	5.0	μA	
	I _{OFF2}		1.4 to 1.65	0	—	5.0		
	I _{OFF3}		1.4 to 1.65	Open	—	5.0		
Quiescent supply current	I _{CCA}	V _{INA} = V _{CCA} or GND V _{INB} = V _{CCB} or GND	1.4 to 1.65	2.7 to 3.6	—	5.0	μA	
	I _{CCB}	V _{INA} = V _{CCA} or GND V _{INB} = V _{CCB} or GND	1.4 to 1.65	2.7 to 3.6	—	5.0		
	I _{CCA}	V _{CCA} ≤ (V _{IN} , V _{OUT}) ≤ 3.6 V	1.4 to 1.65	2.7 to 3.6	—	±5.0	μA	
	I _{CCB}	V _{CCB} ≤ (V _{IN} , V _{OUT}) ≤ 3.6 V	1.4 to 1.65	2.7 to 3.6	—	±5.0		
	I _{CCTB}	V _{INB} = V _{CCB} - 0.6 V per input	1.4 to 1.65	2.7 to 3.6	—	750.0		

Note: It is a necessary electric current to change the input in "L" or "H".

DC Characteristics (1.1 V ≤ V_{CCA} < 1.4 V, 2.7 V < V_{CCB} ≤ 3.6 V)

Characteristics	Symbol	Test Condition	V _{CCA} (V)	V _{CCB} (V)	Ta = -40 to 85°C		Unit
					Min	Max	
H-level input voltage	V _{IHA}	DIR, \overline{OE} , An	1.1 to 1.4	2.7 to 3.6	$0.65 \times V_{CCA}$	—	V
	V _{IHB}	Bn	1.1 to 1.4	2.7 to 3.6	2.0	—	
L-level input voltage	V _{ILA}	DIR, \overline{OE} , An	1.1 to 1.4	2.7 to 3.6	—	$0.30 \times V_{CCA}$	V
	V _{ILB}	Bn	1.1 to 1.4	2.7 to 3.6	—	0.8	
H-level output voltage	V _{OHA}	V _{IN} = V _{IH} or V _{IL}	I _{OHA} = -100 μA	1.1 to 1.4	2.7 to 3.6	V _{CCA} - 0.2	V
	V _{OHB}		I _{OHB} = -100 μA	1.1 to 1.4	2.7 to 3.6	V _{CCB} - 0.2	
			I _{OHB} = -12 mA	1.1 to 1.4	3.0	2.2	
L-level output voltage	V _{OLA}	V _{IN} = V _{IH} or V _{IL}	I _{OLA} = 100 μA	1.1 to 1.4	2.7 to 3.6	—	V
	V _{OLB}		I _{OLB} = 100 μA	1.1 to 1.4	2.7 to 3.6	—	
			I _{OLB} = 12 mA	1.1 to 1.4	3.0	0.55	
3-state output OFF state current	I _{OZA}	V _{IN} = V _{IH} or V _{IL} V _{OUT} = 0 to 3.6 V	1.1 to 1.4	2.7 to 3.6	—	±5.0	μA
	I _{OZB}	V _{IN} = V _{IH} or V _{IL} V _{OUT} = 0 to 3.6 V	1.1 to 1.4	2.7 to 3.6	—	±5.0	
Input leakage current	I _{IN}	V _{IN} (DIR, \overline{OE}) = 0 to 3.6 V	1.1 to 1.4	2.7 to 3.6	—	±2.0	μA
Bushold input minimum drive hold current	I _{IHOLD}	V _{IN} = 0.8 V	1.1 to 1.4	3.0	75	—	μA
		V _{IN} = 2.0 V	1.1 to 1.4	3.0	-75	—	
Bushold input over-drive current to change state (Note)	I _{IOD}	V _{IN} = "L" → "H"	1.1 to 1.4	3.6	—	550	μA
		V _{IN} = "H" → "L"	1.1 to 1.4	3.6	—	-550	
Power-off leakage current	I _{OFF1}	V _{IN} , V _{OUT} = 0 to 3.6 V	0	0	—	5.0	μA
	I _{OFF2}		1.1 to 1.4	0	—	5.0	
	I _{OFF3}		1.1 to 1.4	Open	—	5.0	
Quiescent supply current	I _{CCA}	V _{INA} = V _{CCA} or GND V _{INB} = V _{CCB} or GND	1.1 to 1.4	2.7 to 3.6	—	5.0	μA
	I _{CCB}	V _{INA} = V _{CCA} or GND V _{INB} = V _{CCB} or GND	1.1 to 1.4	2.7 to 3.6	—	5.0	
	I _{CCA}	V _{CCA} ≤ (V _{IN} , V _{OUT}) ≤ 3.6 V	1.1 to 1.4	2.7 to 3.6	—	±5.0	μA
	I _{CCB}	V _{CCB} ≤ (V _{IN} , V _{OUT}) ≤ 3.6 V	1.1 to 1.4	2.7 to 3.6	—	±5.0	
	I _{CCTB}	V _{INB} = V _{CCA} - 0.6 V per input	1.1 to 1.4	2.7 to 3.6	—	750.0	

Note: It is a necessary electric current to change the input in "L" or "H".

DC Characteristics (1.65 V ≤ V_{CCA} < 2.3 V, 2.3 V ≤ V_{CCB} ≤ 2.7 V)

Characteristics	Symbol	Test Condition	V _{CCA} (V)	V _{CCB} (V)	Ta = -40 to 85°C		Unit	
					Min	Max		
H-level input voltage	V _{IHA}	DIR, \overline{OE} , An	1.65 to 2.3	2.3 to 2.7	$0.65 \times V_{CCA}$	—	V	
	V _{IHB}	Bn	1.65 to 2.3	2.3 to 2.7	1.6	—		
L-level input voltage	V _{ILA}	DIR, \overline{OE} , An	1.65 to 2.3	2.3 to 2.7	—	$0.35 \times V_{CCA}$	V	
	V _{ILB}	Bn	1.65 to 2.3	2.3 to 2.7	—	0.7		
H-level output voltage	V _{OHA}	V _{IN} = V _{IH} or V _{IL}	I _{OHA} = -100 μA	1.65 to 2.3	2.3 to 2.7	V _{CCA} - 0.2	—	V
			I _{OHA} = -3 mA	1.65	2.3 to 2.7	1.25	—	
	V _{OHB}		I _{OHB} = -100 μA	1.65 to 2.3	2.3 to 2.7	V _{CCB} - 0.2	—	
			I _{OHB} = -9 mA	1.65 to 2.3	2.3	1.7	—	
L-level output voltage	V _{OLA}	V _{IN} = V _{IH} or V _{IL}	I _{OLA} = 100 μA	1.65 to 2.3	2.3 to 2.7	—	0.2	V
			I _{OLA} = 3 mA	1.65	2.3 to 2.7	—	0.3	
	V _{OLB}		I _{OLB} = 100 μA	1.65 to 2.3	2.3 to 2.7	—	0.2	
			I _{OLB} = 9mA	1.65 to 2.3	2.3	—	0.6	
3-state output OFF state current	I _{OZA}	V _{IN} = V _{IH} or V _{IL} V _{OUT} = 0 to 3.6 V	1.65 to 2.3	2.3 to 2.7	—	±5.0	μA	
	I _{OZB}	V _{IN} = V _{IH} or V _{IL} V _{OUT} = 0 to 3.6 V	1.65 to 2.3	2.3 to 2.7	—	±5.0		
Input leakage current	I _{IN}	V _{IN} (DIR, \overline{OE}) = 0 to 3.6 V	1.65 to 2.3	2.3 to 2.7	—	±2.0	μA	
Bushold input minimum drive hold current	I _{IHOLD}	V _{IN} = 0.7 V	1.65 to 2.3	2.3	45	—	μA	
		V _{IN} = 1.6 V	1.65 to 2.3	2.3	-45	—		
Bushold input over-drive current to change state (Note)	I _{IOD}	V _{IN} = "L" → "H"	1.65 to 2.3	2.7	—	450	μA	
		V _{IN} = "H" → "L"	1.65 to 2.3	2.7	—	-450		
Power-off leakage current	I _{OFF1}	V _{IN} , V _{OUT} = 0 to 3.6 V	0	0	—	5.0	μA	
	I _{OFF2}		1.65 to 2.3	0	—	5.0		
	I _{OFF3}		1.65 to 2.3	Open	—	5.0		
Quiescent supply current	I _{CCA}	V _{INA} = V _{CCA} or GND V _{INB} = V _{CCB} or GND	1.65 to 2.3	2.3 to 2.7	—	5.0	μA	
	I _{CCB}	V _{INA} = V _{CCA} or GND V _{INB} = V _{CCB} or GND	1.65 to 2.3	2.3 to 2.7	—	5.0		
	I _{CCA}	V _{CCA} ≤ (V _{IN} , V _{OUT}) ≤ 3.6 V	1.65 to 2.3	2.3 to 2.7	—	±5.0	μA	
	I _{CCB}	V _{CCB} ≤ (V _{IN} , V _{OUT}) ≤ 3.6 V	1.65 to 2.3	2.3 to 2.7	—	±5.0		

Note: It is a necessary electric current to change the input in "L" or "H".

DC Characteristics (1.4 V ≤ V_{CCA} < 1.65 V, 2.3 V ≤ V_{CCB} ≤ 2.7 V)

Characteristics	Symbol	Test Condition	V _{CCA} (V)	V _{CCB} (V)	Ta = -40 to 85°C		Unit	
					Min	Max		
H-level input voltage	V _{IHA}	DIR, \overline{OE} , An	1.4 to 1.65	2.3 to 2.7	$0.65 \times V_{CCA}$	—	V	
	V _{IHB}	Bn	1.4 to 1.65	2.3 to 2.7	1.6	—		
L-level input voltage	V _{ILA}	DIR, \overline{OE} , An	1.4 to 1.65	2.3 to 2.7	—	$0.30 \times V_{CCA}$	V	
	V _{ILB}	Bn	1.4 to 1.65	2.3 to 2.7	—	0.7		
H-level output voltage	V _{OHA}	V _{IN} = V _{IH} or V _{IL}	I _{OHA} = -100 μA	1.4 to 1.65	2.3 to 2.7	V _{CCA} - 0.2	—	V
			I _{OHA} = -1 mA	1.4	2.3 to 2.7	1.05	—	
	V _{OHB}		I _{OHB} = -100 μA	1.4 to 1.65	2.3 to 2.7	V _{CCB} - 0.2	—	
			I _{OHB} = -9 mA	1.4 to 1.65	2.3	1.7	—	
L-level output voltage	V _{OLA}	V _{IN} = V _{IH} or V _{IL}	I _{OLA} = 100 μA	1.4 to 1.65	2.3 to 2.7	—	0.2	V
			I _{OLA} = 1 mA	1.4	2.3 to 2.7	—	0.35	
	V _{OLB}		I _{OLB} = 100 μA	1.4 to 1.65	2.3 to 2.7	—	0.2	
			I _{OLB} = 9mA	1.4 to 1.65	2.3	—	0.6	
3-state output OFF state current	I _{OZA}	V _{IN} = V _{IH} or V _{IL} V _{OUT} = 0 to 3.6 V	1.4 to 1.65	2.3 to 2.7	—	±5.0	μA	
	I _{OZB}	V _{IN} = V _{IH} or V _{IL} V _{OUT} = 0 to 3.6 V	1.4 to 1.65	2.3 to 2.7	—	±5.0		
Input leakage current	I _{IN}	V _{IN} (DIR, \overline{OE}) = 0 to 3.6 V	1.4 to 1.65	2.3 to 2.7	—	±2.0	μA	
Bushold input minimum drive hold current	I _{IHOLD}	V _{IN} = 0.7 V	1.4 to 1.65	2.3	45	—	μA	
		V _{IN} = 1.6 V	1.4 to 1.65	2.3	-45	—		
Bushold input over-drive current to change state (Note)	I _{IOD}	V _{IN} = "L" → "H"	1.4 to 1.65	2.7	—	450	μA	
		V _{IN} = "H" → "L"	1.4 to 1.65	2.7	—	-450		
Power-off leakage current	I _{OFF1}	V _{IN} , V _{OUT} = 0 to 3.6 V	0	0	—	5.0	μA	
	I _{OFF2}		1.4 to 1.65	0	—	5.0		
	I _{OFF3}		1.4 to 1.65	Open	—	5.0		
Quiescent supply current	I _{CCA}	V _{INA} = V _{CCA} or GND V _{INB} = V _{CCB} or GND	1.4 to 1.65	2.3 to 2.7	—	5.0	μA	
	I _{CCB}	V _{INA} = V _{CCA} or GND V _{INB} = V _{CCB} or GND	1.4 to 1.65	2.3 to 2.7	—	5.0		
	I _{CCA}	V _{CCA} ≤ (V _{IN} , V _{OUT}) ≤ 3.6 V	1.4 to 1.65	2.3 to 2.7	—	±5.0	μA	
	I _{CCB}	V _{CCB} ≤ (V _{IN} , V _{OUT}) ≤ 3.6 V	1.4 to 1.65	2.3 to 2.7	—	±5.0		

Note: It is a necessary electric current to change the input in "L" or "H".

DC Characteristics (1.1 V ≤ V_{CCA} < 1.4 V, 2.3 V ≤ V_{CCB} ≤ 2.7 V)

Characteristics	Symbol	Test Condition	V _{CCA} (V)	V _{CCB} (V)	Ta = -40 to 85°C		Unit
					Min	Max	
H-level input voltage	V _{IHA}	DIR, \overline{OE} , An	1.1 to 1.4	2.3 to 2.7	$0.65 \times V_{CCA}$	—	V
	V _{IHB}	Bn	1.1 to 1.4	2.3 to 2.7	1.6	—	
L-level input voltage	V _{ILA}	DIR, \overline{OE} , An	1.1 to 1.4	2.3 to 2.7	—	$0.30 \times V_{CCA}$	V
	V _{ILB}	Bn	1.1 to 1.4	2.3 to 2.7	—	0.7	
H-level output voltage	V _{OHA}	V _{IN} = V _{IH} or V _{IL}	I _{OHA} = -100 μA	1.1 to 1.4	2.3 to 2.7	V _{CCA} - 0.2	V
	V _{OHB}		I _{OHB} = -100 μA	1.1 to 1.4	2.3 to 2.7	V _{CCB} - 0.2	
			I _{OHB} = -9 mA	1.1 to 1.4	2.3	1.7	
L-level output voltage	V _{OLA}	V _{IN} = V _{IH} or V _{IL}	I _{OLA} = 100 μA	1.1 to 1.4	2.3 to 2.7	—	V
	V _{OLB}		I _{OLB} = 100 μA	1.1 to 1.4	2.3 to 2.7	—	
			I _{OLB} = 9 mA	1.1 to 1.4	2.3	—	
3-state output OFF state current	I _{OZA}	V _{IN} = V _{IH} or V _{IL} V _{OUT} = 0 to 3.6 V	1.1 to 1.4	2.3 to 2.7	—	±5.0	μA
	I _{OZB}	V _{IN} = V _{IH} or V _{IL} V _{OUT} = 0 to 3.6 V	1.1 to 1.4	2.3 to 2.7	—	±5.0	
Input leakage current	I _{IN}	V _{IN} (DIR, \overline{OE}) = 0 to 3.6 V	1.1 to 1.4	2.3 to 2.7	—	±2.0	μA
Bushold input minimum drive hold current	I _{IHOLD}	V _{IN} = 0.7 V	1.1 to 1.4	2.3	45	—	μA
		V _{IN} = 1.6 V	1.1 to 1.4	2.3	-45	—	
Bushold input over-drive current to change state (Note)	I _{IOD}	V _{IN} = "L" → "H"	1.1 to 1.4	2.7	—	450	μA
		V _{IN} = "H" → "L"	1.1 to 1.4	2.7	—	-450	
Power-off leakage current	I _{OFF1}	V _{IN} , V _{OUT} = 0 to 3.6 V	0	0	—	5.0	μA
	I _{OFF2}		1.1 to 1.4	0	—		
	I _{OFF3}		1.1 to 1.4	Open	—		
Quiescent supply current	I _{CCA}	V _{INA} = V _{CCA} or GND V _{INB} = V _{CCB} or GND	1.1 to 1.4	2.3 to 2.7	—	5.0	μA
	I _{CCB}	V _{INA} = V _{CCA} or GND V _{INB} = V _{CCB} or GND	1.1 to 1.4	2.3 to 2.7	—	5.0	
	I _{CCA}	V _{CCA} ≤ (V _{IN} , V _{OUT}) ≤ 3.6 V	1.1 to 1.4	2.3 to 2.7	—	±5.0	μA
	I _{CCB}	V _{CCB} ≤ (V _{IN} , V _{OUT}) ≤ 3.6 V	1.1 to 1.4	2.3 to 2.7	—	±5.0	

Note: It is a necessary electric current to change the input in "L" or "H".

DC Characteristics (1.1 V ≤ V_{CCA} < 1.4 V, 1.65 V ≤ V_{CCB} < 2.3 V)

Characteristics	Symbol	Test Condition	V _{CCA} (V)	V _{CCB} (V)	Ta = -40 to 85°C		Unit	
					Min	Max		
H-level input voltage	V _{IHA}	DIR, \overline{OE} , An	1.1 to 1.4	1.65 to 2.3	$0.65 \times V_{CCA}$	—	V	
	V _{IHB}	Bn	1.1 to 1.4	1.65 to 2.3	$0.65 \times V_{CCB}$	—		
L-level input voltage	V _{ILA}	DIR, \overline{OE} , An	1.1 to 1.4	1.65 to 2.3	—	$0.30 \times V_{CCA}$	V	
	V _{ILB}	Bn	1.1 to 1.4	1.65 to 2.3	—	$0.35 \times V_{CCB}$		
H-level output voltage	V _{OHA}	V _{IN} = V _{IH} or V _{IL}	I _{OHA} = -100 μA	1.1 to 1.4	1.65 to 2.3	V _{CCA} - 0.2	—	V
			I _{OHB} = -100 μA	1.1 to 1.4	1.65 to 2.3	V _{CCB} - 0.2	—	
	I _{OHB} = -3 mA		1.1 to 1.4	1.65	1.25	—		
L-level output voltage	V _{OLA}	V _{IN} = V _{IH} or V _{IL}	I _{OLA} = 100 μA	1.1 to 1.4	1.65 to 2.3	—	0.2	V
			I _{OLB} = 100 μA	1.1 to 1.4	1.65 to 2.3	—	0.2	
	I _{OLB} = 3 mA		1.1 to 1.4	1.65	—	0.3		
3-state output OFF state current	I _{OZA}	V _{IN} = V _{IH} or V _{IL} V _{OUT} = 0 to 3.6 V	1.1 to 1.4	1.65 to 2.3	—	±5.0	μA	
	I _{OZB}	V _{IN} = V _{IH} or V _{IL} V _{OUT} = 0 to 3.6 V	1.1 to 1.4	1.65 to 2.3	—	±5.0		
Input leakage current	I _{IN}	V _{IN} (DIR, \overline{OE}) = 0 to 3.6 V	1.1 to 1.4	1.65 to 2.3	—	±2.0	μA	
Bushold input minimum drive hold current	I _{IHOLD}	V _{IN} = 0.58 V	1.1 to 1.4	1.65	20	—	μA	
		V _{IN} = 1.07 V	1.1 to 1.4	1.65	-20	—		
Bushold input over-drive current to change state (Note)	I _{IOD}	V _{IN} = "L" → "H"	1.1 to 1.4	1.95	—	300	μA	
		V _{IN} = "H" → "L"	1.1 to 1.4	1.95	—	-300		
Power-off leakage current	I _{OFF1}	V _{IN} , V _{OUT} = 0 to 3.6 V	0	0	—	5.0	μA	
	I _{OFF2}		1.1 to 1.4	0	—	5.0		
	I _{OFF3}		1.1 to 1.4	Open	—	5.0		
Quiescent supply current	I _{CCA}	V _{INA} = V _{CCA} or GND V _{INB} = V _{CCB} or GND	1.1 to 1.4	1.65 to 2.3	—	5.0	μA	
	I _{CCB}	V _{INA} = V _{CCA} or GND V _{INB} = V _{CCB} or GND	1.1 to 1.4	1.65 to 2.3	—	5.0		
	I _{CCA}	V _{CCA} ≤ (V _{IN} , V _{OUT}) ≤ 3.6 V	1.1 to 1.4	1.65 to 2.3	—	±5.0	μA	
	I _{CCB}	V _{CCB} ≤ (V _{IN} , V _{OUT}) ≤ 3.6 V	1.1 to 1.4	1.65 to 2.3	—	±5.0		

Note: It is a necessary electric current to change the input in "L" or "H".

AC Characteristics (Ta = -40 to 85°C, Input: tr = tf = 2.0 ns)

VCCA = 2.5 ± 0.2 V, VCCB = 3.3 ± 0.3 V

Characteristics	Symbol	Test Condition	Min	Max	Unit
Propagation delay time (Bn → An)	t _{pLH} t _{pHL}	Figure 1, Figure 2	1.0	5.4	ns
3-state output enable time (\overline{OE} → An)	t _{pZL} t _{pZH}	Figure 1, Figure 3	1.0	8.4	
3-state output disable time (\overline{OE} → An)	t _{pLZ} t _{pHZ}	Figure 1, Figure 3	1.0	6.7	
Propagation delay time (An → Bn)	t _{pLH} t _{pHL}	Figure 1, Figure 2	1.0	6.8	ns
3-state output enable time (\overline{OE} → Bn)	t _{pZL} t _{pZH}	Figure 1, Figure 3	1.0	8.7	
3-state output disable time (\overline{OE} → Bn)	t _{pLZ} t _{pHZ}	Figure 1, Figure 3	1.0	3.9	
Output to output skew	t _{osLH} t _{osHL}	(Note)		0.5	ns

Note: Parameter guaranteed by design.

$$(t_{osLH} = |t_{pLHm} - t_{pLHn}|, t_{osHL} = |t_{pHLm} - t_{pHLn}|)$$

VCCA = 1.8 ± 0.15 V, VCCB = 3.3 ± 0.3 V

Characteristics	Symbol	Test Condition	Min	Max	Unit
Propagation delay time (Bn → An)	t _{pLH} t _{pHL}	Figure 1, Figure 2	1.0	8.9	ns
3-state output enable time (\overline{OE} → An)	t _{pZL} t _{pZH}	Figure 1, Figure 3	1.0	13.4	
3-state output disable time (\overline{OE} → An)	t _{pLZ} t _{pHZ}	Figure 1, Figure 3	1.0	10.9	
Propagation delay time (An → Bn)	t _{pLH} t _{pHL}	Figure 1, Figure 2	1.0	7.8	ns
3-state output enable time (\overline{OE} → Bn)	t _{pZL} t _{pZH}	Figure 1, Figure 3	1.0	10.7	
3-state output disable time (\overline{OE} → Bn)	t _{pLZ} t _{pHZ}	Figure 1, Figure 3	1.0	5.2	
Output to output skew	t _{osLH} t _{osHL}	(Note)	—	0.5	ns

Note: Parameter guaranteed by design.

$$(t_{osLH} = |t_{pLHm} - t_{pLHn}|, t_{osHL} = |t_{pHLm} - t_{pHLn}|)$$

$V_{CCA} = 1.5 \pm 0.1 \text{ V}$, $V_{CCB} = 3.3 \pm 0.3 \text{ V}$

Characteristics	Symbol	Test Condition	Min	Max	Unit
Propagation delay time (Bn → An)	t_{pLH} t_{pHL}	Figure 1, Figure 2	1.0	10.3	ns
3-state output enable time (\overline{OE} → An)	t_{pZL} t_{pZH}	Figure 1, Figure 3	1.0	18.5	
3-state output disable time (\overline{OE} → An)	t_{pLZ} t_{pHZ}	Figure 1, Figure 3	1.0	13.0	
Propagation delay time (An → Bn)	t_{pLH} t_{pHL}	Figure 1, Figure 2	1.0	8.6	ns
3-state output enable time (\overline{OE} → Bn)	t_{pZL} t_{pZH}	Figure 1, Figure 3	1.0	14.3	
3-state output disable time (\overline{OE} → Bn)	t_{pLZ} t_{pHZ}	Figure 1, Figure 3	1.0	6.6	
Output to output skew	$t_{oS LH}$ $t_{oS HL}$	(Note)	—	1.5	ns

Note: Parameter guaranteed by design.

$$(t_{oS LH} = |t_{pLHm} - t_{pLHn}|, t_{oS HL} = |t_{pHLm} - t_{pHLn}|)$$

$V_{CCA} = 1.2 \pm 0.1 \text{ V}$, $V_{CCB} = 3.3 \pm 0.3 \text{ V}$

Characteristics	Symbol	Test Condition	Min	Max	Unit
Propagation delay time (Bn → An)	t_{pLH} t_{pHL}	Figure 1, Figure 2	1.0	61	ns
3-state output enable time (\overline{OE} → An)	t_{pZL} t_{pZH}	Figure 1, Figure 3	1.0	95	
3-state output disable time (\overline{OE} → An)	t_{pLZ} t_{pHZ}	Figure 1, Figure 3	1.0	44	
Propagation delay time (An → Bn)	t_{pLH} t_{pHL}	Figure 1, Figure 2	1.0	22	ns
3-state output enable time (\overline{OE} → Bn)	t_{pZL} t_{pZH}	Figure 1, Figure 3	1.0	52	
3-state output disable time (\overline{OE} → Bn)	t_{pLZ} t_{pHZ}	Figure 1, Figure 3	1.0	18	
Output to output skew	$t_{oS LH}$ $t_{oS HL}$	(Note)	—	1.5	ns

Note: Parameter guaranteed by design.

$$(t_{oS LH} = |t_{pLHm} - t_{pLHn}|, t_{oS HL} = |t_{pHLm} - t_{pHLn}|)$$

$V_{CCA} = 1.8 \pm 0.15 \text{ V}$, $V_{CCB} = 2.5 \pm 0.2 \text{ V}$

Characteristics	Symbol	Test Condition	Min	Max	Unit
Propagation delay time (Bn → An)	t_{pLH} t_{pHL}	Figure 1, Figure 2	1.0	9.1	ns
3-state output enable time (\overline{OE} → An)	t_{pZL} t_{pZH}	Figure 1, Figure 3	1.0	13.5	
3-state output disable time (\overline{OE} → An)	t_{pLZ} t_{pHZ}	Figure 1, Figure 3	1.0	11.8	
Propagation delay time (An → Bn)	t_{pLH} t_{pHL}	Figure 1, Figure 2	1.0	9.5	ns
3-state output enable time (\overline{OE} → Bn)	t_{pZL} t_{pZH}	Figure 1, Figure 3	1.0	12.6	
3-state output disable time (\overline{OE} → Bn)	t_{pLZ} t_{pHZ}	Figure 1, Figure 3	1.0	5.1	
Output to output skew	$t_{oS LH}$ $t_{oS HL}$	(Note 1)	—	0.5	ns

Note: Parameter guaranteed by design.

$$(t_{oS LH} = |t_{pLHm} - t_{pLHn}|, t_{oS HL} = |t_{pHLm} - t_{pHLn}|)$$

$V_{CCA} = 1.5 \pm 0.1 \text{ V}$, $V_{CCB} = 2.5 \pm 0.2 \text{ V}$

Characteristics	Symbol	Test Condition	Min	Max	Unit
Propagation delay time (Bn → An)	t_{pLH} t_{pHL}	Figure 1, Figure 2	1.0	10.8	ns
3-state output enable time (\overline{OE} → An)	t_{pZL} t_{pZH}	Figure 1, Figure 3	1.0	18.3	
3-state output disable time (\overline{OE} → An)	t_{pLZ} t_{pHZ}	Figure 1, Figure 3	1.0	14.2	
Propagation delay time (An → Bn)	t_{pLH} t_{pHL}	Figure 1, Figure 2	1.0	10.5	ns
3-state output enable time (\overline{OE} → Bn)	t_{pZL} t_{pZH}	Figure 1, Figure 3	1.0	15.4	
3-state output disable time (\overline{OE} → Bn)	t_{pLZ} t_{pHZ}	Figure 1, Figure 3	1.0	6.4	
Output to output skew	$t_{oS LH}$ $t_{oS HL}$	(Note)	—	1.5	ns

Note: Parameter guaranteed by design.

$$(t_{oS LH} = |t_{pLHm} - t_{pLHn}|, t_{oS HL} = |t_{pHLm} - t_{pHLn}|)$$

$V_{CCA} = 1.2 \pm 0.1 \text{ V}$, $V_{CCB} = 2.5 \pm 0.2 \text{ V}$

Characteristics	Symbol	Test Condition	Min	Max	Unit
Propagation delay time (Bn → An)	t_{pLH} t_{pHL}	Figure 1, Figure 2	1.0	60	ns
3-state output enable time (\overline{OE} → An)	t_{pZL} t_{pZH}	Figure 1, Figure 3	1.0	95	
3-state output disable time (\overline{OE} → An)	t_{pLZ} t_{pHZ}	Figure 1, Figure 3	1.0	45	
Propagation delay time (An → Bn)	t_{pLH} t_{pHL}	Figure 1, Figure 2	1.0	23	ns
3-state output enable time (\overline{OE} → Bn)	t_{pZL} t_{pZH}	Figure 1, Figure 3	1.0	54	
3-state output disable time (\overline{OE} → Bn)	t_{pLZ} t_{pHZ}	Figure 1, Figure 3	1.0	17	
Output to output skew	$t_{oS LH}$ $t_{oS HL}$	(Note)	—	1.5	ns

Note: Parameter guaranteed by design.

$$(t_{oS LH} = |t_{pLHm} - t_{pLHn}|, t_{oS HL} = |t_{pHLm} - t_{pHLn}|)$$

$V_{CCA} = 1.2 \pm 0.1 \text{ V}$, $V_{CCB} = 1.8 \pm 0.15 \text{ V}$

Characteristics	Symbol	Test Condition	Min	Max	Unit
Propagation delay time (Bn → An)	t_{pLH} t_{pHL}	Figure 1, Figure 2	1.0	58	ns
3-state output enable time (\overline{OE} → An)	t_{pZL} t_{pZH}	Figure 1, Figure 3	1.0	92	
3-state output disable time (\overline{OE} → An)	t_{pLZ} t_{pHZ}	Figure 1, Figure 3	1.0	47	
Propagation delay time (An → Bn)	t_{pLH} t_{pHL}	Figure 1, Figure 2	1.0	30	ns
3-state output enable time (\overline{OE} → Bn)	t_{pZL} t_{pZH}	Figure 1, Figure 3	1.0	55	
3-state output disable time (\overline{OE} → Bn)	t_{pLZ} t_{pHZ}	Figure 1, Figure 3	1.0	17	
Output to output skew	$t_{oS LH}$ $t_{oS HL}$	(Note)	—	1.5	ns

Note: Parameter guaranteed by design.

$$(t_{oS LH} = |t_{pLHm} - t_{pLHn}|, t_{oS HL} = |t_{pHLm} - t_{pHLn}|)$$

Dynamic Switching Characteristics (Ta = 25°C, Input: tr = tf = 2.0 ns, CL = 30 pF)

Characteristics		Symbol	Test Condition	VCC (V)		Typ.	Unit
				VCCA (V)	VCCB (V)		
Quiet output maximum dynamic VOL	A → B	VOLP	VIH = VCC, VIL = 0 V (Note)	2.5	3.3	0.8	V
				1.8	3.3	0.8	
				1.8	2.5	0.6	
	B → A			2.5	3.3	0.6	
				1.8	3.3	0.25	
				1.8	2.5	0.25	
Quiet output minimum dynamic VOL	A → B	VOLV	VIH = VCC, VIL = 0 V (Note)	2.5	3.3	-0.8	V
				1.8	3.3	-0.8	
				1.8	2.5	-0.6	
	B → A			2.5	3.3	-0.6	
				1.8	3.3	-0.25	
				1.8	2.5	-0.25	
Quiet output maximum dynamic VOH	A → B	VOHP	VIH = VCC, VIL = 0 V (Note)	2.5	3.3	4.6	V
				1.8	3.3	4.6	
				1.8	2.5	3.3	
	B → A			2.5	3.3	3.3	
				1.8	3.3	2.3	
				1.8	2.5	2.3	
Quiet output minimum dynamic VOH	A → B	VOHV	VIH = VCC, VIL = 0 V (Note)	2.5	3.3	2.0	V
				1.8	3.3	2.0	
				1.8	2.5	1.7	
	B → A			2.5	3.3	1.7	
				1.8	3.3	1.3	
				1.8	2.5	1.3	

Note: Parameter guaranteed by design.

Capacitive Characteristics (Ta = 25°C)

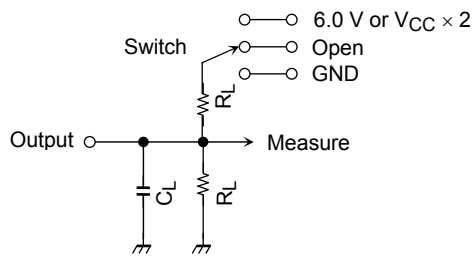
Characteristics	Symbol	Test Circuit		VCC (V)		Typ.	Unit
				VCCA (V)	VCCB (V)		
Input capacitance	CIN	DIR, OE		2.5	3.3	7	pF
Bus I/O capacitance	C _{I/O}	An, Bn		2.5	3.3	8	pF
Power dissipation capacitance (Note)	CPDA	OE = "L"	A → B (DIR = "H")	2.5	3.3	3	pF
			B → A (DIR = "L")	2.5	3.3	16	
		OE = "H"	A → B (DIR = "H")	2.5	3.3	0	
			B → A (DIR = "L")	2.5	3.3	0	
	CPDB	OE = "L"	A → B (DIR = "H")	2.5	3.3	16	
			B → A (DIR = "L")	2.5	3.3	5	
		OE = "H"	A → B (DIR = "H")	2.5	3.3	0	
			B → A (DIR = "L")	2.5	3.3	1	

Note: CPD is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:

$$I_{CC (opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/4 \text{ (per bit)}$$

AC Test Circuit



Parameter	Switch
t_{pLH}, t_{pHL}	Open
t_{pLZ}, t_{pZL}	6.0 V @ $V_{CC} = 3.3 \pm 0.3$ V
	$V_{CC} \times 2$ @ $V_{CC} = 2.5 \pm 0.2$ V
	@ $V_{CC} = 1.8 \pm 0.15$ V
	@ $V_{CC} = 1.5 \pm 0.1$ V
@ $V_{CC} = 1.2 \pm 0.1$ V	
t_{pHZ}, t_{pZH}	GND

Symbol	V_{CC} (output)			
	3.3 ± 0.3 V 2.5 ± 0.2 V	1.8 ± 0.15 V	1.5 ± 0.1 V	1.2 ± 0.1 V
R_L	500 Ω	1 k Ω	2 k Ω	10 k Ω
C_L	30 pF	30 pF	15 pF	15 pF

Figure 1

Not Recommended for New Design

AC Waveform

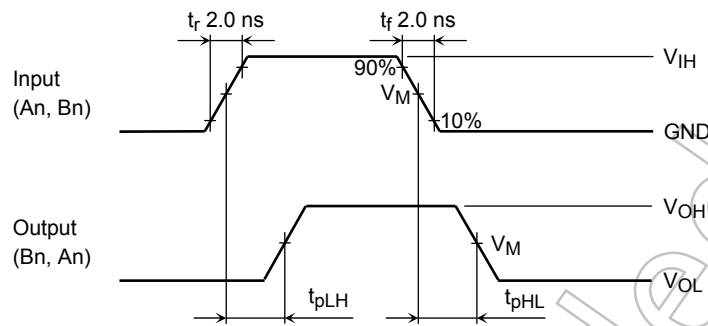


Figure 2 t_{pLH} , t_{pHL}

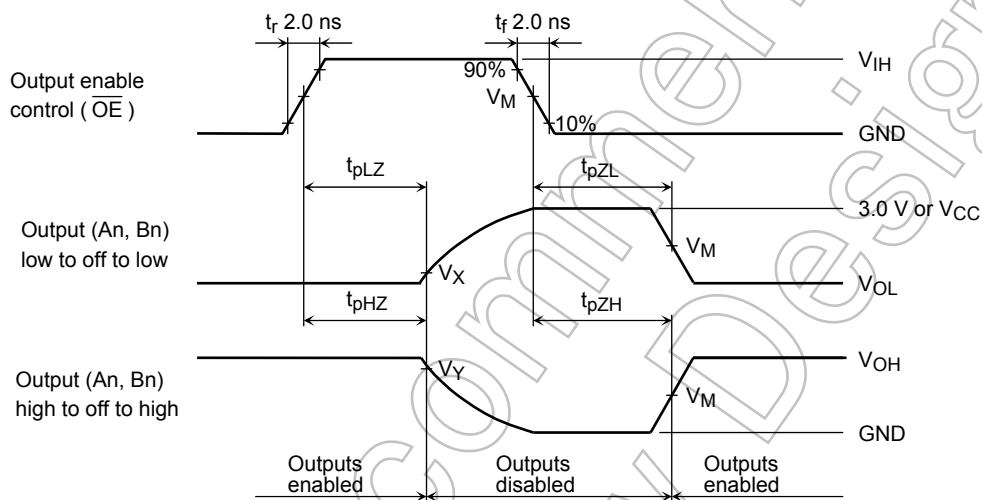


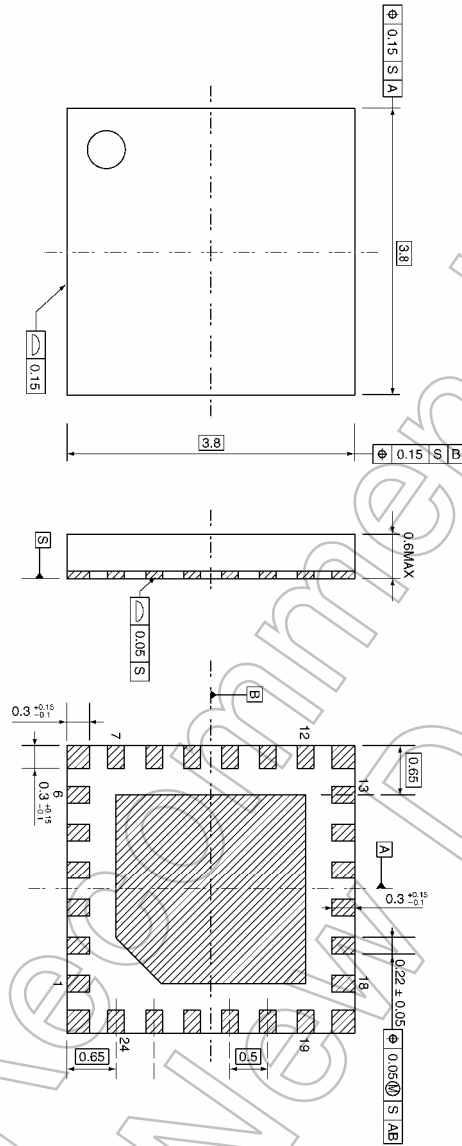
Figure 3 t_{pLZ} , t_{pHZ} , t_{pZL} , t_{pZH}

Symbol	V_{CC}		
	$3.3 \pm 0.3 \text{ V}$	$2.5 \pm 0.2 \text{ V}$ $1.8 \pm 0.15 \text{ V}$	$1.5 \pm 0.1 \text{ V}$ $1.2 \pm 0.1 \text{ V}$
V_{IH}	2.7 V	V_{CC}	V_{CC}
V_M	1.5 V	$V_{CC}/2$	$V_{CC}/2$
V_X	$V_{OL} + 0.3 \text{ V}$	$V_{OL} + 0.15 \text{ V}$	$V_{OL} + 0.1 \text{ V}$
V_Y	$V_{OH} - 0.3 \text{ V}$	$V_{OH} - 0.15 \text{ V}$	$V_{OH} - 0.1 \text{ V}$

Package Dimensions

VQON24-P-0404-0.50

Unit: mm



Weight: 0.03 g (typ.)

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