TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

TC74AC390P, TC74AC390F

Dual Decade Counter

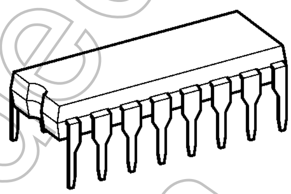
The TC74AC390 is an advanced high speed CMOS DUAL DECADE COUNTER fabricated with silicon gate and double-layer metal wiring C^2MOS technology.

It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

It consists of two independent 4-bit counters, each composed of a divide-by-two and a divide-by-five counter. The divide-by-two counter is incremented on the negative going transition of clock A ($\overline{CKA}$). The divided-by-five counter is incremented on the negative going transition of clock B ($\overline{CKB}$). The counter can be cascaded to form decade, bi-quinary, or various combinations up to a divide-by-100 counter. When the CLEAR input is set high, the Q outputs are set to low independent of the clock inputs.

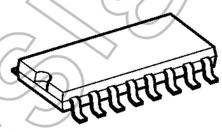
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

TC74AC390P



DIP16-P-300-2.54A

TC74AC390F



SOP16-P-300-1.27A

Weight

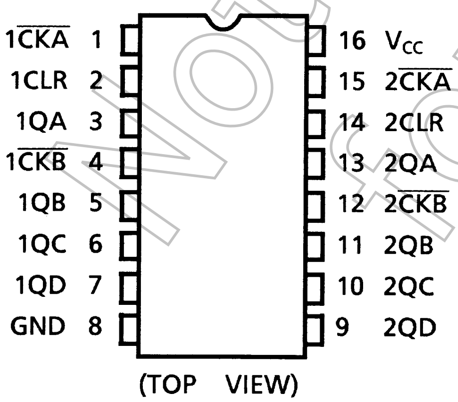
DIP16-P-300-2.54A : 1.00 g (typ.)

SOP16-P-300-1.27A : 0.18 g (typ.)

Features

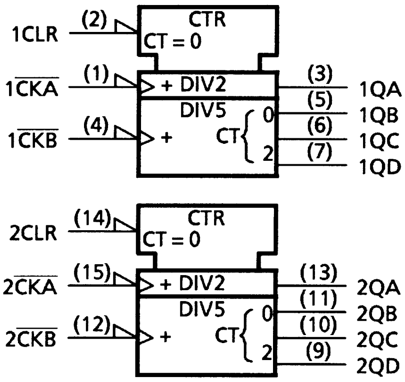
- High speed: f_{max} = 160 MHz (typ.) at V_{CC} = 5 V
- Low power dissipation: I_{CC} = 8 μA (max) at Ta = 25°C
- High noise immunity: $V_{NIH} = V_{NIL}$ = 28% V_{CC} (min)
- Symmetrical output impedance: $|I_{OH}| = I_{OL}$ = 24 mA (min)
  Capability of driving 50 Ω transmission lines.
- Balanced propagation delays: $t_{pLH} \simeq t_{pHL}$
- Wide operating voltage range: V_{CC} (opr) = 2 to 5.5 V
- Pin and function compatible with 74HC390

Pin Assignment

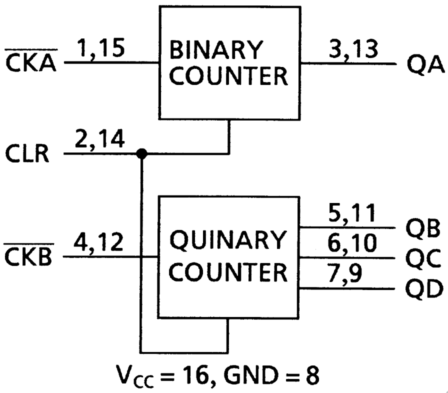


Start of commercial production
1988-10

IEC Logic Symbol



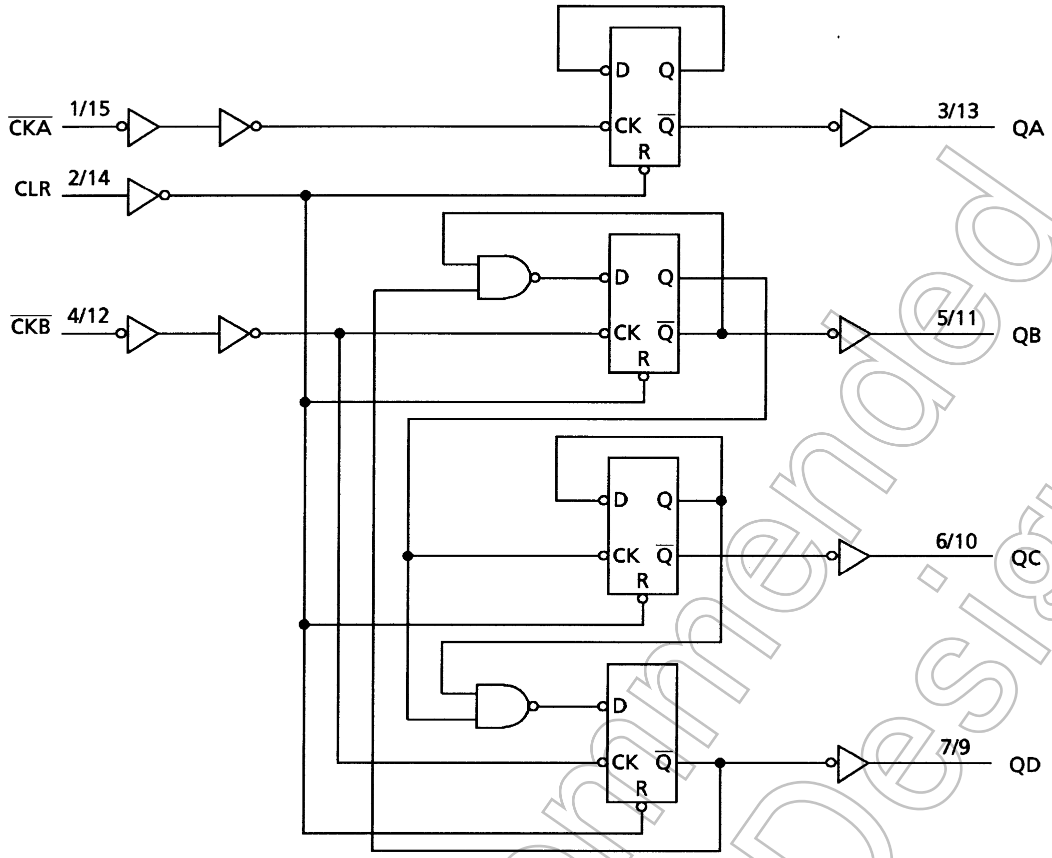
Block Diagram



Truth Table

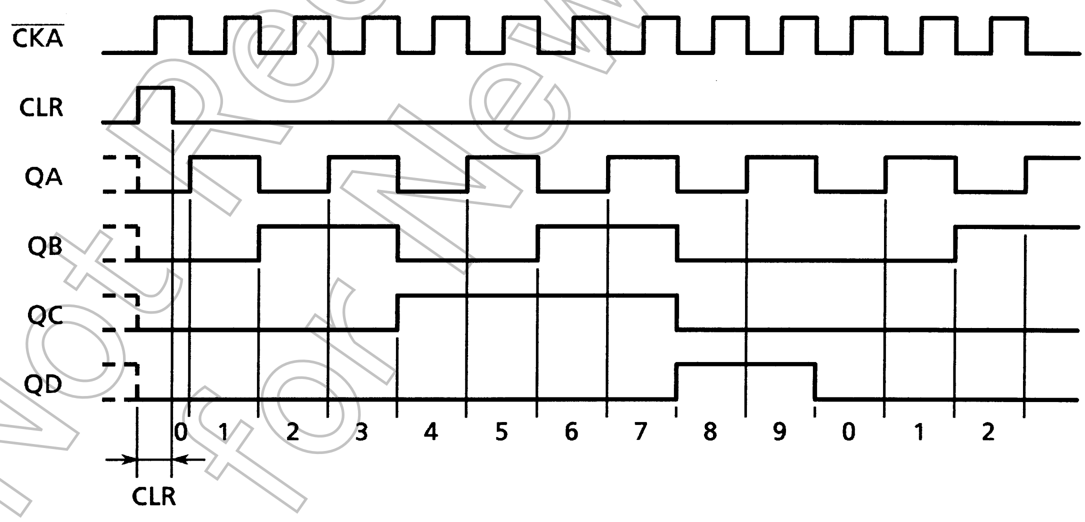
Inputs			Outputs			
$\overline{CKA}$	$\overline{CKB}$	CLR	QA	QB	QC	QD
X	X	H	L	L	L	L
⎺_ (falling edge)	X	L	Binary Count Up			
X	⎺_ (falling edge)	L	Quinary Count Up			

System Diagram



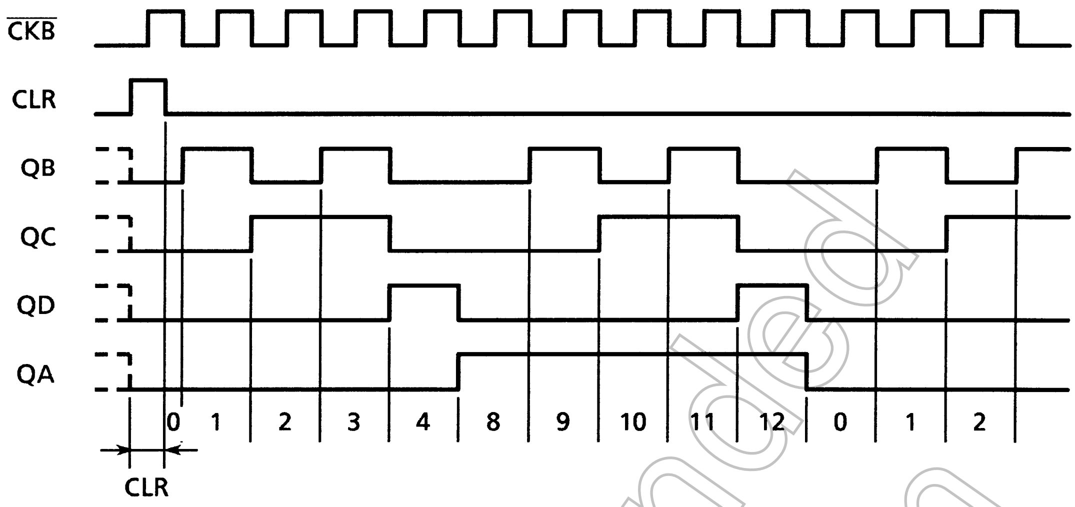
Timing Chart

(1) BCD count sequence (Note)



Note: QA connected to $\overline{CKB}$

(2) Bi-quinary count sequence (Note)



Note: QD connected to $\overline{CKA}$

Absolute Maximum Ratings (Note 1)

Characteristics	Symbol	Rating	Unit
Supply voltage range	V_{CC}	−0.5 to 7.0	V
DC input voltage	V_{IN}	−0.5 to V_{CC} + 0.5	V
DC output voltage	V_{OUT}	−0.5 to V_{CC} + 0.5	V
Input diode current	I_{IK}	±20	mA
Output diode current	I_{OK}	±50	mA
DC output current	I_{OUT}	±50	mA
DC V_{CC}/ground current	I_{CC}	±200	mA
Power dissipation	P_D	500 (DIP) (Note 2)/180 (SOP)	mW
Storage temperature	T_{stg}	−65 to 150	°C

Note 1: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.
Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/Derating Concept and Methods) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 2: 500 mW in the range of Ta = −40 to 65°C. From Ta = 65 to 85°C a derating factor of −10 mW/°C should be applied up to 300 mW.

Operating Ranges (Note)

Characteristics	Symbol	Rating	Unit
Supply voltage	V_{CC}	2.0 to 5.5	V
Input voltage	V_{IN}	0 to V_{CC}	V
Output voltage	V_{OUT}	0 to V_{CC}	V
Operating temperature	T_{opr}	−40 to 85	°C
Input rise and fall time	dt/dV	0 to 100 (V_{CC} = 3.3 ± 0.3 V) 0 to 20 (V_{CC} = 5 ± 0.5 V)	ns/V

Note: The operating ranges must be maintained to ensure the normal operation of the device.
Unused inputs must be tied to either V_{CC} or GND.

Electrical Characteristics

DC Characteristics

Characteristics	Symbol	Test Condition		V_{CC} (V)	Ta = 25°C Min	Ta = 25°C Typ.	Ta = 25°C Max	Ta = −40 to 85°C Min	Ta = −40 to 85°C Max	Unit
High-level input voltage	V_{IH}	—		2.0	1.50	—	—	1.50	—	V
				3.0	2.10	—	—	2.10	—	
				5.5	3.85	—	—	3.85	—	
Low-level input voltage	V_{IL}	—		2.0	—	—	0.50	—	0.50	V
				3.0	—	—	0.90	—	0.90	
				5.5	—	—	1.65	—	1.65	
High-level output voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = −50 μA	2.0	1.9	2.0	—	1.9	—	V
				3.0	2.9	3.0	—	2.9	—	
				4.5	4.4	4.5	—	4.4	—	
			I_{OH} = −4 mA	3.0	2.58	—	—	2.48	—	
			I_{OH} = −24 mA	4.5	3.94	—	—	3.80	—	
			I_{OH} = −75 mA (Note)	5.5	—	—	—	3.85	—	
Low-level output voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 50 μA	2.0	—	0.0	0.1	—	0.1	V
				3.0	—	0.0	0.1	—	0.1	
				4.5	—	0.0	0.1	—	0.1	
			I_{OL} = 12 mA	3.0	—	—	0.36	—	0.44	
			I_{OL} = 24 mA	4.5	—	—	0.36	—	0.44	
			I_{OL} = 75 mA (Note)	5.5	—	—	—	—	1.65	
Input leakage current	I_{IN}	V_{IN} = V_{CC} or GND		5.5	—	—	±0.1	—	±1.0	μA
Quiescent supply current	I_{CC}	V_{IN} = V_{CC} or GND		5.5	—	—	8.0	—	80.0	μA

Note: This spec indicates the capability of driving 50 Ω transmission lines.

One output should be tested at a time for a 10 ms maximum duration.

Timing Requirements (input: $t_r = t_f = 3$ ns)

Characteristics	Symbol	Test Condition	V_{CC} (V)	Ta = 25°C Limit	Ta = −40 to 85°C Limit	Unit
Minimum pulse width ($\overline{CKA}$, $\overline{CKB}$)	$t_{W(H)}$, $t_{W(L)}$	—	3.3 ± 0.3	7.0	7.0	ns
			5.0 ± 0.5	5.0	5.0	
Minimum pulse width (CLR)	$t_{W(H)}$	—	3.3 ± 0.3	7.0	7.0	ns
			5.0 ± 0.5	5.0	5.0	
Minimum removal time	t_{rem}	—	3.3 ± 0.3	7.0	7.0	ns
			5.0 ± 0.5	3.5	3.5	

AC Characteristics (C_L = 50 pF, R_L = 500 Ω, input: $t_r = t_f$ = 3 ns)

Characteristics	Symbol	Test Condition		Ta = 25°C			Ta = −40 to 85°C		Unit
			V_{CC} (V)	Min	Typ.	Max	Min	Max	
Propagation delay time ($\overline{CKA}$ -QA)	t_{pLH}	—	3.3 ± 0.3	—	8.2	14.0	1.0	16.0	ns
	t_{pHL}		5.0 ± 0.5	—	5.5	8.4	1.0	9.6	
Propagation delay time ($\overline{CKA}$ -QC)	t_{pLH}	QA connected to $\overline{CKB}$	3.3 ± 0.3	—	17.0	30.0	1.0	34.0	ns
	t_{pHL}		5.0 ± 0.5	—	10.5	17.5	1.0	20.0	
Propagation delay time ($\overline{CKB}$ -QB, QD)	t_{pLH}	—	3.3 ± 0.3	—	8.8	14.9	1.0	17.0	ns
	t_{pHL}		5.0 ± 0.5	—	6.0	9.4	1.0	10.7	
Propagation delay time ($\overline{CKB}$ -QC)	t_{pLH}	—	3.3 ± 0.3	—	11.0	18.8	1.0	21.5	ns
	t_{pHL}		5.0 ± 0.5	—	7.1	11.3	1.0	12.8	
Propagation delay time (CLR-Qn)	t_{pHL}	—	3.3 ± 0.3	—	7.7	12.5	1.0	14.3	ns
			5.0 ± 0.5	—	5.7	8.5	1.0	9.7	
Maximum clock frequency ($\overline{CKA}$)	f_{max}	—	3.3 ± 0.3	60	120	—	60	—	MHz
			5.0 ± 0.5	100	180	—	100	—	
Maximum clock frequency ($\overline{CKB}$)	f_{max}	—	3.3 ± 0.3	45	90	—	45	—	MHz
			5.0 ± 0.5	90	140	—	90	—	
Input capacitance	C_{IN}	—		—	5	10	—	10	pF
Power dissipation capacitance	C_{PD} (Note)	—		—	40	—	—	—	pF

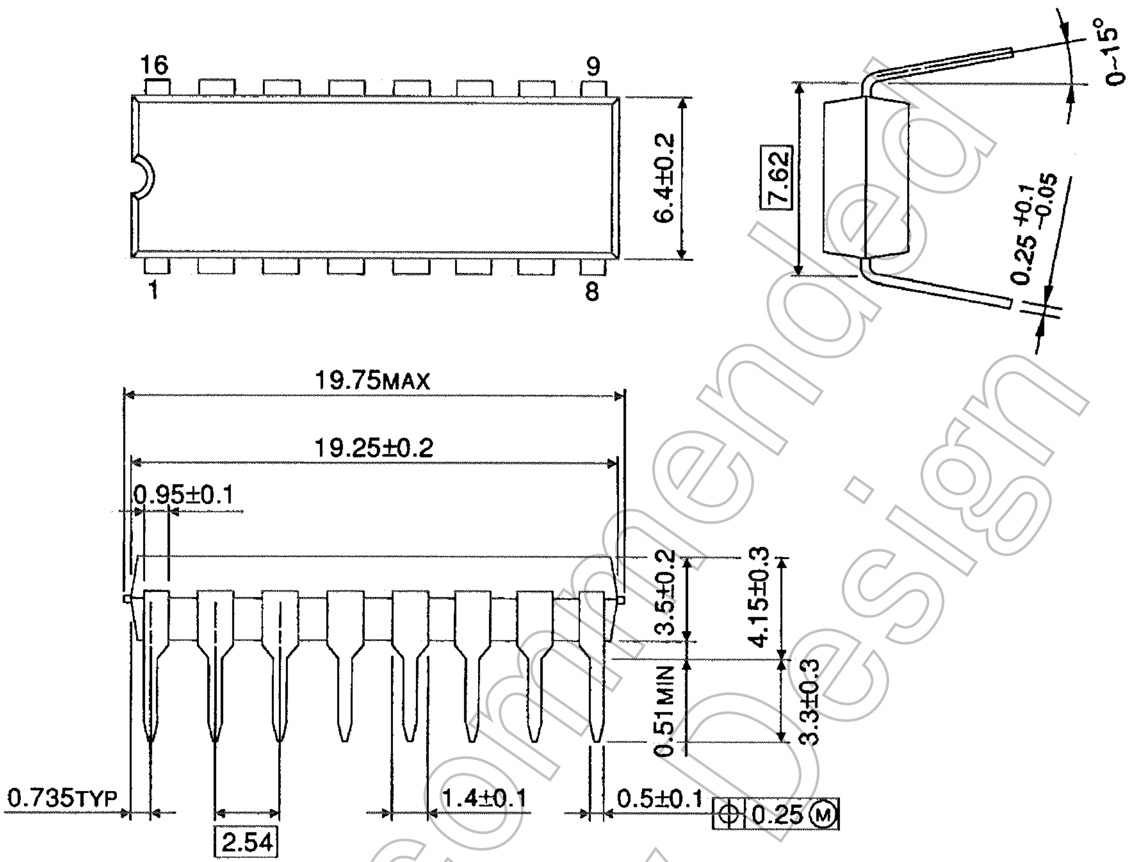
Note: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:

I_{CC} (opr) = $C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/2$ (per counter)

Package Dimensions

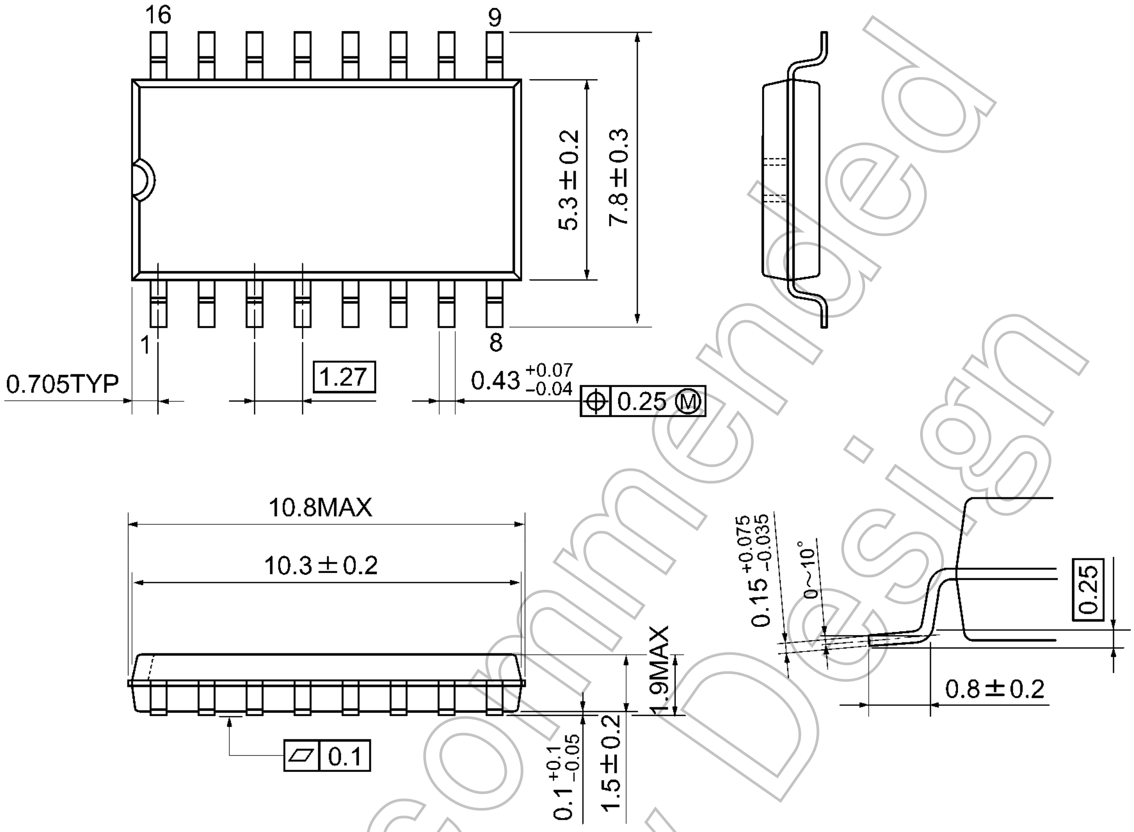
DIP16-P-300-2.54A Unit : mm



Weight: 1.00 g (typ.)

Package Dimensions

SOP16-P-300-1.27A Unit: mm



Weight: 0.18 g (typ.)

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