TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

# TC74AC377P, TC74AC377F

#### Octal D-Type Flip-Flop

The TC74AC377 is an advanced high speed CMOS OCTAL D-TYPE FLIP FLOP fabricated with silicon gate and double-layer metal wiring C<sup>2</sup>MOS technology.

It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

This 8-bit D-type flip-flop is controlled by a clock input (CK) and an enable input ( $\overline{G}$ )

The signal level applied to the D inputs are transferred to Q outputs during the positive going transition of CK.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

#### Features

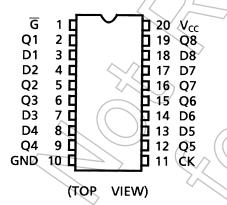
- High speed:  $f_{max} = 140 \text{ MHz}$  (typ.) at  $V_{CC} = 5 \text{ V}$
- Low power dissipation:  $I_{CC} = 8 \ \mu A \ (max)$  at  $Ta = 25^{\circ}C$
- High noise immunity: V<sub>NIH</sub> = V<sub>NIL</sub> = 28% V<sub>CC</sub> (min)
- Symmetrical output impedance:  $|I_{OH}| = I_{OL} = 24 \text{ mA} \text{ (min)}$

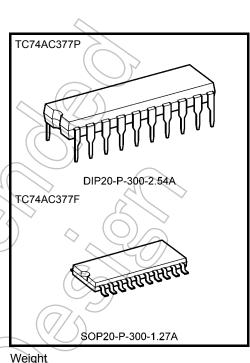
Capability of driving 50  $\Omega$ 

transmission lines.

- Balanced propagation delays:  $t_{pLH} \simeq t_{pHL}$
- Wide operating voltage range: V<sub>CC</sub> (opr) = 2 to 5.5 V
- Pin and function compatible with 74F377

#### **Pin Assignment**





Weight DIP20-P-300-2.54A SOP20-P-300-1.27A

: 1.30 g (typ.) : 0.22 g (typ.)

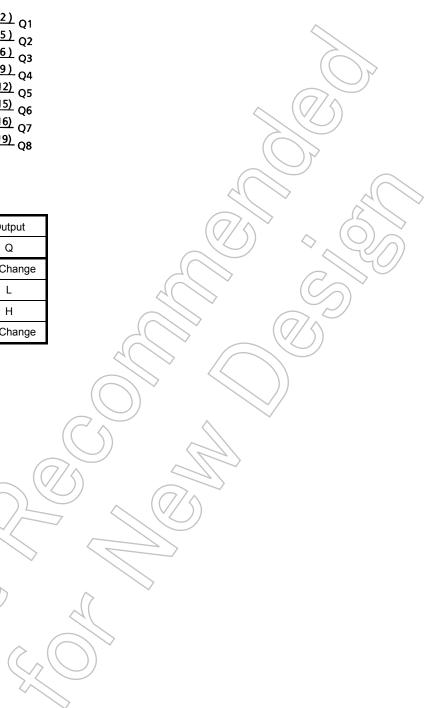
### IEC Logic Symbol

<u>б (1)</u> ск <u>(11)</u>	G1 > 1C2	
$\begin{array}{c} D1 & \underline{(3)} \\ D2 & \underline{(4)} \\ D3 & \underline{(7)} \\ (8) \end{array}$	2 D	(2) (5) Q2 (6) Q3 (9) Q4 (12) Q5
$ \begin{array}{c} \text{D4}  \underline{(13)} \\ \text{D5}  \underline{(13)} \\ \text{D6}  \underline{(14)} \\ \text{D7}  \underline{(17)} \\ \end{array} $		(9) Q4 (12) Q5 (15) Q6 (16) Q7 (19) Q8
D8 (18)		(19) Q8

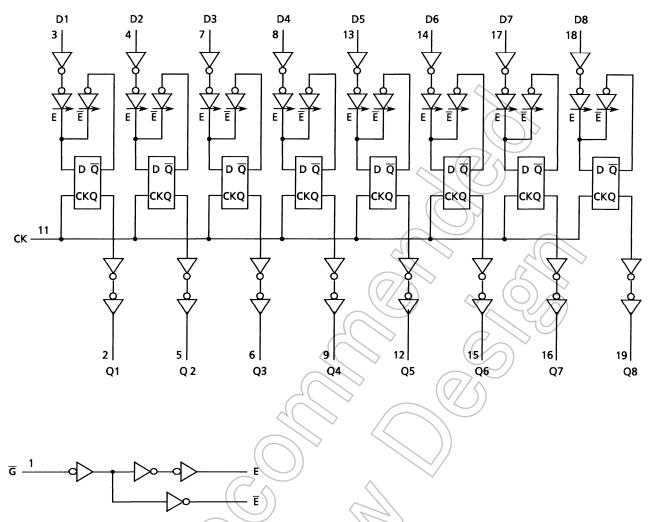
#### Truth Table

Inputs			Output
G	СК	D	Q
Н	Х	Х	No Change
L		L	L
L		Н	Н
Х		Х	No Change

X: Don't care



#### System Diagram



#### Absolute Maximum Ratings (Note 1)

Characteristics	Symbol 🔿	Rating	Unit
Supply voltage range V <sub>CC</sub>		-0.5 to 7.0	V
DC input voltage	VIN	-0.5 to V <sub>CC</sub> + 0.5	V
DC output voltage	Vout	–0.5 to V <sub>CC</sub> + 0.5	V
Input diode current		±20	mA
Output diode current		±50	mA
DC output current	HOUT	±50	mA
DC V <sub>CC</sub> /ground current	Icc	±200	mA
Power dissipation	PD	500 (DIP) (Note 2)/180 (SOP)	mW
Storage temperature	T <sub>stg</sub>	–65 to 150	°C

Note 1: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/Derating Concept and Methods) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 2: 500 mW in the range of Ta = -40 to 65°C. From Ta = 65 to 85°C, a derating factor of -10 mW/°C should be applied up to 300 mW.

#### **Operating Ranges (Note)**

Characteristics	Symbol	Rating	Unit
Supply voltage	V <sub>CC</sub>	2.0 to 5.5	V
Input voltage	V <sub>IN</sub>	0 to V <sub>CC</sub>	V
Output voltage	V <sub>OUT</sub>	0 to V <sub>CC</sub>	V
Operating temperature	T <sub>opr</sub>	–40 to 85	°C
Input rise and fall time	dt/dV	0 to 100 (V_{CC} = 3.3 $\pm$ 0.3 V)	ns/V
	avav	0 to 20 (V <sub>CC</sub> = 5 $\pm$ 0.5 V)	

Note: The operating ranges must be maintained to ensure the normal operation of the device. Unused inputs must be tied to either  $V_{CC}$  or GND.

#### **Electrical Characteristics**

#### **DC Characteristics**

				$\sim \sim$					
Characteristics Symbol		Test Condition		Ta = 25°C			Ta = -40 to 85°C		
			Vcc (V)	Min	Тур.	Max	Min	Max	
			2.0	1.50	_((	5	1.50	—	
High-level input voltage	VIH	-	3.0	2.10		Ì	2.10	—	V
			5.5	3.85	$(H \leq$	) —	3.85		
Low lovel input			2.0		$\searrow$	0.50	—	0.50	
Low-level input voltage	V <sub>IL</sub>		3.0	`	) -	0.90	—	0.90	V
			5.5	$\left  \right\rangle$	//-	1.65	—	1.65	
			2.0	1.9	2.0	—	1.9	—	
		I <sub>OH</sub> = -50 μA	3.0	2.9	3.0	—	2.9	—	
High-level output	V <sub>OH</sub>	V <sub>IN</sub> = V <sub>IH</sub> or	4.5	4.4	4.5	_	4.4	—	V
voltage	VOH	$V_{IL}$ $I_{OH} = -4 \text{ mA}$	3.0	2.58	_		2.48		v
		I <sub>OH</sub> = -24 mA	4.5	3.94	—	—	3.80	—	
		I <sub>OH</sub> = -75 mA (Note)	5.5	—	—	—	3.85	—	
			2.0	—	0.0	0.1	_	0.1	
		I <sub>OL</sub> = 50 μA	3.0	—	0.0	0.1	—	0.1	
Low-level output	Vol	V <sub>IN</sub> = V <sub>IH</sub> or	4.5	—	0.0	0.1	—	0.1	V
voltage		$V_{IL}$ $V_{OL} = 12 \text{ mA}$	3.0	_	_	0.36	_	0.44	v
		I <sub>OL</sub> = 24 mA	4.5	—	—	0.36	—	0.44	
	))	I <sub>OL</sub> = 75 mA (Note)	5.5	—	—	_	—	1.65	
Input leakage current	IIN	VIN = V <sub>CC</sub> or GND	5.5	_	_	±0.1	_	±1.0	μΑ
Quiescent supply current		$V_{IN} = V_{CC}$ or GND	5.5	_	_	8.0	—	80.0	μA

Note: This spec indicates the capability of driving 50  $\Omega$  transmission lines.

One output should be tested at a time for a 10 ms maximum duration.

#### Timing Requirements (input: $t_r = t_f = 3 \text{ ns}$ )

Characteristics	Symbol	Test Condition		Ta = 25°C	Ta = 40 to 85°C	Unit
			V <sub>CC</sub> (V)	Limit	Limit	
Minimum pulse width	t <sub>W (L)</sub>		$\textbf{3.3}\pm\textbf{0.3}$	8.0	8.0	20
(CK)	t <sub>W (H)</sub>		$\textbf{5.0} \pm \textbf{0.5}$	5.0	5.0	ns
Minimum set-up time			3.3 ± 0.3	8.0	8.0	20
(D-CK)	t <sub>s</sub>	—	$5.0 \pm 0.5$	4.0	4.0	ns
Minimum set-up time			$3.3\pm0.3$	9.0	9.0	
( <u>G</u> -CK)	t <sub>s</sub>	- < (	5.0 ± 0.5	4.0	4.0	ns
Minimum hold time	4.		3.3±0.3	1.0	1.0	20
	t <sub>h</sub>	_ (()	5.0 ± 0.5	1.0	1.0	ns

#### AC Characteristics (C<sub>L</sub> = 50 pF, R<sub>L</sub> = 500 $\Omega$ , input: t<sub>r</sub> = t<sub>f</sub> = 3 ns)

Characteristics	Symbol	Test Condition	Vcc (V)	Mín	Га = 25°С Тур.	; Max	Ta -40 to Min	85°C Max	Unit
Propagation delay time (CK-Q)	t <sub>pLH</sub> t <sub>pHL</sub>	-	$3.3 \pm 0.3$ $5.0 \pm 0.5$	_	10.6 7.4	17.6 10.6	1.0 1.0	20.0 12.0	ns
Maximum clock frequency	f <sub>max</sub>	-	$\begin{array}{c} 3.3\pm0.3\\ 5.0\pm0.5\end{array}$	50 80	95 140	)_	50 80	_	MHz
Input capacitance	C <sub>IN</sub>	$\langle \langle \mathcal{F} \rangle \rangle$	/		5	10	—	10	pF
Power dissipation capacitance	C <sub>PD</sub> (Note)	$\bigcirc$		$\searrow$	30		_	_	pF

Note: C<sub>PD</sub> is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:

 $I_{CC}$  (opr) =  $C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8$  (per F/F)

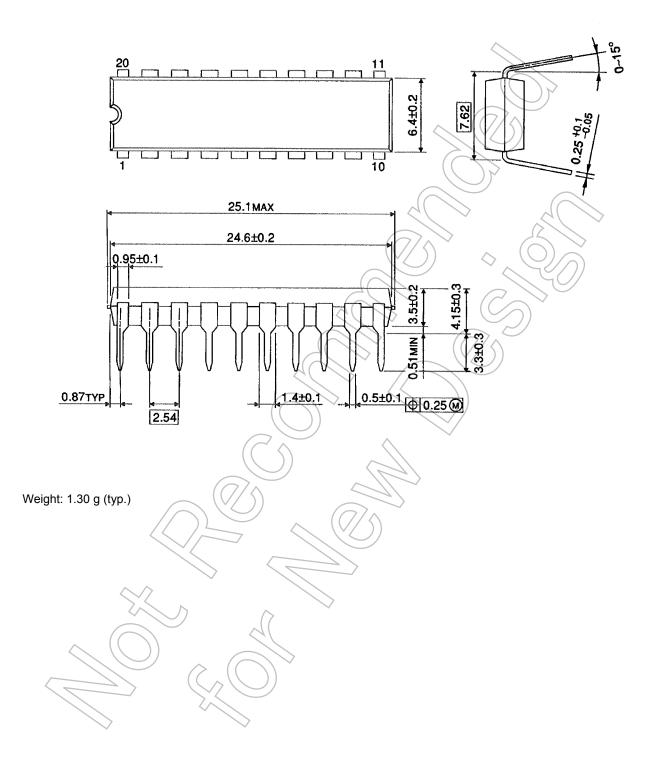
And the total CPD when n pcs. of flip flop operate can be gained by the following equation:

CPD (total) = 20 + 10 · n

#### Package Dimensions

DIP20-P-300-2.54A

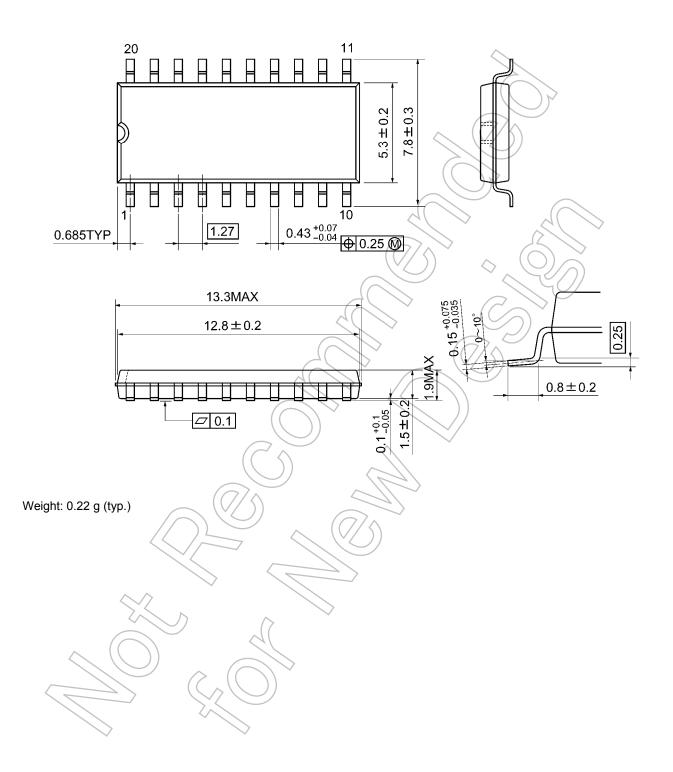
Unit : mm



#### Package Dimensions

SOP20-P-300-1.27A

Unit: mm



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