4,194,304 WORD x 1 BIT DYNAMIC RAM

* This is advanced information and specifications are subject to change without notice.

DESCRIPTION

The TC514102J/Z is the new generation dynamic RAM organized 4,194,304 words by 1 bit. The TC514102J/Z utilizes TOSHIBA's CMOS Silicon gate process technology as well as advanced circuit techniques to provide wide operating margins, both internally and to the system user. Multiplexed address inputs permit the TC514102J/Z to be packaged in a standard 26/20 pin plastic SOJ and 20 pin plastic ZIP. The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment. System oriented features include single power supply of 5V±10% tolerance, direct interfacing capability with high performance logic families such as Schottky TTL.

FEATURES

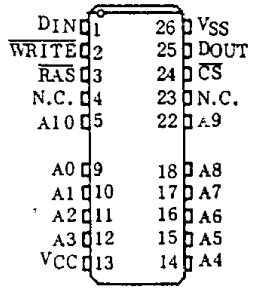
- 4,194,304 word by 1 bit organization
- Fast access time and cycle time

		TC514102J/Z-80/-10	
t_{RAC}	$\overline{RAS}$ Access Time	80ns	100ns
t_{AA}	Column Address Access Time	40ns	50ns
t_{CAC}	$\overline{CS}$ Access Time	20ns	25ns
t_{RC}	Cycle Time	150ns	180ns
t_{SC}	Static Column Mode Cycle Time	45ns	55ns

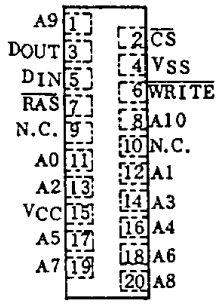
- Single power supply of 5V±10% with a built-in V_{BB} generator
- Low power
  550mW Operating (TC514102J/Z-80)
  468mW Operating (TC514102J/Z-10)
  5.5mW MAX. Standby
- Output unlatched at cycle end allows two-dimensional chip selection
- Common I/O capability using "EARLY WRITE" operation
- Read-Modify-Write, $\overline{CS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$-only refresh, Hidden refresh, Static Column Mode and Test Mode capability
- All inputs and output TTL compatible
- 1024 refresh cycles/16ms
- Package Plastic SOJ: TC514102J
  Plastic ZIP: TC514102Z

PIN CONNECTION (TOP VIEW)

Plastic SOJ



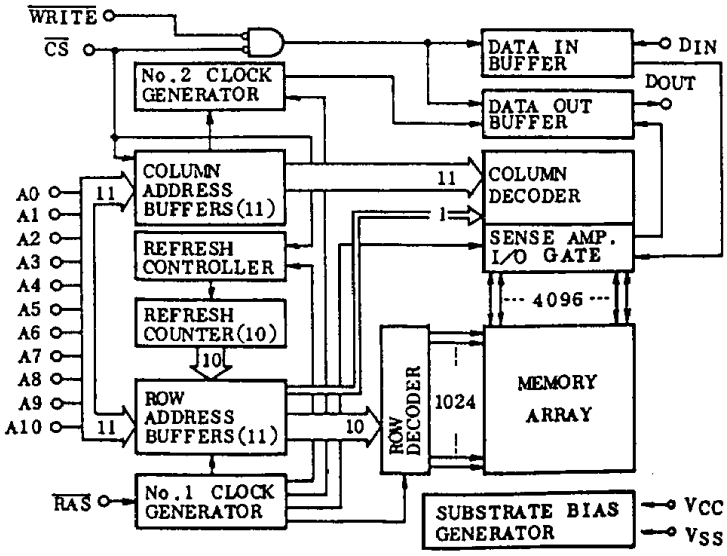
Plastic ZIP



PIN NAMES

A0 ∿ A10	Address Inputs
$\overline{RAS}$	Row Address Strobe
D_{IN}	Data In
D_{OUT}	Data Out
$\overline{CS}$	Chip Select Input
$\overline{WRITE}$	Read/Write Input
V_{CC}	Power (+5V)
V_{SS}	Ground
N.C.	No Connection

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNITS	NOTE
Input Voltage	V_{IN}	-1 ~ 7	V	1
Output Voltage	V_{OUT}	-1 ~ 7	V	1
Power Supply Voltage	V_{CC}	-1 ~ 7	V	1
Operating Temperature	T_{OPR}	0 ~ 70	°C	1
Storage Temperature	T_{STG}	-55 ~ 150	°C	1
Soldering Temperature · Time	T_{SOLDER}	260 · 10	°C·sec	1
Power Dissipation	P_D	600	mW	1
Short Circuit Output Current	I_{OUT}	50	mA	1

RECOMMENDED DC OPERATING CONDITIONS ($Ta=0 \sim 70°C$)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTE
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	-	6.5	V	2
V_{IL}	Input Low Voltage	-1.0	-	0.8	V	2

DC ELECTRICAL CHARACTERISTICS ($V_{CC}=5V \pm 10\%$, $Ta=0 \sim 70°C$)

SYMBOL	PARAMETER		MIN.	MAX.	UNITS	NOTES
I_{CC1}	OPERATING CURRENT Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CS}$, Address Cycling: $t_{RC}=t_{RC}$ MIN.)	TC514102J/Z-80	-	100	mA	3,4,5
		TC514102J/Z-10	-	85		
I_{CC2}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}=\overline{CS}=V_{IH}$)		-	2	mA	
I_{CC3}	$\overline{RAS}$ ONLY REFRESH CURRENT Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CS}=V_{IH}$: $t_{RC}=t_{RC}$ MIN.)	TC514102J/Z-80	-	100	mA	3,5
		TC514102J/Z-10	-	85		
I_{CC4}	STATIC COLUMN MODE CURRENT Average Power Supply Current, Static Column Mode ($\overline{RAS}=\overline{CS}=V_{IL}$, Address Cycling: $t_{SC}=t_{SC}$ MIN.)	TC514102J/Z-80	-	75	mA	3,4,5
		TC514102J/Z-10	-	65		
I_{CC5}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}=\overline{CS}=V_{CC}-0.2V$)		-	1	mA	
I_{CC6}	$\overline{CS}$ BEFORE $\overline{RAS}$ REFRESH CURRENT Average Power Supply Current, $\overline{CS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CS}$ Cycling: $t_{RC}=t_{RC}$ MIN.)	TC514102J/Z-80	-	100	mA	3
		TC514102J/Z-10	-	85		
$I_{I(L)}$	INPUT LEAKAGE CURRENT Input Leakage Current, any input ($0V \leqq V_{IN} \leqq 6.5V$, All Other Pins Not Under Test=0V)		-10	10	μA	
$I_{I(L)}$	OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, $0V \leqq V_{OUT} \leqq 5.5V$)		-10	10	μA	
V_{OH}	OUTPUT LEVEL Output "H" Level Voltage ($I_{OUT}=-5mA$)		2.4	-	V	
V_{OL}	OUTPUT LEVEL Output "L" Level Voltage ($I_{OUT}=4.2mA$)		-	0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(V_{CC}=5V±10%, Ta=0∿70°C)(Notes 6, 7, 8)

SYMBOL	PARAMETER	TC514102J/Z -80		TC514102J/Z -10		UNIT	NOTES
		MIN.	MAX.	MIN.	MAX.		
t_{RC}	Random Read or Write Cycle Time	150	-	180	-	ns	
t_{RMW}	Read-Modify-Write Cycle Time	175	-	210	-	ns	
t_{SC}	Static Column Mode Cycle Time	45	-	55	-	ns	
t_{SRMW}	Static Column Mode Read-Modify-Write Cycle Time	80	-	100	-	ns	
t_{RAC}	Access Time from $\overline{RAS}$	-	80	-	100	ns	9,14,15
t_{CAC}	Access Time from $\overline{CS}$	-	20	-	25	ns	9,14
t_{AA}	Access Time from Column Address	-	40	-	50	ns	9,15
t_{ALW}	Access Time from Last Write	-	75	-	95	ns	9,16
t_{CLZ}	$\overline{CS}$ to Output in Low-Z	0	-	0	-	ns	9
t_{OFF}	Output Buffer Turn-off Delay	0	20	0	20	ns	10
t_{AOH}	Output Data Hold Time from Column Address	5	-	5	-	ns	
t_{OW}	Output Data Enable Time from $\overline{WRITE}$	-	25	-	30	ns	
t_{WOH}	Output Data Hold Time from $\overline{WRITE}$	0	-	0	-	ns	
t_T	Transition Time (Rise and Fall)	3	50	3	50	ns	8
t_{RP}	$\overline{RAS}$ Precharge Time	60	-	70	-	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	80	10,000	100	10,000	ns	
t_{RASC}	$\overline{RAS}$ Pulse Width (Static Column Mode)	80	200,000	100	200,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	20	-	25	-	ns	
t_{CSH}	$\overline{CS}$ Hold Time	80	-	100	-	ns	
t_{CS}	$\overline{CS}$ Pulse Width	20	10,000	25	10,000	ns	
t_{CSC}	$\overline{CS}$ Pulse Width (Static Column Mode)	20	200,000	25	200,000	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CS}$ Delay Time	20	60	25	75	ns	14
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	40	20	50	ns	15
t_{CRP}	$\overline{CS}$ to $\overline{RAS}$ Precharge Time	5	-	10	-	ns	
t_{CP}	$\overline{CS}$ Precharge Time	10	-	10	-	ns	
t_{ASR}	Row Address Set-Up Time	0	-	0	-	ns	
t_{RAH}	Row Address Hold Time	10	-	15	-	ns	
t_{ASC}	Column Address Set-Up Time	0	-	0	-	ns	
t_{CAH}	Column Address Hold Time	15	-	20	-	ns	
t_{AWR}	Write Address Hold Time referenced to $\overline{RAS}$	60	-	75	-	ns	
t_{AR}	Column Address Hold Time referenced to $\overline{RAS}$	90	-	115	-	ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (Continued)

SYMBOL	PARAMETER	TC514102J/Z -80		TC514102J/Z -10		UNITS	NOTES
		MIN.	MAX.	MIN.	MAX.		
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	40	–	50	–	ns	
t_{RCS}	Read Command Set-Up Time	0	–	0	–	ns	
t_{RCH}	Read Command Hold Time	0	–	0	–	ns	11
t_{RRH}	Read Command Hold Time referenced to $\overline{RAS}$	0	–	0	–	ns	11
t_{WCH}	Write Command Hold Time	15	–	20	–	ns	
t_{WCR}	Write Command Hold Time referenced to $\overline{RAS}$	60	–	75	–	ns	
t_{WP}	Write Command Pulse Width	15	–	20	–	ns	
t_{WI}	Write Command Inactive Time	10	–	10	–	ns	
t_{AH}	Column Address Hold Time referenced to $\overline{RAS}$ Rise	5	–	10	–	ns	17
t_{LWAD}	Last Write to Column Address Delay Time	20	35	25	45	ns	16
t_{AHLW}	Last Write to Column Address Hold Time	75	–	95	–	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20	–	25	–	ns	
t_{CWL}	Write Command to $\overline{CS}$ Lead Time	20	–	25	–	ns	
t_{DS}	Data Set-Up Time	0	–	0	–	ns	12
t_{DH}	Data Hold Time	15	–	20	–	ns	12
t_{DHR}	Data Hold Time referenced to $\overline{RAS}$	60	–	75	–	ns	
t_{REF}	Refresh Period	–	16	–	16	ms	
t_{WCS}	Write Command Set-Up Time	0	–	0	–	ns	13
t_{CWD}	$\overline{CS}$ to $\overline{WRITE}$ Delay Time	20	–	25	–	ns	13
t_{RWD}	$\overline{RAS}$ to $\overline{WRITE}$ Delay Time	80	–	100	–	ns	13
t_{AWD}	Column Address to $\overline{WRITE}$ Delay Time	40	–	50	–	ns	13
t_{CSR}	$\overline{CS}$ Set-Up Time ($\overline{CS}$ before $\overline{RAS}$ Cycle)	5	–	5	–	ns	
t_{CHR}	$\overline{CS}$ Hold Time ($\overline{CS}$ before $\overline{RAS}$ Cycle)	15	–	20	–	ns	
t_{RPC}	$\overline{RAS}$ to $\overline{CS}$ Precharge Time	0	–	0	–	ns	
t_{CPT}	$\overline{CS}$ Precharge Time ($\overline{CS}$ before $\overline{RAS}$ Counter Test Cycle)	40	–	50	–	ns	
t_{WTS}	Write Command Set-Up Time (Test Mode In)	10	–	10	–	ns	
t_{WTH}	Write Command Hold Time (Test Mode In)	10	–	10	–	ns	
t_{WRP}	$\overline{WRITE}$ to $\overline{RAS}$ Precharge Time ($\overline{CS}$ before $\overline{RAS}$ Cycle)	10	–	10	–	ns	
t_{WRH}	$\overline{WRITE}$ to $\overline{RAS}$ Hold Time ($\overline{CS}$ before $\overline{RAS}$ Cycle)	10	–	10	–	ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS IN THE TEST MODE

(V_{CC}=5V±10%, Ta=0~70°C) (Notes 6, 7, 8)

SYMBOL	PARAMETER	TC514102J/Z -80		TC514102J/Z -10		UNIT	NOTES
		MIN.	MAX.	MIN.	MAX.		
t_{RC}	Random Read or Write Cycle Time	155	-	185	-	ns	
t_{SC}	Static Column Mode Cycle Time	50	-	60	-	ns	
t_{RAC}	Access Time from $\overline{RAS}$	-	85	-	105	ns	9,14,15
t_{CAC}	Access Time from $\overline{CS}$	-	25	-	30	ns	9,14
t_{AA}	Access Time from Column Address	-	45	-	55	ns	9,15
t_{RAS}	$\overline{RAS}$ Pulse Width	85	10,000	105	10,000	ns	
t_{RASC}	$\overline{RAS}$ Pulse Width (Static Column Mode)	85	200,000	105	200,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	25	-	30	-	ns	
t_{CSH}	$\overline{CS}$ Hold Time	85	-	105	-	ns	
t_{CS}	$\overline{CS}$ Pulse Width	25	10,000	30	10,000	ns	
t_{CSC}	$\overline{CS}$ Pulse Width (Static Column Mode)	25	200,000	30	200,000	ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	45	-	55	-	ns	

CAPACITANCE (V_{CC}=5V±10%, f=1MHz, Ta=0~70°C)

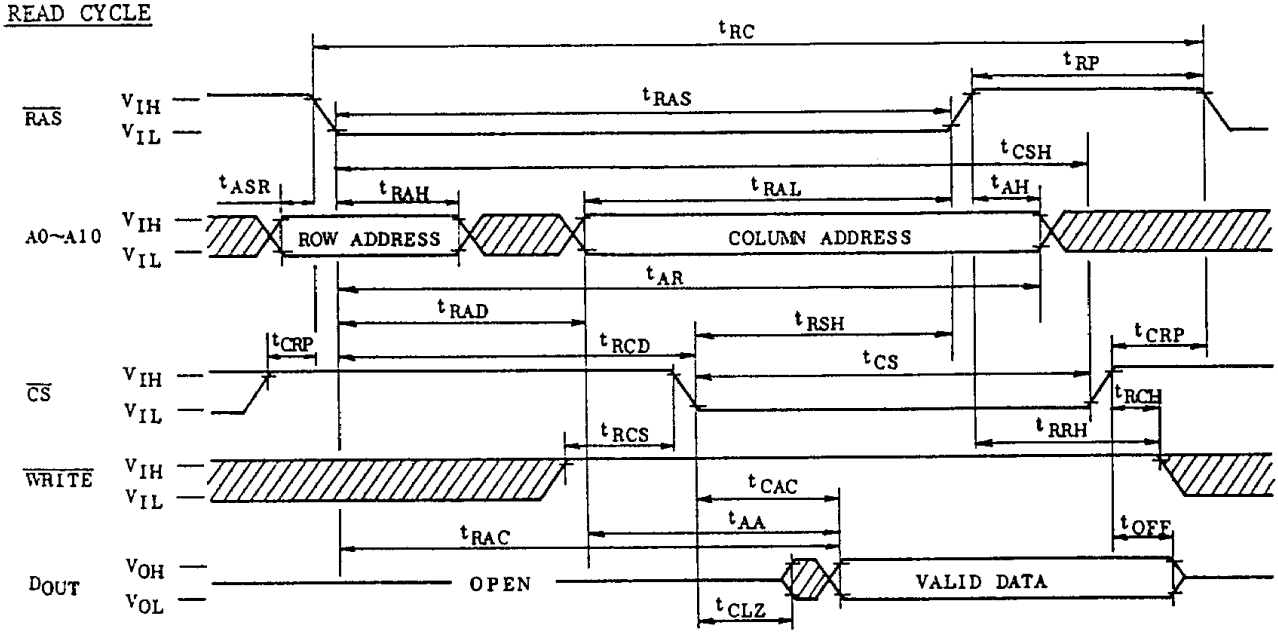
SYMBOL	PARAMETER	MIN.	MAX.	UNIT
C_{I1}	Input Capacitance (A0~A10, D_{IN})	-	5	pF
C_{I2}	Input Capacitance ($\overline{RAS}$, $\overline{CS}$, $\overline{WRITE}$)	-	7	pF
C_O	Output Capacitance (D_{OUT})	-	7	pF

NOTES:

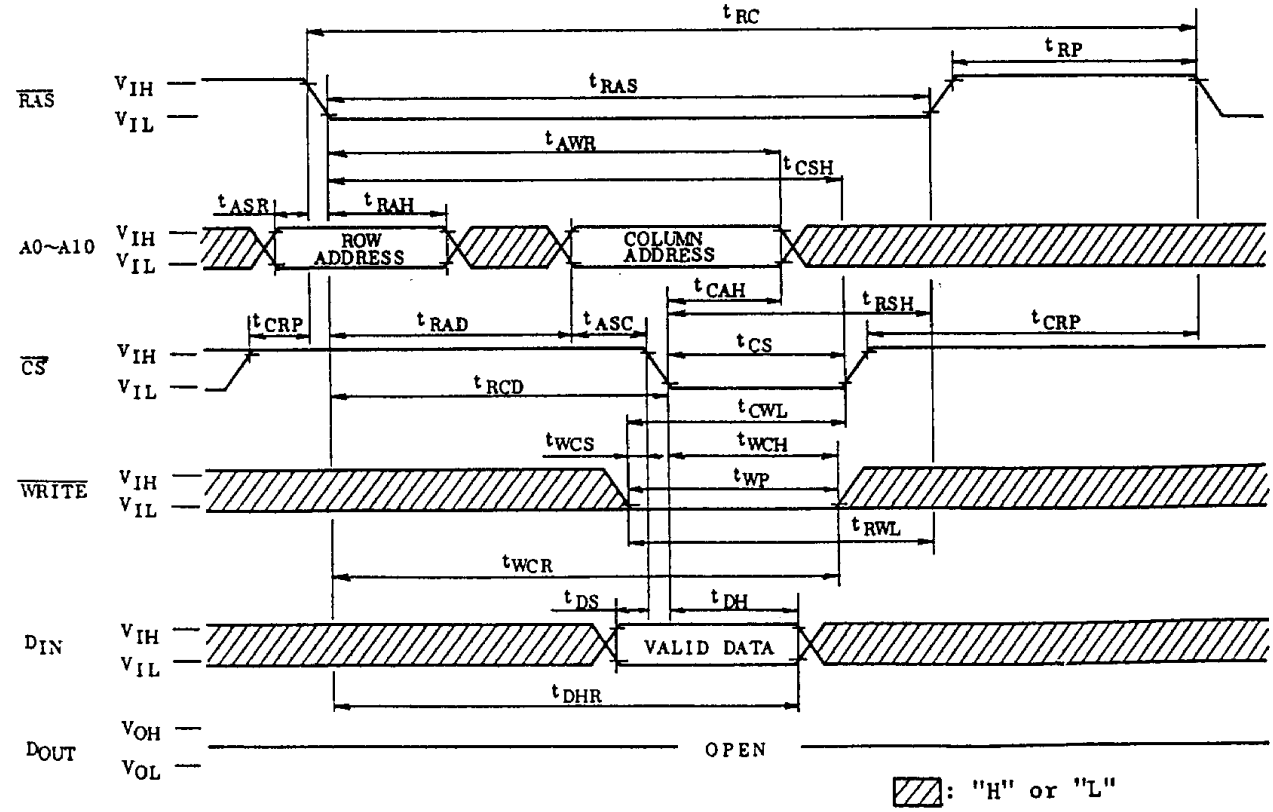
1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
2. All voltages are referenced to V_{SS}.
3. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6} depend on cycle rate.
4. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.
5. Column address can be changed once or less while $\overline{RAS}=V_{IL}$.
6. An initial pause of 200μs is required after power-up followed by any 8 $\overline{RAS}$ only refresh cycles before proper device operation is achieved.
   In case of using internal refresh counter, a minimum of 8 $\overline{CS}$ before $\overline{RAS}$ refresh cycles instead of 8 $\overline{RAS}$ only refresh cycles are required.
7. AC measurements assume $t_T=5ns$.
8. V_{IH}(min.) and V_{IL}(max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
9. Measured with a load equivalent to 2 TTL loads and 100pF.
10. t_{OFF}(max.) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
11. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
12. These parameters are referenced to $\overline{CS}$ leading edge in early write cycles and to $\overline{WRITE}$ leading edge in read-modify-write cycles.
13. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min.), the cycle is an early write cycle and data out pin will remain open circuit (high impedance) throughout the entire cycles; If $t_{RWD} \geq t_{RWD}$(min.), $t_{CWD} \geq t_{CWD}$(min.) and $t_{AWD} \geq t_{AWD}$(min.), the cycle is a read-modify-write cycle and the data out will contain data read from the selected cell: If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
14. Operation within the t_{RCD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RCD}(max.) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD}(max.) limit, then access time is controlled by t_{CAC}.
15. Operation within the t_{RAD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RAD}(max.) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD}(max.) limit, then access time is controlled exclusively by t_{AA}.
16. Operation within the t_{LWAD}(max.) limit insures that t_{ALW}(max.) can be met. t_{LWAD}(max.) is specified as a reference point only: If t_{LWAD} is greater than the specified t_{LWAD}(max.) limit, then access time is controlled exclusively by t_{AA}.
17. t_{AH} is the condition to latch column address when $\overline{RAS}$ has rised up.

TIMING WAVEFORMS

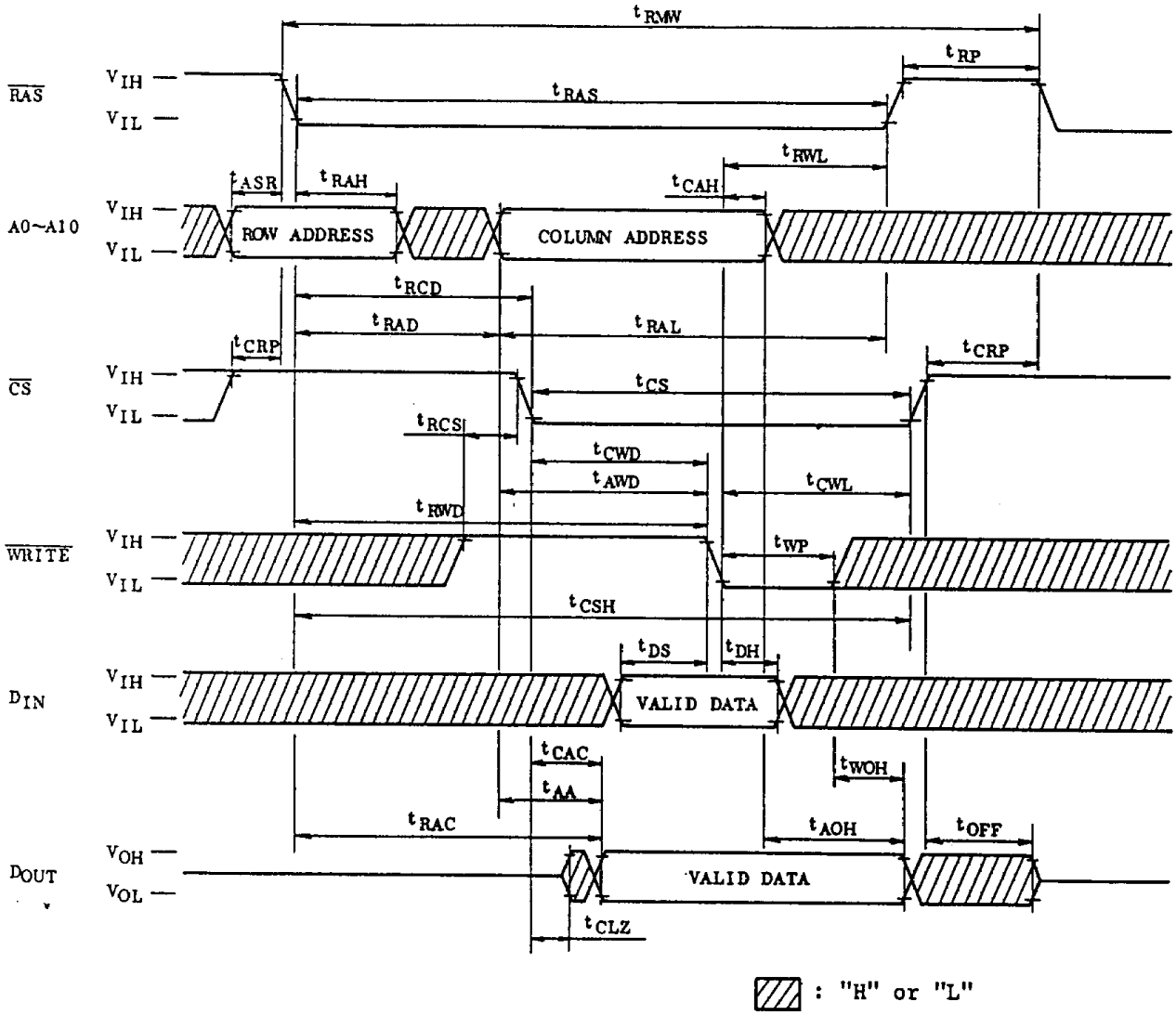
READ CYCLE



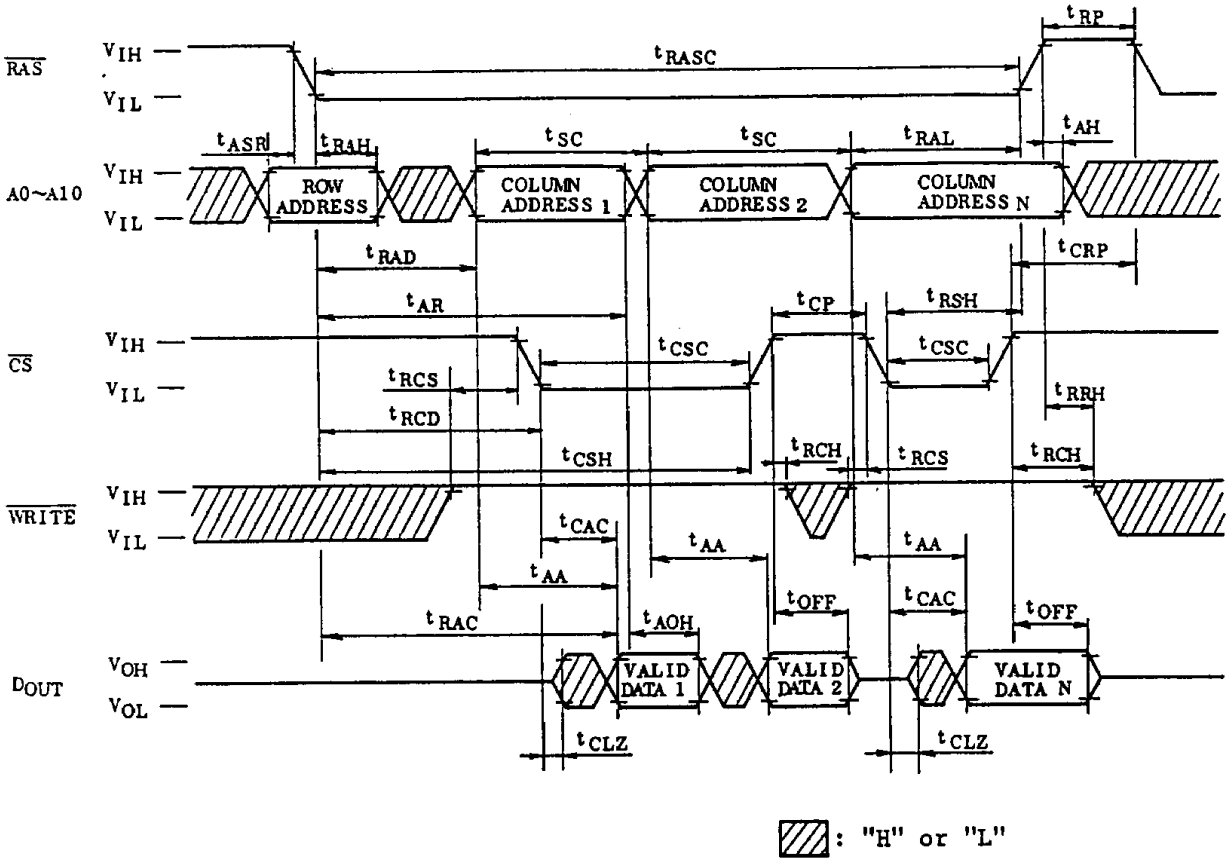
WRITE CYLCE (EARLY WRITE)



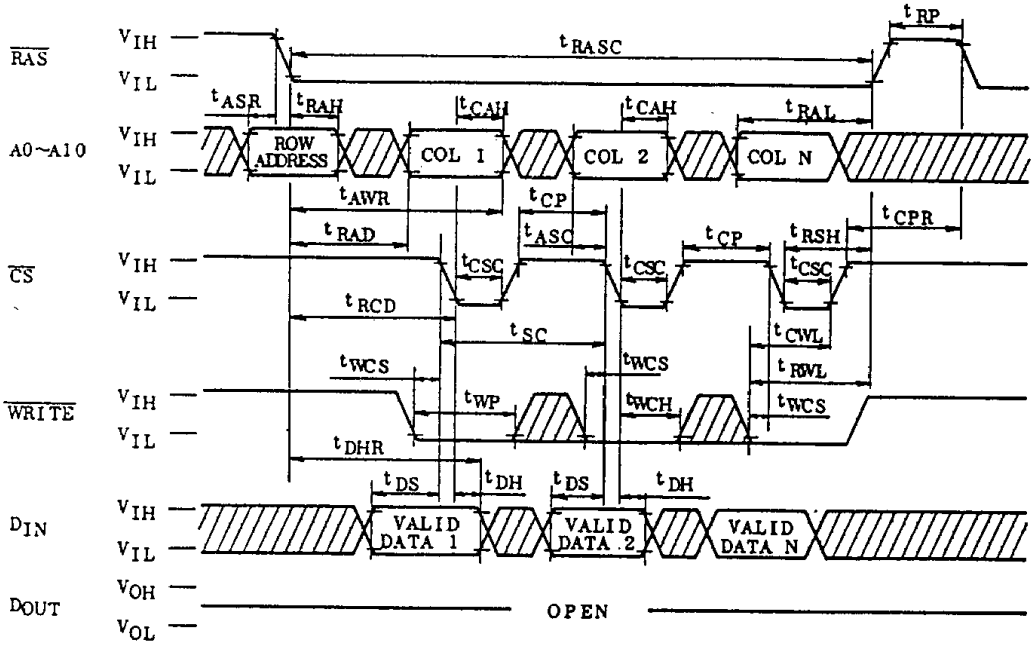
READ-MODIFY-WRITE CYCLE



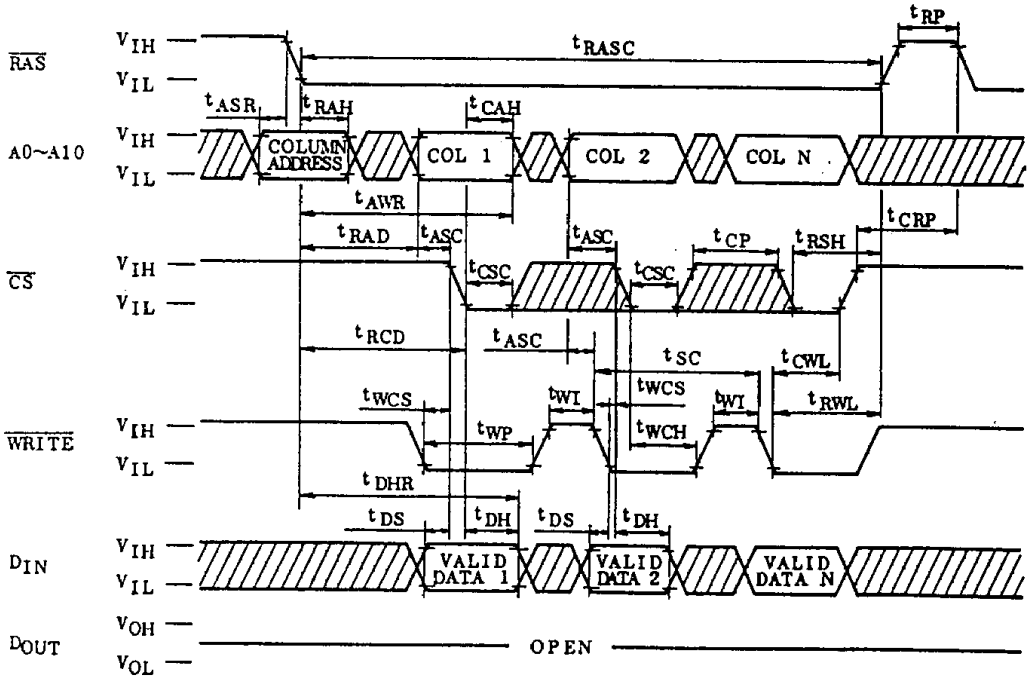
STATIC COLUMN MODE READ CYCLE



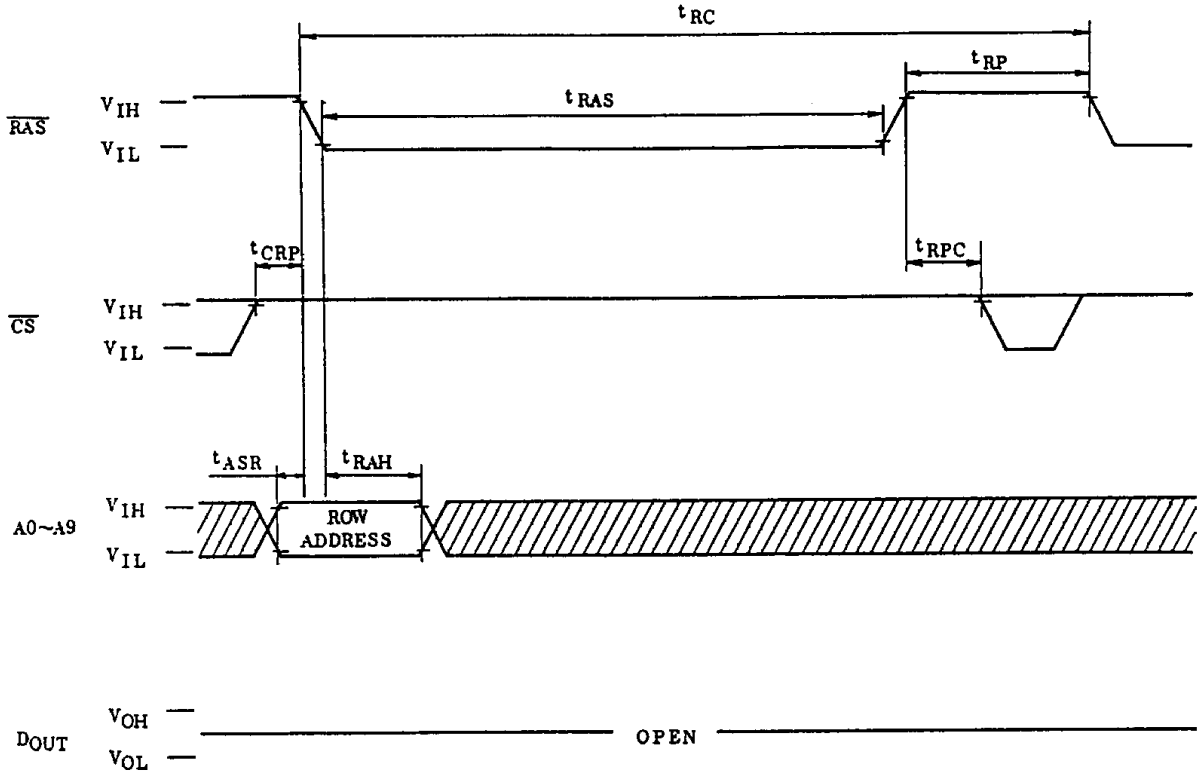
STATIC COLUMN MODE WRITE CYCLE (EARLY WRITE)



STATIC COLUMN MODE WRITE CYCLE (EARLY WRITE)

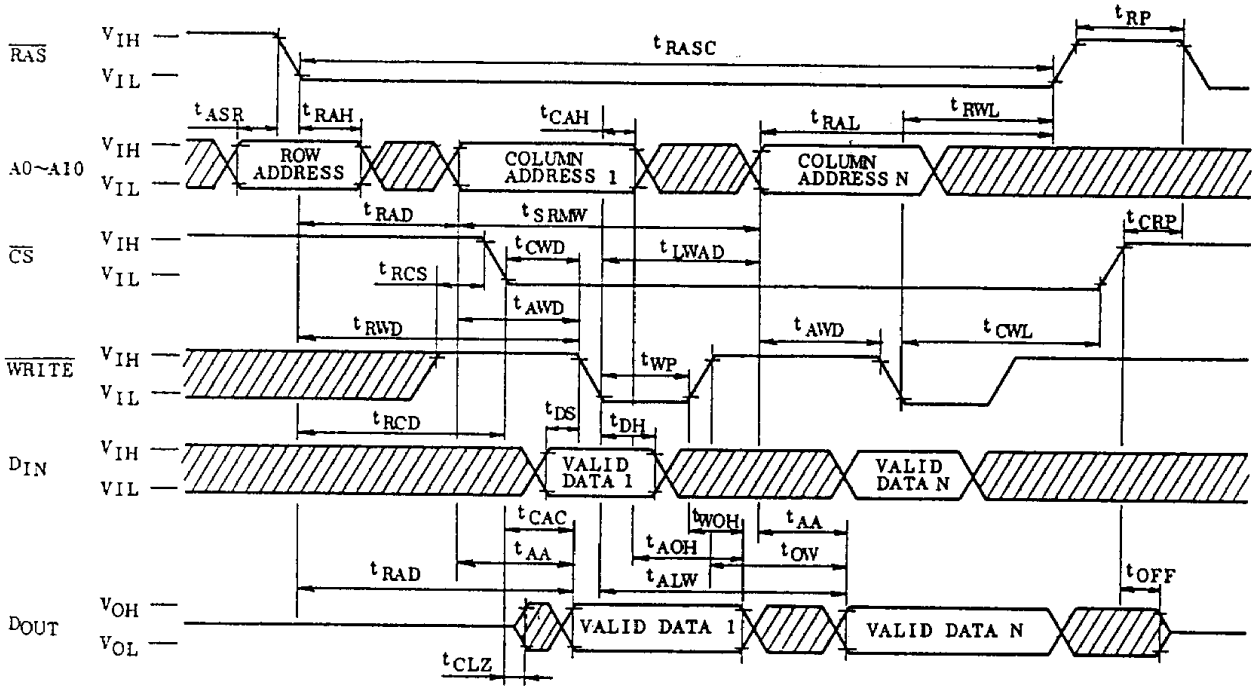


$\overline{RAS}$ ONLY REFRESH CYCLE

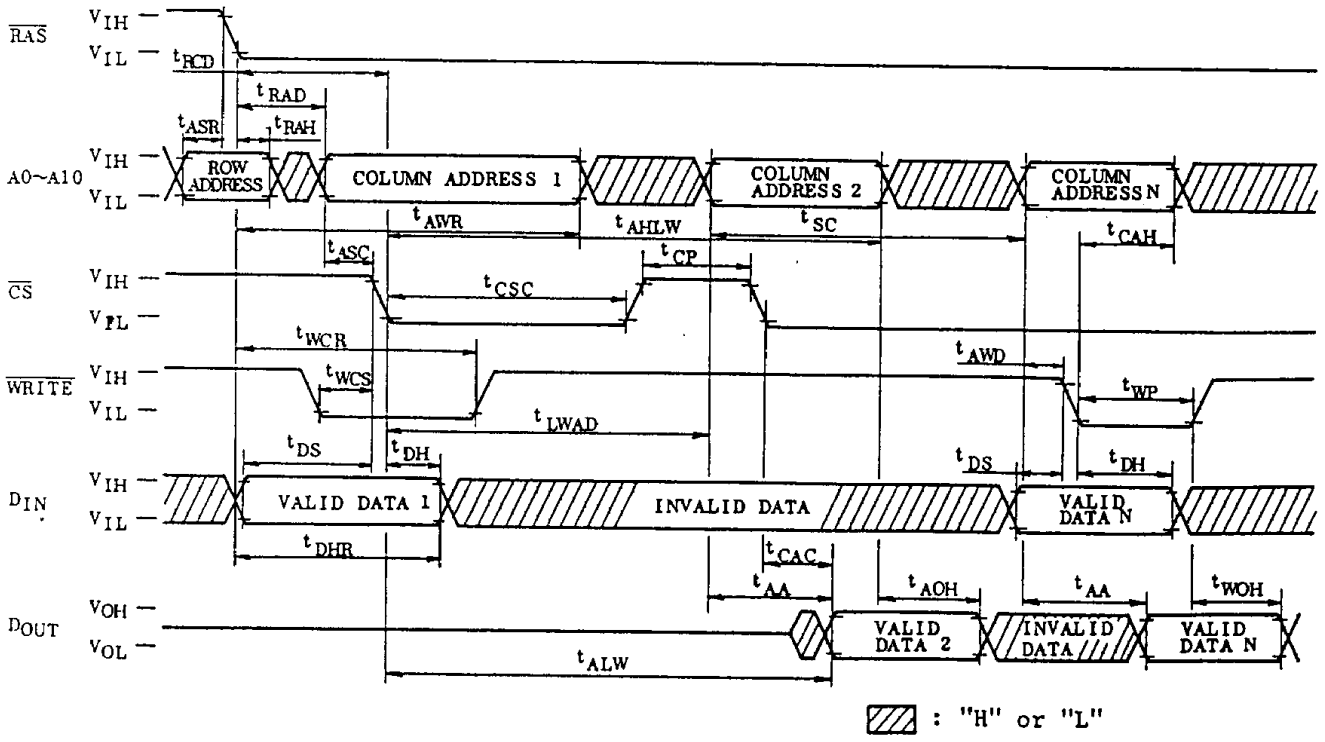


NOTE: $\overline{WRITE}$="H" or "L", A10="H" or "L"

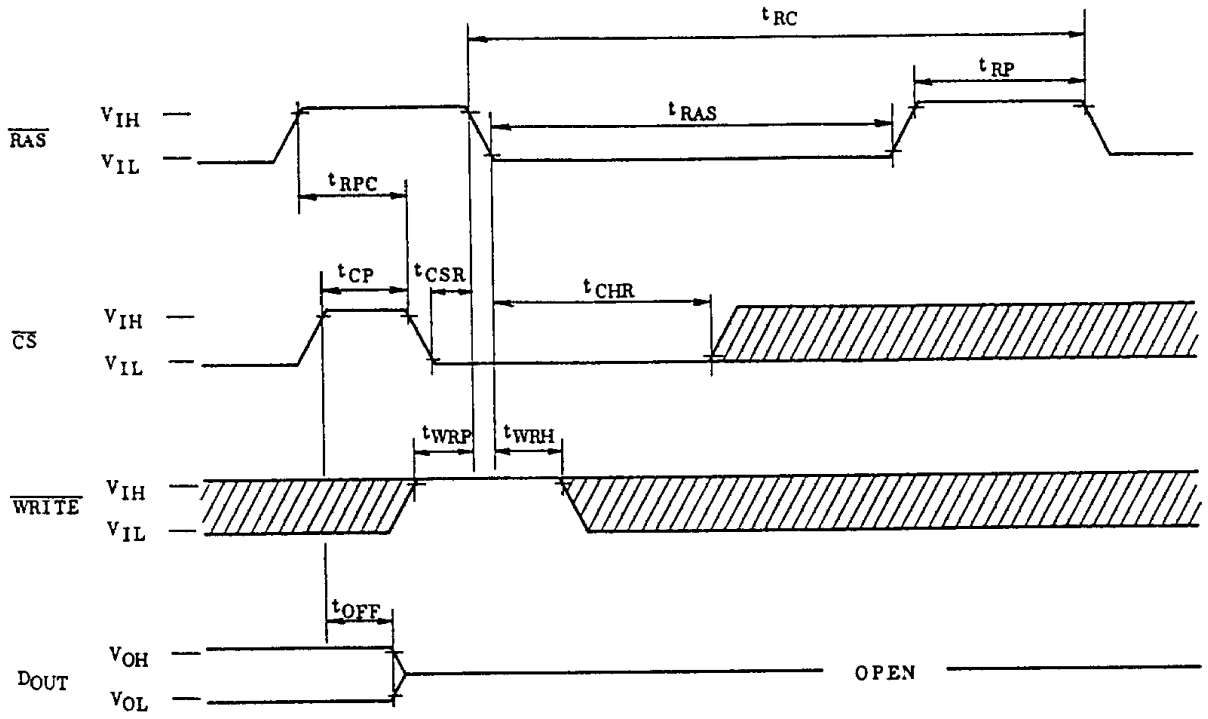
STATIC COLUMN MODE READ-MODIFY-WRITE CYCLE



STATIC COLUMN MODE READ/WRITE MIXED CYCLE

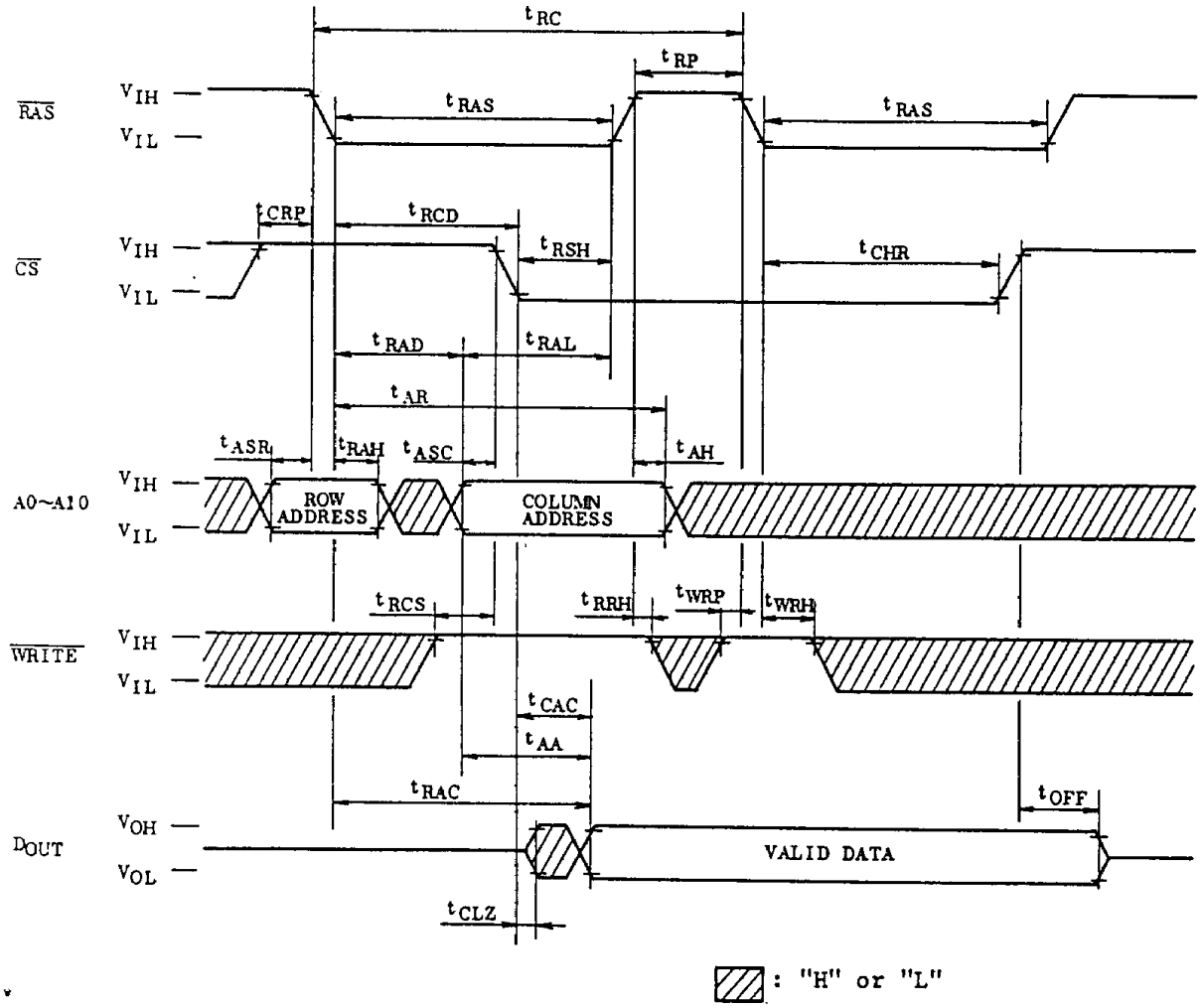


$\overline{CS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE

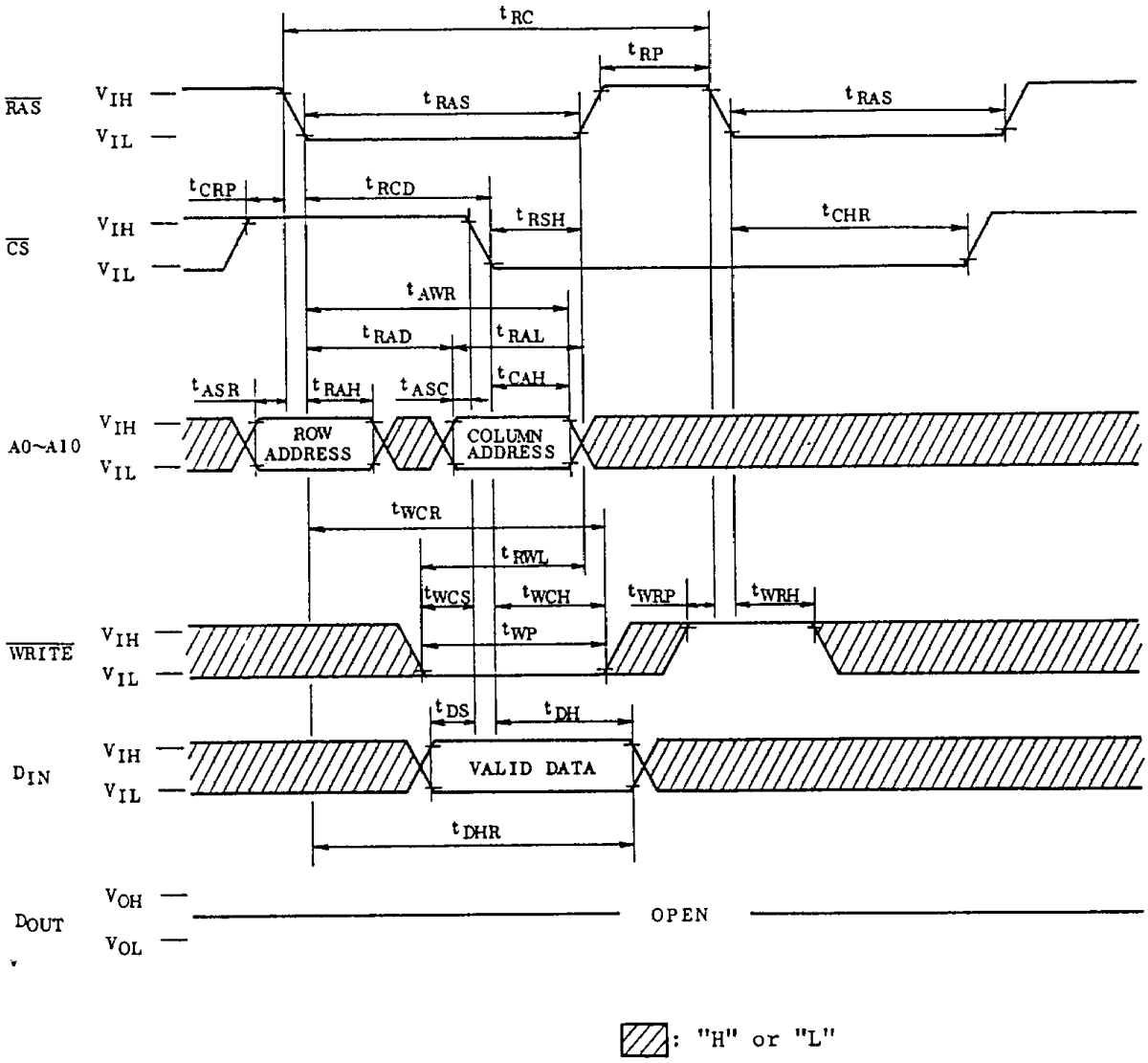


NOTE: A0 ∿ A10="H" or "L" ▨ : "H" or "L"

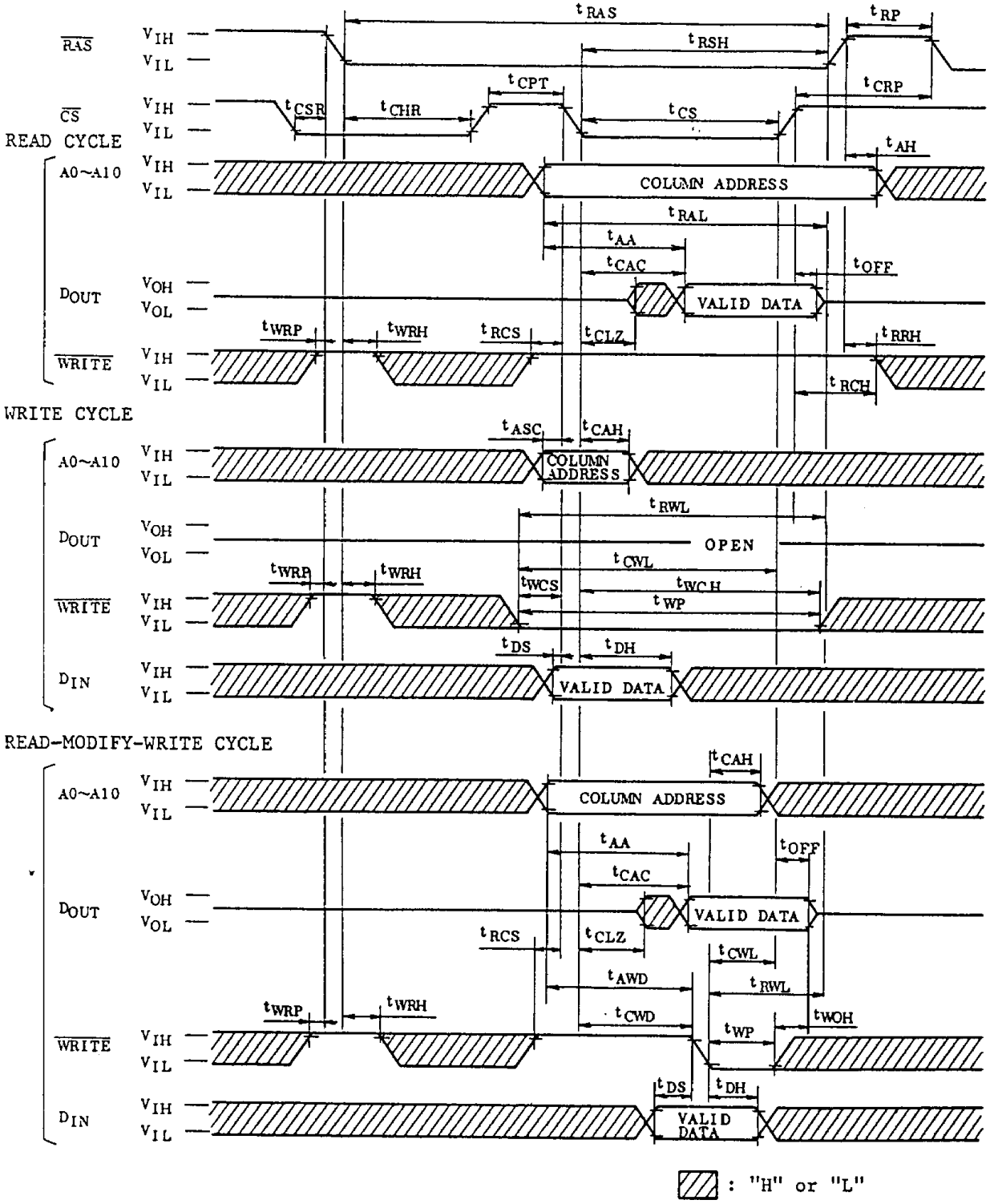
HIDDEN REFRESH CYCLE (READ)



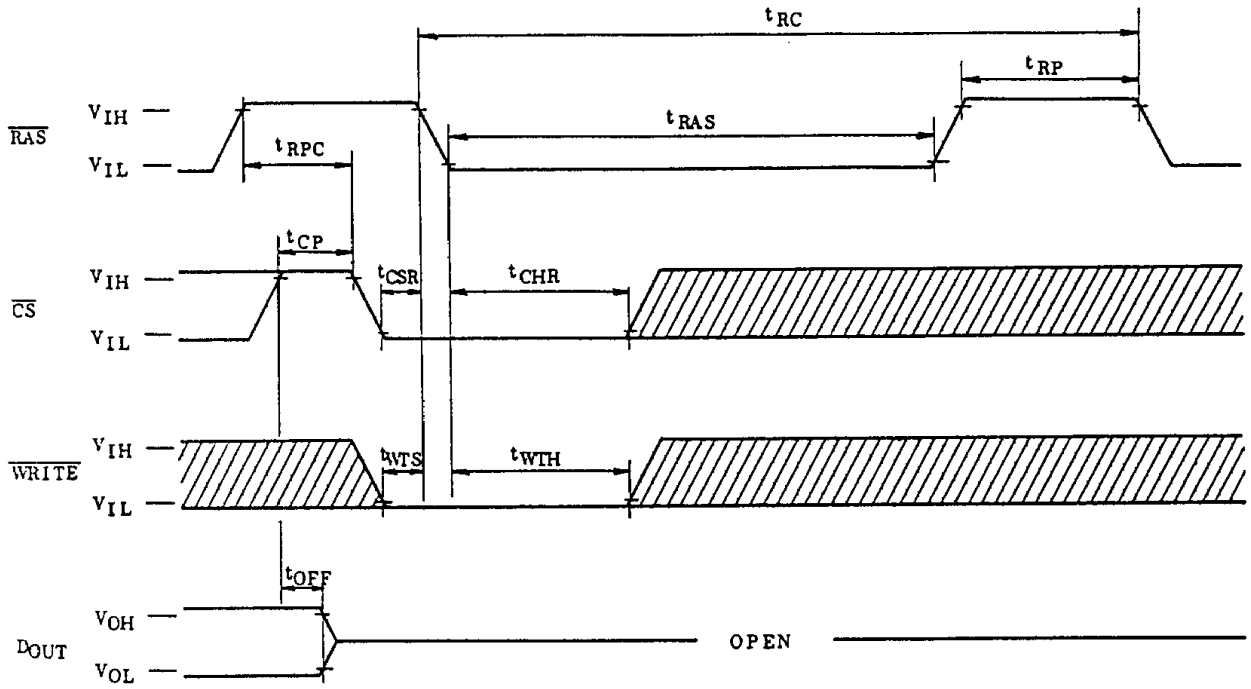
HIDDEN REFRESH CYCLE (WRITE)



$\overline{CS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST CYCLE

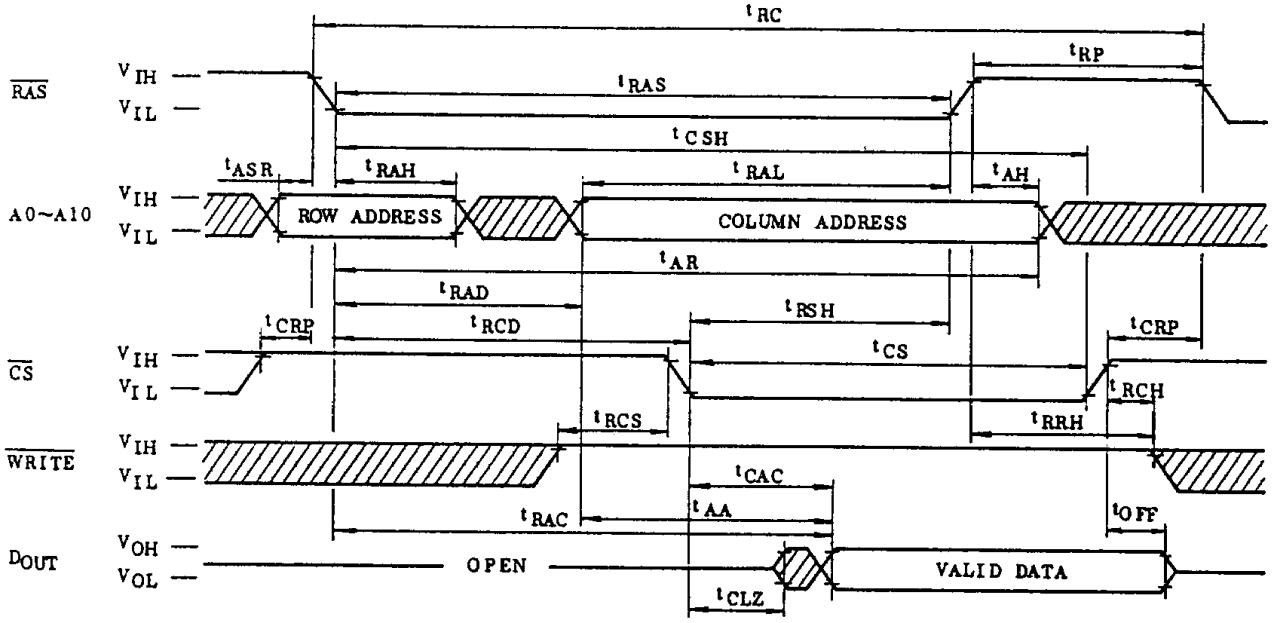


$\overline{\text{WRITE}}$, $\overline{\text{CS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH CYCLE

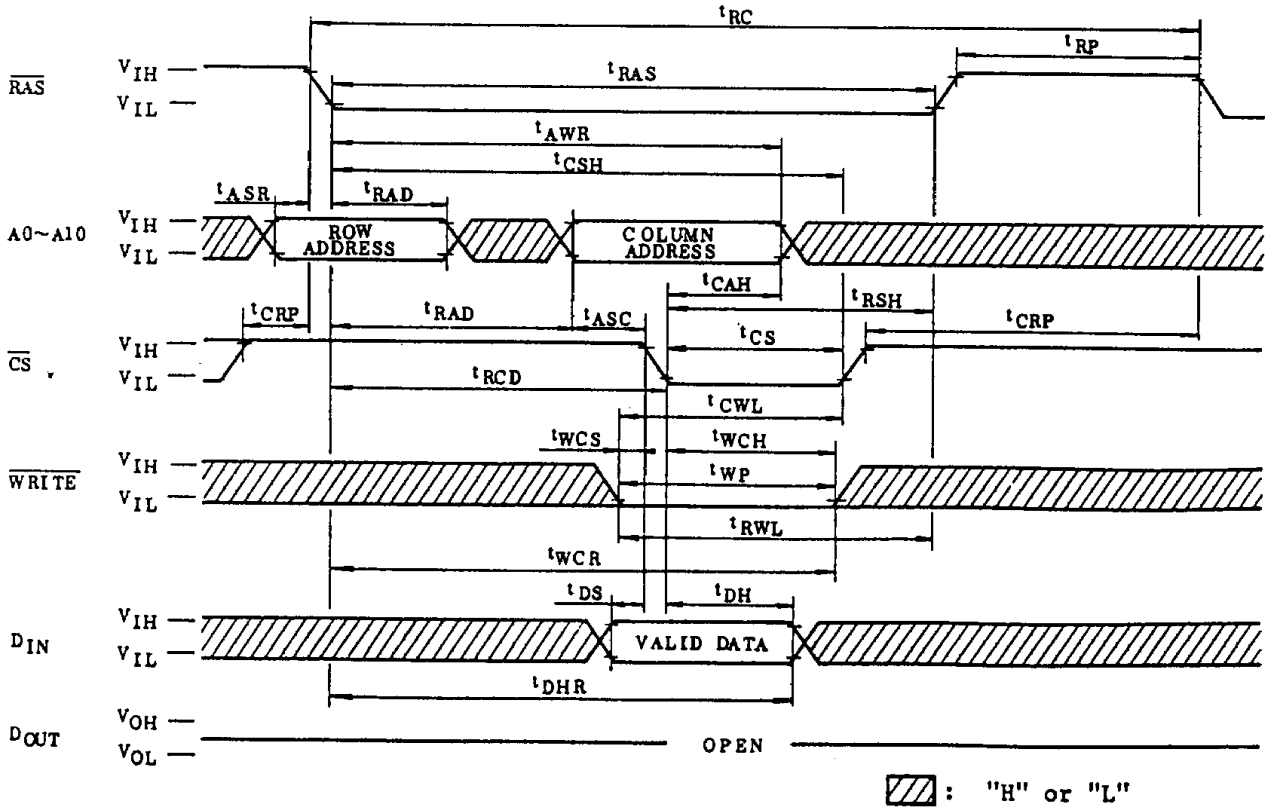


NOTE: D_{IN}, A0 ∿ A10: "H" or "L" ▨ : "H" or "L"

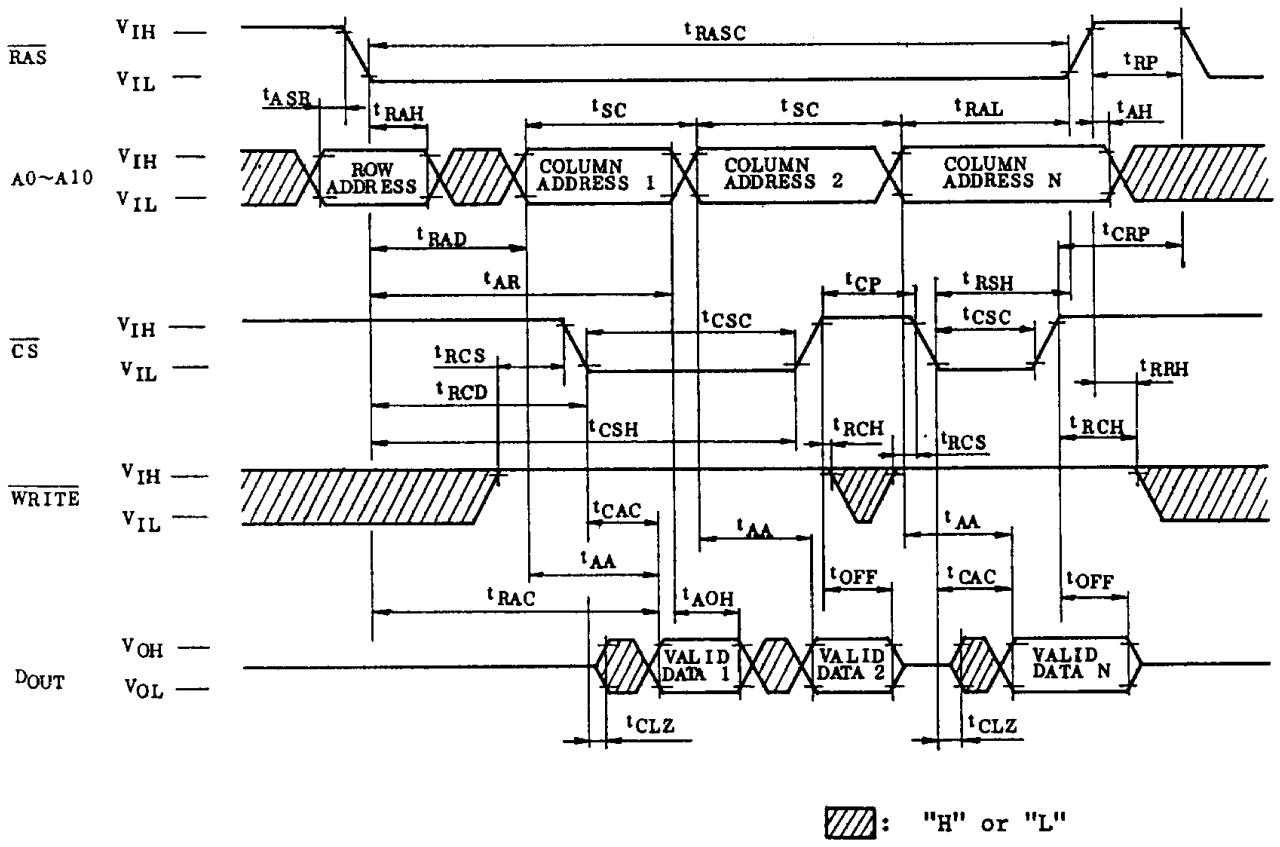
READ CYCLE IN THE TEST MODE



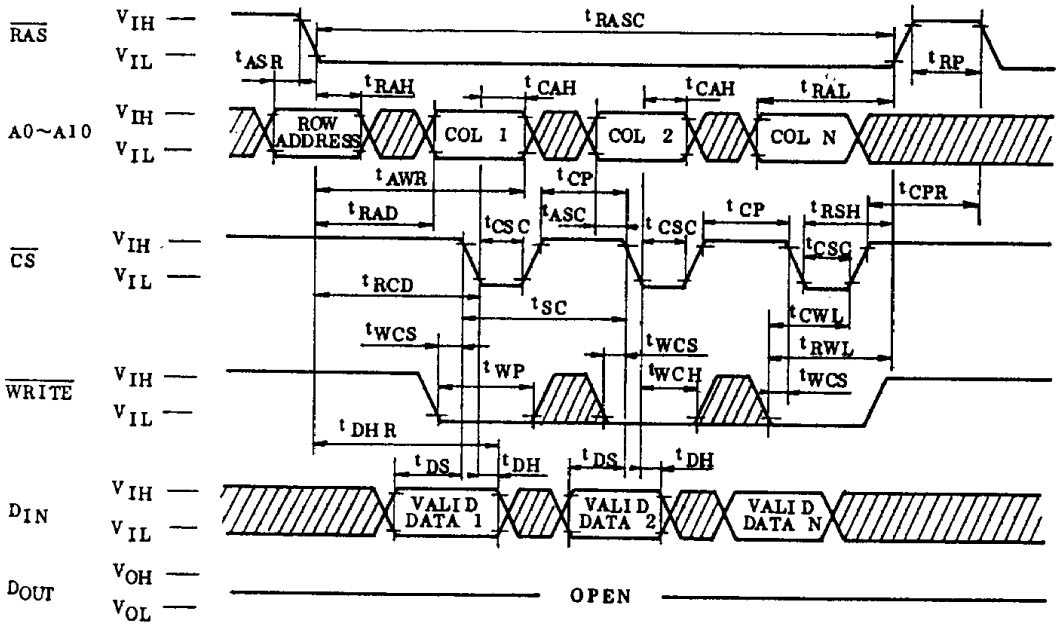
WRITE CYCLE (EARLY WRITE) IN THE TEST MODE



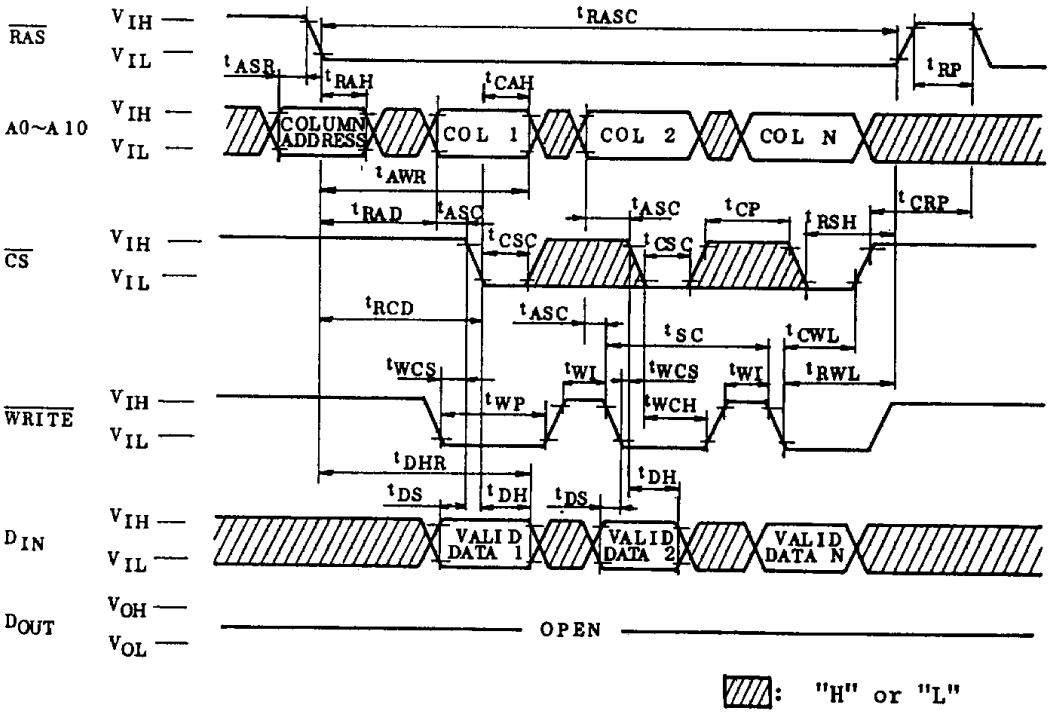
STATIC COLUMN MODE READ CYCLE IN THE TEST MODE



STATIC COLUMN MODE WRITE CYCLE (EARLY WRITE) IN THE TEST MODE



STATIC COLUMN MODE WRITE CYCLE (EARLY WRITE) IN THE TEST MODE



▨: "H" or "L"

TEST MODE

The TC514102J/Z is the RAM organized 4,194,304 words by 1 bit, it is internally organized 524,288 words by 8 bits. In "Test Mode", data are written into 8 sectors in parallel and retrieved the same way. A10R, A10C and A0C are not used. If, upon reading, all bits are equal (all "1"s or "0"s), the data output pin indicates a "1". If any of the bits differed, the data output pin would indicate a "0". Fig. 1 shows the block diagram of TC514102J/Z. In "Test Mode", the 4M DRAM can be tested as if it were a 512K DRAM.

"$\overline{\text{WRITE}}$, $\overline{\text{CS}}$ Before $\overline{\text{RAS}}$ Refresh Cycle" puts the device into "Test Mode". And "$\overline{\text{CS}}$ Before $\overline{\text{RAS}}$ Refresh Cycle" or "$\overline{\text{RAS}}$ Only Refresh Cycle" puts it back into "Normal Mode". In the Test Mode, "$\overline{\text{WRITE}}$, $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh Cycle" performs the refresh operation with the internal refresh address counter. The "Test Mode" function reduces test times (1/8 in case of N test pattern).

BLOCK DIAGRAM IN THE TEST MODE

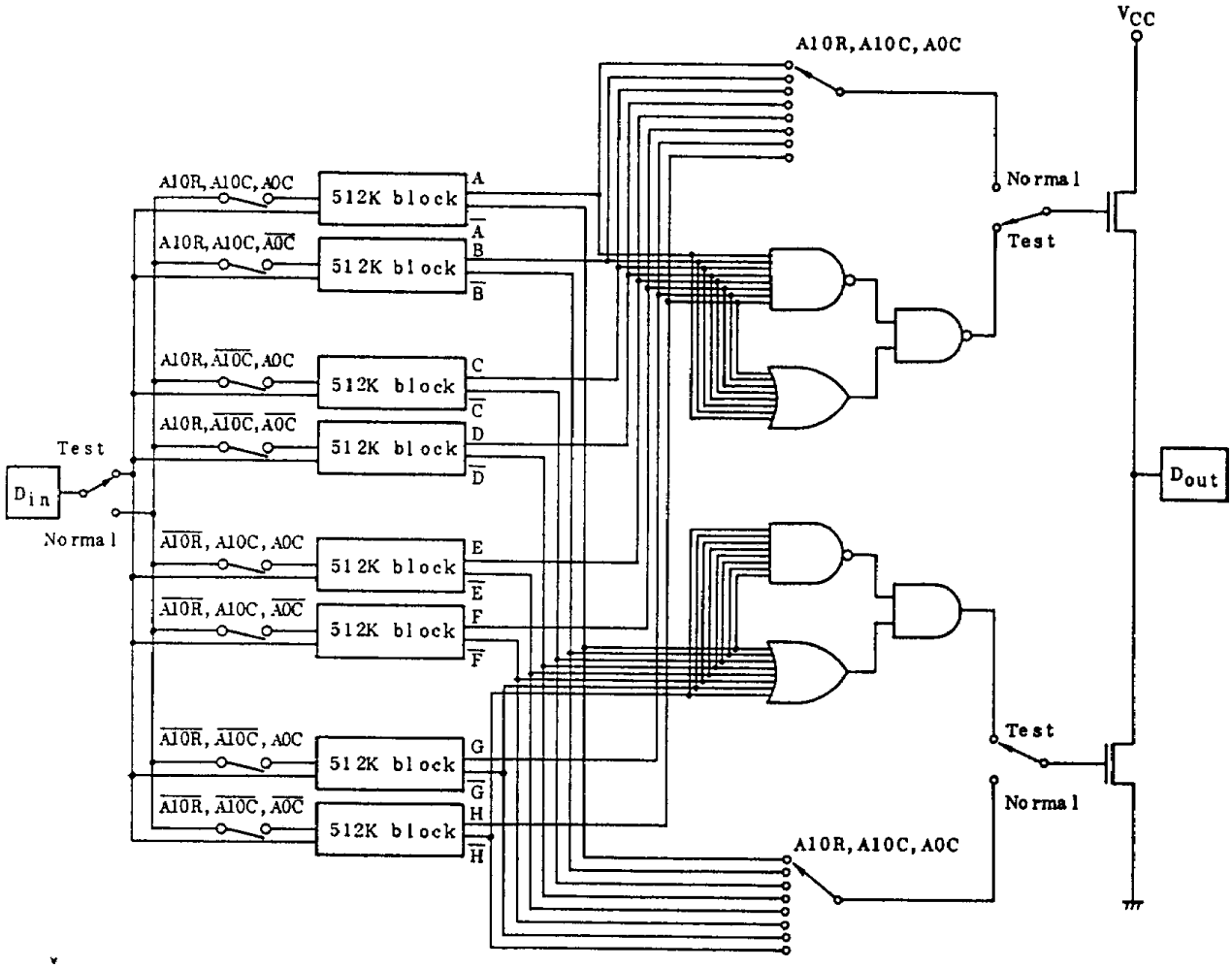


Fig. 1