

**Features**

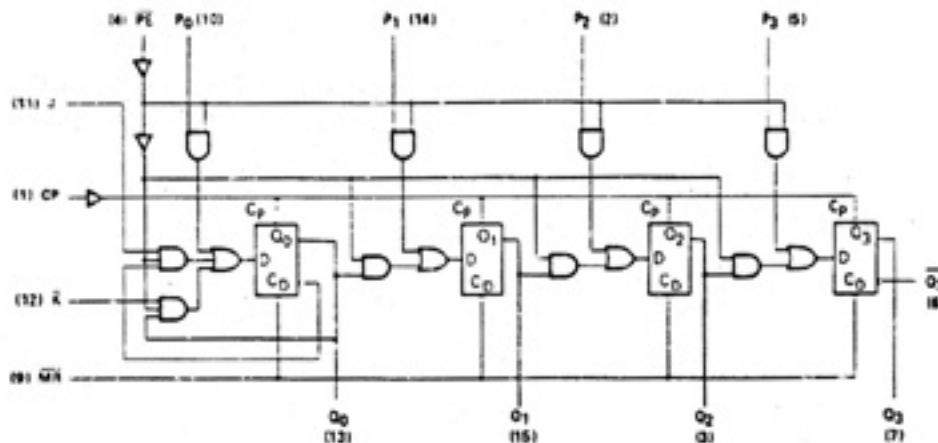
- 3.5 WORST CASE NOISE IMMUNITY
- SERIAL IN, SERIAL OUT, PARALLEL IN, PARALLEL OUT MODES
- FULL SYNCHRONOUS OPERATION OF ALL DATA INPUTS
- $\bar{J}\bar{K}$  FIRST STAGE INPUTS AND  $Q$  AND  $\bar{Q}$  LAST STAGE OUTPUTS FOR EASY CASCADE OPERATION
- OVERRIDING ASYNCHRONOUS COMMON RESET
- BUFFERED CLOCK INPUT - ONLY 1 UNIT LOAD (UL)

- 3MHz TYPICAL SHIFT RATE
- CAN BE USED AS FOUR INDEPENDENT "D" CLOCKED FLIP-FLOPS

**General Description**

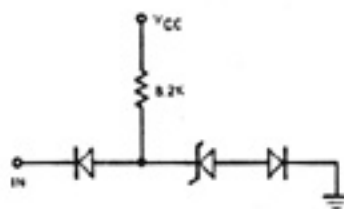
The 375 4-bit shift register is a universal shift register and storage element. It can be used with either serial or parallel inputs and either serial or parallel outputs. For increased flexibility, both parallel entry enable and master reset pins are provided. To facilitate serial entry and easy cascading to longer word lengths, J and  $\bar{K}$  inputs have been provided as well as  $Q_3$  and  $\bar{Q}_3$  outputs.

**Logic Diagram**

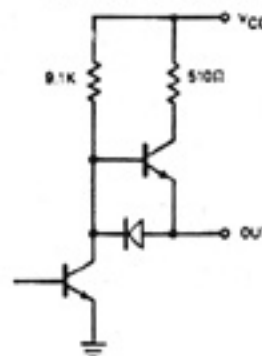


**Equivalent Circuits**

TYPICAL INPUT



TYPICAL OUTPUT



Truth Tables

	$\overline{PE}$	$P_0$	$P_1$	$P_2$	$P_3$	J	$\overline{K}$	$\overline{MR}$
SERIAL ENTRY	1	X	X	X	X	See Tables II and III		1
PARALLEL ENTRY	0	See Table I				X	X	1

NOTE: X = Don't Care

TABLE I  
PARALLEL ENTRY  
 $\overline{PE} = 0, \overline{MR} = 1$

D - INPUT ( $P_0, P_1, P_2,$ or $P_3$ )	OUTPUT Q AT $t_{n+1}$ ( $Q_0, Q_1, Q_2,$ or $Q_3$ )
0	0
1	1

NOTE: (n + 1) indicates output state after next clock transition.

TABLE II  
SERIAL ENTRY  
 $\overline{PE} = 1, \overline{MR} = 1$

J	$\overline{K}$	$Q_0$ at $t_{n+1}$
0	0	0
0	1	$Q_0$ at $t_n$ (no change)
1	0	$\overline{Q_0}$ at $t_n$ (toggles)
1	1	1

TABLE III  
SERIAL ENTRY  
 $\overline{PE} = 1, \overline{MR} = 1$

J and $\overline{K}$ CONNECTED	$Q_0$ at $t_{n+1}$
0	0
1	1

Specifications

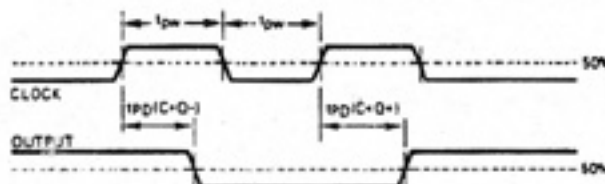
$I_{CC}$ (worst case)	48 mA @ 13V, 64 mA @ 16V		
$t_{PD}$	550 ns	600 ns	600 ns
I/O Function for $t_{PD}$	CP+Q-	CP+Q+	$\overline{MR}$ -Q-

NOTE:  $t_{PD}$  is guaranteed at  $V_{CC} \pm 1$  V and across the applicable temp range with the output loaded with 3 unit loads.

See page 12 for electrical summary data.

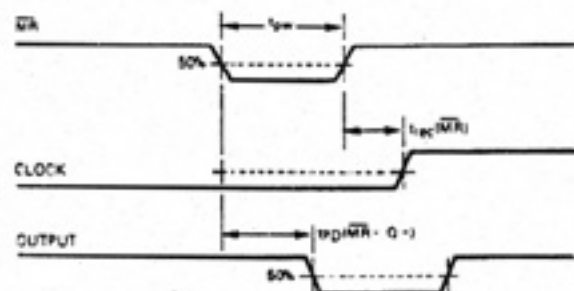
Switching Time Waveforms

Clock to Output Delays and Clock Pulse Width.



OTHER CONDITIONS:  $J = \overline{PE} = \overline{MR} = H$   
 $\overline{K} = L$

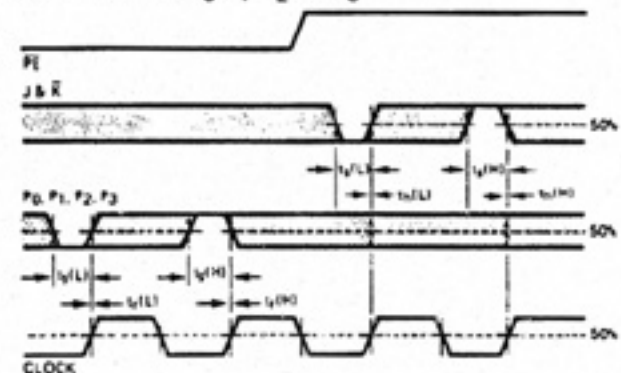
Master Reset Pulse Width, Master Reset to Output Delay and Master Reset to Clock Recovery Time.



OTHER CONDITIONS:  $\overline{PE} = L$   
 $P_0 = P_1 = P_2 = P_3 = H$

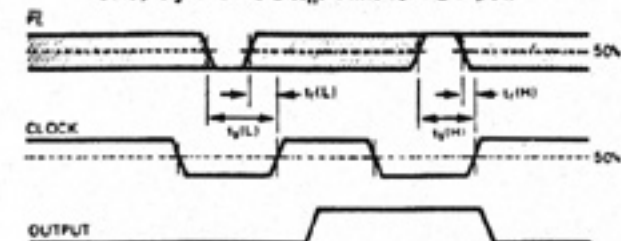
NOTE: The shaded areas indicate when the input is permitted to change for predictable output performance.

Setup ( $t_s$ ) and Hold ( $t_h$ ) Time for Serial Data (J and  $\overline{K}$ ) and Parallel Data ( $P_0, P_1, P_2$  and  $P_3$ )



OTHER CONDITIONS:  $\overline{MR} = H$   
\*J &  $\overline{K}$  SETUP TIME AFFECTS  $Q_0$  ONLY

Setup ( $t_s$ ) and Hold ( $t_h$ ) Time for  $\overline{PE}$  Input.



OTHER CONDITIONS:  $\overline{MR} = H, J = \overline{K} = L$   
 $P_0 = P_1 = P_2 = P_3 = H$

## Switching Time Waveforms (contd.)

### TIMING REQUIREMENTS

The following timing requirements apply across the applicable temperature range and  $V_{CC}$  spread:

CLOCK PULSE WIDTH $t_{pw}$ (CP)	500 ns min.
DATA INPUT SETUP TIME $t_s$ (DATA)	210 ns min.
DATA INPUT RELEASE TIME $t_r$ (DATA)	0 ns min.
$\overline{PE}$ INPUT SETUP TIME $t_s$ ( $\overline{PE}$ )	250 ns min.
$\overline{PE}$ INPUT RELEASE TIME $t_r$ ( $\overline{PE}$ )	0 ns min.
$\overline{MR}$ PULSE WIDTH $t_{pw}$ ( $\overline{MR}$ )	300 ns min.
$\overline{MR}$ RECOVERY TIME $t_{rec}$ ( $\overline{MR}$ )	220 ns min.

SETUP TIME is the minimum time required for the logic level to be present at the logic input prior to the clock transition from LOW to HIGH in order for the flip-flops to respond.

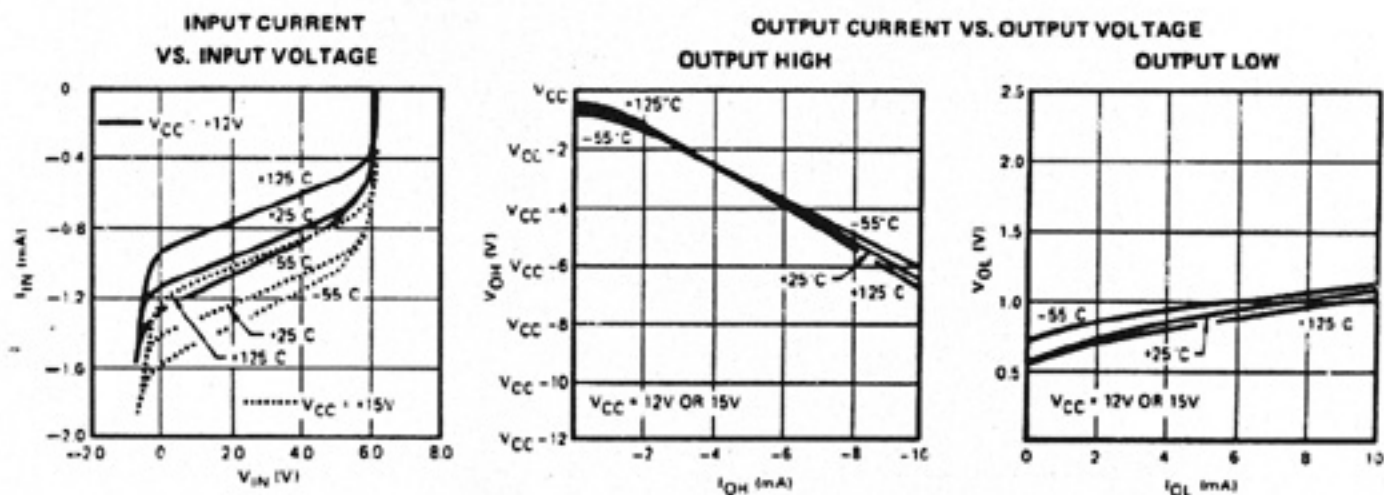
RELEASE TIME is the minimum time that the logic level is required to be present at the logic input after the clock transition from LOW to HIGH in order for the flip-flops to respond.

RECOVERY TIME is defined as the minimum time required between the end of the Reset pulse and the clock transition from LOW to HIGH in order to recognize and transfer HIGH data to the Q outputs.

### Loading Table

PINS	FUNCTION	LOADING
J, $\overline{K}$ , P <sub>0</sub> , P <sub>1</sub> , P <sub>2</sub> , P <sub>3</sub>	Data Inputs	1 UL
$\overline{MR}$	Master Reset	1 UL
$\overline{PE}$	Parallel Enable	1 UL
CP	Clock	1 UL
Q <sub>0</sub> , Q <sub>1</sub> , Q <sub>2</sub> , Q <sub>3</sub> , $\overline{Q}$ <sub>3</sub>	All Outputs	3 UL

## Typical Performance Characteristics

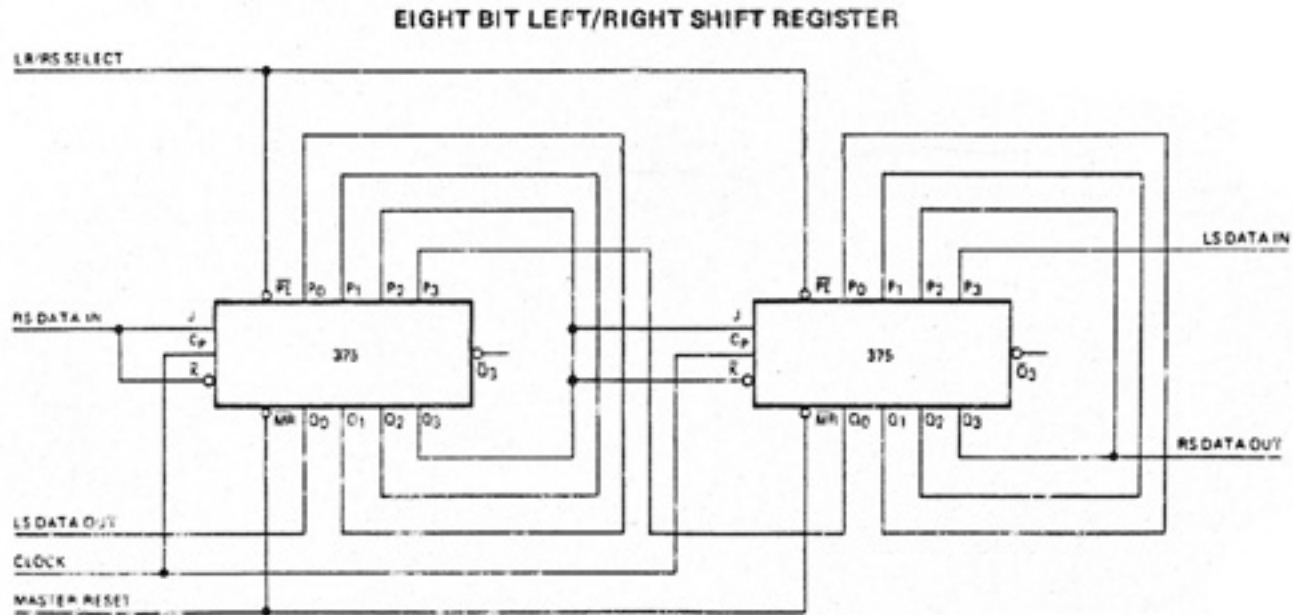


## Typical Applications

The HiNIL 375 4-bit shift register is a universal shift register/storage register. It consists of four master-slave type D flip-flops and some gating circuits to make the device more flexible. The flip-flops are designed so that they will only change on a low-to-high transition of the clock signal. The D inputs of the flip-flops can be logically connected in one of two ways, determined by the state of the  $\overline{PE}$  input. When  $\overline{PE}$  is low, the inputs are controlled by the state of P<sub>0</sub>, P<sub>1</sub>, P<sub>2</sub>, and P<sub>3</sub> inputs. Thus with  $\overline{PE}$  low, the flip-flops are loaded directly through the para-

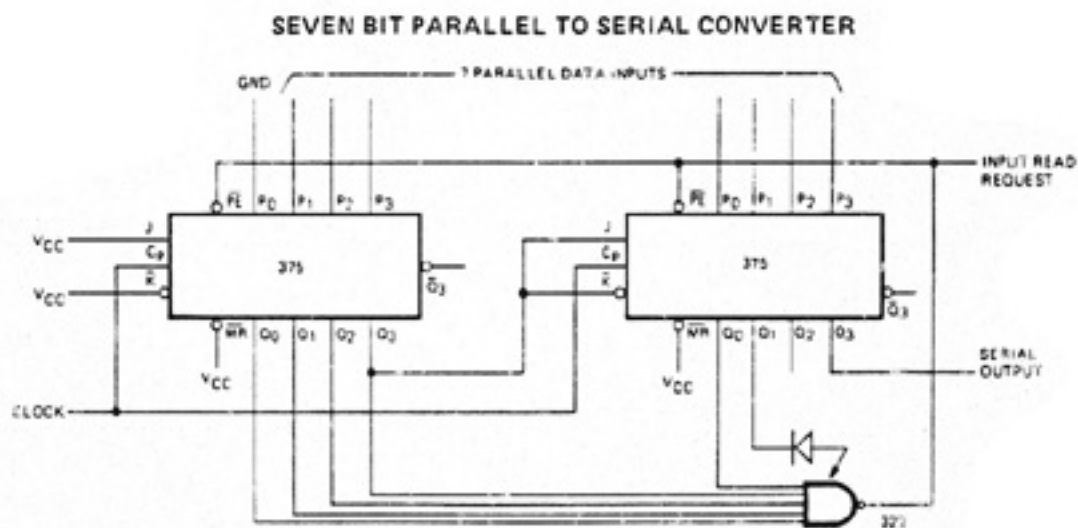
llel inputs. When  $\overline{PE}$  is high, the D inputs of stages Q<sub>1</sub>, Q<sub>2</sub>, and Q<sub>3</sub> are connected to the outputs of Q<sub>0</sub>, Q<sub>1</sub>, and Q<sub>2</sub> respectively. The input of Q<sub>0</sub> is connected through suitable gating to provide JK. Thus with  $\overline{PE}$  high, the 375 operates as a shift right shift register. The  $\overline{MR}$  input resets all flip-flops regardless of the clock and other input states. By wiring J and  $\overline{K}$  together this set of inputs becomes a type D input for easy serial input. For similar reasons, a complementary output has been provided on the last flip-flop.

## Typical Applications (contd.)



This register uses the  $\overline{PE}$  pin to select a left shift or a right shift mode. If this input is high, the normal shift-right operation is performed. If  $\overline{PE}$  is low, the  $\overline{JK}$  inputs are overridden and the

flip-flops are loaded (through the parallel inputs) by the outputs of the following flip-flop, which corresponds to a shift-left operation.



This circuit operates with a continuous logic low on the  $P_0$  input. Thus when the flip-flops are loaded through the parallel inputs, at least one of them will be in the low state and the output of the 322 will be forced high. This disables  $\overline{PE}$  so further inputs will be through the serial  $\overline{JK}$  inputs. Since both of these inputs are high, each clock pulse will load a logic ONE into the front end of the register. Thus the information

previously loaded in the flip-flops will be shifted out, bit-by-bit, until the "0" bit loaded through  $P_0$  reaches  $Q_2$ . The last bit of data is now at  $Q_3$  (and hence the entire seven-bit word has been shifted out), and the 322 is now in a logic ZERO state. The next clock pulse will thus load another seven-bit word into the parallel inputs and the cycle will begin again.