agere systems

Advance Data Sheet
September 2001

CelXpres™ T8208 ATM Interconnect

1 Product Overview

1.1 Features

- OC-12 data throughput on UTOPIA (16-bit) (independently on RX and TX UTOPIA)
- Shared UTOPIA mode
- UTOPIA Level 1 and 2 (8-bit/16-bit) cell-level handshake interface (ATM or PHY layers)
- Multi-PHY (MPHY) operation
- Programmable ATM layer supports up to 64 PHY ports
- Egress SDRAM buffer support to extend UTOPIA output priority queues for 32K to 512K cells:
  — 128 queues configurable up to four queues per PHY with programmable sizes
  — Programmable number of UTOPIA output queues with four levels of priority
- Support of ATM traffic management via partial packet discard (PPD), forward explicit congestion notification (FECN), and the cell loss priority (CLP) bit
- Programmable slew rate GTL+ I/O:
  — Programmable as bus arbiter
  — 1.7 Gbits/s cell bus operation
- Flexible per port cell counters
- Cell header insertion with virtual path identifier (VPI) and virtual channel identifier (VCI) translation via external SRAM (up to 64K entries)
- Support of network node interface (NNI) and user network interface (UNI) header types with optional generic flow-control (GFC) insertion
- Optional sourcing of cell bus clocks from device
- LUT bypass option
- TX UTOPIA cell buffer increased to 256 cells for better queue management with SDRAM queue bypass option
- Ability for cell bus arbiter to mask devices on the cell bus
- Ability to modify cell bus priority based on RX PHY FIFO thresholds
- Programmable priority for control/data cells transmission onto cell bus
- Microprocessor access to all headers of control cell
- Ability to clear counters on read
- Simplified looping to any system device with a single register programming
- UTOPIA clock sourcing with additional settings
- Programmable operations and maintenance and resource management (OAM/RM) cell routing
- Support of multicast and broadcast cells per PHY
- Optional monitoring of misrouted cells
- Counters for dropped cells per queue
- Digital loopback before cell bus
- Microprocessor interface, supporting both *Motorola*® and *Intel*® modes (multiplexed and nonmultiplexed)
- Control cell transmission and reception through microprocessor port
- Single 3.3 V power supply
- 3.3 V TTL I/O (5 V tolerant)
- 272-pin plastic ball grid array (PBGA) package
- Industrial temperature range (–40 °C to +85 °C)
- Hot insertion capability
- Eight GPIO pins
- JTAG support
- Compatible with *Transwitch CellBus*®

1.2 Applications

- Asymmetric digital subscriber line (ADSL) digital subscriber line access multiplexers (DSLAMs)
- Access gateways
- Access multiplexers/concentrators
- Multiservice platforms

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1.3 Description

The *CelXpres* T8208 device integrates all of the required functionality to transport ATM cells across a backplane architecture with high-speed cell traffic exceeding 1.5 Gbits/s to a maximum of 32 destinations. The management of multiple service categories and monitoring of performance on ATM and PHY interfaces is incorporated in the device's functionality. Traffic delivery to multi-PHYs (MPHYs) is managed through the UTOPIA interface.

The T8208 device meets the ATM Forum's universal test and operations PHY interface for ATM (UTOPIA) Level 1, Version 2.01 and Level 2, Version 1.0 specifications for cell-level handshake and MPHY data path operation with rates up to 635 Mbits/s. The T8208 supports the required MPHY operation as described in Sections 4.1 and 4.2 of the ATM Forum's level 2 specification. The T8208 supports MPHY operation with one transmit cell available (TxCLAV) signal and one receive cell available (RxCLAV) signal for up to 16 PHY ports for an 8-bit UTOPIA 2 interface configuration. With four transmit cells available/enable (TxCLAV/Enb*) pairs of signals and receive cell available/enable (RxCLAV/Enb*) pairs of signals, 64 MPHYs can be supported. For a 16-bit UTOPIA 2 interface configuration, the T8208 supports MPHY operation with one transmit cell available (TxCLAV) signal and one receive cell available (RxCLAV) signal for up to 8 PHY ports. With four transmit cell available (TxCLAV/Enb*) signals and four receive cell available (RxCLAV/Enb*) signals, 32 MPHYs can be supported in 16-bit UTOPIA 2 interface configuration. In addition to the required UTOPIA signals, the optional transmit parity (TxPRTY) and receive parity (RxPRTY) signals are provided.

The T8208 may be configured as an ATM or PHY level device providing cell routing between UTOPIA and a 32-bit wide cell bus. In addition to the 32 data signals, the bus has the following signals:

- Read clock
- Write clock
- Frame sync
- Acknowledge

ATM cells arriving from the UTOPIA interface may get VPI and VCI translation and routing information from a look-up table in external SRAM. An external synchronous dynamic random access memory (SDRAM) is used to extend the buffering for ATM cells destined for the UTOPIA interface. This external SDRAM may be partitioned into four or less independently sized queues per PHY for a configuration of 32 MPHYs and two queues per PHY or a programmable number of queues per PHY for a configuration of 64 MPHYs. The four queues may be used to support quality of service (QoS) by directing different traffic categories to each queue. The number of cells per queue per PHY is programmable.

The *CelXpres* T8208 provides a shared UTOPIA mode, which allows two devices on different cell buses to share the same UTOPIA bus in ATM mode. Using a glueless interface, the two T8208 devices resolve queue priorities and arbitrate the use of the UTOPIA bus. This shared mode can be used to provide redundancy or increase UTOPIA traffic capacity by supporting traffic from multiple cell busses.

The *CelXpres* T8208 supports the transport of control and loopback cells with an external microprocessor. Control or loopback cells may be sent or received through the microprocessor interface. The 8-bit microprocessor interface may be configured to be *Motorola* or *Intel* compatible and is used to configure and monitor the device.

1 Product Overview (continued)

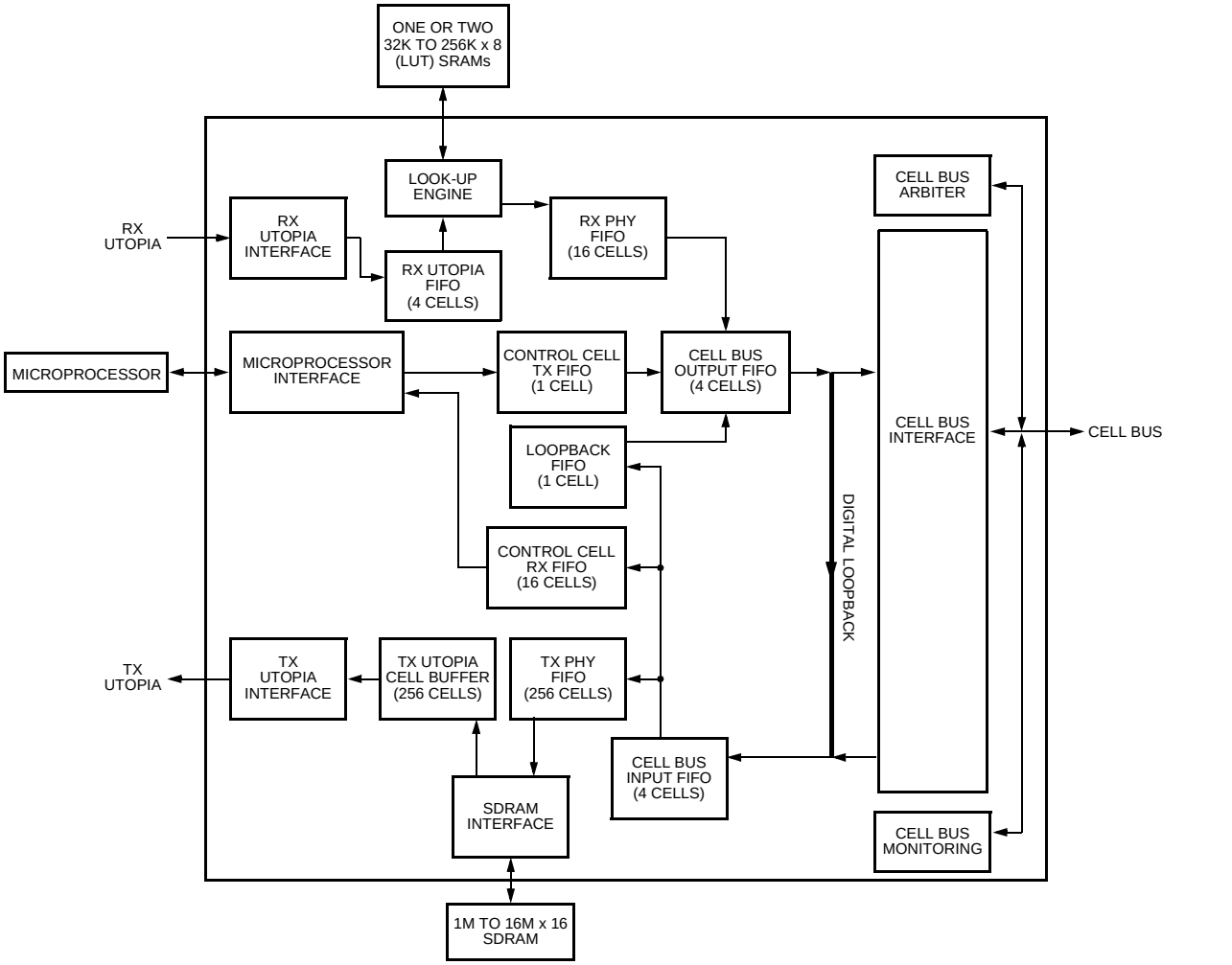

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Figure 1. Functional Block Diagram

1 Product Overview (continued)

Figure 2 illustrates the use of the *CelXpres* T8208 in a system with dual backplane cell buses using shared UTOPIA mode. In this configuration, both T8208 devices on each card receive cells from the UTOPIA bus, and each device uses its translation table to determine if the cell should be transmitted on its backplane cell bus. In the egress direction, each T8208 device receives cells from its cell bus to transmit on the UTOPIA bus. MPHY arbitration and queue priorities are resolved using a six-wire interface between the two devices. Although a single ATM virtual connection is not typically established on both backplane cell buses simultaneously, no restrictions exist for a single PHY utilizing both backplane cell buses for different virtual connections supporting higher throughput from two bus interfaces. Redundant bus configurations can be supported in the event of a bus failure with T8208 devices by configuring one device to assume bus responsibility from the other.

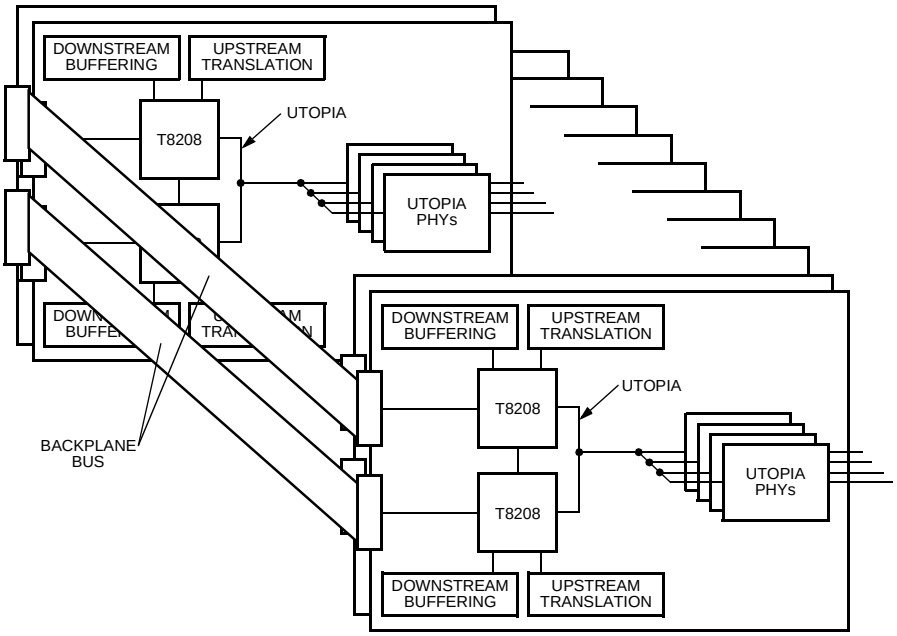

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Figure 2. Dual Bus Implementation

1 Product Overview (continued)

1.4 Conventions

- All numbers in this document are decimals unless otherwise specified.
- Hexadecimal numbers can be identified by the ‘h’ suffix, e.g., A5h.
- Binary numbers are either in double quotes for multiple bits or in single quotes for individual bits, e.g., “1001” and ‘0.’
- A byte is 8 bits, a word is 16 bits, and a double word (dword) is 32 bits.
- A binary value of ‘1’ is high, and a binary value of ‘0’ is low.
- To clear is to change one or multiple bit values to ‘0.’
- To set is to change one or multiple bit values to ‘1.’
- All memory addresses are specified in hexadecimal.
- Addresses are converted from bytes to words or double words using the little-endian format, unless otherwise specified.
- A signal name with a trailing asterisk is active-low, e.g., sd_we*.
- Bits y to x will be designated bits (y:x).

1 Product Overview (continued)

1.5 Glossary

Bus Cell:
Major content of the cell bus frame consisting of 56 bytes, 4 bytes for routing options and 52 bytes for the ATM cell content, which excludes the HEC. The bus cell is preceded by the 4 bytes of request and followed by the 4 bytes of grant and parity information.

CLP:
Cell loss priority. The CLP is a 1-bit field in the cell header that becomes set when the cell violates the negotiated quality of service parameters.

EFCI:
Explicit forward congestion indication. The EFCI is a 1-bit field in the PTI field of the cell header that becomes set when the cell encounters congestion.

FECN:
Forward explicit congestion notification. FECN is a method used by the network to signal to the destination when congestion is encountered. The EFCI bit is used to indicate the congestion.

GFC:
Generic flow control. The GFC is a 4-bit field in the cell header that may be used by a UNI to support traffic and congestion control. Typically, this field is programmed to “0000” indicating that generic flow control is not supported. GFC may be used in priority protocols.

Grant Section:
Last 4 bytes of the cell bus frame. The grant section occurs during the last clock cycle of the cell bus frame. During this cycle, the cell bus arbiter indicates which T8208 may transmit during the next bus cell unit of the cell bus frame. A parity vector is also transmitted during the grant section.

HEC:
Header error control. The HEC is a 1-byte field in the cell header used for bit error detection and correction in the header.

NNI:
Network node interface. The NNI is the interface between nodes in the public network.

OAM Cell:
Operations and maintenance cell. An OAM cell carries local management information.

PPD:
Partial packet discard. PPD is a technique to relieve congestion. When one cell in a packet is lost, all remaining cells in the packet, except the last, are discarded.

PTI:
Payload type identifier. The PTI is a 3-bit field in the cell header containing information about the type of data (user, OAM, or traffic management) and about encountered congestion.

QoS:
Quality of service. Quality of service parameters define the performance requirements and characteristics for traffic on an assigned channel. Some parameters include cell loss ratio, cell transfer delay, cell delay variation, peak cell rate, and sustained cell rate.

Request Section:
First 4 bytes of the cell bus frame. The request section occurs during the first clock cycle of the cell bus frame. During this cycle, 16 T8208 devices assert their transmission requests onto the cell bus.

RM:
Resource management. RM is the local management of network resources.

RxCLAV:
Receive cell available signal as described in the ATM Forum’s universal test and operations PHY interface for ATM (UTOPIA) Level 1, Version 2.01 and Level 2, Version 1.0 specifications.

RxENB:
Receive enable signal as described in the ATM Forum’s universal test and operations PHY interface for ATM (UTOPIA) Level 1, Version 2.01 and Level 2, Version 1.0 specifications.

TxCLAV:
Transmit cell available signal as described in the ATM Forum’s universal test and operations PHY interface for ATM (UTOPIA) Level 1, Version 2.01 and Level 2, Version 1.0 specifications.

TxENB:
Transmit enable signal as described in the ATM Forum’s universal test and operations PHY interface for ATM (UTOPIA) Level 1, Version 2.01 and Level 2, Version 1.0 specifications.

UNI:
User network interface. The UNI is the interface between a private network node and a public network node.

VCI:
Virtual channel identifier. The VCI is a 2-byte field in the cell header that identifies the virtual channel used by the cell.

VPI:
Virtual path identifier. The VPI is an 8-bit field in the UNI cell header or a 12-bit field in the NNI cell header that identifies the virtual path of the cell.

2 Pinout

This section defines the *CelXpres* T8208 pins. All TTL compatible inputs or I/O are 5 V tolerant. No GTL+ inputs or I/O are 5 V tolerant.

Table 1. UTOPIA Pins

Symbol	Ball	Reset Value	Type	Name/Description
u_rxaddr[4:0]	R2, P3, R1, P2, P1	Z	I/O	**RX UTOPIA Address Lines.** 10 mA drive, TTL compatible I/O, 5 V tolerant.
u_rxdata[15:0]	V4, W4, Y2, W3, Y1, W2, V3, W1, V2, U3, T4, V1, U2, T3, U1, T2	—	I	**RX UTOPIA Data Lines.** TTL compatible input, 5 V tolerant.
u_rxclk	T1	Z	I/O	**RX UTOPIA Clock.** 10 mA drive, TTL compatible I/O, 5 V tolerant.
u_rxsoc	P4	—	I	**RX UTOPIA Start of Cell (Active-High).** TTL compatible input, 5 V tolerant.
u_rxclav[0]	L4	Z	I/O	**RX UTOPIA PHY 0 Cell Available (Active-High).** Main RX cell available in single PHY mode. 10 mA drive, TTL compatible I/O, 5 V tolerant. This pin has an internal 50 kΩ pull-up resistor.
u_rxclav[3:1]	M3, M2, M1	—	I	**RX UTOPIA Cell Available Lines (Active-High).** TTL compatible input, 5 V tolerant. These pins have an internal 50 kΩ pull-up resistor.
u_rxenb*[0]	M4	Z	I/O	**RX UTOPIA PHY 0 Enable (Active-Low).** Main RX enable in single PHY mode. 10 mA drive, TTL compatible I/O, 5 V tolerant.
u_rxenb*[3:1]	N3, N2, N1	Z	I/O	**RX UTOPIA PHY Enable Lines (Active-Low).** 10 mA drive, TTL compatible I/O, 5 V tolerant.
u_rxprty	R3	—	I	**RX UTOPIA Odd Parity.** TTL compatible input, 5 V tolerant. This pin has an internal 50 kΩ pull-up resistor.
u_txaddr[4:0]	P17, R19, R20, P18, P19	Z	I/O	**TX UTOPIA Address Lines.** 10 mA drive, TTL compatible I/O. 5 V tolerant.
u_txdata[15:0]	Y18, U16, V17, W18, Y19, V18, W19, Y20, W20, V19, U19, U18, T17, V20, U20, T18	Z	O	**TX UTOPIA Data Lines.** 10 mA drive, TTL compatible output.
u_txclk	R18	Z	I/O	**TX UTOPIA Clock.** 10 mA drive, TTL compatible I/O, 5 V tolerant.
u_txsoc	T20	Z	O	**TX UTOPIA Start of Cell (Active-High).** 10 mA drive, TTL compatible output.
u_txclav[0]	M20	Z	I/O	**TX UTOPIA PHY 0 Cell Available (Active-High).** Main TX cell available in single PHY mode. 10 mA drive, TTL compatible I/O. 5 V tolerant. This pin has an internal 50 kΩ pull-up resistor.
u_txclav[3:1]	M17, M18, M19	—	I	**TX UTOPIA Cell Available Lines (Active-High).** TTL compatible input, 5 V tolerant. These pins have an internal 50 kΩ pull-up resistor.
u_txenb*[0]	N20	Z	I/O	**TX UTOPIA PHY 0 Enable (Active-Low).** Main TX enable in single PHY mode. 10 mA drive, TTL compatible I/O, 5 V tolerant.
u_txenb*[3:1]	P20, N18, N19	Z	O	**TX UTOPIA Enable Lines (Active-Low).** 10 mA drive, TTL compatible output.
u_txprty	T19	Z	O	**TX UTOPIA Odd Parity.** 10 mA drive, TTL compatible output.

2 Pinout (continued)

Table 2. Shared UTOPIA Pins

Symbol	Ball	Reset Value	Type	Name/Description
u_shr_grant[1:0]	W17, V16	1	I/O	**Shared UTOPIA Grant.** Used for grant if device is shared. UTOPIA master to indicate approval of the requested cell transfer. 6 mA drive, TTL compatible I/O. These pins have an internal 50 kΩ pull-up resistor.
u_shr_req[3:0]	B2, B3, C4, D5	1	I/O	**Shared UTOPIA Request.** Used to indicate a cell to be transferred from a requested queue if device is shared UTOPIA slave. 6 mA drive, TTL compatible I/O. These pins have an internal 50 kΩ pull-up resistor.

2 Pinout (continued)

Table 3. Cell Bus Pins

Symbol	Ball	Reset Value	Type	Name/Description
ua*[4:0]	B18, B17, C17, D16, A18	—	I	**Unit Address Lines (Active-Low).** Address assigned to device for cell bus identification. TTL compatible input, 5 V tolerant.
cb_d*[31:0]	B5, C6, D7, A5, B6, C7, A6, B7, A7, C8, B8, A8, D9, C9, B9, A9, A11, C11, B11, A12, B12, C12, D12, A13, B13, C13, A14, B14, C14, A15, B15, D14	Z	I/O	**Cell Bus Data Lines (Active-Low).** GTL+ I/O.
cb_wc*	A10	—	I	**Cell Bus Write Clock (Active-Low).** Uses falling edge to output data on cell bus. Write and read clocks have the same frequency but different phase. GTL+ input.
cb_rc*	B10	—	I	**Cell Bus Read Clock (Active-Low).** Uses falling edge to latch data from cell bus. Write and read clocks have the same frequency but different phase. GTL+ input.
cb_fs*	C15	Z	I/O	**Cell Bus Frame Sync (Active-Low).** GTL+ I/O.
cb_ack*	B16	Z	I/O	**Cell Bus Acknowledge Signal (Active-Low).** Driven low on cycle 0 of the following frame when a valid cell is received from the cell bus. This signal is not driven for broadcast or multicast cells. GTL+ I/O.
arb_en*	A17	—	I	**Cell Bus Arbiter Enable (Active-Low).** Cell bus arbiter enable. Only one device on the cell bus may be configured as arbiter. TTL-compatible input, 5 V tolerant. This pin has an internal 50 kΩ pull-up resistor.
cb_disable*	C16	—	I	**Cell Bus Disable (Active-Low).** CMOS input that 3-states all GTL+ outputs when low, but GTL+ buffer inputs are active. This pin has an internal 50 kΩ pull-up resistor.
cb_iref	A4	—	I	**Cell Bus Current Reference.** Precision current reference for GTL+ buffers. A 1 kΩ, 1% resistor must be connected between this pin and GND.
cb_vref	D10	—	I	**Cell Bus Voltage Reference.** GTL+ buffer threshold voltage reference (1.0 V typical). This voltage reference is 2/3 V_{TT}, created using a voltage divider of three 1 kΩ, 1% resistors between V_{TT} and cb_vref_vss.
cb_vref_vss	C10	—	—	**Cell Bus Voltage Reference Ground.**
cb_gen_wc	A3	—	O	**Cell Bus Generated Write Clock.** TTL Compatible (+5 V) driver. 10 mA drive. This is the write clock generated by the T8208 device. Read/write clock delay set by register 0122h bits[15:13].
cb_gen_rc	B4	—	O	**Cell Bus Generated Read Clock.** TTL Compatible (+5 V) driver. 10 mA drive. This is the read clock generated by the T8208 device. Read/write clock delay set by register 0122h bits[15:13].

2 Pinout (continued)

Table 4. SDRAM Interface Pins

Symbol	Ball	Reset Value	Type	Name/Description
sd_a[11:0]	L19, L18, L20, K20, K19, K18, K17, J20, J19, J18, J17, H20	X	O	**SDRAM Address Lines.** 7 mA drive, TTL compatible output. These buffers are 50 Ω impedance matching buffers. Long printed-wiring board traces should have 50 Ω nominal impedance.
sd_d[15:0]	F19, E20, G17, F18, E19, D20, E18, D19, C20 E17, D18, C19, B20, C18, B19, A20	Z	I/O	**SDRAM Data Lines.** 7 mA drive, TTL compatible I/O. These buffers are 50 Ω impedance matching buffers. Long printed-wiring board traces should have 50 Ω nominal impedance.
sd_bs[1:0]	H18, G20	X	O	**SDRAM Bank Selects.** 7 mA drive, TTL compatible output. These buffers are 50 Ω impedance matching buffers. Long printed-wiring board traces should have 50 Ω nominal impedance.
sd_ras*	G19	1	O	**SDRAM Row Address Select (Active-Low).** 7 mA drive, TTL compatible output. This buffer is a 50 Ω impedance matching buffer. Long printed-wiring board traces should have 50 Ω nominal impedance.
sd_cas*	F20	1	O	**SDRAM Column Address Select (Active-Low).** 7 mA drive, TTL compatible output. This buffer is a 50 Ω impedance matching buffer. Long printed-wiring board traces should have 50 Ω nominal impedance.
sd_we*	G18	1	O	**SDRAM Write Enable (Active-Low).** 7 mA drive, TTL compatible output. This buffer is a 50 Ω impedance matching buffer. Long printed-wiring board traces should have 50 Ω nominal impedance.
sd_clk	H19	Z	O	**SDRAM Clock.** 7 mA drive, TTL compatible output. This buffer is a 50 Ω impedance matching buffer. Long printed-wiring board traces should have 50 Ω nominal impedance.
sd_iref	A19	—	I	**SDRAM Current Reference.** Precision current reference for SDRAM buffers. A 1 kΩ, 1% resistor must be connected between this pin and GND.

2 Pinout (continued)

Table 5. Microprocessor Interface Pins

Symbol	Ball	Reset Value	Type	Name/Description
a[7:1]	W6, Y6, V7, W7, Y7, V8, W8	—	I	**Microprocessor Port Address Lines.** Most significant 7 bits of the address bus. TTL compatible input, 5 V tolerant.
a[0]/ale	Y8	—	I	**Microprocessor Port Address 0/Address Latch Enable.** Least significant bit of the address bus in nonmultiplexed mode or address latch enable in multiplexed mode.
d[7:0]	U9, V9 W9, Y9, W10, V10, Y10, Y11	Z	I/O	**Microprocessor Port Data Lines.** 6 mA drive, TTL compatible I/O, 5 V tolerant.
sel*	W12	—	I	**Microprocessor Chip Select (Active-Low).** TTL compatible input, 5 V tolerant.
wr*_ds*	V12	—	I	**Microprocessor Write/Data Strobe.** Active-low write enable in *Intel* mode. Active-low data strobe in *Motorola* mode. TTL compatible input, 5 V tolerant.
rd*_rw*	U12	—	I	**Microprocessor Read/Write.** Active-low read enable in *Intel* mode, or read/write* enable in *Motorola* mode, where read is active-high and write is active-low. TTL compatible input, 5 V tolerant.
int_irq*	Y12	0/1	O	**CPU Interrupt.** Active-high in *Intel* mode and active-low in *Motorola* mode. 4 mA drive, TTL compatible output.
rdy_dtack*	U11	Z	O	**Ready/Data Transfer Acknowledge.** Active-high ready signal in *Intel* mode and active-low data transfer acknowledge in *Motorola* mode. Indicates access complete. 6 mA drive, TTL compatible output.
mot_sel	Y13	—	I	***Intel*/*Motorola* Selection.** '0' = *Intel*, '1' = *Motorola*. TTL compatible input, 5 V tolerant.
mux	W13	—	I	**Microprocessor Multiplex Select.** Active-high for multiplex mode. TTL compatible input, 5 V tolerant.

2 Pinout (continued)

Table 6. Translation SRAM Interface

Symbol	Ball	Reset Value	Type	Name/Description
tr_a[17:0]	L3, L2, L1, K1, K3, K2, J1, J2, J3, J4, H1, H2, H3, G1, G2, G3, F1, F2	X	O	**Translation RAM Address Lines.** 4 mA drive, TTL compatible output.
tr_d[7:0]	E3, D1, C1, E4, D3, D2, C2, B1	Z	I/O	**Translation RAM Data Lines.** 4 mA drive, TTL compatible I/O, 5 V tolerant.
tr_cs*[1:0]	E1, E2	1	O	**Translation RAM Chip Selects (Active-Low).** Chip selects to select one of two external SRAMs. For connection to one external device, tr_cs*[0] is used. 4 mA drive, TTL compatible output.
tr_oe*	F3	1	O	**External RAM Output Enable (Active-Low).** 4 mA drive, TTL compatible output.
tr_we*	G4	1	O	**External RAM Write Enable (Active-Low).** 4 mA drive, TTL compatible output.

Table 7. JTAG Pins

Symbol	Ball	Reset Value	Type	Name/Description
jtag_tdi	Y16	—	I	**Test Data Input (JTAG).** TTL compatible input, 5 V tolerant. This pin has an internal 50 kΩ pull-up resistor.
jtag_tdo	W16	X	O	**Test Data Output (JTAG).** 4 mA drive, TTL compatible output.
jtag_trst*	W15	—	I	**Test Reset (JTAG) (Active-Low).** Should be pulled low when part is in normal operation. TTL compatible input, 5 V tolerant. This pin has an internal 50 kΩ pull-up resistor.
jtag_tclk	V15	—	I	**Test Clock (JTAG).** TTL compatible input, 5 V tolerant. This pin has an internal 50 kΩ pull-up resistor.
jtag_tms	U14	—	I	**Test Mode Select (JTAG).** TTL compatible input, 5 V tolerant. This pin has an internal 50 kΩ pull-up resistor.

2 Pinout (continued)

Table 8. General-Purpose Pins

Symbol	Ball	Reset Value	Type	Name/Description
gpio[7:0]	U5, Y3, Y4, V5, W5, Y5, V6, U7	—	I/O	**General-Purpose I/O.** 4 mA drive, TTL compatible I/O, 5 V tolerant. These pins have an internal 50 kΩ pull-up resistor.
reset*	V14	—	I	**Reset (Active-Low).** Schmitt trigger, TTL compatible input, 5 V tolerant.
xtalin	V13	—	I	**Crystal Input (pclk).** This input may be driven by either a crystal or an external clock. If a crystal is used, connect it between this pin and xtalout and connect the appropriately valued capacitor from this pin to V_{SS}. If an external clock is used, this is a 5 V tolerant CMOS input with 50 MHz max input frequency.
xtalout	Y14	—	O	**Crystal Output Feedback.** If a crystal is used, connect it between this pin and xtalin and connect the appropriately valued capacitor from this pin to V_{SS}. If an external clock is used to drive xtalin, this pin must be left unconnected.
cko	W11	—	O	**Buffered Clock Output.** If enabled, pclk is output on this pin. 8 mA drive, TTL compatible output. This pin is high impedance if not enabled.
cko_e	V11	—	I	**CKO Enable.** Enable for buffered clock output. If cko is not used, tie this enable pin low. Active-high, TTL compatible input, 5 V tolerant.
NC	A2, A16, C3, C5, Y15, Y17	—	—	**No Connection.** Reserved.

Table 9. Power Pins

Symbol	Ball	Name/Description
V_{DD}	D6, D11, D15, F4, F17, K4, L17, R4, R17, U6, U10, U15	**Power.** 3.3 V. These pins should be properly decoupled using 0.01 µF or 0.1 µF capacitors.
V_{SS}	A1, D4, D8, D13, D17, H4, H17, J9, J10, J11, J12, K9, K10, K11, K12, L9, L10, L11, L12, M9, M10, M11, M12, N4, N17, U4, U8, U13, U17	**Ground.**
V_{DDA}	W14	**Clock Oscillator Power.** 3.3 V. This pin should be properly decoupled using 0.01 µF or 0.1 µF capacitors.

2 Pinout (continued)

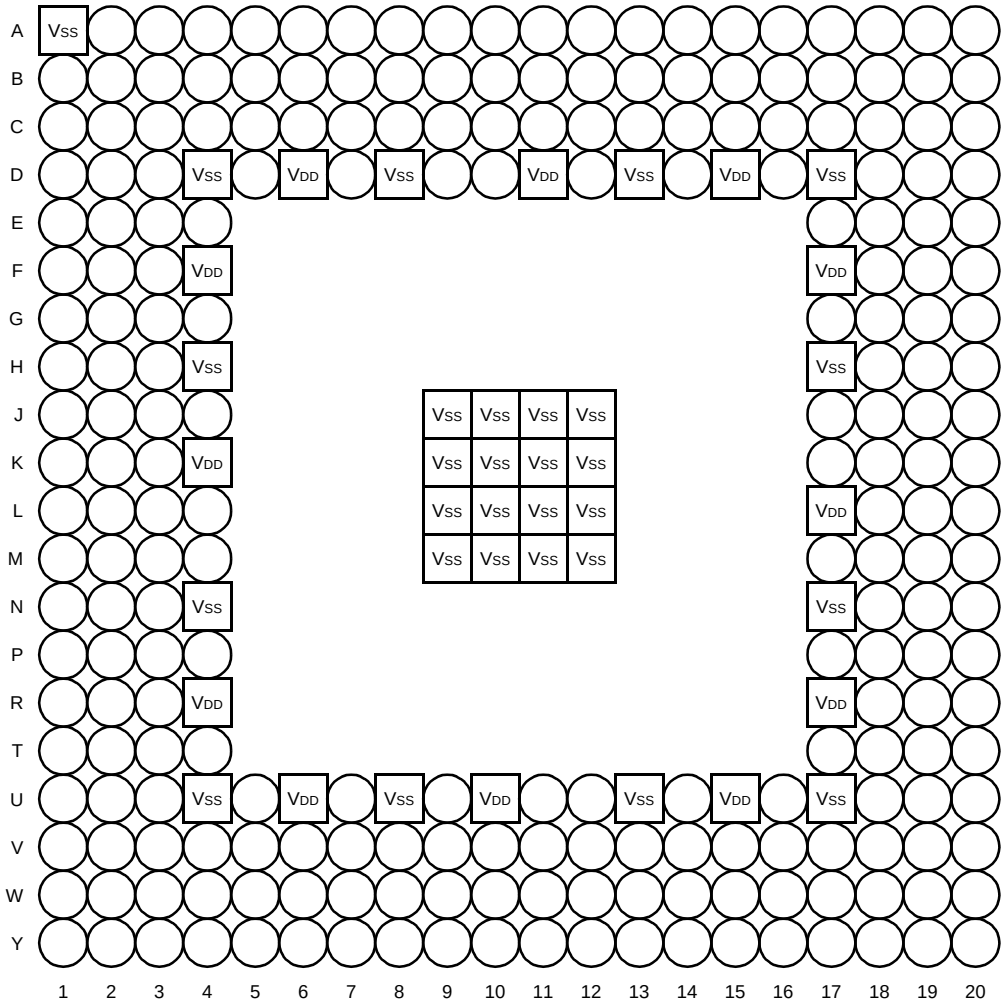

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Figure 3. 272-Pin PBGA—Top View

3 Powerup/Reset Sequence

One of the following two methods may be used to reset the T8208:

1. Assert the reset* pin low for at least 5 pclk periods or 100 ns, whichever is longer, and then return it high for a hardware reset. For a powerup reset, the reset* pin should be held low for at least 5 pclk periods or 100 ns, whichever is longer, after the power supply ramps to its operating voltage and the crystal oscillator is stable.
2. Write both the srst* and srst_reg* bits in the direct configuration/control register (address 28h) to ‘0,’ and leave them at that value for at least 1 µs to perform a software reset.

The device is now in the reset state, and the following start-up procedure must be executed to ensure proper operation:

1. After pclk (xtalin) is provided to the T8208, and the device is in the reset state:
   A. Write the mclk PLL configuration 0 and 1 registers at addresses 2Ah and 2Bh.
   B. Continue after the PLL has stabilized in 100 µs.
2. Set the srst_reg* bit (to take the main registers out of reset), and program the cyc_per_acc and big_end bits in the direct configuration/control register (address 28h).
3. Wait 1 µs for the circuit to stabilize.

Extended memory accesses may now be performed only to the main register group.

4. Write the desired values to the main configuration 1 register (address 0100h), the TX UTOPIA clock configuration register (address 010Ch), and the RX UTOPIA clock configuration register (address 010Eh) in the extended memory registers. These bits should not be modified at a later time without returning to the reset state.
5. Program the main configuration 2 register (address 0112h) and the UTOPIA configuration register (address 0114h). These registers should not be modified at a later time without returning to the reset state.
6. Program the cb_arb_sel and cb_usr_mode bits in the cell bus configuration/status register (address 0130h).
7. Wait one clock period of the slowest clock (cell bus, UTOPIA, or pclk) for the circuit to stabilize.
8. Set the srst* bit in the direct configuration/control register (address 28h).
9. Wait three clock periods of the slowest clock (cell bus, UTOPIA, or pclk) for the circuit to stabilize.

The T8208 device is now out of reset state.

10. Initialize the SDRAM per the SDRAM specifications.
11. Enable the SDRAM by setting the sdram_en bit in the SDRAM control register (address 0400h).
12. Initialize the LUT to benign values (recommended).
13. Initialize the multicast memory to all ’0’ (recommended).
14. Program the four routing information registers (addresses 0200h through 0204h and 0214h) and the seven PPD information registers (addresses 0206h through 0212h).

4 Hot Insertion

When a connector with proper pin sequencing is used, the Agere Systems Inc. GTL+ buffers withstand hot insertion into a backplane without corrupting the cell bus or damaging the device. The ground pins on the connector should extend beyond all other pins so that the ground connections are made first. In addition, the power pins on the connector should extend beyond the signal pins so that the power connections are made before the signal but after the ground connections.

During hot insertion, the cell bus is not corrupted because the GTL+ outputs go to a high-impedance state during the powerup reset. Therefore, proper timing should be met in the external powerup reset circuit.

5 PLL Configuration

The frequency of the device's main clock (mclk) is derived from the clock at the xtalin input (pclk) and is given by the following equation when the PLL is engaged:

$$f_{mclk} = f_{pclk} \times \frac{(M + 2)}{(2 \times (MOD8(N + 1) + 1))}$$

Note: When the PLL is engaged, mclk is the output of the PLL.

M and N are the pll_m[4:0] and pll_n[2:0] counter values in the mclk PLL configuration 1 register (address 2Bh) and must be set so that the voltage-controlled oscillator (VCO) operates in the appropriate range. The maximum value for f_{mclk} is 100 MHz. The valid range for M is between 2 and 22 inclusive, and the valid range for N is between 0 and 7 inclusive. When multiple sets of values can achieve the desired result, choose the lowest value of M and the corresponding value for N.

Note: The output of the PLL must always be at least 50 MHz.

The loop filter must be set properly for correct operation of the PLL. The proper setting of the loop filter bits, lf[3:0], in the mclk PLL configuration 0 register (address 2Ah) is determined by the chosen value for M. The following table lists the lf[3:0] settings for given values of M. Typical PLL lock-in time is 50 µs.

Table 10. Loop Filter Register Settings

M	Mclk PLL Configuration 0 (2Ah) lf[3:0]
22	"0111"
16—21	"0110"
10—15	"0101"
6—9	"0100"
4—5	"0011"
2—3	"0010"

PLL Configuration Example:

Given a pclk frequency of 50 MHz and a desired mclk frequency of 100 MHz, the proper values of M, N, and lf[3:0] are the following:

M = 2

N = 7

lf[3:0] = "0010"

The bypass PLL (bypb) and PLL enable (pllen) bits are used to select the source of mclk for the T8208. To select the output of the PLL as the clock, both bits must be programmed to '1,' and to select pclk as the clock, both bits must be programmed to '0.'

6 Microprocessor Interface

6.1 Microprocessor Interface Configuration

The microprocessor interface may be configured for either *Intel* or *Motorola* mode via the mot_sel input. Tie mot_sel high to select *Motorola* mode and low to select *Intel* mode. In addition, the address and data buses may be configured for multiplexed or nonmultiplexed mode using the mux input. To select multiplexed mode, tie mux high, and to select nonmultiplexed mode, tie mux low. In multiplexed mode, d[7:0] are used for both the address and the data bus, and the a[0] input becomes an address latch enable (ale) signal. In nonmultiplexed mode, separate address, a[7:0], and data, d[7:0], buses are used. In both modes, the active-low sel* input selects the device for microprocessor read or write accesses. The data leads are 3-stated when the sel*, wr*_ds*, or rd*_wr* signal is high.

In *Motorola* mode, rd*_rw* is a read/write enable signal, which indicates the current access is a read when it is high and a write when low. The wr*_ds* signal is data strobe in *Motorola* mode. The rdy_dtack* output is an active-low data transfer acknowledge signal. The T8208 takes this signal low when the microprocessor access is complete. The rdy_dtack* output returns high when the microprocessor acknowledges the access by taking the sel* or wr*_ds* signal high. The rdy_dtack* output then goes high-impedance.

In *Intel* mode, the rd*_rw* input is an active-low read enable signal, and wr*_ds* is an active-low write enable signal. A logic low level on rd*_rw* indicates to the T8208 that the current access is a read, and a logic low level on wr*_ds* indicates the access is a write. Finally, the rdy_dtack* output is an active-high ready signal. The T8208 asserts this signal high when a microprocessor access is complete. The rdy_dtack* output then goes high-impedance when the sel*, wr*_ds*, or rd*_wr* signal goes high.

6.2 Microprocessor Interrupts

The int_irq* output is an active-high interrupt in *Intel* mode and an active-low interrupt request in *Motorola* mode. In *Intel* mode, int_irq* is normally low and goes high when an interrupt is generated. In *Motorola* mode, the interrupt request signal is normally high and goes low during an interrupt. Interrupts are generated when an enabled interrupt status bit becomes set. All interrupt status bits in the T8208 have a corresponding interrupt enable bit. When the enable bit is cleared, the corresponding interrupt status bit is not enabled and will not generate an interrupt. Several registers containing interrupt status bits exist in the four separate extended memory register groups (main, UTOPIA, SDRAM, and bypass SDRAM) of the T8208. The interrupt service request register at direct address 29h indicates which register group is generating the interrupt. Only enabled interrupts will cause the int_serv_mainreg, int_serv_sdramreg, and int_serv_utopiareg bits to become set. For the main register group, a special case exists. The ctrl_cell_sent and the ctrl_cell_av interrupts (in the main interrupt status 1 register) do not cause the main group indication bit to be set in the interrupt service request register. These interrupts have their own dedicated service request bits to optimize sending and receiving control cells. The ctrl_cell_sent and ctrl_cell_av bits may become set whether the corresponding interrupt is enabled or not.

6.3 Accessing the *CelXpres* T8208 via Microprocessor Interface

The *CelXpres* T8208 has two distinct memory spaces: the direct memory access registers and the extended memory registers. The direct memory access registers are directly addressed 8-bit (byte) registers and are mapped between addresses 00h and FFh. The extended memory registers are indirectly addressed and mapped between addresses 0100h and 3FFFFFEh. The extended memory contains the SDRAM memory, the translation RAM, internal memories, and the device's configuration, status, and control registers. Extended memory registers are 16 bits wide, and all accesses to the extended memory registers are executed internally as 16 bits. Direct memory access registers are located in Section 14.2, Direct Memory Access Registers, and extended memory registers are located in Section 14.3, Extended Memory Registers.

6 Microprocessor Interface (continued)

6.3.1 Accessing the Extended Memory Registers

Before accessing the extended memory registers, the powerup sequence, as described in Section 3, Powerup/ Reset Sequence, must be completed. Accesses to extended memory are word accesses internally; therefore, the least significant bit of the address is always ‘0.’ Only the most significant 25 bits are supplied to the extended memory address registers (addresses 30h—34h). The following procedure outlines the steps needed for extended memory accesses in the T8208 device.

6.3.1.1 Extended Memory Writes

1. Write ext_a [25] bit to the extended memory address 4 register (little endian or big endian) (optional).
2. Write ext_a [24:17] byte to the extended memory address register 3 (little endian or big endian) (optional).
3. Write ext_a [16:9] byte to the extended memory address register 2 (little endian or big endian) (optional).
4. Write ext_a [8:6] bits to the extended memory address register 1 (little endian or big endian) (optional).
5. Write ext_d [15:8] byte to the extended memory data high register (little endian or big endian) (optional).
6. Write ext_d [7:0] byte to the extended memory data low register (little endian or big endian) (optional).
7. Write ext_a [5:1] bits; write “01,” “10,” or “11” to ext_we[1:0]; and write ‘1’ to ext_strt_acc in the extended memory access register (little endian or big endian) (mandatory).
8. Read the extended memory access register (little endian or big endian) to determine that the ext_strt_acc bit has been cleared by hardware (mandatory).

6.3.1.2 Extended Memory Reads

1. Write ext_a [25] bit to the extended memory address 4 register (little endian or big endian) (optional).
2. Write ext_a [24:17] byte to the extended memory address register 3 (little endian or big endian) (optional).
3. Write ext_a [16:9] byte to the extended memory address register 2 (little endian or big endian) (optional).
4. Write ext_a [8:6] bits to the extended memory address register 1 (little endian or big endian) (optional).
5. Write ext_a [5:1] bits; write “00” to ext_we[1:0]; and write ‘1’ to ext_strt_acc in the extended memory access register (little endian or big endian) (mandatory).
6. Read the extended memory access register (little endian or big endian) to determine that the ext_strt_acc bit has been cleared by hardware (mandatory).
7. Read ext_d [15:8] byte from the extended memory data high register (little endian or big endian) (optional).
8. Read ext_d [7:0] byte from the extended memory data low register (little endian or big endian) (optional).

Note: Once the ext_strt_acc bit is set by software, only the extended memory access register should be accessed until the ext_strt_acc bit is cleared by hardware.

6 Microprocessor Interface (continued)

6.3.2 *CelXpres* T8208 Access Performance

The times represented in the following table reflect access times for various microprocessor interface reads and writes. For direct access registers, the values represent the time until the rdy_dtack signal transitions indicating the data transfer portion of the access is complete. For accesses to extended memory, the values represent the time from the completion of a write to register 34h until the ext_strt_acc bit is cleared.

The actual times are dependent on the frequency of the pclk and mclk clocks (see Section 5, PLL Configuration). The terms pclkp and mclkp in the table represent the period of pclk and mclk, respectively, in ns.

Table 11. Access Times

Description	Min	Typ	Max	Unit
Read/Write to 28h—3Dh	4 x pclkp	5 x pclkp	5 x pclkp + 30	ns
Reads to: 60h—93h, A0h—D7h, E0h—FFh (direct internal memory)	6 x pclkp + 3 x mclkp	8 x pclkp + 9 x mclkp	12 x pclkp + 15 x mclkp	ns
Writes to: 60h—93h, A0h—D7h, E0h—FFh (direct internal memory)	6 x pclkp	8 x pclkp + 4 x mclkp	10 x pclkp + 9 x mclkp	ns
Reads to Extended Memory Internal Structures	6 x pclkp + 6 x mclkp	8 x pclkp + 12 x mclkp	12 x pclkp + 18 x mclkp	ns
Writes to Extended Memory Internal Structures	6 x pclkp	8 x pclkp + 7 x mclkp	10 x pclkp + 12 x mclkp	ns
Read from LUT SRAM	4 x pclkp + 11 x mclkp	—	10 x pclkp + 50 x mclkp	ns
Write to LUT SRAM	4 x pclkp	—	10 x pclkp + 50 x mclkp	ns

7 General-Purpose I/O (GPIO)

The T8208 has eight programmable general-purpose I/O pins called GPIO. These GPIO pins may be independently programmed, via the GPIO_oe[7:0] bits in the GPIO output enable register (address 39h), to be inputs or outputs. If a GPIO_oe bit is set to ‘1,’ the corresponding GPIO pin is an output, or if cleared to ‘0,’ the corresponding GPIO pin is an input. Input values are read from the GPIO_in[7:0] bits in the GPIO input value register (address 3Dh), and output values are written to the GPIO_out[7:0] bits in the GPIO output value register (address 3Bh). The GPIO[7:0] pins all have internal 50 kΩ pull-up resistors.

8 Look-Up Table

Cells arriving from the UTOPIA bus obtain information from the external static RAM look-up table (LUT), which is divided among VPI, VCI, and OAM/RM records. Each of these records contains specific VPI or VPI/VCI translation and cell bus routing information. The size of the records is programmable to 8 bytes or an extended 16 bytes. The 16-byte mode adds two 32-bit counters to each record. The 16-byte mode is discussed in Section 8.4, Extended Records.

The VPI value in the header, in addition to the PHY port number, of the incoming cell points to a VPI record in the look-up table. This VPI record is examined first. If the VPI record indicates OAM F4 routing, the OAM record, to which the VPI record points, provides the OAM routing and VPI/VCI translation information. If OAM F4 routing is not indicated, information about the type of translation, VPI only or VPI/VCI, is obtained from the original VPI record. For VPI only translation, routing information is obtained from the VPI record, and full or partial VPI translation is performed.

For VPI/VCI translation, the VPI record points to the appropriate VCI record, where VPI/VCI translation and routing information is stored. If the VCI record indicates OAM F5 routing, the OAM record, to which the VCI record points, provides the OAM routing and VPI/VCI translation information. If no OAM F5 routing is indicated, VPI/VCI translation and cell routing are performed using the information in the VCI record.

8.1 Look-Up Table RAM

The number of memory devices (up to two) used for the look-up table and the size of the external SRAM are programmable. The tram_qnty_sel bit in the main configuration 1 register (address 0100h) specifies whether one or two RAM chips are used. If two memory devices are used, separate chip select signals are generated. These chip selects are created from the decoded RAM addresses. The tram_size configuration bits, also in the main configuration 1 register, are used to select memory sizes of 32 Kbytes, 64 Kbytes, 128 Kbytes, or 256 Kbytes. Therefore, the maximum look-up table size of 512 Kbytes is realized when two RAM chips of 256 Kbytes each are used.

If a single SRAM of 512 Kbytes is used (instead of two SRAMs of 256 Kbytes each), then bit 5 in the main configuration 1 register must be set to ‘1.’ If a single SRAM of 512 Kbytes is not used, this bit must be cleared to ‘0.’

8 Look-Up Table (continued)

8.2 Organization

Organization is discussed in terms of 8-byte records. Differences in organization for 8-byte records and 16-byte records will be discussed in Section 8.4, Extended Records. The look-up table may be configured to support up to 64 ports when multi-PHY mode is used, effectively creating a separate look-up table for each port.

All VPI, VCI, and OAM/RM records may be either 8 bytes or 16 bytes in length. (See Section 8.4, Extended Records for information on 16-byte records.) Figure 4 shows the translation RAM memory map for 8-byte records. OAM/RM translation records are located at the bottom of the memory space with 64 OAM/RM records used by each port. If the device is configured to support 64 ports, the first 4096 records will be used for OAM and RM translation records. This translates to 32 Kbytes of memory for 8-byte records. The remaining memory is then used for VPI and VCI records. For 8-byte records, the base addresses of the OAM records are calculated from the following equation:

$OBA = PN \times 8 \times 64$

In this equation, OBA is the OAM base address, PN is the port number, 8 is the number of bytes per record, and 64 is the number of records per port. For example, the OAM/RM translation records for port 2 will have a base address of 1024 or 400h.

Note: If the device is configured to use less than 64 ports, the OAM/RM translation record memory space will be allocated enough memory to handle ports 0 through the maximum port number used. For example, if the device is configured to use ports 0, 2, 4, and 6 (see Section 9, UTOPIA Interface), the OAM/RM translation record memory space will use 448 records (for ports 0 through 6). OAM/RM translation record memory space for ports 1, 3, and 5 will be skipped even though the ports are not used.

Note: If the device is configured in PHY mode (see Section 9, UTOPIA Interface), the device supports only a single PHY and the translation RAM memory will be addressed as port 0.

Separate VPI record base addresses may be set up for each port in multi-PHY mode, and the number of incoming VPI bits used as a pointer into the look-up table may be programmed. (See Section 14.3, Extended Memory Registers, Table 153, PHY Port X Configuration Structure (PPXCF) (4200h to 42FEh).) For 8-byte records, the total memory used by the VPI records is calculated using the following equation:

$MS = NP \times 2^{NB} \times 8$

In this equation, MS is the memory size used for VPI records, NP is the number of ports used, 8 is the number of bytes per record, and NB is the number of incoming VPI bits used to address the look-up table.

This calculated memory space must be reserved for VPI records.

8 Look-Up Table (continued)

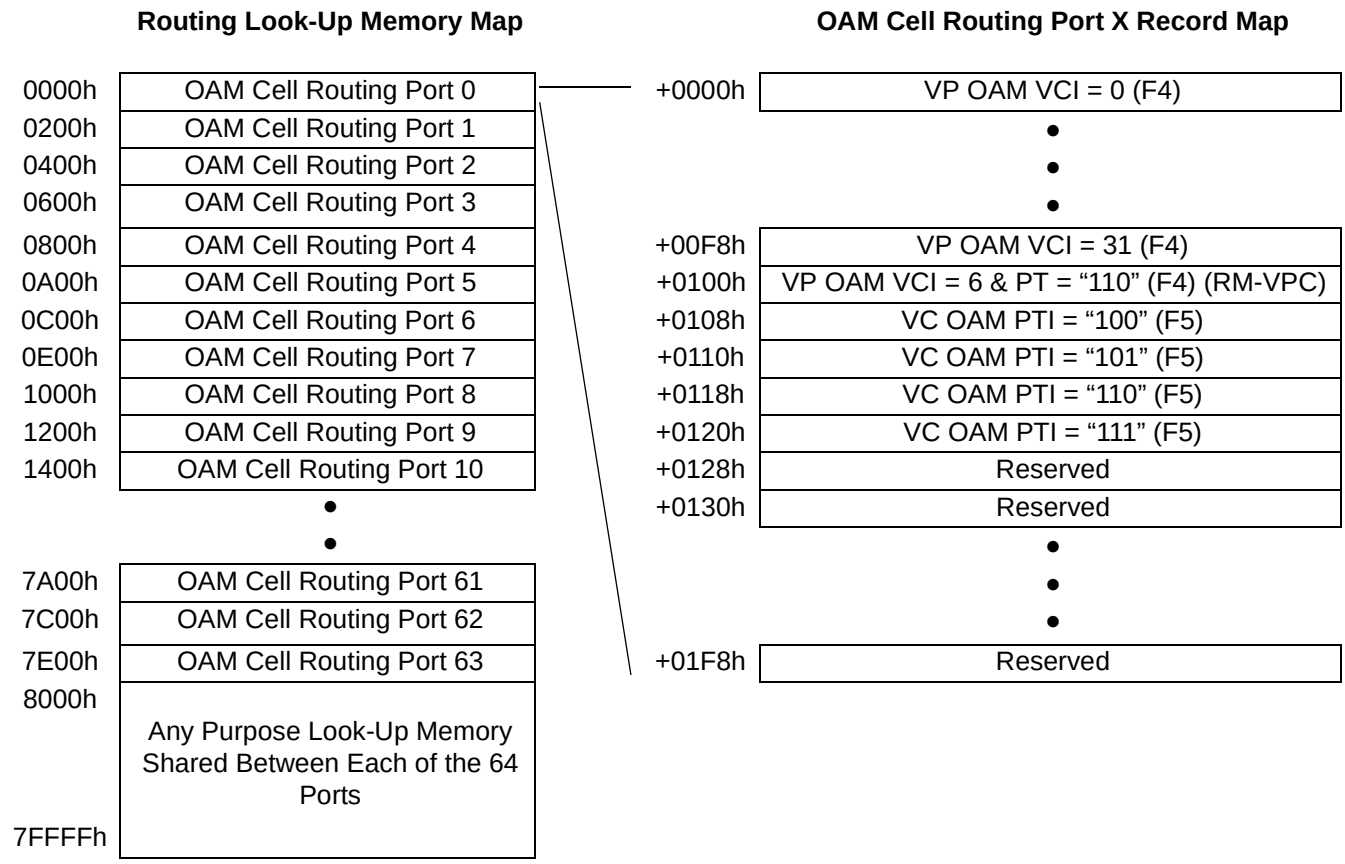


Figure 4. Translation RAM Memory Map—8-Byte Records

The four translation record types (VCI, OAM/RM, VPI only, and VPI for VPI/VCI) for 8-byte records are illustrated in Figure 5. There are two types of VPI translation records: one for VPI translation only and one for VPI/VCI translation. The VPI only translation record differs from other records in that it has the SH and SL bits which are used to indicate full or partial VPI translation. (See Table 13, the VPI Value Truth Table.) The other VPI record is used when VPI/VCI translation occurs. It has the VCI offset bits and max VCI value bits which are used to point to the VCI record where translation and routing information reside. The maximum VCI offset is 19 bits in length; therefore, only bits 3 through 18 are stored in the VPI record.

To address the appropriate VCI translation record, the VCI from the cell’s header is multiplied by 8 and added to bits 3 through 18 of the VCI offset which is obtained from the VPI record. This sum is the final offset into the look-up table. This final offset should then be added to the Translation RAM Memory beginning address 100000h (Table 180) to obtain the final address. The max VCI value indicates the maximum number of VCI translation records in the table. Therefore, if the VCI from the cell’s header is greater than the max VCI value, the cell’s VCI is out of range and is counted as a misrouted cell. Note that VPI records from different ports may reference the same VCI translation record. Other control bits in these records are described following Figure 5.

8 Look-Up Table (continued)

VPI Only Translation Record

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
+0	A	P	E	I	VPI[11:0]											
+2	SH	SL	Reserved													
+4	Cell Bus Routing Header[15:0]															
+6	Tandem Routing Header[15:0]															

VPI for VPI/VCI Translation Record

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
+0	A	P	E	I	Reserved											
+2	Bits 3 Through 18 of VCI Offset[15:0]															
+4	Max VCI Value[15:0]															
+6	Reserved															

VCI Translation Record

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
+0	A	—	E	I	VPI[11:0]											
+2	VCI[15:0]															
+4	Cell Bus Routing Header[15:0]															
+6	Tandem Routing Header[15:0]															

OAM/RM Translation Record

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
+0	A	C1	C0	I	VPI[11:0]											
+2	VCI[15:0]															
+4	Cell Bus Routing Header[15:0]															
+6	Tandem Routing Header[15:0]															

Figure 5. Translation Record Types—8-Byte Records

8 Look-Up Table (continued)

The routing control bits for VPI, VCI, and OAM/RM records are described below:

- Active (A). This bit is one when the VPI or VCI is considered active. See the truth table (Table 12) below. This bit is used in all types of records.
- Ignore (I). When this bit is one, the VPI or VCI is ignored. See the truth table (Table 12) below. This bit is used in all types of records.

  If masking the I bit is required (when the I bit is set to '1'), then the mask_ignore bit (bit 13 in register 0112h) can be used to achieve this masking.

  When this bit is set to 1, the T8208 ignores the ignore bit that was programmed in the look-up records that control the translation of the incoming UTOPIA cells. This can be used for redundancy if desired. For redundancy, the software can populate the look-up tables of two T8208 devices (one active and one inactive for redundancy). The ignore (I) bit needs to be set in both the active and inactive devices. The active device has the mask_ignore bit = 1 and the inactive device has the mask_ignore bit = 0. This way the inactive device will not count, route or translate the incoming cells (ignores them). When the active device fails, its mask_ignore bit becomes 0 and the inactive device becomes active by setting its mask_ignore bit = 1. The failed device now will no longer try to count, route, or translate incoming cells, and the new active device takes over cell routing and VPI/VCI translation.

Table 12. Active and Ignore Truth Table

A	I	Action
0	0	The cell is discarded, considered misrouted, and counted as a received cell.
0	1	The cell is discarded, is not flagged as misrouted, and is not counted as a received cell.
1	0	The cell is valid and is counted as a received cell.
1	1	The cell is discarded, is not flagged as misrouted, and is not counted as a received cell.

8 Look-Up Table (continued)

- Enable OAM/RM Routing (E). When this bit is '1' in the VPI record and the VCI is less than 32, the routing and translation information is obtained from the appropriate OAM/RM F4 record. If this bit is '1' in the VCI record and the most significant bit of the PTI in the cell header is '1,' the routing and translation information is obtained from the appropriate OAM/RM F5 record. This bit is used only in VPI and VCI records.
- VPI Translation (P). When this bit is '1,' translation is on the VPI only. When this bit is '0,' VPI/VCI translation is performed. This bit is used only in VPI records.
- VPI Value High (SH). When this bit is '1,' bits 8 through 11 of the incoming VPI are replaced with the corresponding bits in the VPI record. See the truth table (Table 13) below. This bit is used in VPI only translation records.
- VPI Value Low (SL). When this bit is '1,' bits 0 through 7 of the incoming VPI are replaced with the corresponding bits in the VPI record. See the truth table (Table 13) below. This bit is used in VPI only translation records.

Table 13. VPI Value Truth Table

SH	SL	Action
0	0	No VPI translation is performed.
0	1	VPI translation is performed only on bits 0—7 of the incoming VPI.
1	0	VPI translation is performed only on bits 8—11 of the incoming VPI.
1	1	Complete VPI translation is performed.

- OAM Routing Control (C1, C0). These 2 bits determine if the cell is routed as OAM/RM and if VPI/VCI translation is performed. See the truth table (Table 14) below. These bits are used only in OAM/RM records.

Table 14. OAM Routing Control Truth Table

C1	C0	Action
0	0	Both incoming VPI and VCI are substituted with the VPI[1] and VCI, respectively, in the OAM/RM record, and the cell is routed according to the cell bus and tandem routing headers in the OAM/RM record.
0	1	The cell is not routed as OAM/RM. If the record is OAM/RM F5, the cell is translated and routed according to the cell bus and tandem routing headers in the original VCI record. If the record is OAM/RM F4, the cell is translated and routed according to the cell bus and tandem routing headers in the original VPI record.
1	0	The incoming VPI and VCI will be preserved, and the cell is routed according to the cell bus and tandem routing headers in the OAM/RM record.
1	1	Reserved.

1. The most significant 4 bits of the VPI will only be substituted if the global rplc_gfc bit in the direct configuration/control register (address 28h) is set in UNI mode or if the port is configured in NNI mode.

8 Look-Up Table (continued)

8.3 Look-Up Procedure

Look-up procedure is discussed in terms of 8-byte records. Differences in look-up procedures for 8-byte records and 16-byte records will be discussed in Section 8.4, Extended Records. When a cell is received, the set lutX_vpi_mask bits in the PHY port X configuration structure (Table 153) indicate which incoming VPI bits are used to address the VPI record in the look-up table. The selected incoming VPI bits are multiplied by eight (for 8-byte records) to create an offset into the table. The sum of this offset and the VPI base address, found in the PHY port X configuration structure, creates the actual look-up table address for the VPI record associated with the cell. Note that only bits 3 through 18 of the VPI base address are stored in the PHY port X configuration structure. If the lutX_vpi_chk bit is set, all unused VPI bits in the cell header must be '0,' or the cell will be considered out of range. If the port is configured as UNI, the upper four VPI bits (GFC field) will be ignored in the verification. When the cell is out of range, it is discarded and not counted as a received cell.

The validity of the accessed VPI record is determined by checking its active (A) and ignore (I) bits. If the cell is valid, the enable OAM/RM routing (E) bit is consulted to determine if F4 type OAM cell treatment should occur. (See the definition for these bits in Section 8.2, Organization.)

When the E bit is set and the incoming VCI is less than 32, the OAM record associated with the cell is read. To calculate the translation record address for the OAM/RM cell, the incoming VCI is multiplied by eight (for 8-byte records), and the resulting product is added to the port's OAM base address. (See Section 8.2, Organization.) A special case exists when the incoming VCI is six and the PTI in the cell header is "110." For this case, the OAM translation record address is the sum of the port's OAM base address and 100h.

Next, the validity of the F4 OAM record is determined by checking its A and I bits. If it is valid, the cell is routed as described by the OAM routing control (C1, C0) bits. (See the definition for these bits in Section 8.2, Organization.)

If the E bit in the VPI record is not one or if the C1 and C0 bits in the OAM record are zero and one, respectively, the cell does not receive OAM routing. If the cell is not routed OAM, the virtual path routing bit (P bit) in the original VPI is checked to determine if the cell receives VPI only or VPI/VCI routing. If the P bit indicates VPI only routing, the cell's VPI is replaced as indicated by the switch VPI high and low (SH, SL) bits in the VPI only translation record. (See the definition for these bits in Section 8.2, Organization.) The cell bus routing header and tandem routing header are then added to the cell, and the cell is transmitted on the cell bus.

If the P bit indicates VPI/VCI routing, the VCI translation record is accessed using the VCI offset and max VCI value bits in the VPI for VPI/VCI translation record. (The VCI offset and max VCI value bits are described in Section 8.2, Organization.) Again, the validity of the VCI translation record is determined by checking its A and I bits. Next, if the cell is valid, the E bit in the VCI record and the most significant bit of the PTI value in the cell header are examined to determine if F5 type OAM cell treatment should occur. The value of the incoming cell's PTI and port number determines the address in the OAM/RM record space. The following table outlines the look-up table offsets used for 8-byte records. The OAM translation record address is the sum of this offset and the port's OAM base address.

Table 15. F5 Translation Record Addresses Table—8-Byte Records

PTI	OAM Translation Offset
"100"	Port's OAM base address plus 108h
"101"	Port's OAM base address plus 110h
"110"	Port's OAM base address plus 118h
"111"	Port's OAM base address plus 120h

8 Look-Up Table (continued)

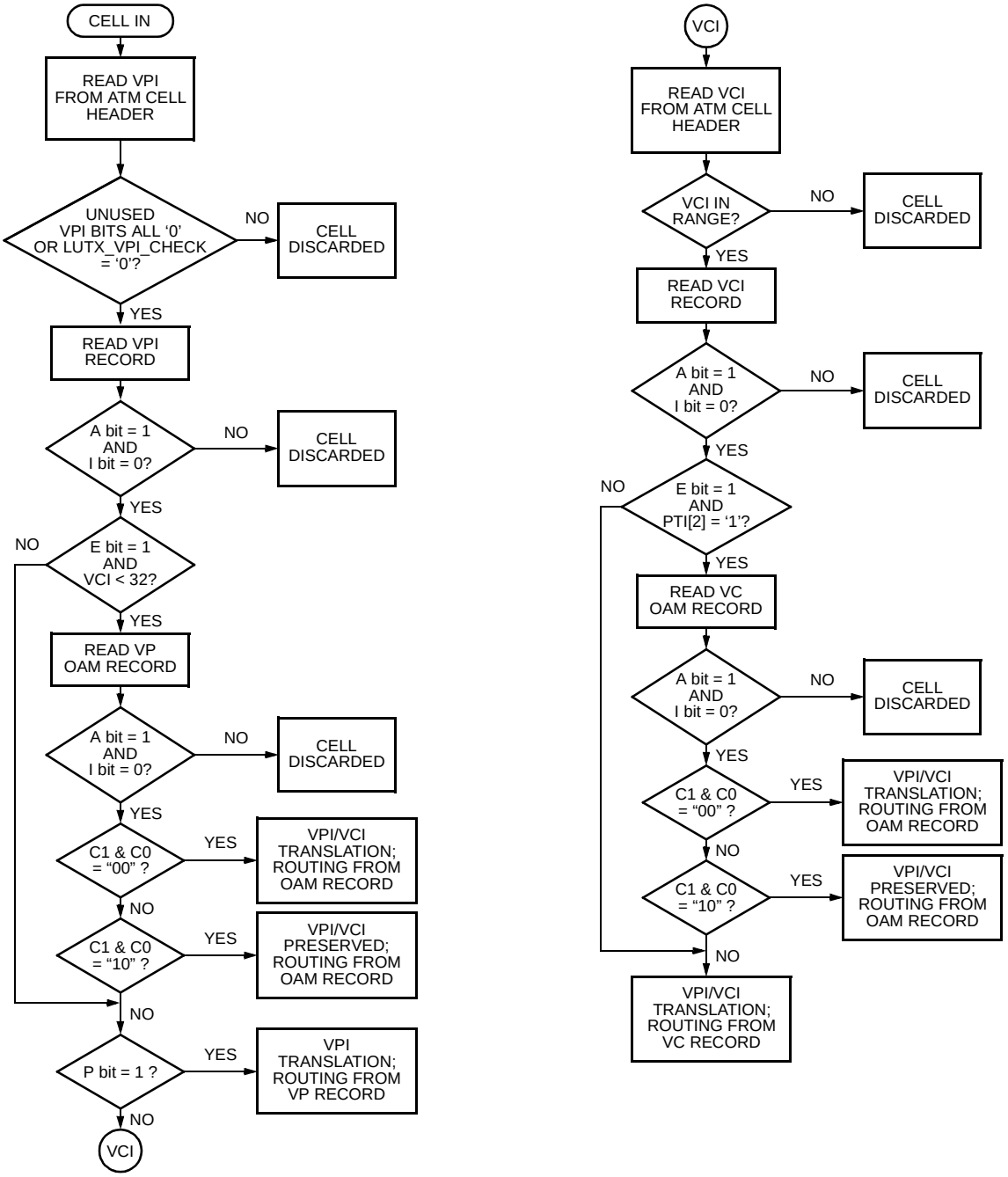
Next, the validity of the F5 OAM record is determined by checking its A and I bits. If it is valid, the cell is routed as described by the OAM routing control (C1, C0) bits. (See the definition for these bits in Section 8.2, Organization.)

If the E bit in the VCI record is not one or if the C1 and C0 bits in the OAM record are zero and one, respectively, the cell does not receive OAM routing. If the cell is not routed as an OAM cell, information in the VCI translation record is used to route the cell. The cell's VPI and VCI are replaced with the VPI and VCI, respectively, in the VCI record. The most significant 4 bits of the VPI will only be substituted if the global rplc_gfc bit in the direct configuration/control register (address 28h) is set or if the port is configured in NNI mode. The cell bus routing header and tandem routing header are then added to the cell, and the cell is transmitted on the cell bus.

Note: Unused OAM cell routing records in the LUT memory space can be used for other purposes.

8 Look-Up Table (continued)

This look-up procedure is outlined in the flow diagram below.



5-7781F and 5-7782F

Figure 6. Translation RAM Flow Diagram

8 Look-Up Table (continued)

8.4 Extended Records

The length of the translation records may be extended to 16 bytes to support two cell counts for each translation record. The lut_rec_form bits in the extended LUT configuration register (address 0138h) are used to select this extended mode. In extended (16-byte) mode, two 32-bit counters are appended to the 8-byte records.

The first counter in the translation record, total cell count, keeps a total count of all incoming cells received from the UTOPIA bus whether ultimately routed or discarded except those in which the VPI is out of range. See the definition of the A and I bits in Section 8.2, Organization.

The second counter, special cell count, is a subset of the total cell count counter. This counter counts only cells whose PTI and CLP values in the cell header match the values specified in the extended LUT control register (address 0120h). For example, this counter may be used to track specific F5 type OAM/RM cells and cells indicating forward congestion (EFCI = 1) or lower priority (CLP = 1).

8 Look-Up Table (continued)

The four translation record types for extended mode are illustrated in Figure 7 below.

Extended VPI Only Translation Record

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
+0	A	P	E	I	VPI[11:0]											
+2	SH	SL	Reserved													
+4	Cell Bus Routing Header[15:0]															
+6	Tandem Routing Header[15:0]															
+8	Total Cell Count[31:16]															
+A	Total Cell Count[15:0]															
+C	Special Cell Count[31:16]															
+E	Special Cell Count[15:0]															

Extended VPI for VPI/VCI Translation Record

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
+0	A	P	E	I	Reserved											
+2	Bits 3 Through 18 of VCI Offset[15:0]															
+4	Max VCI Value[15:0]															
+6	Reserved															
+8	Reserved															
+A	Reserved															
+C	Reserved															
+E	Reserved															

Extended VCI Translation Record

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
+0	A	—	E	I	VPI[11:0]											
+2	VCI[15:0]															
+4	Cell Bus Routing Header[15:0]															
+6	Tandem Routing Header[15:0]															
+8	Total Cell Count[31:16]															
+A	Total Cell Count[15:0]															
+C	Special Cell Count[31:16]															
+E	Special Cell Count[15:0]															

Extended OAM/RM Translation Record

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
+0	A	C1	C0	I	VPI[11:0]											
+2	VCI[15:0]															
+4	Cell Bus Routing Header[15:0]															
+6	Tandem Routing Header[15:0]															
+8	Total Cell Count[31:16]															
+A	Total Cell Count[15:0]															
+C	Special Cell Count[31:16]															
+E	Special Cell Count[15:0]															

Figure 7. Translation Record Types—Extended Mode

8 Look-Up Table (continued)

Because the translation records are larger in extended mode, the look-up table memory map changes, the translation record address calculations change, and the memory size calculations change. Figure 8 shows the new translation RAM memory map for 16-byte records when the device is configured for 64 PHY ports.

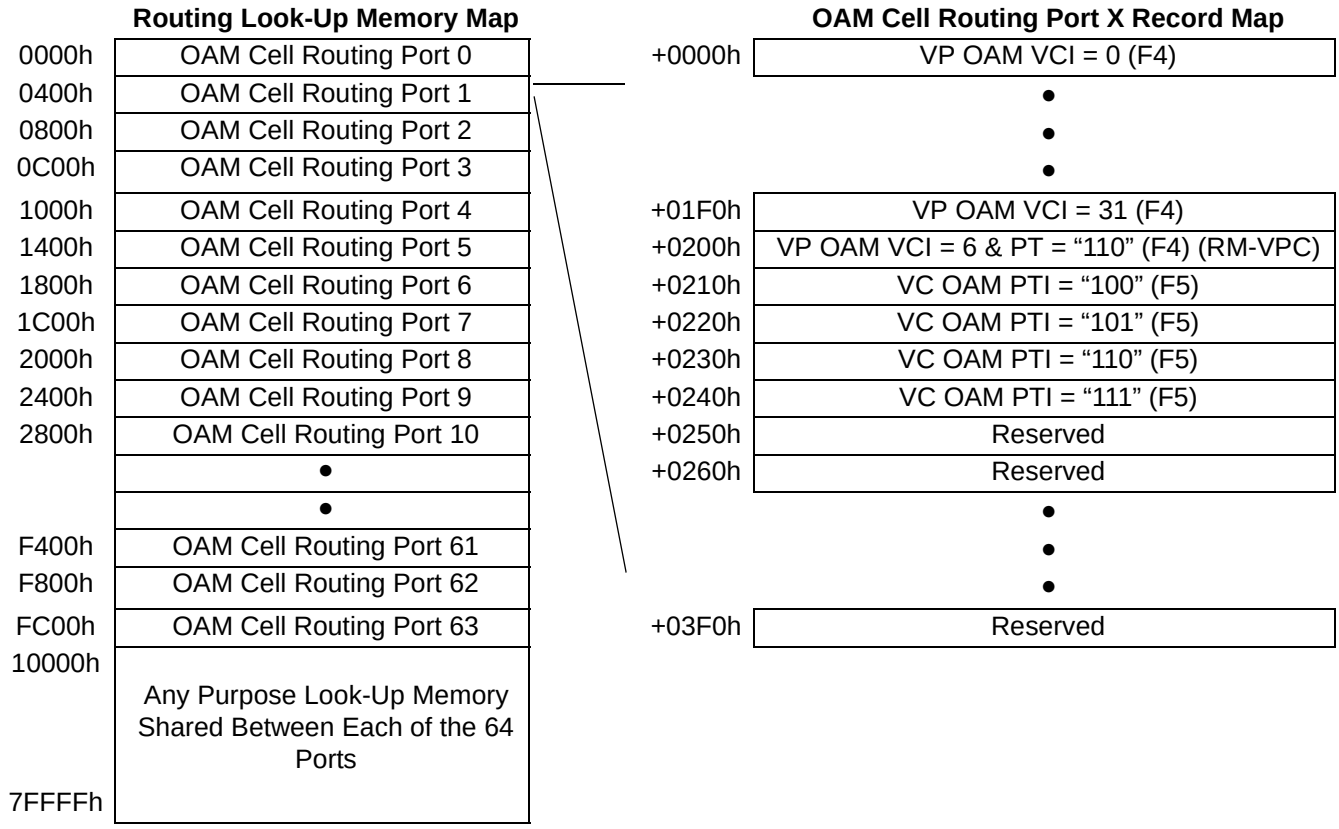


Figure 8. Translation RAM Memory Map—Extended Mode

8 Look-Up Table (continued)

The OAM/RM translation records at the bottom of the memory map now use 64 Kbytes of memory when the device is configured to support 64 MPHY ports, and the base addresses for the OAM records are now calculated using the following equation:

$OBA = PN \times 16 \times 64$

In this equation, OBA is the OAM base address, PN is the port number, 16 is the number of bytes per record, and 64 is the number of records per port.

To calculate the 16-byte translation record address for the F4 type OAM cell, the incoming VCI is multiplied by 16, and the resulting product is added to the port's OAM base address. For the special case when the incoming VCI is six and the PTI in the cell header is "110," the OAM translation record address is the sum of the port's OAM base address and 200h.

The 16-byte OAM type F5 translation record offset is determined from the incoming cell's PTI using the following table. The OAM translation record address is the sum of this offset and the port's OAM base address.

Table 16. F5 Translation Record Addresses Table—Extended Mode

PTI	OAM Translation Offset
"100"	Port's OAM base address plus 210h
"101"	Port's OAM base address plus 220h
"110"	Port's OAM base address plus 230h
"111"	Port's OAM base address plus 240h

In extended mode, the memory space used by the VPI records also changes. The total memory now used by the VPI records is calculated using the following equation:

$MS = NP \times 2^{NB} \times 16$

In this equation, MS is the memory size used for VPI records, NP is the number of ports used, 16 is the number of bytes per record, and NB is the number of incoming VPI bits used to address the look-up table.

To address the 16-byte VPI translation record, the selected incoming VPI bits (see Section 8.3, Look-Up Procedure) are multiplied by 16 to create an offset into the look-up table. The sum of this offset and the VPI base address creates the actual VPI translation record address associated with the incoming cell. Note that only bits 3 through 18 of the VPI base address are stored in the PHY port X configuration structure.

To address the 16-byte VCI translation record, the VCI from the cell's header is multiplied by 16 and added to bits 3 through 18 of the VCI offset, which is obtained from the VPI record. This sum is the final offset into the look-up table. This final offset should then be added to the translation RAM memory beginning address 100000h (Table 180) to obtain the final address.

8 Look-Up Table (continued)

8.5 Diagnostics

The T8208 also includes diagnostics to track misrouted cells. A cell is considered misrouted if its A and I bits are “00,” if its VCI is out of range, or if the lutX_vpi_chk bit is ‘1’ and the unused VPI bits in the incoming cell header are not all zero (see Section 8.3, Look-Up Procedure). When a misrouted cell is detected, the misrouted cell header high and low registers (addresses 0146h and 0148h) may be updated. If enabled, the mis_cell interrupt, the vci_or interrupt, or the vpi_or interrupt will be generated as appropriate (see Table 96 in Section 14.3, Extended Memory Registers).

The misrouted cell header high and low registers contain the first four header bytes of selected misrouted cells. Only a misrouted cell from a port whose mis_cell_lut_sel bit is set will update these registers, and this misrouted cell will update the registers only if it is the first received after the mis_cell_clr bit is set. The lst_mis_cell_lut bits indicate the port from which the header bytes in the misrouted cell header high and low registers were received. The mis_cell_lut_sel bits are located in the misrouted LUT 0, 1, 2, and 3 registers (addresses 0142h, 0140h, 013Eh, and 013Ch respectively). The mis_cell_clr, mis_cell_latch, and lst_mis_cell_lut bits are located in the misrouted LUT 4 register (address 0144h). (See Tables 77, 78, 79, 80, and 81 in Section 14.3, Extended Memory Registers, for a complete description of the above bits.)

8.6 Setup

When configuring the lut_en bits in the LUT X configuration/status register (addresses 0320h through 039Eh), care must be taken to ensure that the enabled ports’ LUTs correspond to the ports chosen in UTOPIA mode. (See Section 9.6, UTOPIA Pin Modes.) If a LUT is not enabled, corresponding bits in the PHY port X configuration structure (Section 14.3.2.4, RX UTOPIA Configuration Monitoring, Table 153) will be ignored. Also, when the device is configured for UTOPIA PHY mode (see Section 9, UTOPIA Interface), only port 0 entries in the external RAM look-up table are used; therefore, the look-up table should be set up accordingly.

8.7 LUT Bypass

This feature allows the elimination of the SRAM (which has the LUT information) in implementations that can provide the cell bus routing header (CBRH) and the tandem routing header (TRH) to the T8208 device. This feature is enabled when bit 6 in register 0100h is set to ‘1.’ When this LUT bypass feature is enabled, the T8208 is expecting 58-byte cells in 16-bit UTOPIA mode and 57-byte cells in 8-bit UTOPIA mode on Rx UTOPIA.

If bit 7 in register 0100h is cleared to ‘0,’ then the T8208 device expects to see the TRH before the CBRH on the incoming cells. But, if bit 7 in register 0100h is set to ‘1,’ the T8208 device expects to see the CBRH before the TRH on the incoming cells.

9 UTOPIA Interface

The *CelXpres* T8208 supports the ATM Forum's UTOPIA level 1 and level 2 specifications for cell-level handshake and MPHY operation with rates up to 635 Mbits/s. The device may be configured as an ATM layer or as a PHY layer by programming the phyen* bit in the main configuration 1 register (address 0100h).

The device may be configured for 16 data bit operation by setting utopia_16 bit (bit 7) in register 0112h. If the utopia-16 bit (bit 7) in register 0112h is cleared to '0,' then the TX and RX UTOPIA interfaces of the T8208 are configured for 8 data bit operation.

In UTOPIA 2, 16 bit data mode, a maximum of 32 MPHYs (64 queues) are supported. In UTOPIA 2, 8-bit data mode, a maximum of 64 MPHYs (128 queues) are supported.

As an ATM layer, the device may interface with a single PHY layer or multiple PHY layers (up to 64). Also as an ATM layer, it may be configured for shared UTOPIA mode for 64 (8-bit data mode) or 32 (16-bit data mode) MPHYs. (Note that if shared UTOPIA mode is not used, the slave_en bit in the main configuration/control register (address 0110h) must be cleared at device setup.)

In PHY mode, the T8208 functions as a single PHY device on the UTOPIA bus or as one of 31 PHY devices on the UTOPIA level 2 bus.

In addition to the required UTOPIA signals, the T8208 supports an additional three transmit and three receive enable (u_txenb*[3:1] and u_rxenb*[3:1]) signals, an additional three transmit and three receive cell available (u_txclav[3:1] and u_rxclav[3:1]) signals, a transmit parity (u_txprty) signal, and a receive parity (u_rxprty) signal.

The T8208 UTOPIA signal names begin with u_tx, for UTOPIA transmit, or u_rx, for UTOPIA receive. References to transmit or receive are made relative to the UTOPIA data flow for the ATM layer UTOPIA interface. Therefore, signals starting with u_rx, such as u_rxenb*[3:0] and u_rxdata[15:0], are receive UTOPIA signals for devices in ATM mode but are transmit UTOPIA signals for devices in PHY mode. Furthermore, signals such as u_txclav[3:0] and u_txaddr[4:0] are transmit UTOPIA signals for devices in ATM mode but are receive UTOPIA signals for devices in PHY mode. The above ATM to PHY terminology will be used throughout this UTOPIA Interface section.

9 UTOPIA Interface (continued)

9.1 Incoming UTOPIA Cell Interface

9.1.1 Incoming PHY Mode (Cells Received by T8208)

In PHY mode, only one enable (u_rxenb*[0]) signal and one cell available (u_rxclav[0]) signal are used. The u_rxenb*[0] signal is an input connected to the ATM layer's TxEnb* signal, and the u_rxclav[0] signal is an output connected to the ATM layer's TxClav signal. As a PHY device, the T8208 uses only the LUT 0 configuration/status register (address 0320h) and PHY port 0 configuration structure register (addresses 4200h—4202h). For UTOPIA level 2 functionality, the PHY address is programmed in the addr_match bits of the UTOPIA configuration register (address 0114h), and the addr_clav_en bits of the main configuration 2 register (address 0112h) can be programmed to any value mentioned in the register **except** "0000." As specified in the UTOPIA level 2 specification, during the polling process, the T8208 drives the u_rxclav[0] signal during the clock cycle following the cycle in which its address appears on the u_rxaddr pins. The u_rxclav[0] pin goes high impedance when not selected to support MPHY operation. In UTOPIA level 1, the above level 2 bits are not meaningful; therefore, the addr_clav_en bits must be programmed to "0000," the u_rxaddr pins must be grounded, and the addr_match bits cleared.

When the T8208 device is in PHY mode, if bit 5 (dont_inhibit_rxphy_clav) of register 0112h is cleared to '0,' the rx_clav signal is deasserted if the RX UTOPIA FIFO is considered full. If this bit is set to '1,' the T8208 keeps the rx_clav signal always asserted high indicating the capability to accept cells even if the RX UTOPIA FIFO could overrun, or is actually overrun.

9.1.2 Incoming ATM Mode (Cells Received by T8208)

In ATM mode, the T8208 may connect to PHY devices that either meet level 1 or level 2 UTOPIA specifications. If the connection is to devices that meet only UTOPIA level 1 specifications, the T8208 may access up to four of these PHY devices using the four enable (u_rxenb*[3:0]) and cell available (u_rxclav[3:0]) signals. Connection to more than one PHY device is possible only if the PHY's data, start of cell, and parity outputs go high impedance when the device is not enabled. Polling of the cell available signals usually occurs while the current cell is received.

If the T8208 connects to PHY devices meeting level 2 UTOPIA specifications, in 8-bit data mode, up to 64 MPHY ports may be accessed. In 8-bit UTOPIA 2 mode, 64 MPHYs are supported with four RxCLAV/RxENB pairs with 16-port addressing per RxCLAV/RxENB pair. For 32 PHY ports, two RxCLAV/RxENB pairs support two groups of 16 PHY ports for a total of 32 PHY ports. In 16-bit UTOPIA 2 mode, the T8208 supports 32 PHYs with four RxCLAV/RxENB pairs with 8-port addressing per RxCLAV/RxENB pair. In ATM MPHY mode, the u_rxdata[15:0], u_rxaddr[4:0], u_rxsoc, and u_rxprty signals are connected to each PHY port. In addition, the T8208 generates the address (u_rxaddr[4:0]) signals, permitting selection and arbitration among the MPHY ports. The number of address lines used in the connection may vary from one to four, giving a maximum address value of 15. (All five address lines must be connected to provide for the NULL address.) Refer to Section 9.6, UTOPIA Pin Modes, for more information about the possible combinations of address, cell available, and enable signals. The UTOPIA specification for operation with one TxClav and one RxClav is used when the T8208 connects to multiple level 2 PHY devices.

Whether the T8208 is connected to several level 1 or level 2 PHY devices, a round robin algorithm is implemented that ensures that all PHY devices are serviced (accessed) in a timely manner. In addition, the number of clock cycles wasted for bus arbitration is minimized because polling is performed during cell transfer.

In ATM mode, all unused u_rxclav inputs require connection to ground.

Note: The u_rxenb outputs are high impedance during powerup and reset. An attached PHY may interpret this high-impedance state as an enable; however, the T8208 is not ready to properly handle input data during this time. Attach pull-up resistors to these outputs if a problem is anticipated.

When the T8208 is in ATM mode, if bit 6 (inhibit_rxuto_fifo_overrun) of register 0112h is set to '1,' the T8208 prevents the RX UTOPIA FIFO from overflowing by deasserting its rx_enb* signal even though the rx_clav signal is high when polled, **if** the RX UTOPIA FIFO is considered full. If this bit is cleared to '0,' the rx_enb* signal is not deasserted even if the RX UTOPIA FIFO is considered full.

9 UTOPIA Interface (continued)

9.2 Outgoing UTOPIA Cell Interface

9.2.1 Outgoing PHY Mode (Cells Sent by T8208)

In PHY mode, only one enable (u_txenb*[0]) signal and one cell available (u_txclav[0]) signal are used. The u_txenb*[0] signal is an input connected to the ATM layer's RxEnb* signal, and the u_txclav[0] signal is an output connected to the ATM layer's RxClav signal. As a PHY device, the T8208 may use queue group 0 (queues 0, 1, 2, and 3) in the SDRAM and TX UTOPIA cell buffer. The div_queue bits in the main configuration 2 register (address 0112h) may be programmed to "000" for 4 queues or "111" for 1 queue, and the port_rte[127:0] bits in the TX PHY FIFO routing 0, 1, 2, 3, 4, 5, 6, and 7 registers (addresses 0170h, 0172h, 0174h, 0176h, 0178h, 017Ah, 017Ch, and 017Eh) must be programmed to zero. If only queue 0 is used, configure and use only the queue 0 registers at addresses 0440h and 2000h through 2016h. Also, if only queue 0 is used, program the mphy_select bits and priority_select bits in the routing information 1, 2, 3, and 4 registers addresses 0200h, 0202h, 0204h, and 0214h to the zero value of "110000." If queues 0, 1, 2, and 3 are used, configure and use only the queue 0, 1, 2, and 3 registers at addresses 0440h through 0446h and 2000h through 2076h. Also, if queues 0, 1, 2, and 3 are used, only the mphy_select bits in the routing information 1, 2, and 4 registers (addresses 0200h, 0202h, and 0214h) must all be programmed to the zero value of "110000."

For UTOPIA level 2 functionality, the PHY address is programmed in the addr_match bits of UTOPIA configuration register (address 0114h), and the addr_clav_en bits of the main configuration 2 register (address 0112h) can be programmed to any value mentioned in the register **except** "0000." As specified in the UTOPIA level 2 specification, the T8208 drives the u_txclav[0] signal during the clock cycle following the one with its address on the u_txaddr pins. The u_txclav[0] pin goes high impedance when not selected to support MPHY operation. When the tx_utopia_hi_z bit in the main configuration 1 register (address 0100h) is cleared, the u_txsoc, u_txdata[7:0], and u_txprty outputs go high impedance when not selected, allowing multiple PHYs to be connected on the same UTOPIA bus. In UTOPIA level 1, the above level 2 bits are not meaningful; therefore, the addr_clav_en bits must be programmed to "0000," the u_txaddr pins must be grounded, and the addr_match bits cleared.

Note: If the SDRAM is bypassed, the TX UTOPIA cell buffer in the T8208 device can be divided into a minimum of 1 queue and a maximum of 128 queues.

Note: Even though the outgoing (egress) queues are 0—3, the egress port is determined by the address match bits in register 0114h.

9 UTOPIA Interface (continued)

9.2.2 Outgoing ATM Mode (Cells Sent by T8208)

In ATM mode, the T8208 may connect to PHY devices that either meet level 1 or level 2 UTOPIA specifications. If connection is to devices that meet only UTOPIA level 1 specifications, the T8208 may access up to four of these PHY devices using the four enable (u_txenb*[3:0]) and cell available (u_txclav[3:0]) signals. Polling of the cell available signals occurs while the current cell is transmitted.

If the T8208 connects to PHY devices meeting level 2 UTOPIA specifications, in 8-bit data mode, up to 64 MPHY ports may be accessed. In 8-bit UTOPIA 2 mode, 64 MPHYs are supported with four TxCLAV/TxENB pairs with 16-port addressing per TxCLAV/TxENB pair. For 32 PHY ports, two TxCLAV/TxENB pairs support two groups of 16 PHY ports for a total of 32 PHY ports. In 16-bit UTOPIA 2 mode, the T8208 supports 32 PHYs with four TxCLAV/TxENB pairs with 8-port addressing per TxCLAV/TxENB pair.

In ATM MPHY mode, the u_txdata[15:0], u_txaddr[4:0], u_txsoc, and u_txprty signals are connected to each PHY port. In addition, the T8208 generates the address (u_txaddr[4:0]) signals, permitting selection and arbitration among the MPHY ports. The number of address lines used in the connection may vary from one to four, giving a maximum address value of 15. (All five address lines must be connected to provide for the NULL address.) Refer to Section 9.6, UTOPIA Pin Modes, for more information about the possible combinations of address, cell available, and enable signals. The UTOPIA specification for operation with one TxClav and one RxClav is used when the T8208 connects to multiple UTOPIA 2 PHY devices.

In ATM mode, all unused u_txclav inputs require connection to ground.

Note: The u_txenb outputs are high impedance during powerup and reset. An attached PHY may interpret this high-impedance state as an enable; however, the T8208 is not ready to send data during this time. Attach pull-up resistors to these outputs if a problem is anticipated.

The TX UTOPIA cell buffer holds the next cells to be transmitted onto the UTOPIA bus. This TX UTOPIA cell buffer, which holds 256 cells, may be divided into 1, 4, 8, 16, 32, 64, or 128 queues using the div_queue bits in the main configuration 2 register (address 0112h). The number of ports that the T8208 supports determines the number of queues that should be chosen. (See Section 9.6, UTOPIA Pin Modes.) The number of cells per queue, held by the buffer, is determined by dividing 256 (maximum number of cells that TX UTOPIA cell buffer holds) by the number of queues selected (e.g., two cells per queue for 128 queues and 64 cells per queue for four queues).

9 UTOPIA Interface (continued)

Each port is assigned four queues in the TX UTOPIA cell buffer except in the case of 64 ports (for 8-bit UTOPIA) and 32 ports (for 16-bit UTOPIA). In the case of 64 ports (for 8-bit UTOPIA) and 32 ports (for 16-bit UTOPIA), each port is assigned two queues or a programmable number of queues per PHY. Each group of four queues is priority encoded where the lowest-numbered queue has the highest priority. Groups of four queues are shared among two ports as follows:

- Queues 0—3 are shared between ports 0 and 1.
- Queues 4—7 are shared between ports 2 and 3.
- Queues 8—11 are shared between ports 4 and 5.
- Queues 12—15 are shared between ports 6 and 7.
- Queues 16—19 are shared between ports 8 and 9.
- Queues 20—23 are shared between ports 10 and 11.
- Queues 24—27 are shared between ports 12 and 13.
- Queues 28—31 are shared between ports 14 and 15.
- Queues 32—35 are shared between ports 16 and 17.
- Queues 36—39 are shared between ports 18 and 19.
- Queues 40—43 are shared between ports 20 and 21.
- Queues 44—47 are shared between ports 22 and 23.
- Queues 48—51 are shared between ports 24 and 25.
- Queues 52—55 are shared between ports 26 and 27.
- Queues 56—59 are shared between ports 28 and 29.
- Queues 60—63 are shared between ports 30 and 31.
- Queues 64—67 are shared between ports 32 and 33.
- Queues 68—71 are shared between ports 34 and 35.
- Queues 72—75 are shared between ports 36 and 37.
- Queues 76—79 are shared between ports 38 and 39.
- Queues 80—83 are shared between ports 40 and 41.
- Queues 84—87 are shared between ports 42 and 43.
- Queues 88—91 are shared between ports 44 and 45.
- Queues 92—95 are shared between ports 46 and 47.
- Queues 96—99 are shared between ports 48 and 49.
- Queues 100—103 are shared between ports 50 and 51.
- Queues 104—107 are shared between ports 52 and 53.
- Queues 108—111 are shared between ports 54 and 55.
- Queues 112—115 are shared between ports 56 and 57.
- Queues 116—119 are shared between ports 58 and 59.
- Queues 120—123 are shared between ports 60 and 61.
- Queues 124—127 are shared between ports 62 and 63.

9 UTOPIA Interface (continued)

If 32 or less ports in 8-bit UTOPIA and 16 or less ports in 16-bit UTOPIA are used, then each port uses four queues with priorities from 0 to 3, where 0 is the highest priority. The lowest-numbered queue in the group of four is assigned priority 0, and the highest-numbered queue in the group is assigned priority 3. For 64 PHY ports in 8-bit UTOPIA and 32 PHY ports in 16-bit UTOPIA, any of the four queues in each group may be assigned to either the even or odd-numbered port. An example, which will be called **normal** 64-port mode, assigns queues with priorities of 0 and 2 to the even-numbered ports and queues with priorities of 1 and 3 to the odd-numbered ports. The configuration of queues to ports is supported by port-rte[127:112] to [15:0] bits in the TX PHY FIFO routing 7 to 0 register structures. Please see addresses 0170h through 017Eh (Tables 113 through 120). Figure 9 illustrates the selection of ports when 64 are used.

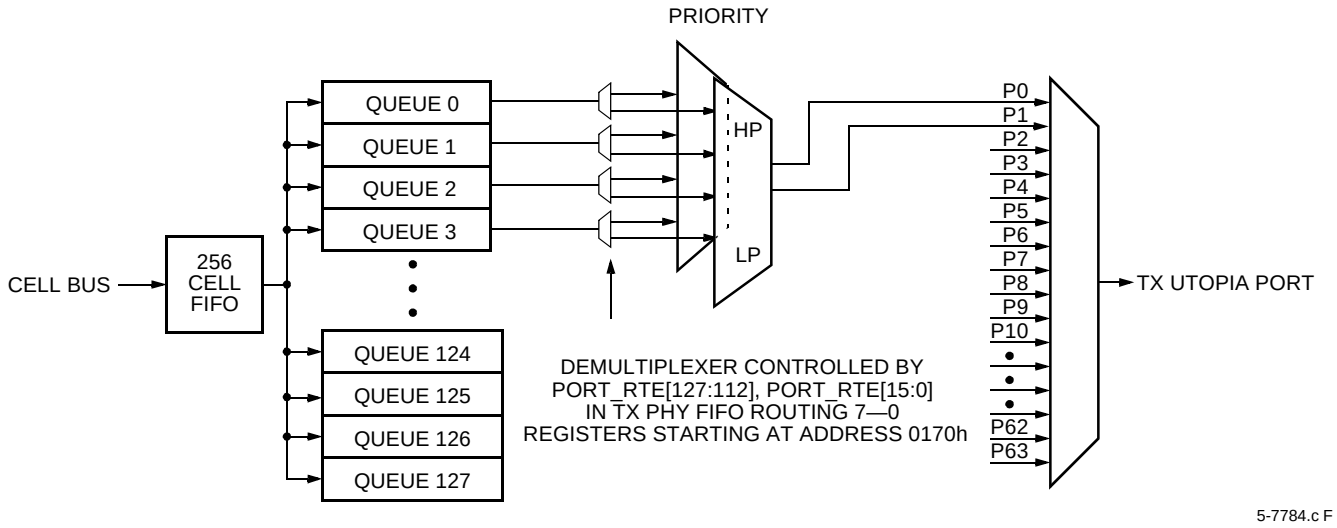


Figure 9. Queue Priority Multiplexing

The TX UTOPIA cell buffer is kept full by cells transferred to it from the SDRAM. Each port has equal priority for transmitting onto the UTOPIA bus. The cell transmitted by any one port is determined by the priority of its queues with cells waiting to be transmitted. In addition, the number of clock cycles wasted for bus arbitration is minimized because polling is performed during cell transfer.

Cells arriving from the cell bus have their header error check (HEC) bytes removed. Therefore, the T8208 calculates the HEC and inserts it into each cell before transmitting it onto the UTOPIA bus. See Figure 10.

9.3 Counters

For each port selected in MPHY mode, two 16-bit registers (in_cnt_phyX[31:16] and in_cnt_phyX[15:0] in Table 152) are used as a 32-bit free-running incoming cell counter. Each port's counter counts valid and misrouted incoming cells. Incoming cells are not counted if they encounter an ignore (I) bit in their translation records that is '1' or if their VPI and/or VCI are out of range. The counter for port 0 is found at addresses 4000h and 4002h. See Table 152 in Section 14.3.2.3, RX UTOPIA Count Monitoring, for the addresses of other ports' incoming cell counters.

Also, for each port selected in MPHY mode, two 16-bit registers (out_cnt_phyX[31:16] and out_cnt_phyX[15:0] in Table 151) are used as a 32-bit free-running outgoing cell counter. Each port's counter counts all outgoing cells to the UTOPIA bus. The counter for port 0 is found at addresses 0600h and 0602h. See Table 151 in Section 14.3.2.2, TX UTOPIA Monitoring, for the addresses of other ports' outgoing cell counters.

9 UTOPIA Interface (continued)

9.3.1 Dropped Cell Counters

There is a 24-bit counter for each queue in the T8208 device that counts all dropped cells. The counter for queue 0 is found at addresses 3000h and 3002h. drop_cell_cnt [15:0] (at address 3002h) and drop_cell_cnt [23:16] (at address 3000h) count the number of dropped cells for queue 0. drop_cell_cnt_ovfl (bit 8 in register 3000h), when set to '1,' indicates that the drop cell counter has overflowed since last read by the microprocessor if clear_on_read is enabled. drop_cell_cnt_clp0 (bit 9 in register 3000h), when set to '1,' indicates that the CLP = 0 cells have been discarded since last read by the microprocessor if clear_on_read is enabled.

The drop cell counters for the remaining queues (1 to 127) are at addresses 3004h to 31FEh.

9.4 55-Byte UTOPIA Mode

In this special UTOPIA mode, the T8208 transmits a 55-byte cell, as opposed to 53 bytes, on the UTOPIA bus. The extra 2 bytes are the tandem routing header received with the cell from the cell bus. These 2 bytes are appended to the beginning of the cell with the tandem routing header [15:8] byte first, followed by the tandem routing header [7:0] byte. Clearing the sp_utopia_sel* bit in the main configuration 1 register (address 0100h) enables this mode. The start of cell signal (u_txsoc) is asserted only once with the first tandem routing header byte. The T8208 may be configured for 55-byte UTOPIA mode whether it is an ATM or PHY device or in 8-bit or 16-bit UTOPIA mode (bit 7 in register 112h).

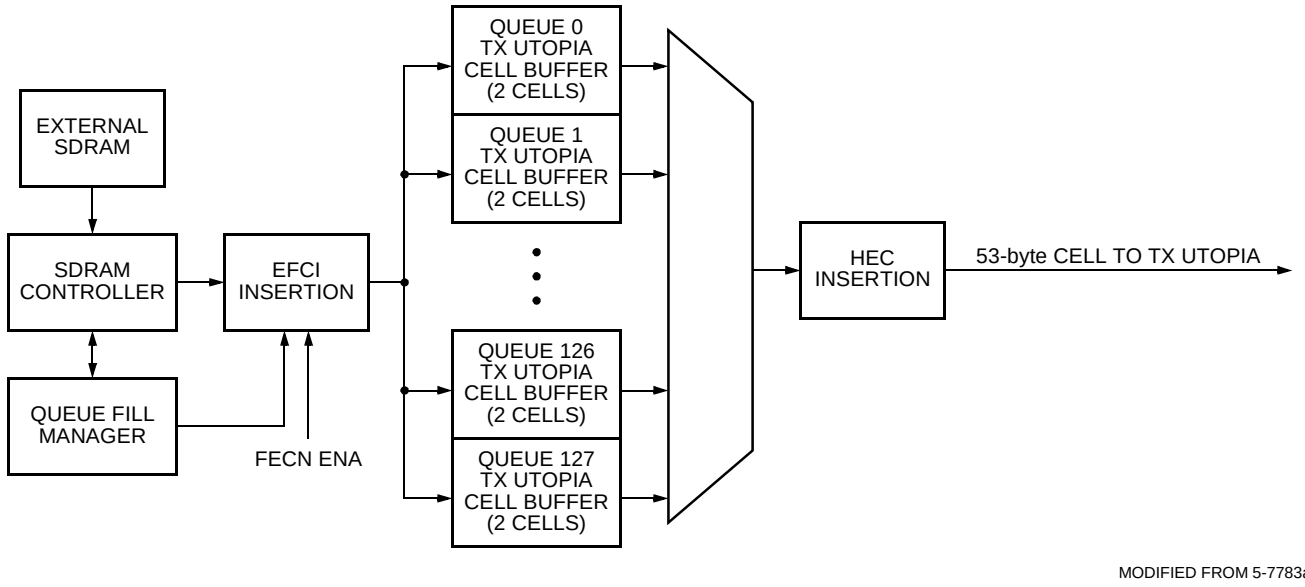


Figure 10. TX UTOPIA Cell Handling

9 UTOPIA Interface (continued)

9.5 Shared UTOPIA Mode

The shared UTOPIA mode allows two T8208 devices on different cell buses to share the same UTOPIA bus. Shared UTOPIA mode functionality requires the T8208 devices to be configured for ATM mode. This configuration is supported for both UTOPIA level 1 and 2 configurations. The shared mode can be used to provide system backplane redundancy or to increase the cell bus system capacity. One T8208 device is configured as master and the other as slave, using the slave_en bit in the main configuration/control register (address 110h). The master and the slave communicate to each other through the shared UTOPIA pins; u_shr_grant[1:0] and u_shr_req[3:0]. For the master, u_shr_grant[1:0] functions as the grant outputs for the cell of specific queue to be sent, and the u_shr_req[3:0] pins function as the request inputs to identify which cell of the 128 queues is to be sent. For the slave, u_shr_grant[1:0] functions as the grant input, and u_shr_req[3:0] as the request output. The configuration for the addr_clav_en bits must be the same in both devices in MCF2 (0112h) and port_rte (0170h to 017Eh) registers.

Note: The T8208 will support shared UTOPIA mode for up to 128 queues (64 MPHYs) in 8-bit UTOPIA mode and will support only 64 queues (32 MPHYs) in 16-bit UTOPIA mode.

The TX UTOPIA cell buffers in the master and the slave may be divided into the same number of queues or different number of queues. The register settings for mast_queue_in[127:112], mast_queue_in[111:96], mast_queue_in[95:80], mast_queue_in[79:64] mast_queue_in[63:48], mast_queue_in[47:32], mast_queue_in[31:16], mast_queue_in[15:0] and slav_queue_in[127:112], slav_queue_in[111:96], slav_queue_in[95:80], slav_queue_in[79:64] slav_queue_in[63:48], slav_queue_in[47:32], slav_queue_in[31:16], and slav_queue_in[15:0] must be configured in the master device. These bits indicate which queues in the master and which queues in the slave are enabled. The master's priority algorithm uses its mast_queue_in information to determine which waiting cell should be transmitted. The slav_queue_in (0160h to 016Eh) registers are ignored in the slave.

The transmit operation in shared UTOPIA mode is illustrated in Figure 11 for 8-bit UTOPIA mode and Figure 12 for 16-bit UTOPIA mode. For the transmit interface, all enable, start of cell, and data signals occur relative to the low-going start of grant signal from the master. The start of grant signal occurs every 60 clock cycles for 8-bit UTOPIA mode and 34 clock cycles for 16-bit UTOPIA mode and is always preceded by at least six clock cycles of ones.

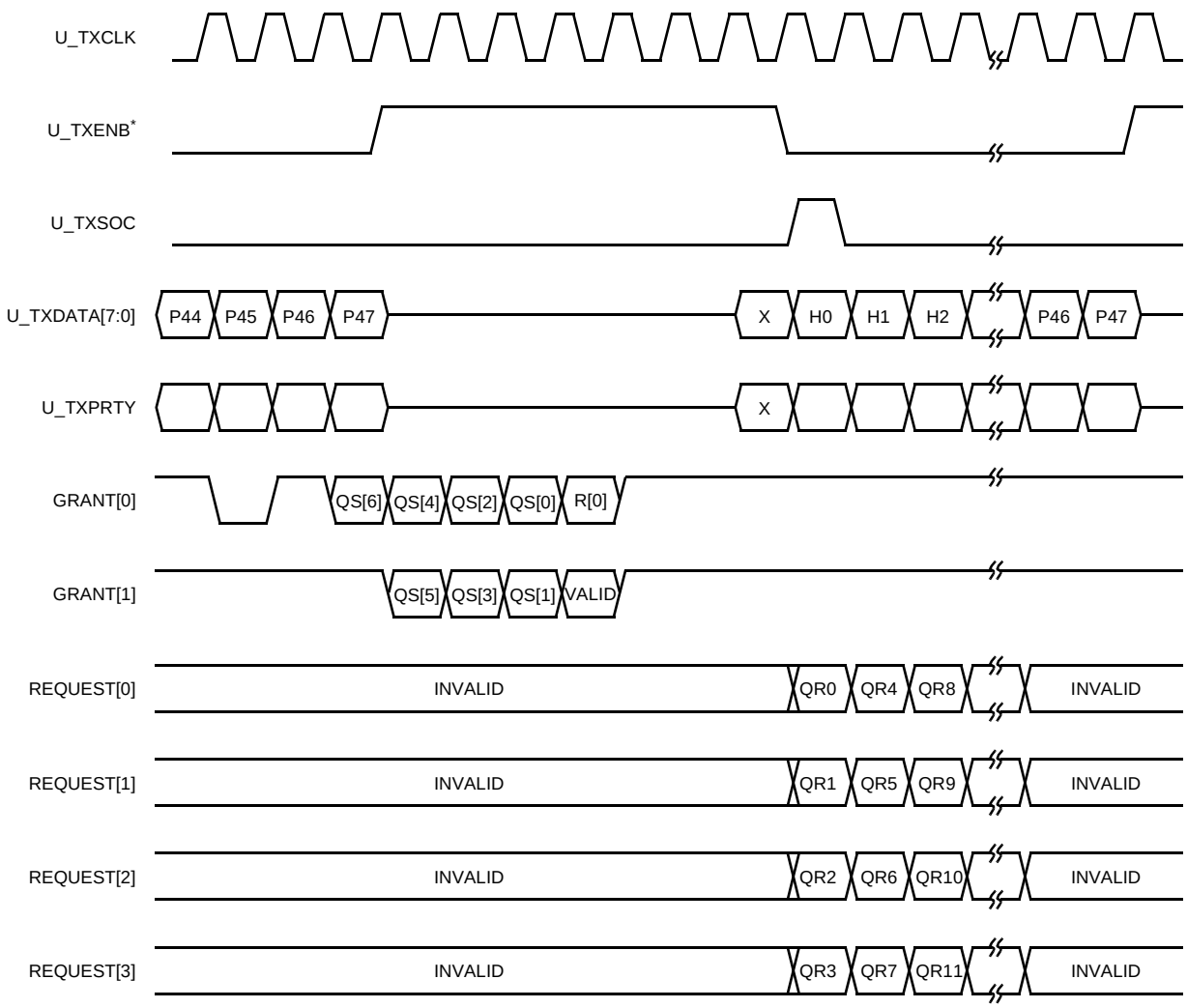
Both devices can transmit on the TX UTOPIA bus; the master arbitrates the bus and grants the slave access via the u_shr_grant pins. When the slave has cells waiting for transmission, it makes a request for each queue (up to 128 in 8-bit UTOPIA mode and 64 in 16-bit UTOPIA mode) that contains cells. To make this request, the slave pulls its u_shr_req pins low for one clock cycle during the queue's request period. The request clock period for each queue is assigned relative to the master's start of grant signal. The request period for first group of queues occurs ten clock cycles after the falling edge of the start of grant. In 8-bit UTOPIA mode, the next 31 clock cycles evaluate queues 4 to 127 and a low bit for the corresponding queue in the 128 queues represents the queue containing a cell to be sent. In 16-bit UTOPIA mode, the next 15 clock cycles evaluate queues 4 to 63 and a low bit for the corresponding queue in the 64 queues represents the queue containing a cell to be sent.

The master uses the received queue requests and a priority algorithm to determine if a slave's cell should be transmitted before one of its own. Both master and slave have an equal chance to transmit cells if the cells have equal priority. The first bit in grant[0] is the low-going grant signal. The next six clock cycles designate the queue number of the cell to be transmitted which only requires 7 of the bits to represent any of the 128 queues in 8-bit UTOPIA mode and 6 bits to represent any of the 64 queues in 16-bit UTOPIA mode. The additional bits in the six clock cycles are reserved. The slave then has 53 cycles (8-bit UTOPIA mode) or 27 cycles (16-bit UTOPIA mode) or 55/28 cycles to transmit its cell depending on the mode.

9 UTOPIA Interface (continued)

In UTOPIA receive mode, the master controls the UTOPIA bus, and the slave only monitors the bus. Both master and slave receive all cells and use their individual look-up tables to determine which cells are destined for their cell bus. The master controls the enable (u_rxenb[3:0]) and address (u_rxaddr[4:0]) signals to the UTOPIA bus. The slave monitors these signals to determine when the cell starts and which port is sending the cell.

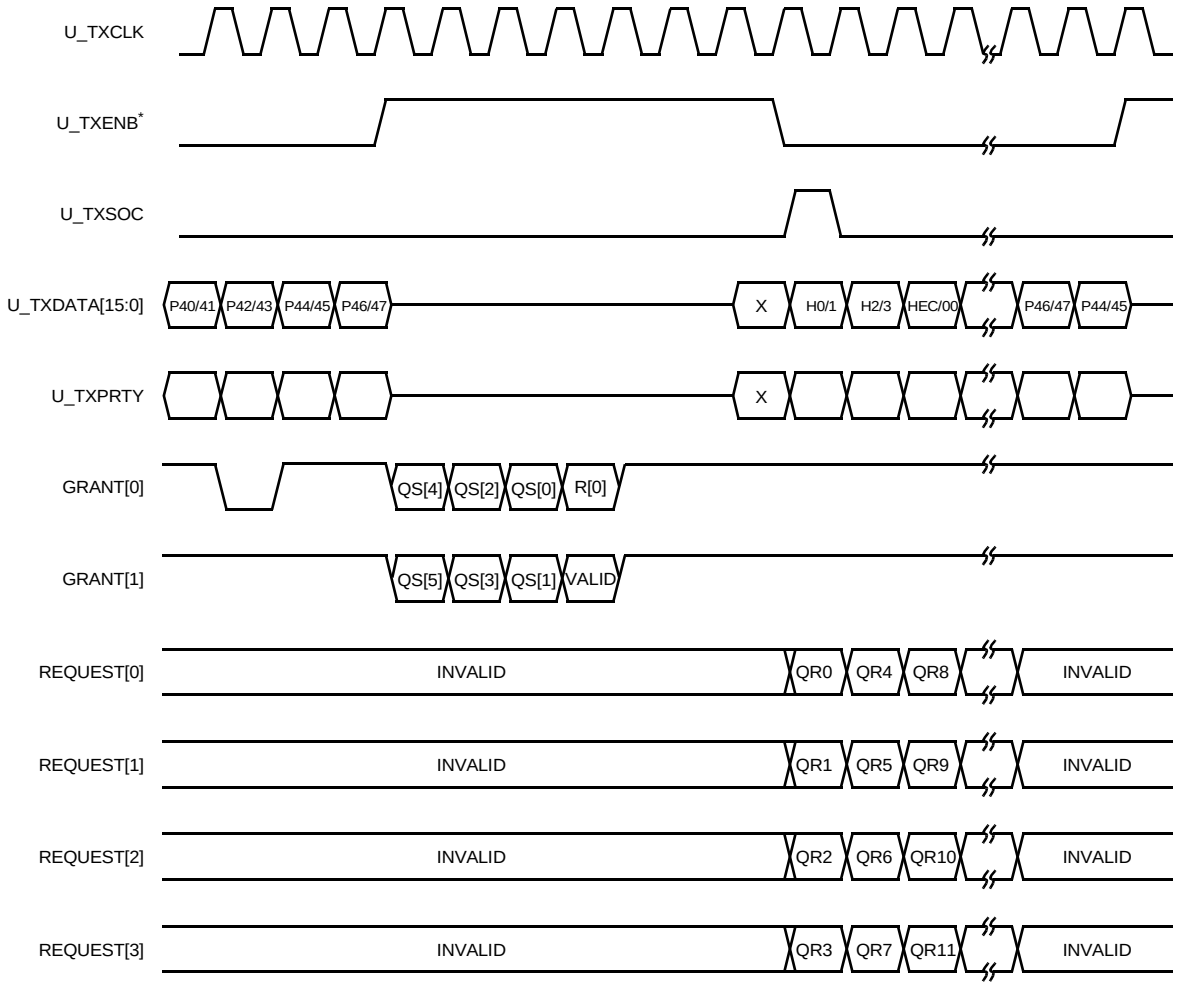
In shared UTOPIA mode, the master always drives the u_rxaddr[4:0], u_txaddr[4:0], u_txsoc, u_rxenb*[3:0], and u_txenb*[3:0] signals. These signals become high impedance on the slave when the slave_en bit in the main configuration/control register (address 0110h) is set. Both the master and slave drive the u_txprty and u_txdata[7:0] signals when they transmit a cell; therefore, these signals must go high impedance when not active. Clear the tx_utopia_hi_z bit in the main configuration 1 register (address 0100h) to force the u_txprty and u_txdata[7:0] signals to a high-impedance state when inactive.



5-7786bF

Figure 11. TX UTOPIA Bus Sharing for 8-Bit UTOPIA Mode

9 UTOPIA Interface (continued)



5-7786cF

Figure 12. TX UTOPIA Bus Sharing for 16-Bit UTOPIA Mode

9.6 UTOPIA Pin Modes

9.6.1 UTOPIA Pin Modes for 8-Bit UTOPIA Operation

In multi-PHY mode, the T8208 interfaces with up to 64 PHY ports in 8-bit UTOPIA operation. Each port is numbered and accessed using a certain combination of the cell available/enable (Clav/Enb*) and address (Addr) signals. The addr_clav_en bits in the main configuration 2 register (address 0112h) are used to select this combination of cell available/enable and address signals. Table 17 indicates the port numbering for each of the possible configurations for 8-bit UTOPIA operation.

The first selection of zero address and four cell available/enable signals (a value of “0000” in bits 3:0 of register 0112h) is used for connection to UTOPIA level one devices. Use this selection to connect from one to four PHY devices to the T8208 in ATM mode. If only one PHY is connected, any of the four cell available signals may be connected to the PHY. For two PHY devices, connect any two, (internal port number must be matched to the Clav being used). All unused u_rxclav inputs require connection to ground. Four queues are allocated per PHY in this configuration.

The second selection of one address and four cell available/enable signals (a value of “0010” in bits 3:0 of register 0112h) is used for connection to UTOPIA level two devices. The selection may be used for up to four PHY groups of two ports each. (See Appendix 1 of *The ATM Forum Technical Committee* UTOPIA Level 2, Version 1.0 specification.) All unused u_rxclav inputs require connection to ground. Four queues are allocated per PHY in this configuration.

9 UTOPIA Interface (continued)

The third selection of two address and four cell available/enable signals (a value of “0101” in bits 3:0 of register 0112h) is used for connection to four UTOPIA level 2 PHY groups of four ports each. Four queues are allocated per PHY in this configuration.

The fourth selection of four address and two cell available/enable signals (a value of “0011” in bits 3:0 of register 0112h) is used for connection to two UTOPIA level 2 PHY groups of sixteen ports each. All unused u_rxclav inputs require connection to ground. Four queues are allocated per PHY in this configuration.

The fifth selection of three address and four cell available/enable signals (a value of “1011” in bits 3:0 of register 0112h) is used for connection to four UTOPIA level 2 PHY groups of eight ports each. Four queues are allocated per PHY in this configuration.

The sixth selection of four address and four cell available/enable signals (a value of “1000” in bits 3:0 of register 0112h) is used for connection to four UTOPIA level 2 PHY groups of sixteen ports each. Two queues are allocated per PHY if the **normal** 64-port mode described in Section 11.4 Queuing is used or a programmable number of queues can be allocated per PHY based on the settings in registers 0170h—017Eh.

Table 17. Pin Configuration for 8-Bit UTOPIA

# of addr	# of clav/enb*	Ports 0—7							
		Port 0	**Port 1**	**Port 2**	**Port 3**	**Port 4**	**Port 5**	**Port 6**	**Port 7**
0	4	enb*[0], clav[0], addr = 0	—	enb*[1], clav[1], addr = 0	—	enb*[2], clav[2], addr = 0	—	enb*[3], clav[3], addr = 0	—
1	4	enb*[0], clav[0], addr = 0	—	enb*[0], clav[0], addr = 2	—	enb*[1], clav[1], addr = 0	—	enb*[1], clav[1], addr = 2	—
2	4	enb*[0], clav[0], addr = 0	—	enb*[0], clav[0], addr = 2	—	enb*[0], clav[0], addr = 4	—	enb*[0], clav[0], addr = 6	—
4	2	enb*[0], clav[0], addr = 0	enb*[0], clav[0], addr = 1	enb*[0], clav[0], addr = 2	enb*[0], clav[0], addr = 3	enb*[0], clav[0], addr = 4	enb*[0], clav[0], addr = 5	enb*[0], clav[0], addr = 6	enb*[0], clav[0], addr = 7
3	4	enb*[0], clav[0], addr = 0	—	enb*[0], clav[0], addr = 2	—	enb*[0], clav[0], addr = 4	—	enb*[0], clav[0], addr = 6	—
4	4	enb*[0], clav[0], addr = 0	enb*[0], clav[0], addr = 1	enb*[0], clav[0], addr = 2	enb*[0], clav[0], addr = 3	enb*[0], clav[0], addr = 4	enb*[0], clav[0], addr = 5	enb*[0], clav[0], addr = 6	enb*[0], clav[0], addr = 7
# of addr	**# of clav/enb***	**Ports 8—15**							
		Port 8	**Port 9**	**Port 10**	**Port 11**	**Port 12**	**Port 13**	**Port 14**	**Port 15**
0	4	—	—	—	—	—	—	—	—
1	4	enb*[2], clav[2], addr = 0	—	enb*[2], clav[2], addr = 2	—	enb*[3], clav[3], addr = 0	—	enb*[3], clav[3], addr = 2	—
2	4	enb*[1], clav[1], addr = 0	—	enb*[1], clav[1], addr = 2	—	enb*[1], clav[1], addr = 4	—	enb*[1], clav[1], addr = 6	—
4	2	enb*[0], clav[0], addr = 8	enb*[0], clav[0], addr = 9	enb*[0], clav[0], addr = 10	enb*[0], clav[0], addr = 11	enb*[0], clav[0], addr = 12	enb*[0], clav[0], addr = 13	enb*[0], clav[0], addr = 14	enb*[0], clav[0], addr = 15
3	4	enb*[0], clav[0], addr = 8	—	enb*[0], clav[0], addr = 10	—	enb*[0], clav[0], addr = 12	—	enb*[0], clav[0], addr = 14	—
4	4	enb*[0], clav[0], addr = 8	enb*[0], clav[0], addr = 9	enb*[0], clav[0], addr = 10	enb*[0], clav[0], addr = 11	enb*[0], clav[0], addr = 12	enb*[0], clav[0], addr = 13	enb*[0], clav[0], addr = 14	enb*[0], clav[0], addr = 15

9 UTOPIA Interface (continued)

Table 17. Pin Configuration for 8-Bit UTOPIA (continued)

# of addr	# of clav/enb*	Ports 16—23							
		Port 16	**Port 17**	**Port 18**	**Port 19**	**Port 20**	**Port 21**	**Port 22**	**Port 23**
0	4	—	—	—	—	—	—	—	—
1	4	—	—	—	—	—	—	—	—
2	4	enb*[2], clav[2], addr = 0	—	enb*[2], clav[2], addr = 2	—	enb*[2], clav[2], addr = 4	—	enb*[2], clav[2], addr = 6	—
4	2	enb*[1], clav[1], addr = 0	enb*[1], clav[1], addr = 1	enb*[1], clav[1], addr = 2	enb*[1], clav[1], addr = 3	enb*[1], clav[1], addr = 4	enb*[1], clav[1], addr = 5	enb*[1], clav[1], addr = 6	enb*[1], clav[1], addr = 7
3	4	enb*[1], clav[1], addr = 0	—	enb*[1], clav[1], addr = 2	—	enb*[1], clav[1], addr = 4	—	enb*[1], clav[1], addr = 6	—
4	4	enb*[1], clav[1], addr = 0	enb*[1], clav[1], addr = 1	enb*[1], clav[1], addr = 2	enb*[1], clav[1], addr = 3	enb*[1], clav[1], addr = 4	enb*[1], clav[1], addr = 5	enb*[1], clav[1], addr = 6	enb*[1], clav[1], addr = 7
# of addr	**# of clav/enb***	**Ports 24—31**							
		Port 24	**Port 25**	**Port 26**	**Port 27**	**Port 28**	**Port 29**	**Port 30**	**Port 31**
0	4	—	—	—	—	—	—	—	—
1	4	—	—	—	—	—	—	—	—
2	4	enb*[3], clav[3], addr = 0	—	enb*[3], clav[3], addr = 2	—	enb*[3], clav[3], addr = 4	—	enb*[3], clav[3], addr = 6	—
4	2	enb*[1], clav[1], addr = 8	enb*[1], clav[1], addr = 9	enb*[1], clav[1], addr = 10	enb*[1], clav[1], addr = 11	enb*[1], clav[1], addr = 12	enb*[1], clav[1], addr = 13	enb*[1], clav[1], addr = 14	enb*[1], clav[1], addr = 15
3	4	enb*[1], clav[1], addr = 8	—	enb*[1], clav[1], addr = 10	—	enb*[1], clav[1], addr = 12	—	enb*[1], clav[1], addr = 14	—
4	4	enb*[1], clav[1], addr = 8	enb*[1], clav[1], addr = 9	enb*[1], clav[1], addr = 10	enb*[1], clav[1], addr = 11	enb*[1], clav[1], addr = 12	enb*[1], clav[1], addr = 13	enb*[1], clav[1], addr = 14	enb*[1], clav[1], addr = 15
# of addr	**# of clav/enb***	**Ports 32—39**							
		Port 32	**Port 33**	**Port 34**	**Port 35**	**Port 36**	**Port 37**	**Port 38**	**Port 39**
0	4	—	—	—	—	—	—	—	—
1	4	—	—	—	—	—	—	—	—
2	4	—	—	—	—	—	—	—	—
4	2	—	—	—	—	—	—	—	—
3	4	enb*[2], clav[2], addr = 0	—	enb*[2], clav[2], addr = 2	—	enb*[2], clav[2], addr = 4	—	enb*[2], clav[2], addr = 6	—
4	4	enb*[2], clav[2], addr = 0	enb*[2], clav[2], addr = 1	enb*[2], clav[2], addr = 2	enb*[2], clav[2], addr = 3	enb*[2], clav[2], addr = 4	enb*[2], clav[2], addr = 5	enb*[2], clav[2], addr = 6	enb*[2], clav[2], addr = 7

9 UTOPIA Interface (continued)

Table 17. Pin Configuration for 8-Bit UTOPIA (continued)

# of addr	# of clav/enb*	Ports 40—47							
		Port 40	**Port 41**	**Port 42**	**Port 43**	**Port 44**	**Port 45**	**Port 46**	**Port 47**
0	4	—	—	—	—	—	—	—	—
1	4	—	—	—	—	—	—	—	—
2	4	—	—	—	—	—	—	—	—
4	2	—	—	—	—	—	—	—	—
3	4	enb*[2], clav[2], addr = 8	—	enb*[2], clav[2], addr = 10	—	enb*[2], clav[2], addr = 12	—	enb*[2], clav[2], addr = 14	—
4	4	enb*[2], clav[2], addr = 8	enb*[2], clav[2], addr = 9	enb*[2], clav[2], addr = 10	enb*[2], clav[2], addr = 11	enb*[2], clav[2], addr = 12	enb*[2], clav[2], addr = 13	enb*[2], clav[2], addr = 14	enb*[2], clav[2], addr = 15
# of addr	**# of clav/enb***	**Ports 48—55**							
		Port 48	**Port 49**	**Port 50**	**Port 51**	**Port 52**	**Port 53**	**Port 54**	**Port 55**
0	4	—	—	—	—	—	—	—	—
1	4	—	—	—	—	—	—	—	—
2	4	—	—	—	—	—	—	—	—
4	2	—	—	—	—	—	—	—	—
3	4	enb*[3], clav[3], addr = 0	—	enb*[3], clav[3], addr = 2	—	enb*[3], clav[3], addr = 4	—	enb*[3], clav[3], addr = 6	—
4	4	enb*[3], clav[3], addr = 0	enb*[3], clav[3], addr = 1	enb*[3], clav[3], addr = 2	enb*[3], clav[3], addr = 3	enb*[3], clav[3], addr = 4	enb*[3], clav[3], addr = 5	enb*[3], clav[3], addr = 6	enb*[3], clav[3], addr = 7
# of addr	**# of clav/enb***	**Ports 56—63**							
		Port 56	**Port 57**	**Port 58**	**Port 59**	**Port 60**	**Port 61**	**Port 62**	**Port 63**
0	4	—	—	—	—	—	—	—	—
1	4	—	—	—	—	—	—	—	—
2	4	—	—	—	—	—	—	—	—
4	2	—	—	—	—	—	—	—	—
3	4	enb*[3], clav[3], addr = 8	—	enb*[3], clav[3], addr = 10	—	enb*[3], clav[3], addr = 12	—	enb*[3], clav[3], addr = 14	—
4	4	enb*[3], clav[3], addr = 8	enb*[3], clav[3], addr = 9	enb*[3], clav[3], addr = 10	enb*[3], clav[3], addr = 11	enb*[3], clav[3], addr = 12	enb*[3], clav[3], addr = 13	enb*[3], clav[3], addr = 14	enb*[3], clav[3], addr = 15

9 UTOPIA Interface (continued)

9.6.2 UTOPIA Pin Modes for 16-Bit UTOPIA Operation

In multi-PHY mode, the T8208 interfaces with up to 32 PHY ports in 16-bit UTOPIA operation. Each port is numbered and accessed using a certain combination of the cell available/enable (Clav/Enb*) and address (Addr) signals. The addr_clav_en bits in the main configuration 2 register (address 0112h) are used to select this combination of cell available/enable and address signals. Table 18 indicates the port numbering for each of the possible configurations for 16-bit UTOPIA operation.

The first selection of zero address and four cell available/enable signals (a value of “0000” in bits 3:0 of register 0112h) is used for connection to UTOPIA level one devices. Use this selection to connect from one to four PHY devices to the T8208 in ATM mode. If only one PHY is connected, any of the four cell available signals may be connected to the PHY. For two PHY devices, connect any two. All unused u_rxclav inputs require connection to ground. Four queues are allocated per PHY in this configuration.

The second selection of one address and four cell available/enable signals (a value of “0010” in bits 3:0 of register 0112h) is used for connection to UTOPIA level two devices. The selection may be used for up to four PHY groups of two ports each. (See Appendix 1 of *The ATM Forum Technical Committee* UTOPIA Level 2, Version 1.0 specification.) All unused u_rxclav inputs require connection to ground. Four queues are allocated per PHY in this configuration.

The third selection of two address and four cell available/enable signals (a value of “0101” in bits 3:0 of register 0112h) is used for connection to four UTOPIA level 2 PHY groups of four ports each. Four queues are allocated per PHY in this configuration.

The fourth selection of three address and four cell available/enable signals (a value of “1001” in bits 3:0 of register 0112h) is used for connection to four UTOPIA level 2 PHY groups of eight ports each. Two queues are allocated per PHY if the **normal** 64-port mode described in Section 11.4 Queuing is used or a programmable number of queues can be allocated per PHY based on the settings in registers 0170h—017Eh.

9 UTOPIA Interface (continued)

Table 18. Pin Configuration for 16-Bit UTOPIA

# of addr	# of clav/enb*	Ports 0—7							
		Port 0	**Port 1**	**Port 2**	**Port 3**	**Port 4**	**Port 5**	**Port 6**	**Port 7**
0	4	enb*[0], clav[0], addr = 0	—	enb*[1], clav[1], addr = 0	—	enb*[2], clav[2], addr = 0	—	enb*[3], clav[3], addr = 0	—
1	4	enb*[0], clav[0], addr = 0	—	enb*[0], clav[0], addr = 2	—	enb*[1], clav[1], addr = 0	—	enb*[1], clav[1], addr = 2	—
2	4	enb*[0], clav[0], addr = 0	—	enb*[0], clav[0], addr = 2	—	enb*[0], clav[0], addr = 4	—	enb*[0], clav[0], addr = 6	—
3	4	enb*[0], clav[0], addr = 0	enb*[0], clav[0], addr = 1	enb*[0], clav[0], addr = 2	enb*[0], clav[0], addr = 3	enb*[0], clav[0], addr = 4	enb*[0], clav[0], addr = 5	enb*[0], clav[0], addr = 6	enb*[0], clav[0], addr = 7
# of addr	**# of clav/enb***	**Ports 8—15**							
		Port 8	**Port 9**	**Port 10**	**Port 11**	**Port 12**	**Port 13**	**Port 14**	**Port 15**
0	4	—	—	—	—	—	—	—	—
1	4	enb*[2], clav[2], addr = 0	—	enb*[2], clav[2], addr = 2	—	enb*[3], clav[3], addr = 0	—	enb*[3], clav[3], addr = 2	—
2	4	enb*[1], clav[1], addr = 0	—	enb*[1], clav[1], addr = 2	—	enb*[1], clav[1], addr = 4	—	enb*[1], clav[1], addr = 6	—
3	4	enb*[1], clav[1], addr = 0	enb*[1], clav[1], addr = 1	enb*[1], clav[1], addr = 2	enb*[1], clav[1], addr = 3	enb*[1], clav[1], addr = 4	enb*[1], clav[1], addr = 5	enb*[1], clav[1], addr = 6	enb*[1], clav[1], addr = 7
# of addr	**# of clav/enb***	**Ports 16—23**							
		Port 16	**Port 17**	**Port 18**	**Port 19**	**Port 20**	**Port 21**	**Port 22**	**Port 23**
0	4	—	—	—	—	—	—	—	—
1	4	—	—	—	—	—	—	—	—
2	4	enb*[2], clav[2], addr = 0	—	enb*[2], clav[2], addr = 2	—	enb*[2], clav[2], addr = 4	—	enb*[2], clav[2], addr = 6	—
3	4	enb*[2], clav[2], addr = 0	enb*[2], clav[2], addr = 1	enb*[2], clav[2], addr = 2	enb*[2], clav[2], addr = 3	enb*[2], clav[2], addr = 4	enb*[2], clav[2], addr = 5	enb*[2], clav[2], addr = 6	enb*[2], clav[2], addr = 7
# of addr	**# of clav/enb***	**Ports 24—31**							
		Port 24	**Port 25**	**Port 26**	**Port 27**	**Port 28**	**Port 29**	**Port 30**	**Port 31**
0	4	—	—	—	—	—	—	—	—
1	4	—	—	—	—	—	—	—	—
2	4	enb*[3], clav[3], addr = 0	—	enb*[3], clav[3], addr = 2	—	enb*[3], clav[3], addr = 4	—	enb*[3], clav[3], addr = 6	—
3	4	enb*[3], clav[3], addr = 0	enb*[3], clav[3], addr = 1	enb*[3], clav[3], addr = 2	enb*[3], clav[3], addr = 3	enb*[3], clav[3], addr = 4	enb*[3], clav[3], addr = 5	enb*[3], clav[3], addr = 6	enb*[3], clav[3], addr = 7

9 UTOPIA Interface (continued)

9.7 UTOPIA Clocking

All TX UTOPIA signals in the T8208 are clocked on the rising edge of the TX UTOPIA clock, and all RX UTOPIA signals are clocked on the rising edge of the RX UTOPIA clock.

The UTOPIA specifications state that the ATM layer supplies the transmit and receive UTOPIA interface clocks to the PHY layers. The T8208 may be configured to drive these clocks or to be driven by them.

In the T8208, the clocks for transmit and receive UTOPIA interfaces may be independently derived from several sources. In addition, each of these clocks may be independently configured. The TX UTOPIA clock configuration (address 010Ch) and RX UTOPIA clock configuration (address 010Eh) registers are used to select and configure the transmit UTOPIA interface and the receive UTOPIA interface clocks, respectively. See these register descriptions for more information.

9.8 Option for Counters to Clear on Read

All the counters (addresses 0600h—06FEh, 3000h—31FEh, 4000h—40FEh, and total and special cell counters of the look-up record if the extended records mode is selected) can be cleared automatically when read by the microprocessor, if the clear_on_read bit (bit 12 in register 0112h) is set to ‘1.’ Both the registers for every PHY (and every queue for dropped cell count) must be read consecutively, (bits 31:16 first, bits 15:0 next) so that both the registers can be cleared automatically.

If this bit (bit 12 in register 0112h) is cleared to ‘0’ then the microprocessor will have to clear the counters individually by writing a ‘0’ to them after reading, if it is needed.

10 Cell Bus Interface

10.1 General Architecture

The high bandwidth, 32-bit cell bus is used to interconnect T8208 devices. Up to 32 devices may be connected to the bus, and cell exchange may occur between any of these devices. Each cell bus frame is 16 clock cycles, and during these 16 cycles, one cell is transmitted. The T8208 is designed to operate with a maximum cell bus frequency of 66 MHz, which translates to a cell bandwidth of 1.7 Gbits/s. The maximum achievable frequency for a given bus implementation is dependent on loading and other design considerations.

In addition to the 32 bits of data, the cell bus uses four additional control signals. The four signals include a read clock, a write clock, a frame synchronization signal, and an acknowledge signal.

The read and write clocks (cb_rc* and cb_wc* pins, respectively) establish the timing for reading and writing cells on the bus and can be generated internally from the T8208 device or from an external clock source. The internal clock source offers the capability to program the required timing skew between write and read clocks. Separate pins are provided for the read and write clock signals. The read clock is used to read the cell from the cell bus, and the write clock is used to write the cell to the cell bus. Because all devices on the cell bus read and write on the same clock edge, the write clock is delayed slightly, relative to the read clock, to ensure sufficient data hold time.

The active-low frame sync (cb_fs*) is generated by the bus arbiter and indicates the first cycle of the cell bus frame in 16-user mode or the first cycle of two cell bus frames for 32-user mode. This signal is generated every 16 clock cycles for 16-user mode or every 32 clock cycles for 32-user mode.

The acknowledge (cb_ack*) signal is used to acknowledge the successful receipt of a cell. This signal is asserted low during the next request cycle by the T8208 that receives the cell. This signal is not asserted for multicast or broadcast cells. In the event of an overflow in the control cell RX FIFO, the loopback FIFO, the TX PHY FIFO, or the cell bus input FIFO, the acknowledge signal will assert low. In the case of an overflow, this signal will not assert low for multicast and broadcast cells.

When cb_disable* is asserted, the device can receive data on the cb_d*[31:0] but cannot transmit data. The device cannot assert the cb_ack* even when a valid cell is received from the cell bus, if cb_disable* is asserted.

Several T8208 devices may reside on the cell bus, but one device must be configured as bus arbiter by clearing the cb_arb_sel bit in the cell bus configuration/status register (address 0130h) or by pulling the arb_en* lead low. The cell bus arbiter receives requests for access to the bus from all resident devices during the first cycle of the cell bus frame and grants one of these requests during the last cycle of the cell bus frame. Before issuing the grant and while a cell is transmitted on the cell bus, the arbiter executes its arbitration algorithm to determine the next device to transmit on the bus. The arbiter also generates the frame synchronization signal. Software will designate only one device as cell bus arbiter, at any given time, to ensure proper operation of the bus.

A 5-bit unit address is assigned to each device (up to 32) on the bus. Each device uses this address to request cell transmission and to identify incoming cells destined for them. Each device is given a unique unit address by individually tying each address (ua*[4:0]) input high or low. The unit address inputs are active-low; therefore, a device with its ua*[4:0] inputs tied to “10000” has address 15. Each device can also be given a unique unit address by writing the address into bits 4:0 in register 0130h, provided bit 7 in register 0130h is also set to 1. The device makes a cell transmission request by driving the two assigned bits during the request cycle, which is the first cycle of a frame. For example, device 15 uses bits 30 and 31 of the request cycle as its request bits. (See Section 10.2, Cell Bus Frames.) Also, each device uses its unit address to determine if a received cell is destined for it. (See Section 10.3, Cell Bus Routing Headers.)

10 Cell Bus Interface (continued)

The cell bus may be configured for 16-user or 32-user mode, using the cb_usr_mode bit in the cell bus configuration/status register (address 0130h). In 16-user mode, all 16 devices assert their transmission requests during the first cycle of each frame, and the transmission grant for the next frame is given during the last cycle of the frame. In 32-user mode, the frame synchronization signal is asserted every two cell bus frames. The two frames are termed the odd and even frames. The frame synchronization signal marks the beginning of the even frame, and the odd frame starts 16 clock cycles later. During the request cycle of the even frame, devices zero through 15 assert their transmission requests, and during the request cycle of the odd frame, devices 16 through 31 assert theirs. Requests received from odd and even frames are serviced as a group, and grants are given in the order that the requests are received with the highest priority serviced first with the same priority requests serviced using a round robin algorithm. Transmission grants for the next frame are always given at the end of the current frame.

Cells to be transmitted onto the cell bus come from three sources internal to the T8208. Data cells from the UTOPIA bus are placed in the RX PHY FIFO to await transmission onto the cell bus. Control cells from the microprocessor wait in the control cell TX FIFO, and loopback cells from the cell bus wait in the loopback FIFO. Cells from these three FIFOs are priority multiplexed onto the cell bus output FIFO to be transmitted onto the cell bus.

Optional high priority can be established for data cells or control cells sent to the cell bus. If bit 9 in register 0130h is cleared to ‘0’ then cells from the RX PHY FIFO have the highest priority, cells from the control cell TX FIFO have next highest, and finally, cells from the loopback FIFO have the lowest. If bit 9 in register 0130h is set to ‘1,’ then cells from the control cell TX FIFO have the highest priority, cells from the RX PHY FIFO have the next highest priority, and finally, cells from the loopback FIFO have the lowest priority. This bit on default is ‘0.’

Incoming cells may be broadcast, multicast, or single address types. The T8208 receiving device accepts single address cells with an address field in the cell bus routing header that matches the device’s unit address. In addition, the device accepts all broadcast cells and certain multicast cells that it is configured to accept. (See Section 10.3.4, Multicast Routing.) Before a cell is accepted, a check is done on the previous grant to verify whether it is a valid grant or not. The receiving device verifies the cell bus routing header cyclic redundancy check (CRC-4) value in the least significant 4 bits of the cell bus routing header. It also verifies the bit interleave parity (BIP-8) value from bits 24 to 31 of the last cell bus frame cycle. If either is corrupt, the cell is discarded. If kept, cells are routed to the loopback FIFO, control FIFO, or TX PHY FIFO, based on the information in its cell bus routing header. See Section 10.3, Cell Bus Routing Headers.

10 Cell Bus Interface (continued)

10.2 Cell Bus Frames

A cell bus frame is always 16 clock cycles. The cell bus frame has three sections (request, bus cell, and grant). During the request section, which is the first clock cycle of the frame, 16 devices assert their transmission requests onto the bus. During the bus cell section, which is the next 14 clock cycles, a cell is transmitted on the cell bus. This bus cell includes the cell bus routing header, the tandem routing header, and the 52-byte body of the cell. During the grant section, which is the last clock cycle of the frame, the grant is asserted, indicating which device may transmit its cell during the next frame. Also, during this last clock cycle, a parity vector is placed on the bus by the transmitting device so that error detection can be performed on the cell. Figure 13 illustrates the format for the cell bus frame.

	31								16 15							0
CYCLE 0	U15	U14	U13	U12	U11	U10	U9	U8	U7	U6	U5	U4	U3	U2	U1	U0
CYCLE 1	CELL BUS ROUTING HEADER								TANDEM ROUTING HEADER							
CYCLE 2	GFC/ VPI[11:8]		VPI[7:0]				VCI[15:0]								PTI	CLP
CYCLE 3	PAYLOAD BYTE 0				PAYLOAD BYTE 1				PAYLOAD BYTE 2				PAYLOAD BYTE 3			
CYCLE 4	PAYLOAD BYTE 4				PAYLOAD BYTE 5				PAYLOAD BYTE 6				PAYLOAD BYTE 7			
CYCLE 5	PAYLOAD BYTE 8				PAYLOAD BYTE 9				PAYLOAD BYTE 10				PAYLOAD BYTE 11			
CYCLE 6	PAYLOAD BYTE 12				PAYLOAD BYTE 13				PAYLOAD BYTE 14				PAYLOAD BYTE 15			
CYCLE 7	PAYLOAD BYTE 16				PAYLOAD BYTE 17				PAYLOAD BYTE 18				PAYLOAD BYTE 19			
CYCLE 8	PAYLOAD BYTE 20				PAYLOAD BYTE 21				PAYLOAD BYTE 22				PAYLOAD BYTE 23			
CYCLE 9	PAYLOAD BYTE 24				PAYLOAD BYTE 25				PAYLOAD BYTE 26				PAYLOAD BYTE 27			
CYCLE 10	PAYLOAD BYTE 28				PAYLOAD BYTE 29				PAYLOAD BYTE 30				PAYLOAD BYTE 31			
CYCLE 11	PAYLOAD BYTE 32				PAYLOAD BYTE 33				PAYLOAD BYTE 34				PAYLOAD BYTE 35			
CYCLE 12	PAYLOAD BYTE 36				PAYLOAD BYTE 37				PAYLOAD BYTE 38				PAYLOAD BYTE 39			
CYCLE 13	PAYLOAD BYTE 40				PAYLOAD BYTE 41				PAYLOAD BYTE 42				PAYLOAD BYTE 43			
CYCLE 14	PAYLOAD BYTE 44				PAYLOAD BYTE 45				PAYLOAD BYTE 46				PAYLOAD BYTE 47			
CYCLE 15	BIT INTERLEAVE PARITY				—	—	—	—	—	—	—	—	—	—	—	—	—	GP	GE	GRANT NUMBER

Figure 13. Cell Bus Frame Format (Bit Positions for 16-User Mode)

10 Cell Bus Interface (continued)

	31								16	15							0
CYCLE 0	U15	U14	U13	U12	U11	U10	U9	U8		U7	U6	U5	U4	U3	U2	U1	U0
CYCLE 1	CELL BUS ROUTING HEADER									TANDEM ROUTING HEADER							
CYCLE 2	GFC/ VPI[11:8]				VPI[7:0]					VCI[15:0]						PTI	CLP
CYCLE 3	PAYLOAD BYTE 0				PAYLOAD BYTE 1					PAYLOAD BYTE 2				PAYLOAD BYTE 3			
CYCLE 4	PAYLOAD BYTE 4				PAYLOAD BYTE 5					PAYLOAD BYTE 6				PAYLOAD BYTE 7			
CYCLE 5	PAYLOAD BYTE 8				PAYLOAD BYTE 9					PAYLOAD BYTE 10				PAYLOAD BYTE 11			
CYCLE 6	PAYLOAD BYTE 12				PAYLOAD BYTE 13					PAYLOAD BYTE 14				PAYLOAD BYTE 15			
CYCLE 7	PAYLOAD BYTE 16				PAYLOAD BYTE 17					PAYLOAD BYTE 18				PAYLOAD BYTE 19			
CYCLE 8	PAYLOAD BYTE 20				PAYLOAD BYTE 21					PAYLOAD BYTE 22				PAYLOAD BYTE 23			
CYCLE 9	PAYLOAD BYTE 24				PAYLOAD BYTE 25					PAYLOAD BYTE 26				PAYLOAD BYTE 27			
CYCLE 10	PAYLOAD BYTE 28				PAYLOAD BYTE 29					PAYLOAD BYTE 30				PAYLOAD BYTE 31			
CYCLE 11	PAYLOAD BYTE 32				PAYLOAD BYTE 33					PAYLOAD BYTE 34				PAYLOAD BYTE 35			
CYCLE 12	PAYLOAD BYTE 36				PAYLOAD BYTE 37					PAYLOAD BYTE 38				PAYLOAD BYTE 39			
CYCLE 13	PAYLOAD BYTE 40				PAYLOAD BYTE 41					PAYLOAD BYTE 42				PAYLOAD BYTE 43			
CYCLE 14	PAYLOAD BYTE 44				PAYLOAD BYTE 45					PAYLOAD BYTE 46				PAYLOAD BYTE 47			
CYCLE 15	BIT INTERLEAVE PARITY				—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	GP	GE	GRANT NUMBER
CYCLE 16	U31	U30	U29	U28	U27	U26	U25	U24		U23	U22	U21	U20	U19	U18	U17	U16
CYCLE 17	CELL BUS ROUTING HEADER									TANDEM ROUTING HEADER							
CYCLE 18	GFC/ VPI[11:8]				VPI[7:0]					VCI[15:0]						PTI	CLP
CYCLE 19	PAYLOAD BYTE 0				PAYLOAD BYTE 1					PAYLOAD BYTE 2				PAYLOAD BYTE 3			
CYCLE 20	PAYLOAD BYTE 4				PAYLOAD BYTE 5					PAYLOAD BYTE 6				PAYLOAD BYTE 7			
CYCLE 21	PAYLOAD BYTE 8				PAYLOAD BYTE 9					PAYLOAD BYTE 10				PAYLOAD BYTE 11			
CYCLE 22	PAYLOAD BYTE 12				PAYLOAD BYTE 13					PAYLOAD BYTE 14				PAYLOAD BYTE 15			
CYCLE 23	PAYLOAD BYTE 16				PAYLOAD BYTE 17					PAYLOAD BYTE 18				PAYLOAD BYTE 19			
CYCLE 24	PAYLOAD BYTE 20				PAYLOAD BYTE 21					PAYLOAD BYTE 22				PAYLOAD BYTE 23			
CYCLE 25	PAYLOAD BYTE 24				PAYLOAD BYTE 25					PAYLOAD BYTE 26				PAYLOAD BYTE 27			
CYCLE 26	PAYLOAD BYTE 28				PAYLOAD BYTE 29					PAYLOAD BYTE 30				PAYLOAD BYTE 31			
CYCLE 27	PAYLOAD BYTE 32				PAYLOAD BYTE 33					PAYLOAD BYTE 34				PAYLOAD BYTE 35			
CYCLE 28	PAYLOAD BYTE 36				PAYLOAD BYTE 37					PAYLOAD BYTE 38				PAYLOAD BYTE 39			
CYCLE 29	PAYLOAD BYTE 40				PAYLOAD BYTE 41					PAYLOAD BYTE 42				PAYLOAD BYTE 43			
CYCLE 30	PAYLOAD BYTE 44				PAYLOAD BYTE 45					PAYLOAD BYTE 46				PAYLOAD BYTE 47			
CYCLE 31	BIT INTERLEAVE PARITY				—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	GP	GE	GRANT NUMBER

Figure 14. Cell Bus Frame Format (Bit Positions for 32-User Mode)

10 Cell Bus Interface (continued)

Devices on the cell bus make their requests during the first cycle of each frame. In 16-user mode, each device asserts a request every frame. In 32-user mode, each device asserts a request every two frames. In 32-user mode, devices with unit addresses 0 through 15 assert their requests during the even frames, and devices with unit addresses 16 through 31 assert their requests during the odd frames. During cycle 0 of their assigned frame, each device drives two of the 32 data bits available. The position of the two request bits for each device is based on the device's unit address. The assigned bit positions for each device are illustrated in Figure 13 and Figure 14 for 16-user and 32-user modes, respectively. For example, in the figures, the device with unit address 0 makes its requests using the 2 bits labeled as U0. Two bits, instead of one, are used for each device so the priority of the request may be included. The priority of the request is set up using the cb_req_pr bits in the main configuration/control register (address 0110h). See Table 59 in Section 14.3, Extended Memory Registers, for more information.

During clock cycles 1 through 14, the device that was granted the bus at the end of the previous frame sends its bus cell. The bus cell sent includes the cell bus routing header, the tandem routing header, and the original UTOPIA cell with the header error check (HEC) byte removed. The HEC byte is removed because the cell bus does its own error check over the complete cell using the bit interleave parity byte. The HEC byte is recreated and inserted before the received cell is placed on the UTOPIA bus.

The cell bus routing header indicates the type of the cell (data, control, loopback) and its destination (single, multicast, broadcast). See Section 10.3, Cell Bus Routing Headers, for more information on the cell bus routing header structure. The tandem routing header is configured by the user.

The 32 bits of the grant section of the frame (clock cycle 15) include the bit interleave parity (BIP-8) byte, the grant parity bit, the grant enable bit, and the grant number. The most significant 8 bits of the grant section of the frame is the BIP-8 byte. The BIP-8 byte is calculated over 54 bytes, starting with the first tandem routing header byte and ending with the last payload byte. To calculate this bit interleave parity, an exclusive-OR operation is performed on the first byte of the tandem routing header and the value "11111111." The exclusive-OR operation then is performed on this result and the following byte. The operation is then repeated with every successive byte through the last data byte of the payload. The resulting byte becomes the BIP-8 byte of the grant section. The next 17 bits of the grant section are unused. The least significant 7 bits of the grant section are used to grant transmission requests. The grant number is located in the least significant 5 bits of the grant section and is the unit address of the device that transmits a cell during the next frame. The grant enable, bit 5, is an active-high signal that indicates if the grant is valid. Finally, the grant parity, bit 6, is the odd parity check calculated over the other six grant bits.

10 Cell Bus Interface (continued)

10.3 Cell Bus Routing Headers

The cell bus routing header gives information about the cell and its routing. There are seven different formats for cell bus routing headers. See Figure 15. These headers cover broadcast, multicast, and single address routing. A T8208 device on the cell bus accepts all broadcast cells and certain multicast cells that it is configured to accept. Broadcast or multicast routed cells may be data cells or control cells. The T8208 receiving device accepts single address cells with an address field in its cell bus routing header that matches the device's unit address. Cells, routed as single address, may be data, control, or loopback cells.

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
MULTICAST CONTROL CELL HEADER	1	1	—	—	MULTICAST NET NUMBER								H			
MULTICAST DATA CELL HEADER	1	0	—	—	MULTICAST NET NUMBER								H			
SINGLE DESTINATION DATA CELL HEADER	0	0	—	—	—	—	0	UNIT ADDRESS					H			
SINGLE DESTINATION CONTROL CELL HEADER	0	1	—	—	—	—	0	UNIT ADDRESS					H			
SINGLE DESTINATION LOOPBACK CELL HEADER	0	0	0	—	—	—	1	UNIT ADDRESS					H			
BROADCAST DATA CELL HEADER	0	0	1	—	—	—	1	—	—	—	—	—	H			
BROADCAST CONTROL CELL HEADER	0	1	1	—	—	—	1	—	—	—	—	—	H			

Figure 15. Cell Bus Routing Headers

The H field (b0 to b3) is the cell bus routing header cyclic redundancy check (CRC-4) calculated over the other 12 bits (b4 to b15) of the header. It is provided for cell bus routing header error detection. When cells arrive from the cell bus, the receiving device calculates the CRC-4 over the most significant 12 bits of the cell bus routing header and compares its calculation to the CRC-4 value stored in the H field of the cell bus routing header. If the two do not match, the cell is discarded.

10 Cell Bus Interface (continued)

10.3.1 Control Cells

The microprocessor connected to the T8208 may send control cells to the cell bus by writing the cell to the control cell transmit direct memory at addresses A0h to D7h (or extended memory at addresses 0900h to 0936h). After the cell is written to memory, the microprocessor sets the cntl_cell_wr bit in the main configuration/control register (address 0110h). This bit returns to zero when the cell is transmitted and memory is available to load a new control cell into the device.

Control cells accepted from the cell bus are routed to the control cell RX FIFO. The microprocessor connected to the T8208 reads the control cell at the head of the FIFO using the control cell receive direct memory at addresses 5Ch to 93h (or extended memory at addresses 07FCh to 0832h). After the microprocessor reads the cell, it sets the cntl_cell_rd bit in the main configuration/control register (address 0110h) to remove the cell from the head of the FIFO.

The microprocessor connected to the T8208 can read the cell bus routing header [15:0] and the tandem routing header [15:0] of the received control cell. The cell bus routing header [7:0] is at address 5Ch and the cell bus routing header [15:8] is at address 5Dh. The tandem routing header [7:0] is at address 5Eh and the tandem routing header [15:8] is at address 5Fh.

10.3.2 Data Cells

Data cells accepted from the cell bus are routed to the TX PHY FIFO. From the TX PHY FIFO, the cell is routed to the appropriate transmit queue using the information about the cell's priority and the queue group to which it is destined. The priority of the cell is indicated by 2 bits obtained from the first 64 bits of the bus cell (cell bus routing header, tandem routing header, and ATM cell header). The position of these 2 bits in the cell are user programmable during configuration using the prior0_sel[5:0] and prior1_sel[5:0] bits of the routing information 3 register (address 0204h). The queue group to which the cell is destined is indicated by 5 bits obtained from the first 64 bits of the bus cell (cell bus routing header, tandem routing header, and ATM cell header). The position of these 5 bits in these headers are user programmable using the mphy1_sel[5:0] and mphy2_sel[5:0] bits of the routing information 1 register (address 0200h), the mphy0_sel[5:0] bits of the routing information 2 register (address 0202h) and the mphy3_sel[5:0] and mphy4_sel[5:0] bits of the routing information 3 register (address 0214h). See Tables 139, 140, 141, and 149 in Section 14.3, Extended Memory Registers. None of the priority or MPHY bits are required to be adjacent. For more information on queue groups, see Section 11.4, Queuing.

10 Cell Bus Interface (continued)

10.3.3 Loopback Cells

A loopback cell may be sent to the cell bus for diagnostic purposes. Initially, the loopback cell is sent from one T8208 (device 1) to a second T8208 (device 2). The second T8208 (device 2) returns the cell to the first T8208 (device 1), or, if desired, the second T8208 (device 2) may send the cell on to one or more entirely different T8208 devices. Device 2 accepts the loopback cell and replaces the most significant 12 bits of the cell bus routing header with the routing_header bits in its loopback register (address 0136h). The 12 routing_header bits in the loopback register correspond to the upper 12 bits of a single destination control cell header, a multicast control cell header, or a broadcast control cell header.

To create a loopback path from device 1 to device 2, and back to device 1, coordinated control of device 1 and device 2 is needed. First, the microprocessor connected to device 2 sets up the loopback by writing the routing_header bits in the loopback register of device 2. The routing_header bits indicate a single destination control cell with a unit address field for device 1. Second, the microprocessor connected to device 1 writes a loopback cell to the control cell transmit direct memory (addresses A0h to D7h) of device 1. (See Section 10.3.1, Control Cells, of this document.) The cell bus routing header of this cell is the single destination loopback type, and the unit address section of the header contains the address of device 2. To send the loopback cell, a ‘1' is then written to the cntl_cell_wr bit of the main configuration/control register (address 0110h).

Care must be taken to ensure that the routing_header bits in a T8208 device are not changed until any previously set up loopback cell has been received and retransmitted. If these bits are changed prematurely, misrouting will occur.

Instead of having to program the loopback register (0136h) of device 2, the tandem routing header of the incoming loopback cell (into device 2) can be used as the new cell bus routing header of the outgoing loopback cell. If the insert_cb_lpbk_hdr bit (bit 8 in register 0130h) is cleared to ‘0’ then the T8208 device uses the tandem routing header of the incoming loopback cell as the new cell bus routing header of the outgoing loopback cell and as a result, also inserts the programmed loopback header (in register 0136h) as the tandem routing header of the outgoing loopback cell. If this bit (bit 8 in register 0130h) is set to ‘1’ the T8208 inserts the programmed loopback header (in register 0136h) as the new cell bus routing header of the loopback cell.

10.3.4 Multicast Routing

The T8208 may be programmed to accept certain multicast data cells using the multicast memories at addresses E0h through FFh (or C00h through C1Eh) and C20h through FFEh. The net numbers of accepted multicast control cells are programmed in the memory space E0h through FFh (or C00h through C1Eh) and C20h through FFEh. These memory spaces hold 256 bits each. Each bit represents a multicast net number from 0 to 255.

Note: To prevent potential multicast memory errors, these memory spaces should be cleared during the initialization process.

For 8-bit UTOPIA ATM mode, the net numbers of accepted multicast data cells are programmed in the multicast number memories, which are divided among 32 queue groups. If 64 ports are used, each memory space is shared between two ports, e.g., ports zero and one use the memory assigned to PHY 0, ports two and three use the memory assigned to PHY 1, and so on.

For 16-bit UTOPIA ATM mode, the net numbers of accepted multicast data cells are programmed in the multicast number memories, which are divided among 16 queue groups. If 32 ports are used, each memory space is shared between two ports, e.g., ports zero and one use the memory assigned to PHY 0, ports two and three use the memory assigned to PHY 1, and so on.

The cell priority bits select the specific queue in the queue group to which the cell is routed. (See Section 11.4, Queuing). Note that multicast control cells use the same multicast number memory as PHY 0 multicast data cells. See Table 176 in Section 14.3, Extended Memory Registers and Table 53 in Section 14.2, Direct Memory Access Registers, respectively.

For PHY mode, multicast cells are only transmitted to queue group 0, and only the PHY port 0 and control cell multicast direct memory at addresses E0h through FFh (or C00h through C1Eh) is used. The cell priority determines the specific queue in queue group 0 to which the cell is routed. (See Section 10.3.2, Data Cells.)

10 Cell Bus Interface (continued)

10.3.5 Broadcast Routing

Broadcast control cells are transmitted and received as described in Section 10.3.1, Control Cells. The broadcast control cell bus routing header has a broadcast control cell header type.

For ATM mode, all PHY ports receive the broadcast data cell. The cell priority bits select the specific queue in the queue group to which the cell is routed.

For PHY mode, if SDRAM is bypassed, broadcast data cells are only transmitted to queue 0. If the SDRAM is **not** bypassed, broadcast data cells are only transmitted to queue group 0, and only PHY port 0 is used (although the device will take the time to try to broadcast data cells to all the ports, cells will not be stored in queue groups other than 0).

10.4 Cell Bus Arbitration

One of the T8208 devices sharing the cell bus must be configured as bus arbiter by clearing the cb_arb_sel bit in the cell bus configuration/status register (address 0130h) or by pulling the arb_en* lead low. Using an arbitration algorithm, the arbiter decides the next device to transmit on the cell bus and issues the grant signals at the end of the cell bus frame. The arbiter also generates the active-low frame synchronization signal that occurs every 16 clock cycles in 16-user mode and every 32 clock cycles in 32-user mode.

To grant transmission requests, the arbiter must analyze requests received during the request section of the current frame for 16-user mode or during two request cycles for 32-user mode. The arbitration algorithm used is round robin and based on the priority of the request and the last request granted.

The arbiter circuitry in all T8208 devices on the cell bus will synchronize to the active arbiter on the cell bus. So, when an inactive device becomes the arbiter, it will begin sending frame synchronization signals that coincide to the clock cycle that the original arbiter would have sent its next frame synchronization signal. This prevents the new arbiter from misinterpreting random signals on its first request cycle as valid requests.

The T8208 that has been configured as the bus arbiter can mask (remove) any of the active devices on the cell bus from the arbitration logic so that they will never be granted the bus. If any of the bits are set in register 12Eh (en_req_low_bp[15:0]) and register 12Ch (en_req_up_bp[15:0]), then the cell bus access requests from the corresponding unit address on the bus are enabled into the arbitration logic. If any of the bits are cleared to ‘0’, access requests are masked and ignored by the arbitration logic.

10 Cell Bus Interface (continued)

10.5 Cell Bus Monitoring

Every T8208 device monitors the cell bus for proper operation. The monitoring section of the T8208 checks for the presence of the read clock, the write clock, and the frame synchronization signal. The cb_wc_miss bit in the main interrupt status 1 register (address 0102h) is set when the write clock is inactive for 32 mclk cycles. Likewise, the cb_rc_miss bit in the main interrupt status 1 register is set when the read clock is inactive for 32 mclk cycles. In addition, the cb_fs_miss bit in the main interrupt status 1 register is set when the frame synchronization signal is inactive for greater than 16 cell bus read clock cycles for 16-user mode or for greater than 32 read clock cycles for 32-user mode. This bit is also set when the cell bus write clock is inactive for 32 mclk cycles.

When cells arrive from the cell bus, the cell bus monitoring section of the receiving device calculates the bit interleave parity value over the 54-byte field from the first tandem routing header byte through the final payload byte. If this calculated value does not match the value in bits 24 through 31 of the final clock cycle of the frame, the cell is discarded.

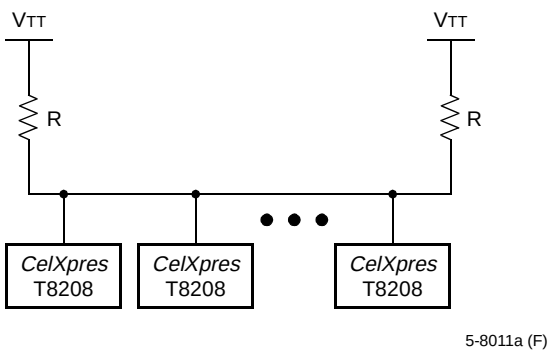
The T8208 detects when a device asserts transmission requests and is not granted permission within a programmable time period. The cb_grnt_to bit in the main interrupt status 1 register (address 0102h) is set when a device has not been granted permission to transmit within the number of frames programmed in the cb_req_to bits of the main configuration 3 register (address 0116h).

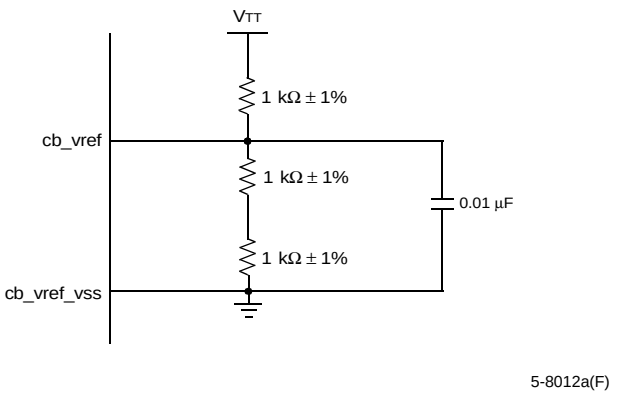
10.6 GTL+ Logic

For the T8208, the cell bus data, frame sync, and acknowledge signals use onboard GTL+ transceivers, and the cell bus clock signals use onboard GTL+ receivers. The GTL+ bus drivers are open drain and require terminating resistors at both ends of each line. The terminating resistor (R) may be from 40 Ω to 50 Ω and should be pulled up to 1.5 V ± 10% (V_{TT}). The actual value of the terminating resistors should be chosen to match the bus line impedance. Figure 16A below illustrates the terminating resistors and the configuration of one GTL+ bus line. The termination resistors are typically placed at the ends of the bus of the backplane.

The signal rise and fall times from the transceivers are carefully controlled to minimize out-of-band signals without affecting the overall transmission rates. These controlled signal edges, in addition to proper resistive line termination, minimize noise and ringing. The slew rate of the GTL+ buffers can be programmed using bits [2:0] of register 2Eh.

The GTL+ receiver compares its input signal to a voltage reference, cb_vref, to determine the logic level of the input. The value of the voltage reference is 2/3 V_{TT} and is created using the voltage divider shown in Figure 16B. The 1 kΩ resistors are 1% because the cb_vref voltage must track V_{TT} by 1%. The 0.01 µF capacitor is a decoupling capacitor on the cb_vref input.





A. GTL+ Bus with Terminating Resistors **B. GTL+ Threshold Voltage Reference**

Figure 16. GTL+ External Circuitry

10 Cell Bus Interface (continued)

10.7 Cell Bus Write and Read Clocks

The read and write clocks (cb_wc* and cb_rc* pins) are supplied from an external source. The write clock should be delayed 1.5 ns to 4 ns relative to the read clock to ensure sufficient data hold time. The position of the clock source relative to the cell bus devices on the card or on connecting cards determines the actual delay that should be used. When the clock source is centrally located among the cell bus devices, a longer delay may be used. When the clock source is at either end of the cell bus devices, a shorter delay is needed. Also, a higher clock frequency requires a shorter delay.

The T8208 can generate both the read and write clocks internally for the cell bus logic, if bit 6 in register 2Eh is cleared to ‘0’ and bit 10 in register 122h is set to ‘1.’ It includes the ability to derive these clocks from several sources (PCLK or MCLK or PLL VCO frequency [twice the MCLK]) and set the skew between the read and write clocks with a programmable granularity (bits 15:13 in register 122h). This feature is useful if the digital loopback (see Section 10.9) is to be used when the card containing the T8208 is operated outside the system.

If bit 6 in register 2Eh is cleared to ‘0’ and bit 10 in register 0122h is set to ‘1,’ then the generated read and write cell bus clocks not only drive the internal cell bus logic of this device but also come out on pins cb_gen_rc and cb_gen_wc (pins B4 and A3, respectively) of this device which can then be used to drive the remaining devices on the backplane.

Note: Due to the inherent propagation delay between the clocks that drive the cell bus logic of the generating device and the other devices on the backplane, it is recommended that customers set bit 6 in register 2Eh to ‘1’ and set bit 10 in register 0122h to ‘1’ and route these generated clocks (through a GTL+ driver) back to the cb_wc* and cb_rc* pins (pins A10 and B10, respectively).

If this bit (bit 10 in register 0122h) is cleared to ‘0’ these 2 pins, cb_gen_rc and cb_gen_wc, are inactive and are 3-stated. In this case, bit 6 in register 2Eh is set to ‘1’ to indicate that pins A10 and B10 will be receiving clocks from a different source on the board. Please see registers 2Eh and 0122h for more details.

10 Cell Bus Interface (continued)

10.8 Modify Cell Bus Request Priority Based on RX PHY FIFO Threshold

This allows the T8208 device to modify the request priority for a cell on the cell bus, based on the RX PHY FIFO thresholds. This feature is useful to raise the priority of cells to avoid a situation where the queue is getting filled with low priority cells and hence the high priority cells are blocking low priority cells from being sent to the cell bus.

There are two thresholds. Threshold 1 to force request priority to MEDIUM and Threshold 2 to force request priority to HIGH.

Bit 4 in register 126h, cb_prio2_thr_en when set, enables the threshold 2. Bits [3:0] in register 0126h, cb_prio2_thr, set the threshold 2.

Bit 12 in register 126h, cb_prio1_thr_en when set, enables the threshold 1. Bits [11:8] in register 0126h, cb_prio1_thr, set the threshold 1.

Cell Bus Request Priority Bits 3:2 in Register 110h	Priority when Threshold 1 Is Reached	Priority when Threshold 2 Is Reached
00 = disabled	medium	high
01 = low priority	medium	high
10 = medium priority	medium	high
11 = high priority	high	high

Note: When bits 3:2 in register 0110h are set to ‘00’ (disabled) and this feature is enabled, cells are transmitted onto the cell bus as soon as the priority **medium** is reached. To prevent this, either the feature needs to be disabled or cells should not be transmitted to this FIFO.

Note: These threshold levels cannot be changed when there is data flowing through the *CelXpres* device.

10.9 Digital Loopback Before Cell Bus

The digital loopback allows loopback of **all** cells without requiring the cell to be sent to the cell bus. The output of the cell bus output FIFO is connected to the input of the cell bus input FIFO internally, so that the cells do not have to go through the GTL+ buffers. The cells being received on the RX UTOPIA should still be addressed properly with in-range VPI/VCI and routing information for the device to be able to loopback the cells.

Bit 7 (dig_lpbk_en) in register 2Eh must be set to ‘1’ **and** bit 2 (GTLTPDN) in register 2Fh must be cleared to ‘0’ to enable a digital loopback.

11 SDRAM Interface

For outgoing UTOPIA cells, the TX UTOPIA cell buffer supports 128 queues. These queues are separated into 32 queue groups, each consisting of four different priority queues as described in Section 9.2.2, Outgoing ATM Mode (Cells Sent by T8208). This cell buffer holds 256 outgoing cells. Additional buffering is provided by an external SDRAM. Connection to an external SDRAM is selected by clearing the sdram_bypass bit in the main configuration 1 register (address 0100h).

If the SDRAM is not used, it is bypassed by setting the sdram_bypass bit in the main configuration 1 register at start-up. When the SDRAM is bypassed, the minimum number of queues that the TX UTOPIA cell buffer can be divided into is 1 queue and the maximum number of queues is 128 queues (ATM mode) or 4 queues (PHY mode). The buffering available in this mode is the 256-cell internal memory (TX PHY FIFO) and up to 256 cells of the TX UTOPIA cell buffer. (The two buffers are not concatenated.) The setting of the div_queue bits in the main configuration 2 register (address 0112h) determines the number of cell locations allocated to queues of the TX UTOPIA cell buffer.

11.1 Memory Configuration

The SDRAM interface supports from 2 Mbytes to 32 Mbytes of memory. This memory size is realized using 16 Mbit or 64 Mbit devices. Table 19 below outlines the various memory configurations supported.

Table 19. Supported Memory Configurations

Number of Devices	Device Memory Size and Data Bus Organization	Number of Columns	Number of Banks	Number of Rows	Total Memory
1	16 Mbit, 16-bit data bus	256	2	2048	2 Mbyte
2	16 Mbit, 8-bit data bus	512	2	2048	4 Mbyte
4	16 Mbit, 4-bit data bus	1024	2	2048	8 Mbyte
1	64 Mbit, 16-bit data bus	256	4	4096	8 Mbyte
2	64 Mbit, 8-bit data bus	512	4	4096	16 Mbyte
4	64 Mbit, 4-bit data bus	1024	4	4096	32 Mbyte

11.2 Powerup Sequence

The powerup sequence for the SDRAM must be performed manually before the SDRAM is enabled. Using the idle state 1 and 2 registers (addresses 0420h and 0422h), the manual access state 1 and 2 registers (addresses 0424h and 0426h), and the gen_man_acc bit in the SDRAM control register (address 0400h), follow the powerup command sequence prescribed by the SDRAM manufacturer. The T8208 does not control the chip select, the clock enable, and the DQM inputs to the SDRAM. These signals should be externally tied to the appropriate logic level or external control signal.

To manually execute SDRAM commands, first set up the idle values for CAS*, RAS*, WE*, bank select (BS), and the address signals using the cas_idle, ras_idle, we_idle, bs_idle[1:0], and addr_idle[11:0] bits in the idle state 1 and 2 registers. Then manually set up the value of these signals for the first SDRAM command using the cas_man, ras_man, we_man, bs_man[1:0], and addr_man[11:0] bits in the manual access state 1 and 2 registers. Finally, write a ‘1’ to the gen_man_acc bit in the SDRAM control register. Writing this ‘1’ drives the CAS, RAS, WE*, BS, and address values (in the manual access state 1 and 2 registers) onto the associated pins for one SDRAM clock cycle. After the one clock cycle, these signals return to their idle state. Repeat this process, making sure minimum timing between commands is met, until the powerup process has been completed.

In the powerup sequence, configure the mode register of the SDRAM for a burst length of one and a CAS latency of two or three. With a burst length of one, sequential and interleave addressing behave the same, so the SDRAM may be configured for either addressing mode.

11 SDRAM Interface (continued)

11.3 SDRAM Interface Timing

The mclk clock is the source of the SDRAM clock (sd_clk) from the T8208. Based on the frequency of the SDRAM clock and the speed grade of the SDRAM, four timing parameters must be programmed into the SDRAM configuration register at address 0408h. These timing parameters are specified in SDRAM (mclk) clock cycles and are listed below:

- RAS inactive to CAS active (ras2cas)—its value may be set from two to four SDRAM clock cycles.
- CAS inactive to precharge command active (cas2pre)—its value may be set from one to four SDRAM clock cycles.
- Precharge command inactive to next command active (pre2cmd)—its value may be set from one to four SDRAM clock cycles.
- CAS before RAS (CBR) refresh command inactive to next CBR refresh command active (ref2cmd)—its value may be set to three, seven, or fifteen SDRAM clock cycles.

Actual values for these parameters are obtained from the data sheet of the SDRAM used. For optimum performance, these parameters should be programmed to the lowest acceptable values. The earliest time that a CAS may be asserted after an RAS may be obtained from the data sheet parameter that describes the minimum time from the activate command to the read/write command. Three parameters affect the earliest time that a precharge command may follow a CAS. For read commands, a precharge command may be issued one clock earlier than the last read data. The actual number of clock cycles depends on the CAS latency needed for the device. For write commands, the earliest time that a precharge command may be issued following a CAS may be obtained from the SDRAM data sheet parameter that describes the minimum time from the last data in to the precharge command. In addition to these two parameters, the minimum time from the activate command to the precharge command may need to be considered to obtain the value for cas2pre. If the SDRAM is only accessed for queuing purposes, 28 consecutive CAS commands will be executed between the activate command and the precharge command, and the minimum time from the activate command to the precharge command does not need to be considered. If the microprocessor reads and writes the SDRAM memory, only one CAS command will be executed between the activate command and the precharge command. In this case, the minimum time from the activate command to the precharge command is significant and must be considered. The minimum time from the precharge command to the next command may be obtained from the data sheet parameter that describes the minimum time from the precharge command to the activate command. The minimum time from the CBR refresh command to the next CBR refresh command may be obtained from the data sheet. In the T8208, the minimum time from CBR refresh to any other command is 15 SDRAM clock cycles. In the data sheet, the parameters may be specified in actual time units rather than clock cycles. To determine the number of clock cycles, divide the parameter value by the SDRAM clock period. Figure 17 below illustrates these timing parameters and the number of clock cycles needed to read or write a cell using the default values for the parameters.

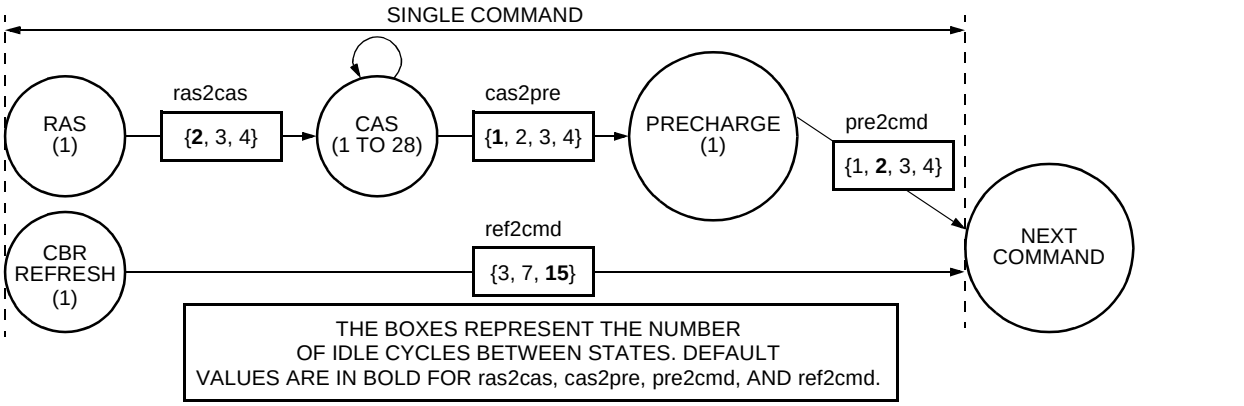


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Figure 17. SDRAM Timing Parameters

11 SDRAM Interface (continued)

11.4 Queuing

For a device configured in ATM mode, up to 32 groups of queues with four priorities per group may be configured in the SDRAM for a total of 128 queues. Therefore, the five port group address bits point to one of 32 queue groups, and the two priority bits point to one of four queues in the group. (For a description of the port group address and priority bits, see Section 10.3.2, Data Cells.) Priority bits with a value of zero represent the highest priority, and those with a value of three, the lowest priority.

If an ATM is configured to support 32 PHY ports in 8-bit UTOPIA mode (a value of “0011” in bits 3:0 of register 0112h), each port is assigned to its associated queue group as illustrated in Table 20, regardless of the value of the port_rte[127:0] bits. In this case, port 0 is assigned to queue group 0, port 1 to queue group 1, and so on.

For an ATM configured to support 64 PHY ports in 8-bit UTOPIA mode and 32 PHY ports in 16-bit UTOPIA mode, each queue group is shared between two ports as specified in Section 9.2.2, Outgoing ATM Mode (cells sent by T8208), and the four queues may be split in any way between the two ports using the port_rte[127:0] bits. Table 21 illustrates the relationship between the queue organization and the port group address/priority bits for a device configured to support 64 PHY ports in 8-bit UTOPIA mode and 32 PHY ports in 16-bit UTOPIA mode, and whose port_rte[127:0] bits are programmed to the **normal** 64-port mode as described in Section 9.2.2, Outgoing ATM Mode (cells sent by T8208). See the TxPHY FIFO routing 7, 6, 5, 4, 3, 2, 1, and 0 registers at addresses 0170h, 0172h, 0174h, 0176h, 0178h, 017Ah, 017Ch, and 017Eh, respectively.

11 SDRAM Interface (continued)

Table 20. Queue Organization and Port Group Address/Priority Bits for 32 Ports in 8-Bit UTOPIA Mode

Port Number	Queue Group	Queue Number	Priority	Port Group Address Bits	Priority Bits
0	0	0	Highest	“00000”	“00”
0	0	1	High	“00000”	“01”
0	0	2	Low	“00000”	“10”
0	0	3	Lowest	“00000”	“11”
1	1	4	Highest	“00001”	“00”
1	1	5	High	“00001”	“01”
1	1	6	Low	“00001”	“10”
1	1	7	Lowest	“00001”	“11”
2	2	8	Highest	“00010”	“00”
2	2	9	High	“00010”	“01”
2	2	10	Low	“00010”	“10”
2	2	11	Lowest	“00010”	“11”
3	3	12	Highest	“00011”	“00”
3	3	13	High	“00011”	“01”
3	3	14	Low	“00011”	“10”
3	3	15	Lowest	“00011”	“11”
4	4	16	Highest	“00100”	“00”
4	4	17	High	“00100”	“01”
4	4	18	Low	“00100”	“10”
4	4	19	Lowest	“00100”	“11”
5	5	20	Highest	“00101”	“00”
5	5	21	High	“00101”	“01”
5	5	22	Low	“00101”	“10”
5	5	23	Lowest	“00101”	“11”
6	6	24	Highest	“00110”	“00”
6	6	25	High	“00110”	“01”
6	6	26	Low	“00110”	“10”
6	6	27	Lowest	“00110”	“11”
7	7	28	Highest	“00111”	“00”
7	7	29	High	“00111”	“01”
7	7	30	Low	“00111”	“10”
7	7	31	Lowest	“00111”	“11”
8	8	32	Highest	“01000”	“00”
8	8	33	High	“01000”	“01”
8	8	34	Low	“01000”	“10”
8	8	35	Lowest	“01000”	“11”
9	9	36	Highest	“01001”	“00”
9	9	37	High	“01001”	“01”
9	9	38	Low	“01001”	“10”
9	9	39	Lowest	“01001”	“11”

11 SDRAM Interface (continued)

Table 20. Queue Organization and Port Group Address/Priority Bits for 32 Ports in 8-Bit UTOPIA Mode (continued)

Port Number	Queue Group	Queue Number	Priority	Port Group Address Bits	Priority Bits
10	10	40	Highest	“01010”	“00”
10	10	41	High	“01010”	“01”
10	10	42	Low	“01010”	“10”
10	10	43	Lowest	“01010”	“11”
11	11	44	Highest	“01011”	“00”
11	11	45	High	“01011”	“01”
11	11	46	Low	“01011”	“10”
11	11	47	Lowest	“01011”	“11”
12	12	48	Highest	“01100”	“00”
12	12	49	High	“01100”	“01”
12	12	50	Low	“01100”	“10”
12	12	51	Lowest	“01100”	“11”
13	13	52	Highest	“01101”	“00”
13	13	53	High	“01101”	“01”
13	13	54	Low	“01101”	“10”
13	13	55	Lowest	“01101”	“11”
14	14	56	Highest	“01110”	“00”
14	14	57	High	“01110”	“01”
14	14	58	Low	“01110”	“10”
14	14	59	Lowest	“01110”	“11”
15	15	60	Highest	“01111”	“00”
15	15	61	High	“01111”	“01”
15	15	62	Low	“01111”	“10”
15	15	63	Lowest	“01111”	“11”
16	16	64	Highest	“10000”	“00”
16	16	65	High	“10000”	“01”
16	16	66	Low	“10000”	“10”
16	16	67	Lowest	“10000”	“11”
17	17	68	Highest	“10001”	“00”
17	17	69	High	“10001”	“01”
17	17	70	Low	“10001”	“10”
17	17	71	Lowest	“10001”	“11”
18	18	72	Highest	“10010”	“00”
18	18	73	High	“10010”	“01”
18	18	74	Low	“10010”	“10”
18	18	75	Lowest	“10010”	“11”
19	19	76	Highest	“10011”	“00”
19	19	77	High	“10011”	“01”
19	19	78	Low	“10011”	“10”
19	19	79	Lowest	“10011”	“11”
20	20	80	Highest	“10100”	“00”
20	20	81	High	“10100”	“01”
20	20	82	Low	“10100”	“10”
20	20	83	Lowest	“10100”	“11”

11 SDRAM Interface (continued)

Table 20. Queue Organization and Port Group Address/Priority Bits for 32 Ports in 8-Bit UTOPIA Mode (continued)

Port Number	Queue Group	Queue Number	Priority	Port Group Address Bits	Priority Bits
21	21	84	Highest	“10101”	“00”
21	21	85	High	“10101”	“01”
21	21	86	Low	“10101”	“10”
21	21	87	Lowest	“10101”	“11”
22	22	88	Highest	“10110”	“00”
22	22	89	High	“10110”	“01”
22	22	90	Low	“10110”	“10”
22	22	91	Lowest	“10110”	“11”
23	23	92	Highest	“10111”	“00”
23	23	93	High	“10111”	“01”
23	23	94	Low	“10111”	“10”
23	23	95	Lowest	“10111”	“11”
24	24	96	Highest	“11000”	“00”
24	24	97	High	“11000”	“01”
24	24	98	Low	“11000”	“10”
24	24	99	Lowest	“11000”	“11”
25	25	100	Highest	“11001”	“00”
25	25	101	High	“11001”	“01”
25	25	102	Low	“11001”	“10”
25	25	103	Lowest	“11001”	“11”
26	26	104	Highest	“11010”	“00”
26	26	105	High	“11010”	“01”
26	26	106	Low	“11010”	“10”
26	26	107	Lowest	“11010”	“11”
27	27	108	Highest	“11011”	“00”
27	27	109	High	“11011”	“01”
27	27	110	Low	“11011”	“10”
27	27	111	Lowest	“11011”	“11”
28	28	112	Highest	“11100”	“00”
28	28	113	High	“11100”	“01”
28	28	114	Low	“11100”	“10”
28	28	115	Lowest	“11100”	“11”
29	29	116	Highest	“11101”	“00”
29	29	117	High	“11101”	“01”
29	29	118	Low	“11101”	“10”
29	29	119	Lowest	“11101”	“11”
30	30	120	Highest	“11110”	“00”
30	30	121	High	“11110”	“01”
30	30	122	Low	“11110”	“10”
30	30	123	Lowest	“11110”	“11”
31	31	124	Highest	“11111”	“00”
31	31	125	High	“11111”	“01”
31	31	126	Low	“11111”	“10”
31	31	127	Lowest	“11111”	“11”

11 SDRAM Interface (continued)

Table 21. Queue Organization and Port Group Address/Priority Bits for 64 Ports in 8-Bit UTOPIA Mode and 32 Ports in 16-Bit UTOPIA Mode

Port Number	Queue Group	Queue Number	Priority	Port Group Address Bits	Priority Bits
0	0	0	High	“00000”	“00”
0	0	2	Low	“00000”	“10”
1	0	1	High	“00000”	“01”
1	0	3	Low	“00000”	“11”
2	1	4	High	“00001”	“00”
2	1	6	Low	“00001”	“10”
3	1	5	High	“00001”	“01”
3	1	7	Low	“00001”	“11”
4	2	8	High	“00010”	“00”
4	2	10	Low	“00010”	“10”
5	2	9	High	“00010”	“01”
5	2	11	Low	“00010”	“11”
6	3	12	High	“00011”	“00”
6	3	14	Low	“00011”	“10”
7	3	13	High	“00011”	“01”
7	3	15	Low	“00011”	“11”
8	4	16	High	“00100”	“00”
8	4	18	Low	“00100”	“10”
9	4	17	High	“00100”	“01”
9	4	19	Low	“00100”	“11”
10	5	20	High	“00101”	“00”
10	5	22	Low	“00101”	“10”
11	5	21	High	“00101”	“01”
11	5	23	Low	“00101”	“11”
12	6	24	High	“00110”	“00”
12	6	26	Low	“00110”	“10”
13	6	25	High	“00110”	“01”
13	6	27	Low	“00110”	“11”
14	7	28	High	“00111”	“00”
14	7	30	Low	“00111”	“10”
15	7	29	High	“00111”	“01”
15	7	31	Low	“00111”	“11”
16	8	32	High	“01000”	“00”
16	8	34	Low	“01000”	“10”
17	8	33	High	“01000”	“01”
17	8	35	Low	“01000”	“11”
18	9	36	High	“01001”	“00”
18	9	38	Low	“01001”	“10”
19	9	37	High	“01001”	“01”
19	9	39	Low	“01001”	“11”
20	10	40	High	“01010”	“00”
20	10	42	Low	“01010”	“10”
21	10	41	High	“01010”	“01”
21	10	43	Low	“01010”	“11”

11 SDRAM Interface (continued)

Table 21. Queue Organization and Port Group Address/Priority Bits for 64 Ports in 8-Bit UTOPIA Mode and 32 Ports in 16-Bit UTOPIA Mode (continued)

Port Number	Queue Group	Queue Number	Priority	Port Group Address Bits	Priority Bits
22	11	44	High	“01011”	“00”
22	11	46	Low	“01011”	“10”
23	11	45	High	“01011”	“01”
23	11	47	Low	“01011”	“11”
24	12	48	High	“01100”	“00”
24	12	50	Low	“01100”	“10”
25	12	49	High	“01100”	“01”
25	12	51	Low	“01100”	“11”
26	13	52	High	“01101”	“00”
26	13	54	Low	“01101”	“10”
27	13	53	High	“01101”	“01”
27	13	55	Low	“01101”	“11”
28	14	56	High	“01110”	“00”
28	14	58	Low	“01110”	“10”
29	14	57	High	“01110”	“01”
29	14	59	Low	“01110”	“11”
30	15	60	High	“01111”	“00”
30	15	62	Low	“01111”	“10”
31	15	61	High	“01111”	“01”
31	15	63	Low	“01111”	“11”
32	16	64	High	“10000”	“00”
32	16	66	Low	“10000”	“10”
33	16	65	High	“10000”	“01”
33	16	67	Low	“10000”	“11”
34	17	68	High	“10001”	“00”
34	17	70	Low	“10001”	“10”
35	17	69	High	“10001”	“01”
35	17	71	Low	“10001”	“11”
36	18	72	High	“10010”	“00”
36	18	74	Low	“10010”	“10”
37	18	73	High	“10010”	“01”
37	18	75	Low	“10010”	“11”
38	19	76	High	“10011”	“00”
38	19	78	Low	“10011”	“10”
39	19	77	High	“10011”	“01”
39	19	79	Low	“10011”	“11”
40	20	80	High	“10100”	“00”
40	20	82	Low	“10100”	“10”
41	20	81	High	“10100”	“01”
41	20	83	Low	“10100”	“11”

11 SDRAM Interface (continued)

Table 21. Queue Organization and Port Group Address/Priority Bits for 64 Ports in 8-Bit UTOPIA Mode and 32 Ports in 16-Bit UTOPIA Mode (continued)

Port Number	Queue Group	Queue Number	Priority	Port Group Address Bits	Priority Bits
42	21	84	High	“10101”	“00”
42	21	86	Low	“10101”	“10”
43	21	85	High	“10101”	“01”
43	21	87	Low	“10101”	“11”
44	22	88	High	“10110”	“00”
44	22	90	Low	“10110”	“10”
45	22	89	High	“10110”	“01”
45	22	91	Low	“10110”	“11”
46	23	92	High	“10111”	“00”
46	23	94	Low	“10111”	“10”
47	23	93	High	“10111”	“01”
47	23	95	Low	“10111”	“11”
48	24	96	High	“11000”	“00”
48	24	98	Low	“11000”	“10”
49	24	97	High	“11000”	“01”
49	24	99	Low	“11000”	“11”
50	25	100	High	“11001”	“00”
50	25	102	Low	“11001”	“10”
51	25	101	High	“11001”	“01”
51	25	103	Low	“11001”	“11”
52	26	104	High	“11010”	“00”
52	26	106	Low	“11010”	“10”
53	26	105	High	“11010”	“01”
53	26	107	Low	“11010”	“11”
54	27	108	High	“11011”	“00”
54	27	110	Low	“11011”	“10”
55	27	109	High	“11011”	“01”
55	27	111	Low	“11011”	“11”
56	28	112	High	“11100”	“00”
56	28	114	Low	“11100”	“10”
57	28	113	High	“11100”	“01”
57	28	115	Low	“11100”	“11”
58	29	116	High	“11101”	“00”
58	29	118	Low	“11101”	“10”
59	29	117	High	“11101”	“01”
59	29	119	Low	“11101”	“11”
60	30	120	High	“11110”	“00”
60	30	122	Low	“11110”	“10”
61	30	121	High	“11110”	“01”
61	30	123	Low	“11110”	“11”
62	31	124	High	“11111”	“00”
62	31	126	Low	“11111”	“10”
63	31	125	High	“11111”	“01”
63	31	127	Low	“11111”	“11”

11 SDRAM Interface (continued)

Of the four priority queues, the highest-priority (priority zero), lowest-delay queue may be used for constant bit rate (CBR) traffic. The other three queues, in descending order of priority, may be used for variable bit rate (VBR), available bit rate (ABR), and unspecified bit rate (UBR) traffic, respectively. Generally, as the priority becomes lower, the queues become larger because lower-priority cells are likely to accumulate while higher-priority cells are transmitted.

The size and location of each queue is programmable using the base_addressX[24:6] and end_addrX[24:6] bits in the Queue X Definition Structure, shown in Table 173. Using these base and end address registers, the size of each queue may be programmed to a minimum of four cells and up to a maximum of 512K cells in one-cell increments.

Each queue must be disabled during queue configuration by clearing the queueX_rd_en and queueX_wr_en bits in the queue X registers (addresses 0440h through 053Eh) (shown in Table 172).

Cells sent to write-disabled queues will be discarded. Cells sent to read-disabled queues will be written into the SDRAM but never transmitted to the TX UTOPIA port. Read-disabled queues may be used, as large external memory, to store cells bound for the microprocessor. The microprocessor may use as many queues as required for different type cells. Because the microprocessor reads only 2 bytes from the SDRAM per access, the cas2pre value (see Section 11.3, SDRAM Interface Timing) may need to be larger than that required for the transferring of cells only. Therefore, to maximize the bandwidth of the SDRAM for cell bus to UTOPIA traffic, restrict microprocessor access of the SDRAM to the initialization function (e.g., downloading microcode over the cell bus).

When the microprocessor increments the read pointer to read the SDRAM, it must first write the three least significant bits (rd_pntX[8:6]) of the read pointer for the appropriate queue followed by the 16 most significant bits (rd_pntX[24:9]). This order must be followed for proper operation. All queues used for microprocessor cell reception must be at least 32 cells long. (See Queue X Definition Structure, Table 173, for more information on these bits.)

11.5 SDRAM Refresh

The T8208 SDRAM interface performs CAS before RAS (CBR) refresh commands at a rate programmed in the ref_cnt bits of the refresh register (address 0410h). The value in the refresh register represents refresh cycles in SDRAM clock cycles. One refresh command is executed every ref_cnt clock cycles, on average, when the SDRAM is idle. In addition, the value programmed in the refresh lateness register (address 0412h) represents the maximum time, in programmed refresh cycles, between actual refresh cycles. If this limit is exceeded, the ref_late bit in the SDRAM interrupt status register (address 0402h) will be set, and if the ref_late interrupt is enabled, an interrupt will be generated. The ref_late indication is provided for diagnostic purposes and does not necessarily indicate a fatal error. Bit errors in the actual cell are reported in the crc8_err_even and crc8_err_odd bits of the SDRAM interrupt status register.

11 SDRAM Interface (continued)

11.6 SDRAM Throughput

The SDRAM clock frequency must be fast enough for cell transfers, to and from the SDRAM, to occur without overruns to the TX PHY FIFO. Using the default values for ras2cas, cas2pre, and pre2cmd, thirty-five clock cycles are required to transfer one cell (56 bytes) into or out of the SDRAM. The assumed efficiency rate is 90%. Therefore, the number of cells per second that can be read or written into the SDRAM is calculated using the following equation:

Cell Rate = (f_{mclk}/35 cycles per cell x 90%)

where f_{mclk} is the frequency of the SDRAM clock.

The maximum UTOPIA and cell bus bandwidths must be calculated to ensure that the SDRAM clock frequency supports these bandwidths. For example, assume that the total bandwidth on the UTOPIA bus is 64 Mbits/s and that the cell bus clock rate is 33 MHz. The maximum number of cells per second that the cell bus can send is:

$$\frac{33\ \text{MHz}}{16\ \text{cycles per cell}} = 2.06\ \text{Mcells per second.}$$

On the UTOPIA port, the total number of cells that can be sent is:

$$\frac{64\ \text{Mbits/s}}{53\ \text{bytes per cell} \times 8\ \text{bits per byte}} = 151\ \text{Kcells per second.}$$

Thus, the total number of cells per second from the cell bus and to the UTOPIA bus is 2.21 Mcells per second. For the cell rate equation above, the required SDRAM clock frequency is:

$$\frac{2.21\ \text{Mcells per second}}{0.9} * 35\ \text{cycles per cell} = 86\ \text{MHz.}$$

This is a worst-case example and assumes that all potential cells on the cell bus are going to this one device. The SDRAM frequency calculation produces a lower frequency if the actual system characteristics are considered and if the distribution of cells is controlled.

12 Traffic Management

12.1 Cell Loss Priority (CLP)

To avoid congestion, cells with their CLP bit set may be automatically discarded upon reception at the TX PHY FIFO or upon reception at a queue in the SDRAM. The cells are discarded if the TX PHY FIFO or SDRAM queue is filled beyond the programmed limit and this feature is enabled.

For the TX PHY FIFO, this limit is programmed in the clp_fill_limit bits of the main configuration/control register (address 0110h). The feature is enabled when the cell_drop_en bit in the main configuration/control register (address 0110h) is set.

For the SDRAM queues, this limit is programmed for each queue (X) in the clp_fillX[24:9] and clp_fillX[8:6] bits in Table 173. The feature is enabled when the queueX_clp_en bit in the queue X registers (address 0440h through 053Eh) is set. When a received cell exceeds the CLP fill level for a queue, the T8208 sets the corresponding queueX_clp_lim status bit in the queue X registers. If the fill level is set to zero, the corresponding queueX_clp_lim bit is set by the first received cell for the queue. Any fill greater than zero has an inherent inaccuracy of seven cells; therefore, a fill limit of eight or less is not meaningful. The number of cells in each queue may be determined by reading the value of the read and write pointers for the specific queue.

12.2 Forward Explicit Congestion Notification (FECN)

The T8208 supports FECN for data cells using the explicit forward congestion indication (EFCI) bit in the cell header PTI. If enabled, FECN indicates cells that have encountered congestion by setting their EFCI bit. The T8208 sets the EFCI bit in cells that leave a queue that is filled beyond the limit programmed in the fecn_fillX[24:9] and fecn_fillX[8:6] bits. The T8208 only sets the EFCI bit in cells when the function is enabled by the queueX_fecn_en bit in the queue X registers (address 0440h through 053Eh). When a received cell exceeds the FECN fill level for a queue, the T8208 sets the corresponding queueX_fecn_lim status bit in the queue X registers. If the fill level is set to zero, the corresponding queueX_fecn_lim bit is set by the first received cell for the queue. Any fill greater than zero has an inherent inaccuracy of seven cells; therefore, a fill limit of eight or less is not meaningful. The number of cells in each queue may be determined by reading the value of the read and write pointers for the specific queue.

12 Traffic Management (continued)

12.3 Partial Packet Discard (PPD)

Partial packet discard (PPD) is accomplished through the cooperation of the T8208 (source), which places the cell on the cell bus and the T8208 (destination), which receives the cell from the bus. The source T8208 uses its translation RAM to place a unique ID (PPD pointer) and PPD enable bit in the cell for each AAL5 connection. The PPD pointer and PPD enable bit may consist of any bit in the first 64 bits of the bus cell (cell bus routing header, tandem routing header, and ATM cell header) and are created at connection establishment.

The destination T8208 uses the PPD state memory (address 1000h to 13FEh) to track the state of AAL5 virtual channels for partial packet discard. Each bit in the memory represents one of 8192 potential AAL5 virtual channels. When the virtual channel connection is initially established, the bit in PPD state memory pointed to by the PPD pointer should have been cleared. When a cell that has its PPD enabled is discarded, the bit pointed to by the PPD pointer becomes set. Once this bit is set, successive cells with the same PPD pointer will be discarded until the last cell is received. The last cell is identified using the SDU-type bit in the PTI of the cell header. When the last cell of the packet is received, the virtual channel's corresponding bit in the PPD state memory is automatically cleared, and the last cell is transmitted.

The ppd_en_sel[5:0] bits in the PPD information 1 register specify which of the bus cell's first 64 bits (cell bus routing header, tandem routing header, and ATM cell header) enable PPD. PPD is enabled when the associated bit in the headers is one. The partial packet discard bits specify which of the bus cell's first 64 bits are used to create the PPD pointer. These pointer bits are ppd_pnt0_sel[5:0] through ppd_pnt12_sel[5:0] in the PPD information 1 through 7 registers (addresses 0206h through 0212h). When an AAL5 virtual channel connection is initially established, its PPD bit in the PPD state memory can be cleared using the write_pul, write_val, and write_addr bits in the PPD memory write register at address 0418h.

13 JTAG Test Access Port

A 5-pin test access port, consisting of the jtag_tclk, jtag_tms, jtag_tdi, jtag_tdo, and jtag_trst signals, provides the standard interface to the test logic. The jtag_trst signal is active-low and resets the JTAG circuitry. When jtag_trst is high, the JTAG interface is enabled. If the JTAG port is not used, jtag_trst should be tied low.

JTAG may be used only to test the inputs, outputs, and their connection to the printed-wiring board. In JTAG, serial bit patterns are shifted into the device through the jtag_tdi pin, and the results can be observed at the I/O and at the corresponding JTAG serial output, jtag_tdo. Since this JTAG conforms to the JTAG standard, the jtag_tdi and jtag_tdo may be linked to the JTAG port of other devices for systemic testing. The boundary-scan description language may be found on the Agere website.

13.1 Instruction Register

The instruction register (IR) is 3 bits in length. The instructions are defined in Table 22.

Table 22. Instruction Register

Instruction	Binary Code	Description
EXTEST	“000”	Places the boundary-scan register in extest mode.
SAMPLE	“001”	Places the boundary-scan register in sample mode.
HIGHZ	“010”	Places the boundary-scan register in highz mode.
RUNBIST	“100”	Places the boundary-scan register in runbist mode.
IDCODE	“101”	Places the boundary-scan register in idcode mode.
BYPASS	“011,” “110,” “111”	Places the bypass register in the scan chain.

13 JTAG Test Access Port (continued)

13.2 Boundary-Scan Register

The boundary-scan register (BSR) is 245 bits in length. Table 23 gives descriptions of each cell in the boundary-scan chain beginning with the least significant bit.

Table 23. Boundary-Scan Register Descriptions

Boundary-Scan Register Bit	Name	Pin Name	Description
0	TR_D_OE	—	TR_D(0:7) are inputs when TR_D_OE = 0.
1	TR_CONT_OE	—	TR_OE_N, TR_WE_N, TR_A(17:0), and TR_CS(1:0) are high impedance when TR_CONT_OE = 0.
2	U_RXCLAV0_OE	—	U_RXCLV0 is an input when U_RXCLAV0_OE = 0.
3	U_RXENB0_OE	—	U_RXENB(0) is an input when U_RXENB0_OE = 0.
4	U_RXENB_OE	—	U_RXENB(1:3) are inputs when U_RXENB_OE = 0.
5	U_RXADDR_OE	—	U_RXADD(0:4) are inputs when U_RXADDR_OE = 0.
6	U_RXCLK_OE	—	U_RXCLK is an input when U_RXCLK_OE = 0.
7	GPIO_OE(7)	—	GPIO(7) is an input when GPIO_OE(7) = 0.
8	GPIO_OE(6)	—	GPIO(6) is an input when GPIO_OE(6) = 0.
9	GPIO_OE(5)	—	GPIO(5) is an input when GPIO_OE(5) = 0.
10	GPIO_OE(4)	—	GPIO(4) is an input when GPIO_OE(4) = 0.
11	GPIO_OE(3)	—	GPIO(3) is an input when GPIO_OE(3) = 0.
12	GPIO_OE(2)	—	GPIO(2) is an input when GPIO_OE(2) = 0.
13	GPIO_OE(1)	—	GPIO(1) is an input when GPIO_OE(1) = 0.
14	GPIO_OE(0)	—	GPIO(0) is an input when GPIO_OE(0) = 0.
15	D_OE	—	D(7:0) are inputs when D_OE = 0.
16	CKO_OE	—	CKO is high impedance when CKO_OE = 0.
17	RDY_DTACK_N_OE	—	RDYDTACK is high impedance when RDY_DTACK_N_OE = 0.
18	DEVHIZ_N_HIGH_DRIVE	—	INT_IRQ, SD_A(11:0), SD_BS(1:0), SD_CAS_N, SD_RAS_N, and SD_WE_N are high impedance when DEVHIZ_N_HIGH_DRIVE = 0.
19	U_SHR_GNT_OE	—	U_SHR_GNT(0:1) are inputs when U_SHR_GNT_OE = 0.
20	U_TXDATA_OE	—	U_TXDAT(15:0) are high impedance when U_TXDATA_OE = 0.
21	U_TXPRTY_OE	—	U_TXPRTY is an input when U_TXPRTY_OE = 0.
22	U_TXSOC_OE	—	U_TXSOC is high impedance when U_TXSOC_OE = 0.
23	U_TXCLK_OE	—	U_TXCLK is an input when U_TXCLK_OE = 0.
24	U_TXADDR_OE	—	U_TXADD(4:0) are inputs when U_TXADDR_OE = 0.
25	U_TXENB_OE	—	U_TXENB(3:1) are high impedance when U_TXENB_OE = 0.
26	U_TXENB0_OE	—	U_TXENB0 is an input when U_TXENB0_OE = 0.
27	U_TXCLAV0_OE	—	U_TXCLV0 is an input when U_TXCLAV0_OE = 0.

13 JTAG Test Access Port (continued)

Table 23. Boundary-Scan Register Descriptions (continued)

Boundary-Scan Register Bit	Name	Pin Name	Description
28	SD_CLK_OE	—	SD_CLK is an input when SD_CLK_OE = 0.
29	SD_D_OE	—	SD_D(15:0) are inputs when SD_D_OE = 0.
30	CB_GEN_OE	—	CB_GEN_RC and CB_GEN_WC are inputs when CB_GEN_OE = 0.
31	U_SHR_REQ_OE	—	U_SHR_REQ(0:3) are inputs when U_SHR_REQ_OE = 0.
32-39	TR_D(0:7)	tr_d[0:7]	Bidirectional.
40-41	TR_CS(0:1)	tr_cs*[0:1]	3-statable output.
42	TR_OE_N	tr_oe*	3-statable output.
43	TR_WE_N	tr_we*	3-statable output.
44-61	TR_A(0:17)	tr_a[0:17]	3-statable output.
62	U_RXCLV0	u_rxclav[0]	Bidirectional.
63-65	U_RXCLV(1:3)	u_rxclav[1:3]	Input.
66	U_RXENB(0)	u_rxenb*[0]	Bidirectional.
67-69	U_RXENB(1:3)	u_rxenb*[1:3]	Bidirectional.
70-74	U_RXADD(0:4)	u_rxaddr[0:4]	Bidirectional.
75	U_RXCLK	T1	Bidirectional.
76	U_RXSOC	u_rxsoc	Input.
77	U_RXPRTY	u_rxprty	Input.
78-93	U_RXDAT(0:15)	u_rxdata[0:15]	Input.
94	GPIO(7)	gpio[7]	Bidirectional.
95	GPIO(6)	gpio[6]	Bidirectional.
96	GPIO(5)	gpio[5]	Bidirectional.
97	GPIO(4)	gpio[4]	Bidirectional.
98	GPIO(3)	gpio[3]	Bidirectional.
99	GPIO(2)	gpio[2]	Bidirectional.
100	GPIO(1)	gpio[1]	Bidirectional.
101	GPIO(0)	gpio[0]	Bidirectional.
102-109	A(7:0)	a[7:1] a[0]/ale	Input.
110-117	D(7:0)	d[7:0]	Bidirectional.
118	CKO	cko	3-statable output.
119	CKOE	cko_e	Input.
120	RDYDTACK	rdy_dtack*	3-statable output.
121	INT_IRQ	int_irq*	3-statable output.
122	SEL_N	sel*	Input.

13 JTAG Test Access Port (continued)

Table 23. Boundary-Scan Register Descriptions (continued)

Boundary-Scan Register Bit	Name	Pin Name	Description
123	WR_N	wr*_ds*	Input.
124	RD_WR_N	rd*_rw*	Input.
125	MOTO	mot_sel	Input.
126	MUX	mux	Input.
127	RESET_N	reset*	Input.
128-129	U_SHR_GNT(0:1)	u_shr_gnt(0:1)	Bidirectional.
130-145	U_TXDAT(15:0)	u_txdata[15:0]	3-statable output.
146	U_TXPRTY	u_txprty	Bidirectional.
147	U_TXSOC	u_txsoc	3-statable output.
148	U_TXCLK	u_txclk	Bidirectional.
149-153	U_TXADD(4:0)	u_txaddr[4:0]	Bidirectional.
154-156	U_TXENB(3:1)	u_txenb*[3:1]	3-statable output.
157	U_TXENB0	u_txenb*[0]	Bidirectional.
158-160	U_TXCLV(3:1)	u_txclav[3:1]	Input.
161	U_TXCLV0	u_txclav[0]	Bidirectional.
162-173	SD_A(11:0)	sd_a[11:0]	3-statable output.
174	SD_CLK	sd_clk	Bidirectional.
175-176	SD_BS(1:0)	sd_bs[1:0]	3-statable output.
177	SD_RAS_N	sd_ras*	3-statable output.
178	SD_CAS_N	sd_cas*	3-statable output.
179	SD_WE_N	sd_we*	3-statable output.
180-195	SD_D(15:0)	sd_d[15:0]	Bidirectional.
196-200	UA_N(4:0)	ua*[4:0]	Input.
201	ENARB	arb_enb*	Input.
202	CB_DISBL	cb_disable*	Input.
203	CB_ACK_N	cb_ack*	Bidirectional.
204	CB_F_N	cb_fs*	Bidirectional.
205-220	CB_D_N(0:15)	cb_d*[0:15]	Bidirectional.
221	CB_WC_N	cb_wc*	Input.
222	CB_RC_N	cb_rc*	Input.
223-238	CB_D_N(16:31)	cb_d*[16:31]	Bidirectional.
239	CB_GEN_RC_N	cb_gen_rc*	Bidirectional.
240	CB_GEN_WC_N	cb_gen_wc*	Bidirectional.
241-244	U_SHR_REQ(0:3)	u_shr_req(0:3)	Bidirectional.

14 Registers

The T8208 has two distinct memory spaces: the direct memory access registers and the extended memory registers. The direct memory access registers are directly addressed 8-bit (byte) registers and are mapped between addresses 00h and FFh. The extended memory registers are indirectly addressed and mapped between addresses 0100h and 3FFFFFEh. The extended memory registers are mapped into three major blocks: the main registers, the UTOPIA registers, and the SDRAM registers. They contain the SDRAM memory, the translation RAM, internal memories, and the device's configuration, status, and control registers. Extended memory registers are 16 bits wide, and all accesses to the extended memory registers are executed internally as 16 bits. Direct memory access registers are located in Section 14.2, Direct Memory Access Registers, and extended memory registers are located in Section 14.3, Extended Memory Registers.

14.1 Register Types

Read/Write (RW): These registers may be written or read.

Read Only (RO): These registers may only be read.

Read-Only Latch (ROL): The read-only latch is used for interrupt status registers. Reading a read-only latch register has no effect on the contents. To clear a bit set in an ROL register, a one must be written to the bit. Writing a zero to the bit has no effect. If the corresponding interrupt enable bit is set, an interrupt will be continuously generated until the bit in the ROL register is cleared.

Write Only (WO): These registers may only be written. The write only registers in the T8208 are a pulse type. When they are written to one, they generate a pulse internally for one clock cycle and then return to zero.

Table 24. Register Map

Register Name	Address (h)	Reference Page
Direct Configuration/Control Register (DCCR)	28h	93
Interrupt Service Request (ISREQ)	29h	94
mclk PLL Configuration 0 (MPLLCF0)	2Ah	94
mclk PLL Configuration 1 (MPLLCF1)	2Bh	95
GTL+ Slew Rate Configuration (GTLSRCF)	2Eh	95
GTL+ Control (GTLCNTRL)	2Fh	96
Extended Memory Address 1 (Little Endian) (EMA1_LE)	30h	97
Extended Memory Address 2 (Little Endian) (EMA2_LE)	31h	97
Extended Memory Address 3 (Little Endian) (EMA3_LE)	32h	97
Extended Memory Address 4 (Little Endian) (EMA4_LE)	33h	97
Extended Memory Access (Little Endian) (EMA_LE)	34h	97
Extended Memory Data Low (Little Endian) (EMDL_LE)	36h	98
Extended Memory Data High (Little Endian) (EMDH_LE)	37h	98
Extended Memory Address 4 (Big Endian) (EMA4_BE)	30h	99
Extended Memory Address 3 (Big Endian) (EMA3_BE)	31h	99
Extended Memory Address 2 (Big Endian) (EMA2_BE)	32h	99
Extended Memory Address 1 (Big Endian) (EMA1_BE)	33h	99
Extended Memory Access (Big Endian) (EMA_BE)	34h	100
Extended Memory Data High (Big Endian) (EMDH_BE)	36h	100
Extended Memory Data Low (Big Endian) (EMDL_BE)	37h	100
GPIO Output Enable (GPIO_OE)	39h	101
GPIO Output Value (GPIO_OV)	3Bh	101
GPIO Input Value (GPIO_IV)	3Dh	101
Control Cell Receive Direct Memory (CCRXDM)	5Ch to 93h	102
Control Cell Transmit Direct Memory (CCTXDM)	A0h to D7h	102
PHY Port 0 and Control Cells Multicast Direct Memory (PP0MDM)	E0h to FFh	103

14 Registers (continued)

Table 24. Register Map (continued)

Register Name	Address (h)	Reference Page
Main Configuration 1 (MCF1)	0100h	104
Main Interrupt Status 1 (MIS1)	0102h	105
Main Interrupt Enable 1 (MIE1)	0104h	106
TX UTOPIA Clock Configuration (TXUCCF)	010Ch	107
RX UTOPIA Clock Configuration (RXUCCF)	010Eh	108
Main Configuration/Control (MCFCT)	0110h	109
Main Configuration 2 (MCF2)	0112h	110
UTOPIA Configuration (UCF)	0114h	113
Main Configuration 3 (MCF3)	0116h	113
UTOPIA Configuration 5 (UCF5)	0118h	114
UTOPIA Configuration 4 (UCF4)	011Ah	114
UTOPIA Configuration 3 (UCF3)	011Ch	114
UTOPIA Configuration 2 (UCF2)	011Eh	114
Extended LUT Control (ELUTCN)	0120h	115
Generated Cell Bus Clocks Control Register (GCBCCR)	0122h	116
RX PHY FIFO Thresholds to Change Cell Bus Request Priority (RXPFTCRP)	0126h	118
Enable Request on Upper Backplane (ERUB)	012Ch	119
Enable Request on Lower Backplane (ERLB)	012Eh	119
Cell Bus Configuration/Status (CBCFS)	0130h	120
Main Interrupt Status 2 (MIS2)	0132h	121
Main Interrupt Enable 2 (MIE2)	0134h	122
Loopback (LB)	0136h	122
Extended LUT Configuration (ELUTCF)	0138h	122
Misrouted Cell LUT 3 (MLUT3)	013Ch	123
Misrouted Cell LUT 2 (MLUT2)	013Eh	123
Misrouted Cell LUT 1 (MLUT1)	0140h	123
Misrouted Cell LUT 0 (MLUT0)	0142h	123
Misrouted Cell LUT 4 (MLUT4)	0144h	124
Misrouted Cell Header High (MCHH)	0146h	124
Misrouted Cell Header Low (MCHL)	0148h	124
HEC Interrupt Status 3 (HIS3)	0300h	125
HEC Interrupt Status 2 (HIS2)	0302h	125
HEC Interrupt Status 1 (HIS1)	0304h	125
HEC Interrupt Status 0 (HIS0)	0306h	125
HEC Interrupt Enable 3 (HIE3)	0308h	126
HEC Interrupt Enable 2 (HIE2)	030Ah	126
HEC Interrupt Enable 1 (HIE1)	030Ch	126
HEC Interrupt Enable 0 (HIE0)	030Eh	126
HEC Interrupt Enable 3 (HIE3)	0308h	126
HEC Interrupt Enable 2 (HIE2)	030Ah	126
HEC Interrupt Enable 1 (HIE1)	030Ch	126
HEC Interrupt Enable 0 (HIE0)	030Eh	126
LUT Interrupt Service Request 3 (LUTISR3)	0310h	127
LUT Interrupt Service Request 2 (LUTISR2)	0312h	127
LUT Interrupt Service Request 1 (LUTISR1)	0314h	127
LUT Interrupt Service Request 0 (LUTISR0)	0316h	127

14 Registers (continued)

Table 24. Register Map (continued)

Register Name	Address (h)	Reference Page
LUT X Configuration/Status (LUTXCFS)	0320h to 039Eh	128
Master Queue 7 (MQ7)	0150h	130
Master Queue 6 (MQ6)	0152h	130
Master Queue 5 (MQ5)	0154h	130
Master Queue 4 (MQ4)	0156h	131
Master Queue 3 (MQ3)	0158h	131
Master Queue 2 (MQ2)	015Ah	131
Master Queue 1 (MQ1)	015Ch	132
Master Queue 0 (MQ0)	015Eh	132
Slave Queue 7 (SQ7)	0160h	133
Slave Queue 6 (SQ6)	0162h	133
Slave Queue 5 (SQ5)	0164h	134
Slave Queue 4 (SQ4)	0166h	134
Slave Queue 3 (SQ3)	0168h	134
Slave Queue 2 (SQ2)	016Ah	135
Slave Queue 1 (SQ1)	016Ch	135
Slave Queue 0 (SQ0)	016Eh	135
TX PHY FIFO Routing 7 (TXPFR7)	0170h	136
TX PHY FIFO Routing 6 (TXPFR6)	0172h	137
TX PHY FIFO Routing 5 (TXPFR5)	0174h	138
TX PHY FIFO Routing 4 (TXPFR4)	0176h	139
TX PHY FIFO Routing 3 (TXPFR3)	0178h	140
TX PHY FIFO Routing 2 (TXPFR2)	017Ah	141
TX PHY FIFO Routing 1 (TXPFR1)	017Ch	142
TX PHY FIFO Routing 0 (TXPFR0)	017Eh	143
Global Bypass SDRAM Control Register (GBSCR)	01B0h	144
Bypass SDRAM Service Request Register (BSSR)	01BEh	145
Bypass SDRAM Queue Interrupt Status Register 0 (BSQISR0)	01C0h	147
Bypass SDRAM Queue Interrupt Status Register 1 (BSQISR1)	01C2h	148
Bypass SDRAM Queue Interrupt Status Register 2 (BSQISR2)	01C4h	149
Bypass SDRAM Queue Interrupt Status Register 3 (BSQISR3)	01C6h	150
Bypass SDRAM Queue Interrupt Status Register 4 (BSQISR4)	01C8h	151
Bypass SDRAM Queue Interrupt Status Register 5 (BSQISR5)	01CAh	152
Bypass SDRAM Queue Interrupt Status Register 6 (BSQISR6)	01CCh	153
Bypass SDRAM Queue Interrupt Status Register 7 (BSQISR7)	01CEh	154
Bypass SDRAM Queue Interrupt Status Register 8 (BSQISR8)	01D0h	155
Bypass SDRAM Queue Interrupt Status Register 9 (BSQISR9)	01D2h	156
Bypass SDRAM Queue Interrupt Status Register 10 (BSQISR10)	01D4h	157
Bypass SDRAM Queue Interrupt Status Register 11 (BSQISR11)	01D6h	158
Bypass SDRAM Queue Interrupt Status Register 12 (BSQISR12)	01D8h	159
Bypass SDRAM Queue Interrupt Status Register 13 (BSQISR13)	01DAh	160
Bypass SDRAM Queue Interrupt Status Register 14 (BSQISR14)	01DCh	161
Bypass SDRAM Queue Interrupt Status Register 15 (BSQISR15)	01DEh	162

14 Registers (continued)

Table 24. Register Map (continued)

Register Name	Address (h)	Reference Page
Routing Information 1 (RI1)	0200h	163
Routing Information 2 (RI2)	0202h	164
Routing Information 3 (RI3)	0204h	165
PPD Information 1 (PPDI1)	0206h	166
PPD Information 2 (PPDI2)	0208h	167
PPD Information 3 (PPDI3)	020Ah	168
PPD Information 4 (PPDI4)	020Ch	169
PPD Information 5 (PPDI5)	020Eh	170
PPD Information 6 (PPDI6)	0210h	171
PPD Information 7 (PPDI7)	0212h	172
Routing Information 4 (RI4)	0214h	173
PPD Memory Write (PPDMW)	0418h	174
PHY Port X Transmit Count Structure (PPXTXCNT)	0600h to 06FEh	175
PHY Port X Receive Count Structure (PPXRXCNT)	4000h to 40FEh	176
PHY Port X Configuration Structure (PPXCF)	4200h to 42FEh	176
SDRAM Control (SCT)	0400h	179
SDRAM Interrupt Status (SIS)	0402h	179
SDRAM Interrupt Enable (SIE)	0404h	179
SDRAM Configuration (SCF)	0408h	180
Refresh (RFRSH)	0410h	181
Refresh Lateness (RFRSHL)	0412h	181
Idle State 1 (IS1)	0420h	181
Idle State 2 (IS2)	0422h	181
Manual Access State 1 (MAS1)	0424h	182
Manual Access State 2 (MAS2)	0426h	182
SDRAM Interrupt Service Request 7 (SISR7)	0430h	183
SDRAM Interrupt Service Request 6 (SISR6)	0432h	183
SDRAM Interrupt Service Request 5 (SISR5)	0434h	183
SDRAM Interrupt Service Request 4 (SISR4)	0436h	183
SDRAM Interrupt Service Request 3 (SISR3)	0438h	183
SDRAM Interrupt Service Request 2 (SISR2)	043Ah	184
SDRAM Interrupt Service Request 1 (SISR1)	043Ch	184
SDRAM Interrupt Service Request 0 (SISR0)	043Eh	184
Queue X (QX)	0440h to 053Eh	185
Queue X Definition Structure (QXDEF)	2000h to 2FFEh	187
Control Cell Receive Extended Memory (CCRXEM)	07FCh to 0832h	190
Control Cell Transmit Extended Memory (CCTXEM)	0900h to 0936h	190
PHY Port 0 and Control Cells Multicast Extended Memory (PP0MEM)	0C00h to 0C1Eh	191
PHY Port X Multicast Memory (PPXMM)	0C20h to 0FFEh	192
PPD Memory (PPDM)	1000h to 13FEh	193
Queue X Dropped Cell Count (QXDCC)	3000h to 31FEh	194
Translation RAM Memory (TRAM)	100000h to 17FFFEh	197
SDRAM (SDRAM)	2000000h to 3FFFFFEh	197

14 Registers (continued)

14.2 Direct Memory Access Registers

The direct memory access registers are the only registers that can be directly addressed. These registers provide some status and initial control of the device. In addition, the direct memory access register set includes some extended memory access registers, which are used to indirectly access the extended memory registers. All undefined addresses in the direct memory access registers' memory map, 00h to FFh, are reserved and should not be accessed.

Table 25. Identification 0 (IDNT0) (00h)

Name	Bit Pos.	Type	Reset	Description
Device ID 0	7:0	RO	4Fh	Device Identification 0.

Table 26. Identification 1 (IDNT1) (01h)

Name	Bit Pos.	Type	Reset	Description
Device ID 1	7:0	RO	08h	Device Identification 1.

Table 27. Identification 2 (IDNT2) (02h)

Name	Bit Pos.	Type	Reset	Description
Revision	7:0	RO	RN[1]	Revision Number.

1. RN represents the current revision number of the device.

14 Registers (continued)

Table 28. Direct Configuration/Control Register (DCCR) (28h)

Name	Bit Pos.	Type	Reset	Description
cyc_per_acc	0	RW	0	**Cycles Per Access.** This bit is used to indicate the number of cycles per read/write to the translation RAM. '0' = 2 mclk cycles. '1' = 3 mclk cycles.
srst_reg*	1	RW	0	**Software Reset Main Registers.** A logic level zero on this bit resets the main registers only. The direct memory access registers (including this one) are not affected by this reset. This bit must be '0' while the mclk PLL configuration 0 and 1 registers are being modified. Active-low.
srst*	2	RW	0	**Software Reset**. A logic level zero on this bit resets the entire device except the direct memory registers and the main registers. This bit must be '0' while the mclk PLL configuration 0 and 1 registers are being modified and clocks are not present. Active-low.
Reserved	3	RO	0	**Reserved.** This bit must be programmed to '1.'
rplc_gfc	4	RW	0	**Replace GFC.** If this bit is '1' and the device is in UNI mode, the GFC field of incoming cells will be replaced during a VPI-VCI translation. If this bit is '0' and the device is in UNI mode, the GFC field will be left untouched. When the device is in NNI mode or when a VPI only translation is performed, this bit has no effect.
big_end	5	RW	0	**Big Endian.** If this bit is '0,' register fields in the direct address space, 30h to 37h, will be in little-endian format. If '1,' fields in the direct address space, 30h to 37h, will be in big-endian format.
Reserved	7:6	RW	0	**Reserved.** These bits must be written to '0.'

14 Registers (continued)

Table 29. Interrupt Service Request (ISREQ) (29h)

Name	Bit Pos.	Type	Reset	Description
Reserved	0	RO	0	**Reserved.**
int_serv_mainreg	1	RO	0	**Interrupt Service Request for Main Registers.** When this bit is '1,' an interrupt in the main register group of the extended memory registers needs servicing. The control cell sent and control cell available status bits do not affect this bit. Only enabled interrupts will cause this bit to become set.
int_serv_sdramreg	2	RO	0	**Interrupt Service Request for SDRAM Registers.** When this bit is '1,' an interrupt in the SDRAM register group of the extended memory registers needs servicing. Only enabled interrupts will cause this bit to become set.
int_serv_utopiareg	3	RO	0	**Interrupt Service Request for UTOPIA Registers.** When this bit is '1,' an interrupt in the UTOPIA register group of the extended memory registers needs servicing. Only enabled interrupts will cause this bit to become set.
int_serv _sdrambypreg	4	RO	0	**Interrupt Service Request for SDRAM Bypass Registers.** When this bit is '1,' an interrupt in the SDRAM bypass register group of the extended memory registers needs servicing. Only enabled interrupts will cause this bit to become set.
ctrl_cell_sent_sr	5	RO	0	**Control Cell Sent Interrupt Service Request.** When this bit is '1,' the control cell sent interrupt in the main interrupt status 1 register needs servicing. The corresponding interrupt does not need to be enabled for this bit to become set.
ctrl_cell_av_sr	6	RO	0	**Control Cell Available Interrupt Service Request.** When this bit is '1,' the control cell available interrupt in the main interrupt status 1 register needs servicing. The corresponding interrupt does not need to be enabled for this bit to become set.
Reserved	7	RO	0	**Reserved.**

Table 30. mclk PLL Configuration 0 (MPLLCF0) (2Ah)

Name	Bit Pos.	Type	Reset	Description
lf[3:0]	3:0	RW	0	**Loop Filter.** See Section 5, PLL Configuration, for information on these bits.
Reserved	5:4	RO	0	**Reserved.**
bypb	6	RW	0	**Bypass PLL.** If this bit is '0,' the PLL is bypassed. If '1,' the output of the PLL supplies mclk.
pllen	7	RW	0	**PLL Enable.** If this bit is '1,' the PLL is enabled. If '0,' the PLL is disabled.

14 Registers (continued)

Table 31. mclk PLL Configuration 1 (MPLLCF1) (2Bh)

Name	Bit Pos.	Type	Reset	Description
pll_m[4:0]	4:0	RW	0	**PLL M Count Value.** See Section 5, PLL Configuration, for information on these bits.
pll_n[2:0]	7:5	RW	0	**PLL N Count Value.** See Section 5, PLL Configuration, for information on these bits.

Table 32. GTL+ Slew Rate Configuration (GTLSRCF) (2Eh)

Name	Bit Pos.	Type	Reset	Description
slew_rate[2:0]	2:0	RW	4h	**GTL+ Slew Rate Control [2:0].** The slew rates of the GTL+ (cell bus) output signals are controlled by these bits. The minimum slew rate is 0.9 ns and the maximum slew rate is 3.3 ns. “000” = Fastest slew rate “001” “010” “011” = Nominal slew rate (on fast side) “100” = Nominal slew rate (on slow side) “101” “110” “111” = Slowest slew rate
Reserved	3	RW	1	**Reserved.** Program to ‘1.’
Reserved	5:4	RW	0	**Reserved.** Program to ‘0.’
select_gtl_clocks	6	RW	1	**Select GTL+ Clocks.** When this bit is cleared to ‘0,’ the cell bus clocks that clock the internal cell bus interface and cell bus circuitry are no longer sourced from the GTL+ input (pins A10 and B10) but rather from the generated clocks (pins A3 and B4), if they are enabled (bit 10 in 0122h = 1). If these generated clocks are disabled (bit 10 in 0122h = 0), then pins A3 and B4 become 3-stated. When this bit is set to ‘1,’ the T8208 will receive the cell bus clocks from the GTL+ pins A10 and B10. **Note:** Due to the inherent propagation delay between the clocks that drive the cell bus logic of the generating device and the other devices on the backplane, it is recommended that customers set bit 6 in register 2Eh to ‘1’ and set bit 10 in register 0122h to ‘1’ and route these generated clocks (through a GTL+ driver) back to the cb_wc* and cb_rc* pins (pins A10 and B10, respectively).
dig_lpbk_en	7	RW	0	**Digital Loopback Enable.** This bit must be set to ‘1’ **and** bit 2 (GTLTPDN) of register 2Fh must be cleared to ‘0’ to enable a digital loopback (loopback before the cell bus). The digital loopback allows loopback of **all** cells without requiring the cell to be sent to the cell bus. The output of the cell bus output FIFO is connected to the input of the cell bus input FIFO internally, so that the cells do not have to go through the GTL+ buffers. The cells being received on the RX UTOPIA should still be addressed properly with the in-range VPI/VCI and routing information for the device to be able to loopback the cells. When this bit is cleared to ‘0,’ there is no digital loopback.

14 Registers (continued)

Table 33. GTL+ Control (GTLCNTRL) (2Fh)

Name	Bit Pos.	Type	Reset	Description
Reserved	0	R	1	**Reserved.** Program to ‘1.’
GTLRPDN	1	RW	1	**GTL+ Receive Powerdown.** When this bit is cleared to ‘0,’ the GTL+ receivers on the cell bus pins are powered down. Under this condition, no cells can be received from the backplane. When this bit is set to ‘1,’ the GTL+ receivers are powered up and cells are received from the backplane.
GTLTPDN	2	RW	1	**GTL+ Transmit Powerdown.** When this bit is cleared to ‘0,’ the GTL+ transmitters on the cell bus pins are powered down. Under this condition, no cells can be transmitted to the backplane. When this bit is set to ‘1,’ the GTL+ transmitters are powered up and cells are transmitted to the backplane.
Reserved	4:3	R	0	**Reserved.** Program to ‘0.’
Reserved	5	R	1	**Reserved.** Program to ‘1.’
Reserved	7:6	R	0	**Reserved.** Program to ‘0.’

14 Registers (continued)

14.2.1 Little-Endian Format (big_end = 0) for Extended Memory Access Registers 30h—37h

Table 34. Extended Memory Address 1 (Little Endian) (EMA1_LE) (30h)

Name	Bit Pos.	Type	Reset	Description
Reserved	4:0	RO	0	**Reserved.**
ext_a[8:6]	7:5	RW	0	**Extended Access Address [8:6].** This extended access register points to words.

Table 35. Extended Memory Address 2 (Little Endian) (EMA2_LE) (31h)

Name	Bit Pos.	Type	Reset	Description
ext_a[16:9]	7:0	RW	0	**Extended Access Address [16:9].** This extended access register points to words.

Table 36. Extended Memory Address 3 (Little Endian) (EMA3_LE) (32h)

Name	Bit Pos.	Type	Reset	Description
ext_a[24:17]	7:0	RW	0	**Extended Access Address [24:17].** This extended access register points to words.

Table 37. Extended Memory Address 4 (Little Endian) (EMA4_LE) (33h)

Name	Bit Pos.	Type	Reset	Description
ext_a[25]	0	RW	0	**Extended Access Address [25].** This extended access register points to words.
Reserved	7:1	RO	0	**Reserved.**

Table 38. Extended Memory Access (Little Endian) (EMA_LE) (34h)

Name	Bit Pos.	Type	Reset	Description
ext_a[5:1]	4:0	RW	0	**Extended Access Address [5:1].** This extended access register points to words. ext_a[0] is hardwired to ‘0.’
ext_we[1:0]	6:5	RW	0	**Extended Access Write Enable.** These bits are active-high write enables for word accesses. If both bits are low, a read is performed. If ext_we[1] is high, the contents of ext_d[15:8] is written, and if ext_we[0] is high, the contents of ext_d[7:0] is written. If both bits are high, both data bytes are written.
ext_strt_acc	7	RW	0	**Start Access to Extended Memory.** Write a ‘1’ to this bit to start the access to the extended memory registers. This bit is automatically cleared when the access is complete.

14 Registers (continued)

Table 39. Extended Memory Data Low (Little Endian) (EMDL_LE) (36h)

Name	Bit Pos.	Type	Reset	Description
ext_d[7:0]	7:0	RW	0	**Extended Access Data Low.** The least significant byte of data to be written to extended memory is written here before the extended write begins. The least significant byte of data read from extended memory is available here after the extended read is complete.

Table 40. Extended Memory Data High (Little Endian) (EMDH_LE) (37h)

Name	Bit Pos.	Type	Reset	Description
ext_d[15:8]	7:0	RW	0	**Extended Access Data High.** The most significant byte of data to be written to extended memory is written here before the extended write begins. The most significant byte of data read from extended memory is available here after the extended read is complete.

14 Registers (continued)

14.2.2 Big-Endian Format (big_end = 1) for Extended Memory Access Registers 30h—37h

Table 41. Extended Memory Address 4 (Big Endian) (EMA4_BE) (30h)

Name	Bit Pos.	Type	Reset	Description
ext_a[25]	0	RW	0	**Extended Access Address [25].** This extended access register points to words.
Reserved	7:1	RO	0	**Reserved.**

Table 42. Extended Memory Address 3 (Big Endian) (EMA3_BE) (31h)

Name	Bit Pos.	Type	Reset	Description
ext_a[24:17]	7:0	RW	0	**Extended Access Address [24:17].** This extended access register points to words.

Table 43. Extended Memory Address 2 (Big Endian) (EMA2_BE) (32h)

Name	Bit Pos.	Type	Reset	Description
ext_a[16:9]	7:0	RW	0	**Extended Access Address [16:9].** This extended access register points to words.

Table 44. Extended Memory Address 1 (Big Endian) (EMA1_BE) (33h)

Name	Bit Pos.	Type	Reset	Description
Reserved	4:0	RO	0	**Reserved.**
ext_a[8:6]	7:5	RW	0	**Extended Access Address [8:6].** This extended access register points to words.

14 Registers (continued)

Table 45. Extended Memory Access (Big Endian) (EMA_BE) (34h)

Name	Bit Pos.	Type	Reset	Description
ext_a[5:1]	4:0	RW	0	**Extended Access Address [5:1].** This extended access register points to words. ext_a[0] is hardwired to '0.'
ext_we[1:0]	6:5	RW	0	**Extended Access Write Enable.** These bits are active-high write enables for word accesses. If both bits are low, a read is performed. If ext_we[1] is high, the contents of ext_d[15:8] is written, and if ext_we[0] is high, the contents of ext_d[7:0] is written. If both bits are high, both data bytes are written.
ext_strt_acc	7	RW	0	**Start Access to Extended Memory.** Write a '1' to this bit to start the access to the extended memory registers. This bit is automatically cleared when the access is complete.

Table 46. Extended Memory Data High (Big Endian) (EMDH_BE) (36h)

Name	Bit Pos.	Type	Reset	Description
ext_d[15:8]	7:0	RW	0	**Extended Access Data High.** The most significant byte of data to be written to extended memory is written here before the extended write begins. The most significant byte of data read from extended memory is available here after the extended read is complete.

Table 47. Extended Memory Data Low (Big Endian) (EMDL_BE) (37h)

Name	Bit Pos.	Type	Reset	Description
ext_d[7:0]	7:0	RW	0	**Extended Access Data Low.** The least significant byte of data to be written to extended memory is written here before the extended write begins. The least significant byte of data read from extended memory is available here after the extended read is complete.

14 Registers (continued)

14.2.3 General-Purpose I/O Control Registers

Table 48. GPIO Output Enable (GPIO_OE) (39h)

Name	Bit Pos.	Type	Reset	Description
GPIO_oe[7:0]	7:0	RW	0	**GPIO Output Enable.** If this bit is set to ‘1,’ the corresponding GPIO pin is an output. If cleared to ‘0,’ the corresponding GPIO pin is an input.

Table 49. GPIO Output Value (GPIO_OV) (3Bh)

Name	Bit Pos.	Type	Reset	Description
GPIO_out[7:0]	7:0	RW	0	**GPIO Output Buffer.** Output bits for the GPIO[7:0] pins are written to this buffer. A bit in this buffer is only written to the pin if the corresponding output enable bit is high.

Table 50. GPIO Input Value (GPIO_IV) (3Dh)

Name	Bit Pos.	Type	Reset	Description
GPIO_in[7:0]	7:0	RO	0	**GPIO Input Buffer.** This buffer contains the values at the GPIO[7:0] pins.

14 Registers (continued)

14.2.4 Control Cells

Table 51. Control Cell Receive Direct Memory (CCRXDM) (5Ch to 93h)

The control cell receive memory may also be accessed from extended memory. See Table 174.

Name	Offset	Type	Reset	Description
cell_bus_routing_header[15:8]	00h	RO	X	These 56 bytes are the control cell received from the cell bus. This memory space in direct memory is a shadow of the control cell receive extended memory. When present, the control cell should be read from this direct memory space.
cell_bus_routing_header[7:0]	01h			
tandem_routing_header[15:8]	02h			
tandem_routing_header[7:0]	03h			
header[31:24]	04h			
header[23:16]	05h			
header[15:8]	06h			
header[7:0]	07h			
payload_byte0	08h			
payload_byte1	09h			
. . .	. . .			
payload_byte46	36h			
payload_byte47	37h			

Table 52. Control Cell Transmit Direct Memory (CCTXDM) (A0h to D7h)

The control cell transmit memory may also be accessed from extended memory. See Table 175.

Name	Offset	Type	Reset	Description
cell_bus_routing_header[15:8]	00h	RW	X	These 56 bytes are the cell routing header, the tandem routing header, and the control cell to be transmitted onto the cell bus. This memory space in direct memory is a shadow of the control cell transmit extended memory. A control cell to be transmitted should be written to this direct memory space.
cell_bus_routing_header[7:0]	01h			
tandem_routing_header[15:8]	02h			
tandem_routing_header[7:0]	03h			
header[31:24]	04h			
header[23:16]	05h			
header[15:8]	06h			
header[7:0]	07h			
payload_byte0	08h			
payload_byte1	09h			
. . .	. . .			
payload_byte46	36h			
payload_byte47	37h			

14 Registers (continued)

14.2.5 Multicast Memories

Table 53. PHY Port 0 and Control Cells Multicast Direct Memory (PP0MDM) (E0h to FFh)

The PHY port 0 and control cells multicast memory may also be accessed from extended memory (see Table 176).

Name	Offset	Type	Reset	Description
multicast_receive_enable[15:0]	00h	RW	X	This memory space contains 256 active-high enable bits. Each bit represents a multicast net number from 0 through 255. If a bit is set, the corresponding multicast net number data cell is sent to the queue group for PHY port 0, or the corresponding multicast control cell is sent to the control cell receive direct and extended memory. The least significant bit is multicast net number 0. This memory space in direct memory is a shadow of the PHY port 0 and control cells multicast extended memory space.
multicast_receive_enable[31:16]	02h			
multicast_receive_enable[47:32]	04h			
. . .	. . .			
multicast_receive_enable[159:144]	12h			
multicast_receive_enable[175:160]	14h			
multicast_receive_enable[191:176]	16h			
multicast_receive_enable[207:192]	18h			
multicast_receive_enable[223:208]	1Ah			
multicast_receive_enable[239:224]	1Ch			
multicast_receive_enable[255:240]	1Eh			

14.3 Extended Memory Registers

The *CelXpres* T8208's extended memory registers are mapped into three major blocks: the main registers, the UTOPIA registers, and the SDRAM registers.

14.3.1 Main Registers

Table 54. Main Configuration 1 (MCF1) (0100h)

Name	Bit Pos.	Type	Reset	Description
Reserved	4:0	RO	00h	**Reserved.**
tram_512k	5	RW	0	**Translation RAM 512K Bytes.** When a single SRAM of 512K bytes is used (instead of two 256K bytes SRAM), this bit should be set to '1.' When this bit is set, the tram_qnty_sel and tram_size[1:0] bits in this register are ignored. Clear this bit to '0' if a single SRAM of 512K bytes is not used.
bypass_lut	6	RW	0	**Bypass LUT.** When this bit is set to '1,' it indicates that no LUT option is selected for look up. This means that the cells being received on RX UTOPIA are not going to pass through an LUT. When this bit is cleared to '0,' the T8208 will perform an LUT access for cells being received on RX UTOPIA.
cbrh_before_trh	7	RW	0	**Cell Bus Routing Header Before Tandem Routing Header.** When the bypass LUT option is set in the above bit, then the T8208 is expecting 58 byte cells in 16-bit UTOPIA mode and 57 byte cells in 8-bit UTOPIA mode on RX UTOPIA. When this bit is cleared to '0,' the T8208 expects to see the tandem routing header come before the cell bus routing header on the incoming cells. When this bit is set to '1,' the T8208 device expects to see the cell bus routing header before the tandem routing header on the incoming cells.

14 Registers (continued)

Table 54. Main Configuration 1 (MCF1) (0100h) (continued)

Name	Bit Pos.	Type	Reset	Description
tx_utopia_hi_z	8	RW	0	**Transmit UTOPIA High Impedance.** When the device is in ATM and shared UTOPIA mode, this bit must be cleared to '0': ■ For the slave device, the u_txsoc output will always be high impedance while the u_txdata[7:0] and u_txprty outputs go high impedance when not active. ■ For the master device, the u_txdata[7:0] and u_txprty outputs go high impedance when not active. When the device is in ATM and nonshared UTOPIA mode and this bit is cleared to '0,' the u_txdata[7:0] and u_txprty outputs go high impedance when not active. When the device is in PHY mode and this bit is cleared to '0,' the u_txsoc, u_txdata[7:0], and u_txprty outputs go high impedance when not active. If the device acts as one of the multi-PHY devices, then this bit must be cleared to '0.' When this bit is set to '1,' the u_txsoc, u_txdata[7:0], and u_txprty outputs never go high impedance.
sdram_bypass	9	RW	0	**SDRAM Bypass.** When this bit is '1,' the T8208 will not use SDRAM and will use only internal memory to buffer cell bus data. Clear this bit to enable the SDRAM interface.
phyen	10	RW	1	**PHY Enable.** When this bit is '1,' the UTOPIA bus is configured for ATM mode. When '0,' the UTOPIA bus is configured for PHY mode.
tram_qnty_sel	11	RW	0	**Translation RAM Quantity Select.** When two external SRAM devices are used, this bit should be set. When this bit is cleared, only one external SRAM will be accessed using tr_cs*[0].
sp_utopia_sel	12	RW	1	**Special UTOPIA Mode Select.** When this bit is '1,' the T8208 will send 53-byte cells on the UTOPIA bus. When it is '0,' the 55-byte UTOPIA mode is selected, and the tandem routing header bytes will be appended to the beginning of each cell.
tram_size	14:13	RW	0	**Translation RAM Size.** These bits identify the size of the external SRAM used for the look-up table RAM. "00" = 32K bytes. "01" = 64K bytes. "10" = 128K bytes. "11" = 256K bytes.
Reserved	15	RW	0	**Reserved.** Program to '0.'

14 Registers (continued)

Table 55. Main Interrupt Status 1 (MIS1) (0102h)

Name	Bit Pos.	Type	Reset	Description
cb_wc_miss	0	ROL	0	**Cell Bus Write Clock Missing.** This bit is set when the cell bus write clock is inactive for 32 mclk cycles. An interrupt is generated if the corresponding enable bit is set.
cb_rc_miss	1	ROL	0	**Cell Bus Read Clock Missing.** This bit is set when the cell bus read clock is inactive for 32 mclk cycles. An interrupt is generated if the corresponding enable bit is set.
cb_fs_miss	2	ROL	0	**Cell Bus Frame Synchronization Signal Missing.** This bit is set when the cell bus frame sync is not asserted every 16 read clock cycles in 16-user mode or every 32 read clock cycles in 32-user mode. It is also set when cell bus write clock is not present because the frame synchronization signal is clocked onto the cell bus by the write clock. An interrupt is generated if the corresponding enable bit is set.
BIP8_err	3	ROL	0	**Bit Interleave Parity Error.** This bit is set when an error is detected in the BIP-8 field of the last cell bus frame cycle. An interrupt is generated if the corresponding enable bit is set.
ctrl_cell_ack	4	ROL	0	**Control Cell Acknowledged.** This bit is set when a control cell is sent on the cell bus and an acknowledge is received. This bit is not set for broadcast or multicast cells. An interrupt is generated if the corresponding enable bit is set.
ctrl_cell_nack	5	ROL	0	**Control Cell Not Acknowledged.** This bit is set when a control cell is sent on the cell bus and an acknowledge is not received. This bit is not set for broadcast or multicast cells. An interrupt is generated if the corresponding enable bit is set.
cb_grnt_to	6	ROL	0	**Cell Bus Grant Time-Out.** This bit is set when a cell bus request has not been granted within the time programmed in the cb_req_to bits. An interrupt is generated if the corresponding enable bit is set.
ctrl_cell_sent	7	ROL	0	**Control Cell Sent.** This bit is set when a control cell is sent onto the cell bus. An interrupt is generated if the corresponding enable bit is set.
ctrl_cell_av	8	ROL	0	**Control Cell Available.** This bit is set when a control cell is waiting to be read by the microprocessor. An interrupt is generated if the corresponding enable bit is set.
cb_rh_crc_err	9	ROL	0	**Cell Bus Routing Header CRC Error.** This bit is set when an error is detected in the CRC field of the cell bus routing header. An interrupt is generated if the corresponding enable bit is set.
rx_prty_err	10	ROL	0	**Receive Parity Error.** This bit is set when the odd parity calculated over the data received on the RX UTOPIA port does not match the u_rxprty signal. An interrupt is generated if the corresponding enable bit is set. When a receive parity error occurs, the cell is still counted as received and is translated and routed.
soc_err	11	ROL	0	**Start of Cell Error.** This bit is set when an SOC framing error is detected on the RX UTOPIA port. An interrupt is generated if the corresponding enable bit is set. When a start of cell error occurs, the received cells are dropped.
Reserved	15:12	RO	0	**Reserved.**

Note: Immediately following device setup, write FFFFh to this register to clear erroneously set bits.

14 Registers (continued)

Table 56. Main Interrupt Enable 1 (MIE1) (0104h)

Name	Bit Pos.	Type	Reset	Description
cb_wc_miss_ie	0	RW	0	**Cell Bus Write Clock Missing Interrupt Enable.** An interrupt is generated if this bit and the corresponding status bit are set. The interrupt is generated until this bit or the corresponding status bit is reset.
cb_rc_miss_ie	1	RW	0	**Cell Bus Read Clock Missing Interrupt Enable.** An interrupt is generated if this bit and the corresponding status bit are set. The interrupt is generated until this bit or the corresponding status bit is reset.
cb_fs_miss_ie	2	RW	0	**Cell Bus Frame Synchronization Signal Missing Interrupt Enable.** An interrupt is generated if this bit and the corresponding status bit are set. The interrupt is generated until this bit or the corresponding status bit is reset.
BIP8_err_ie	3	RW	0	**Bit Interleave Parity Error Interrupt Enable.** An interrupt is generated if this bit and the corresponding status bit are set. The interrupt is generated until this bit or the corresponding status bit is reset.
ctrl_cell_ack_ie	4	RW	0	**Control Cell Acknowledged Interrupt Enable.** An interrupt is generated if this bit and the corresponding status bit are set. The interrupt is generated until this bit or the corresponding status bit is reset.
ctrl_cell_nack_ie	5	RW	0	**Control Cell Not Acknowledged Interrupt Enable.** An interrupt is generated if this bit and the corresponding status bit are set. The interrupt is generated until this bit or the corresponding status bit is reset.
cb_grnt_to_ie	6	RW	0	**Cell Bus Grant Time-Out Interrupt Enable.** An interrupt is generated if this bit and the corresponding status bit are set. The interrupt is generated until this bit or the corresponding status bit is reset.
ctrl_cell_sent_ie	7	RW	0	**Control Cell Sent Interrupt Enable.** An interrupt is generated if this bit and the corresponding status bit are set. The interrupt is generated until this bit or the corresponding status bit is reset.
ctrl_cell_av_ie	8	RW	0	**Control Cell Available Interrupt Enable.** An interrupt is generated if this bit and the corresponding status bit are set. The interrupt is generated until this bit or the corresponding status bit is reset.
cb_rh_crc_err_ie	9	RW	0	**Cell Bus Routing Header CRC Error Interrupt Enable.** An interrupt is generated if this bit and the corresponding status bit are set. The interrupt is generated until this bit or the corresponding status bit is reset.
rx_prty_err_ie	10	RW	0	**Receive Parity Error Interrupt Enable.** An interrupt is generated if this bit and the corresponding status bit are set. The interrupt is generated until this bit or the corresponding status bit is reset.
soc_err_ie	11	RW	0	**Start of Cell Error Interrupt Enable.** An interrupt is generated if this bit and the corresponding status bit are set. The interrupt is generated until this bit or the corresponding status bit is reset.
Reserved	15:12	RO	0	**Reserved.**

14 Registers (continued)

Table 57. TX UTOPIA Clock Configuration (TXUCCF) (010Ch)

Name	Bit Pos.	Type	Reset	Description
tx_utopia_clk_div	7:0	RW	01h	**TX UTOPIA Clock Division.** The selected TX UTOPIA clock source is divided by the number programmed in these bits as follows: “00000000” = reserved “00000001” = no division “00000010” = divide by 2 “00000011” = divide by 3 . . . “11111111” = divide by 255 These bits are meaningful only when the T8208 generates the TX UTOPIA clock.
tx_utopia_clk_src_sel	9:8	RW	0	**TX UTOPIA Clock Source Select.** The source of the TX UTOPIA clock is selected via these bits as follows: “00” = cell bus write clock “01” = PLL VCO frequency (twice the MCLK) “10” = pclk “11” = mclk These bits are meaningful only when the T8208 generates the TX UTOPIA clock.
Reserved	10	RO	0	**Reserved.** Program to ‘0.’
tx_utopia_clk_en	11	RW	0	**TX UTOPIA Clock Enable.** If this bit is ‘1,’ the T8208 generates the TX UTOPIA clock on the u_txclk pin. If this bit is ‘0,’ the u_txclk pin is configured as an input.
Reserved	15:12	RO	0	**Reserved.**

14 Registers (continued)

Table 58. RX UTOPIA Clock Configuration (RXUCCF) (010Eh)

Name	Bit Pos.	Type	Reset	Description
rx_utopia_clk_div	7:0	RW	01h	**RX UTOPIA Clock Division.** The selected RX UTOPIA clock source is divided by the number programmed in these bits as follows: “00000000” = reserved “00000001” = no division “00000010” = divide by 2 “00000011” = divide by 3 . . . “11111111” = divide by 255 These bits are meaningful only when the T8208 generates the RX UTOPIA clock.
rx_utopia_clk_src_sel	9:8	RW	0	**RX UTOPIA Clock Source Select.** The source of the RX UTOPIA clock is selected via these bits as follows: “00” = cell bus write clock “01” = PLL VCO frequency (twice the MCLK) “10” = pclk “11” = mclk These bits are meaningful only when the T8208 generates the RX UTOPIA clock.
Reserved	10	RO	0	**Reserved.** Program to ‘0.’
rx_utopia_clk_en	11	RW	0	**RX UTOPIA Clock Enable.** If this bit is ‘1,’ the T8208 generates the RX UTOPIA clock on the u_rxclk pin. If this bit is ‘0,’ the u_rxclk pin is configured as an input.
Reserved	15:12	RO	0	**Reserved.**

14 Registers (continued)

Table 59. Main Configuration/Control (MCFCT) (0110h)

Name	Bit Pos.	Type	Reset	Description
cntl_cell_rd	0	WO	0	**Control Cell Has Been Read.** Write ‘1’ to this bit after a control cell is read from the control cell FIFO. The ‘1’ will pulse for one clock cycle and will clear to ‘0’ automatically.
cntl_cell_wr	1	RW	0	**Control Cell Written in Control Cell Memory.** Write ‘1’ to this bit after a control cell is written in the control cell memory. This bit is automatically cleared when the cell is transmitted to the cell bus.
cb_req_pr	3:2	RW	0	**Cell Bus Request Priority.** These bits indicate the priority of standard requests sent on the cell bus as follows: “00” = disabled, receives cells from cell bus but cannot transmit “01” = low priority “10” = medium priority “11” = high priority
clp_fill_limit	11:4	RW	0	**CLP Fill Limit.** These bits indicate the TX PHY FIFO fill level at which cells with their CLP bit set to ‘1’ will be discarded.
cell_drop_en	12	RW	0	**Cell Drop Enable.** If this bit is ‘1,’ incoming cells with their CLP bit set to ‘1’ will be discarded when the TX PHY FIFO fill limit programmed in the clp_fill_limit bits is reached.
inv_crc	13	RW	0	**Invert CRC.** If this bit is ‘1,’ the CRC-4 in the routing header is inverted before transmission to the cell bus. This bit is used to simulate errors.
cb_rx_en	14	RW	1	**Cell Bus Receive Enable.** If this bit is ‘1,’ cells are received from the cell bus. If ‘0,’ cells are not accepted.
slave_en	15	RO	0	**Slave Enable.** If this bit is ‘1,’ the T8208 is configured as a slave in shared UTOPIA mode. The default value of this bit is ‘1.’ Clear this bit if shared UTOPIA is not used. For shared UTOPIA, only one of the two devices may have this bit cleared. Dynamically changing this bit will cause cell loss. When this bit is ‘1,’ u_rxenb*[0] and u_rxenb*[3:1] become inputs.

14 Registers (continued)

Table 60. Main Configuration 2 (MCF2) (0112h)

Name	Bit Pos.	Type	Reset	Description
addr_clav_en	3:0	RW	0	**UTOPIA Address, Cell Available, and Enable Signals.** These bits configure the number of address, cell available, and enable signals on the UTOPIA bus as follows (please see Section 9.6 for the PHY address selection in 8-bit and 16-bit UTOPIA modes): “0000” = 0 ADDR, 4 CLAV; 4ENB (8-bit and 16-bit UTOPIA) “0010” = 1 ADDR, 4 CLAV; 4ENB (8-bit and 16-bit UTOPIA) “0011” = 4 ADDR, 2 CLAV; 2ENB (8-bit UTOPIA) “0101” = 2 ADDR, 4 CLAV; 4ENB (8-bit and 16-bit UTOPIA) “1000” = 4 ADDR, 4 CLAV; 4ENB (8-bit UTOPIA) “1001” = 3 ADDR, 4 CLAV; 4ENB. (16-bit UTOPIA) “1011” = 3 ADDR, 4 CLAV; 4ENB (8-bit UTOPIA) Other modes are reserved.
Reserved	4	RO	0	**Reserved.** Program to ‘0.’
dont_inhibit_rxphy_clav	5	RW	0	**Don’t Inhibit RX PHY_CLAV.** This bit, when set to ‘1,’ keeps the rx_clav signal always asserted high, indicating the capability to accept cells even if the RX UTOPIA FIFO could overrun, or is actually overrun. This bit is valid only when the RX UTOPIA is in PHY mode. When this bit is cleared to ‘0,’ the rx_clav signal is deasserted if the RX UTOPIA FIFO is considered full.
inhibit_rxuto_fifo_overrun	6	RW	0	**Inhibit RX UTOPIA FIFO Overrun.** This bit, when set to ‘1,’ prevents the RX UTOPIA FIFO from overflowing by deasserting its rx_enb* signal, even though the rx_clav signal is high when polled, **if** the RX UTOPIA FIFO is considered full. It is considered full when 4 cells are stored in it that have not yet been read and processed by the T8208. This bit is valid when the RX UTOPIA is in ATM mode. When this bit is cleared to ‘0,’ the rx_enb* signal is not deasserted even if the RX UTOPIA FIFO is considered full.
utopia_16bit	7	RW	0	**UTOPIA 16-Bit.** When this bit is set to ‘1,’ the TX and RX UTOPIA interfaces are 16 bits wide (instead of 8 bits). This mode achieves the OC-12 rate on the UTOPIA interfaces. When this bit is cleared to ‘0,’ the TX and RX UTOPIA interfaces are 8 bits wide.

14 Registers (continued)

Table 60. Main Configuration 2 (MCF2) (0112h) (continued)

Name	Bit Pos.	Type	Reset	Description
div_queue	10:8	RW	0	**Divide into Queues.** These bits indicate the number of queues used in the TX UTOPIA cell buffer as follows: “000” = 4 queues—64 cells per queue “001” = 8 queues—32 cells per queue “010” = 16 queues—16 cells per queue “011” = 32 queues—8 cells per queue “100” = 64 queues—4 cells per queue “101” = 128 queues—2 cells per queue “111” = 1 queue—256 cells per queue In PHY mode, the maximum number of queues that can be selected are four. To maximize cell buffering the number of queues must be one. In multi-PHY mode, each PHY port uses four queues unless 64 PHY ports are selected (in 8-bit UTOPIA mode). If 64 PHY ports are selected, each PHY port uses two queues or a programmable number of queues per PHY. In 16-bit UTOPIA mode, each PHY port uses four queues, unless 32 PHY ports are selected. If 32 PHY ports are selected, each PHY port uses two queues or a programmable number of queues per PHY.
Reserved	11	RO	0	**Reserved.** Program to ‘0.’
clear_on_read	12	RW	1	**Clear On Read.** When this bit is set to ‘1,’ the following counters are going to be automatically cleared when read by the microprocessor: ■ RX PHY cell counters (incoming cell count) 4000h—40FEh. ■ TX PHY cell counters (outgoing cell count) 0600h—06FEh. ■ Dropped cell counters 3000h—31FEh. ■ Total and special cell counters of the look-up record if the extended records mode is selected. Both the registers for every PHY (and every queue for dropped cell count) **must** be read consecutively (bits 31:16 first, bits 15:0 next). When this bit is cleared to ‘0,’ the microprocessor must clear the counters after it reads them, if it is needed.
mask_ignore	13	RW	0	**Mask Ignore.** When this bit is set to ‘1,’ the T8208 ignores the ignore bit that was programmed in the look-up records that control the translation of the incoming UTOPIA cells. When this bit is cleared to ‘0,’ the T8208 processes the ignore bit programmed in the look-up records.

14 Registers (continued)

Table 60. Main Configuration 2 (MCF2) (0112h) (continued)

Name	Bit Pos.	Type	Reset	Description
initialize_counters	14	RW	0	**Initialize Counters.** This bit can be set and polled until it goes back to zero to indicate the completion of clearing the following counters during the initialization process: ■ RX PHY cell counters (incoming cell count) 4000h—40FEh. ■ TX PHY cell counters (outgoing cell count) 0600h—06FEh. ■ Dropped cell counters 3000h—31FEh. Note that this bit does **not** clear the total and special cell counters of the look-up record if the extended records mode is selected. The user could set this bit to '1,' initialize other registers if desired, and at the end come back to poll this bit before removing the reset from the main circuitry. Note that this feature will **not** work unless the main registers are out of reset and the remaining circuitry is in reset. (This bit can be used to clear the above counters as part of the extended memory access after the srst_reg* is set as part of the powerup sequence; see section 3 on page 22).
initialize_LUT	15	RW	0	**Initialize LUT.** This bit can be set and polled until it goes back to zero to indicate the completion of clearing the look-up table. Note that the memory size in the SRAM indicated by the bits set in 0100h will be cleared, **not** the maximum possible size of the SRAM, unless the configuration bits of register 0100h indicate that the largest possible SRAM size is being used. The user could set this bit to '1,' initialize other registers if desired, and, at the end, come back to poll this bit before removing the reset from the main circuitry. Note that this feature will **not** work unless the main registers are out of reset and the remaining circuitry is in reset. (This bit can be used to clear the above counters as part of the extended memory access after the srst_reg* is set as part of the powerup sequence; see section 3 on page 22).

14 Registers (continued)

Table 61. UTOPIA Configuration (UCF) (0114h)

Name	Bit Pos.	Type	Reset	Description
hec_mask	7:0	RW	55h	**Header Error Control (HEC) Mask.** An exclusive-OR function is performed on these bits and the HEC value received from the UTOPIA bus before the HEC is checked for error. Also, an exclusive-OR function is performed on these bits and the HEC value calculated before it is transmitted on the UTOPIA bus. Note that a value of zero will not change the HEC value, and a value of FFh will invert the HEC value.
addr_match	12:8	RW	0	**Address Match.** These bits represent the UTOPIA address of the T8208 in level 2 UTOPIA multi-PHY mode. These bits are only used when the T8208 is configured as a PHY.
Reserved	15:13	RO	0	**Reserved.**

Table 62. Main Configuration 3 (MCF3) (0116h)

Name	Bit Pos.	Type	Reset	Description
cb_req_to	7:0	RW	0	**Cell Bus Request Time-Out.** These bits determine the number of frames that a cell bus request may be present before the cell bus grant time-out (cb_grnt_to) status bit is set.
gfc_value	11:8	RW	0	**Generic Flow Control (GFC) Value.** These are the bits inserted in the GFC field of the TX UTOPIA outgoing cells when the GFC insert feature is enabled.
gfc_insert_en	12	RW	0	**GFC Insert Enable.** If this bit is ‘1,’ the gfc_value will be inserted in all cells transmitted to the UTOPIA bus.
Reserved	15:13	RO	0	**Reserved.**

14 Registers (continued)

Table 63. UTOPIA Configuration 5 (UCF5) (0118h)

Name	Bit Pos.	Type	Reset	Description
rx_port_en[63:48]	15:0	RW	0	**Receive Port Enable.** Each bit in this field represents one of the 48—63 PHY ports where the least significant bit is port 48. If the corresponding bit is ‘1,’ cells will be received on the designated UTOPIA port.

Table 64. UTOPIA Configuration 4 (UCF4) (011Ah)

Name	Bit Pos.	Type	Reset	Description
rx_port_en[47:32]	15:0	RW	0	**Receive Port Enable.** Each bit in this field represents one of the 32—47 PHY ports where the least significant bit is port 32. If the corresponding bit is ‘1,’ cells will be received on the designated UTOPIA port.

Table 65. UTOPIA Configuration 3 (UCF3) (011Ch)

Name	Bit Pos.	Type	Reset	Description
rx_port_en[31:16]	15:0	RW	0	**Receive Port Enable.** Each bit in this field represents one of the 16—31 PHY ports where the least significant bit is port 16. If the corresponding bit is ‘1,’ cells will be received on the designated UTOPIA port.

Table 66. UTOPIA Configuration 2 (UCF2) (011Eh)

Name	Bit Pos.	Type	Reset	Description
rx_port_en[15:0]	15:0	RW	0	**Receive Port Enable.** Each bit in this field represents one of the 0—15 PHY ports where the least significant bit is port 0. If the corresponding bit is ‘1,’ cells will be received on the designated UTOPIA port.

14 Registers (continued)

Refer to Section 8.4 for descriptions of special cell counters.

Table 67. Extended LUT Control (ELUTCN) (0120h)

Name	Bit Pos.	Type	Reset	Description
spc_cell_cnt_sel0	0	RW	0	**Special Cell Count Select 0.** When this bit is '1,' cells, whose four least significant bits of their header are "0000," are counted in the special cell count.
spc_cell_cnt_sel1	1	RW	0	**Special Cell Count Select 1.** When this bit is '1,' cells, whose four least significant bits of their header are "0001," are counted in the special cell count.
spc_cell_cnt_sel2	2	RW	0	**Special Cell Count Select 2.** When this bit is '1,' cells, whose four least significant bits of their header are "0010," are counted in the special cell count.
spc_cell_cnt_sel3	3	RW	0	**Special Cell Count Select 3.** When this bit is '1,' cells, whose four least significant bits of their header are "0011," are counted in the special cell count.
spc_cell_cnt_sel4	4	RW	0	**Special Cell Count Select 4.** When this bit is '1,' cells, whose four least significant bits of their header are "0100," are counted in the special cell count.
spc_cell_cnt_sel5	5	RW	0	**Special Cell Count Select 5.** When this bit is '1,' cells, whose four least significant bits of their header are "0101," are counted in the special cell count.
spc_cell_cnt_sel6	6	RW	0	**Special Cell Count Select 6.** When this bit is '1,' cells, whose four least significant bits of their header are "0110," are counted in the special cell count.
spc_cell_cnt_sel7	7	RW	0	**Special Cell Count Select 7.** When this bit is '1,' cells, whose four least significant bits of their header are "0111," are counted in the special cell count.
spc_cell_cnt_sel8	8	RW	0	**Special Cell Count Select 8.** When this bit is '1,' cells, whose four least significant bits of their header are "1000," are counted in the special cell count.
spc_cell_cnt_sel9	9	RW	0	**Special Cell Count Select 9.** When this bit is '1,' cells, whose four least significant bits of their header are "1001," are counted in the special cell count.
spc_cell_cnt_sel10	10	RW	0	**Special Cell Count Select 10.** When this bit is '1,' cells, whose four least significant bits of their header are "1010," are counted in the special cell count.
spc_cell_cnt_sel11	11	RW	0	**Special Cell Count Select 11.** When this bit is '1,' cells, whose four least significant bits of their header are "1011," are counted in the special cell count.
spc_cell_cnt_sel12	12	RW	0	**Special Cell Count Select 12.** When this bit is '1,' cells, whose four least significant bits of their header are "1100," are counted in the special cell count.
spc_cell_cnt_sel13	13	RW	0	**Special Cell Count Select 13.** When this bit is '1,' cells, whose four least significant bits of their header are "1101," are counted in the special cell count.
spc_cell_cnt_sel14	14	RW	0	**Special Cell Count Select 14.** When this bit is '1,' cells, whose four least significant bits of their header are "1110," are counted in the special cell count.
spc_cell_cnt_sel15	15	RW	0	**Special Cell Count Select 15.** When this bit is '1,' cells, whose four least significant bits of their header are "1111," are counted in the special cell count.

14 Registers (continued)

Table 68. Generated Cell Bus Clocks Control Register (GCBCCR) (0122h)

The cb_gen_wc and cb_gen_rc clocks are TTL compatible and hence the customer needs to use an external GTL+ driver.

Name	Bit Pos.	Type	Reset	Description
divisor_value	7:0	RW	00000010	**Divisor Value.** These bits contain the divisor value that is used to divide one of the three clock sources down to generate the cb_gen_wc and cb_gen_rc clocks that are available on pins A3 and B4 of the T8208. The divisor controls both clocks, as cb_gen_wc is obtained by simply delaying cb_gen_rc by a certain programmable value. “00000000” = reserved “00000001” = no division “00000010” = divide by 2 “00000011” = divide by 3 . . . “11111111” = divide by 255
clock_select	9:8	RW	10	**Clock Select.** These bits select one of the following clocks as the source of the I/O clocks, cb_gen_wc and cb_gen_rc: "00”: reserved. "01”: PLL VCO frequency (twice the Mclk). "10”: pclk "11”: mclk.
clock_enable	10	RW	0	**Clock Enable.** When this bit is set to ‘1,’ the generated cell bus clocks come out on the cb_gen_wc and cb_gen_rc pins (A3 and B4 respectively) and also drive the internal cell bus logic of this generating device if select_gtl_clocks (bit 6) in register 2Eh is cleared to ‘0.’ When this bit is cleared to ‘0,’ the cb_gen_wc and cb_gen_rc pins are 3-stated and are inactive. **Note:** Due to the inherent propagation delay between the clocks that drive the cell bus logic of the generating device and the other devices on the backplane, it is recommended that customers set bit 6 in register 2Eh to ‘1’ and set bit 10 in register 0122h to ‘1’ and route these generated clocks (through a GTL+ driver) back to the cb_wc* and cb_rc* pins (pins A10 and B10, respectively).
switching_complete	11	RW	0	**Switching Complete.** When this bit is set by the T8208 internal logic to ‘1,’ it indicates that the new clock source that was programmed in bits 9:8 has now taken over as the source of cb_gen_wc and cb_gen_rc. There is no need to clear this bit as it is automatically cleared when a new source is selected.

14 Registers (continued)

Table 68. Generated Cell Bus Clocks Control Register (GCBCCR) (0122h) (continued)

The cb_gen_wc and cb_gen_rc clocks are TTL compatible and hence the customer needs to use an external GTL+ driver.

Name	Bit Pos.	Type	Reset	Description
divisor_active	12	RW	0	**Divisor Active.** When this bit is set by the T8208 internal logic to '1,' it indicates that the new divisor value that was just programmed in bits 7:0 of this register is now in effect in dividing the cb_gen_wc and cb_gen_rc. There is no need to clear this bit as it is automatically cleared when a new divisor is selected.
delay_select	15:13	RW	010	**Delay Select.** These bits control the delay to be observed between cb_gen_wc and cb_gen_rc. The range of programmable delays are: "000": 1.0 ns. "001": 1.5 ns. "010": 2.0 ns. "011": 2.5 ns. "100": 3.0 ns. "101": 3.5 ns. "110": 4.0 ns. "111": 4.5 ns.

Note: The following should be done when attempting to source the generated clocks from a new source:

a. Program the new clock_select value into register 122 Hex.
b. Poll bit 11 of register 122 Hex until it is set to '1'.

Note: The following should be done when attempting to program a new divisor for the generated clocks:

a. Program the new divisor_value into register 122 Hex.
b. Poll bit 12 of register 122 Hex until it is set to '1'.

Note: The following should be done when attempting to do a handoff of the generated clocks on the backplane from one device to another:

a. Set the clock_enable bit of register 122 Hex in the presently generating T8208 to '0'.
b. Poll bits 0 and 1 of register 102 Hex (cb_wc_miss and cb_rc_miss) until they both become high, indicating that the cell bus clocks were found to be dead for 32 consecutive mclk cycles.
c. If needed, program the new clock source into register 122 Hex of the new T8208 clock master as per the procedure outlined above.
d. If needed, program the new divisor value into register 122 Hex of the new T8208 clock master as per the procedure outlined above.
e. Enable the new generated clocks from the new T8208 by setting the clock_enable bit of register 122 Hex.
f. Read bits 2:0 of register 102 Hex (cb_fs_miss, cb_rc_miss and cb_wc_miss).
g. If the bits read in step f (above) are set to 1, proceed to step h; else, go to step i.
h. Clear those 3 bits by writing a 1 to them (in register 102 Hex). Go back to step f.
i. Handoff is done.

Note: The above delay_select bits have an accuracy of +10% and –50%.

14 Registers (continued)

Table 69. RX PHY FIFO Thresholds to Change Cell Bus Request Priority (RXPFTCRP) (0126h)

Name	Bit Pos.	Type	Reset	Description
cb_prio2_thr	3:0	RW	1111	**Cell Bus Priority 2 Threshold.** These bits contain the RX PHY FIFO threshold level value after which the cell bus request priority will be set to high in an attempt to flush the cells from the RX PHY FIFO onto the backplane.
cb_prio2_thr_en	4	RW	0	**Cell Bus Priority 2 Threshold Enable.** When this bit is set to '1,' it enables the change in the cell bus request priority to its highest value (as mentioned in bits 3:0 above).
Reserved	7:5	RO	000	**Reserved.**
cb_prio1_thr	11:8	RW	1111	**Cell Bus Priority 1 Threshold.** These bits contain the RX PHY FIFO threshold level value after which the cell bus request priority will be set to medium in an attempt to flush the cells from the RX PHY FIFO onto the backplane.
cb_prio1_thr_en	12	RW	0	**Cell Bus Priority 1 Threshold Enable.** When this bit is set to '1,' it enables the change in the cell bus request priority to its medium value (as mentioned in bits 11:8 above).
Reserved	15:13	RO	000	**Reserved.**

The information below shows the change in cell bus request priority when cell bus priority 1 threshold and cell bus priority 2 threshold are reached.

Cell Bus Request Priority Bits 3:2 in Register 0110h	Priority when Threshold 1 Is Reached	Priority when Threshold 2 Is Reached
00 = disabled	medium	high
01 = low priority	medium	high
10 = medium priority	medium	high
11 = high priority	high	high

Note: When bits 3:2 in register 0110h are set to '00' (disabled) and this feature is enabled, cells are transmitted onto the cell bus as soon as the priority **medium** is reached. To prevent this, either the feature needs to be disabled or cells should not be transmitted to this FIFO.

Note: These threshold levels cannot be changed when there is data flowing through the *CelXpres* device.

14 Registers (continued)

Table 70. Enable Request on Upper Backplane Address (ERUB) (012Ch)

Name	Bit Pos.	Type	Reset	Description
en_req_up_bp	15:0	RW	FFFFh	**Enable Request on Upper Backplane.** When set to one, the arbiter T8208, in which this register is programmed, will recognize and process the requests on the backplane with device addresses in the range 16—31. Bit 0 corresponds to device address 16, bit 1 to device address 17, etc. When any bit is cleared to '0,' the device address associated with that bit will not have its request served on the backplane. It is strongly recommended that, in the case that a customer has a master card that acts as the arbiter, and a slave card that acts as a backup and is switched as the arbiter in the event that the master card fails, the same value be programmed in this register for both the master and the slave cards.

Table 71. Enable Request on Lower Backplane Address (ERLB) (012Eh)

Name	Bit Pos.	Type	Reset	Description
en_req_low_bp	15:0	RW	FFFFh	**Enable Request on Lower Backplane.** When set to one, the arbiter T8208, in which this register is programmed, will recognize and process the requests on the backplane with device addresses in the range 0—15. Bit 0 corresponds to device address 0, bit 1 to device address 1, etc. When any bit is cleared to '0,' the device address associated with that bit will not have its request served on the backplane. It is strongly recommended that, in the case that a customer has a master card that acts as the arbiter, and a slave card that acts as a backup and is switched as the arbiter in the event that the master card fails, the same value be programmed in this register for both the master and the slave cards.

14 Registers (continued)

Table 72. Cell Bus Configuration/Status (CBCFS) (0130h)

Name	Bit Pos.	Type	Reset	Description
unit_addr*	4:0	RW	ua*[4:0]	**Unit Address.** These bits indicate the values at the pins ua*[4:0] (backplane device address). These bits are read-only if bit 7 in this register is cleared to '0' and writable if bit 7 is set to '1.' When these bits are written to, the value written overwrites the address on the pins ua*[4:0] and this new value will be the backplane address of the T8208.
cb_arb_sel*	5	RW	1	**Cell Bus Arbiter Select.** If this bit is '0,' cell bus arbiter is selected. Only one device on the cell bus may be configured as arbiter. All other devices should set this bit to '1.'
cb_usr_mode	6	RW	0	**Cell Bus User Mode.** If this bit is '0,' 32-user mode is selected on the cell bus. If '1,' 16-user mode is selected.
use_prog_addr	7	RW	0	**Use Programmed Address.** When this bit is set to '1,' it allows the microprocessor to program any address (that can be different from the address on pins ua*[4:0]) in bits [4:0] of this register and ignores the address programmed at pins ua*[4:0]. Set this bit to '1' and then program the new address into bits 4:0.
insert_cb_lpbk_hdr	8	RW	1	**Insert Cell Bus Loopback Header.** When this bit is set to '1,' the T8208 inserts the programmed loopback header (in register address 0136h) as the new cell bus routing header of the loopback cell. If this bit is cleared to '0,' the T8208 uses the tandem routing header of the incoming loopback cell as the new cell bus routing header of the outgoing loopback cell, and as a result, also inserts the programmed loopback header (in register address 0136h) as the tandem routing header of the outgoing loopback cell.
cntrl_cell_prio	9	RW	0	**Control Cell Priority.** If this bit is cleared to '0,' then cells from the RX PHY FIFO have the highest priority, cells from the control cell TX FIFO have next highest, and finally, cells from the loopback FIFO have the lowest. If this bit is set to '1,' then cells from the control cell TX FIFO have the highest priority, cells from the RX PHY FIFO have the next highest priority, and finally cells from the loopback FIFO have the lowest priority. **Note:** It is recommended that this bit be set during the powerup/reset sequence (Section 3), if necessary. It is strongly advised not to set this bit during data flow.
Reserved	15:10	RO	0	**Reserved.**

14 Registers (continued)

Table 73. Main Interrupt Status 2 (MIS2) (0132h)

Name	Bit Pos.	Type	Reset	Description
lb_cell_lost	0	ROL	0	**Loopback Cell Lost.** This bit is set if a loopback cell is discarded when the loopback FIFO is full. An interrupt is generated if the corresponding enable bit is set.
Reserved	1	ROL	0	**Reserved.**
cb_in_fifo_ovrn	2	ROL	0	**Cell Bus Input FIFO Overrun.** This bit is set if the four-cell incoming cell bus input FIFO overflows. If this bit becomes set, mclk may be too slow compared to the cb_wc* input. An interrupt is generated if the corresponding enable bit is set.
tx_phy_fifo_ovrn	3	ROL	0	**TX PHY FIFO Overrun.** This bit is set if the 256-cell TX PHY FIFO overflows. If this bit becomes set, bandwidth to the SDRAM may be insufficient. An interrupt is generated if the corresponding enable bit is set.
cell_clp1_dis	4	ROL	0	**Cell with CLP Set to One Discarded.** This bit is set if a cell with its CLP bit set to one is discarded when the 256-cell TX PHY FIFO goes over the clp_fill_limit. An interrupt is generated if the corresponding enable bit is set.
rx_utopia_fifo_ovrn	5	ROL	0	**RX UTOPIA FIFO Overrun.** This bit is set if the RX UTOPIA FIFO overflows. If this bit becomes set, bandwidth to the translation RAM or the cell bus may be insufficient. An interrupt is generated if the corresponding enable bit is set.
cntl_cell_rx_fifo_ovrn	6	ROL	0	**Control Cell RX FIFO Overrun.** This bit is set when the control cell RX FIFO overflows. An interrupt is generated if the corresponding enable bit is set.
Reserved	15:7	RO	0	**Reserved.**

14 Registers (continued)

Table 74. Main Interrupt Enable 2 (MIE2) (0134h)

Name	Bit Pos.	Type	Reset	Description
lb_cell_lost_ie	0	RW	0	**Loopback Cell Lost Interrupt Enable.** An interrupt is generated if this bit and the corresponding status bit are set. The interrupt is generated until this bit or the corresponding status bit is reset.
Reserved	1	RW	0	**Reserved.** Program this bit to zero.
cb_in_fifo_ovrn_ie	2	RW	0	**Cell Bus Input FIFO Overrun Interrupt Enable.** An interrupt is generated if this bit and the corresponding status bit are set. The interrupt is generated until this bit or the corresponding status bit is reset.
tx_phy_fifo_ovrn_ie	3	RW	0	**TX PHY FIFO Overrun Interrupt Enable.** An interrupt is generated if this bit and the corresponding status bit are set. The interrupt is generated until this bit or the corresponding status bit is reset.
cell_clp1_dis_ie	4	RW	0	**Cell with CLP Set to One Discarded Interrupt Enable.** An interrupt is generated if this bit and the corresponding status bit are set. The interrupt is generated until this bit or the corresponding status bit is reset.
rx_utopia_fifo_ovrn_ie	5	RW	0	**RX UTOPIA FIFO Overrun Interrupt Enable.** An interrupt is generated if this bit and the corresponding status bit are set. The interrupt is generated until this bit or the corresponding status bit is reset.
cntl_cell_rx_fifo_ovrn_ie	6	RW	0	**Control Cell RX FIFO Overrun Interrupt Enable.** An interrupt is generated if this bit and the corresponding status bit are set. The interrupt is generated until this bit or the corresponding status bit is reset.
Reserved	15:7	RO	0	**Reserved.**

Table 75. Loopback (LB) (0136h)

Name	Bit Pos.	Type	Reset	Description
loopback_cbrh	15:0	RW	0	**Loopback Cell Bus Routing Header.** Bits 15:4 of this register will act as the new cell bus routing header of the outgoing loopback cell, **if** bit 8 of register 0130h is set to ‘1.’ If bit 8 of register 0130h is cleared to ‘0,’ the contents (bits 15:0) of this register will be used as the tandem routing header of the outgoing loopback cell. If the contents of this register are used as the cell bus routing header, then the CRC4 need not be calculated, as the T8208 automatically calculates it and prepends it (in bits 3:0 of this register) for all outgoing cells.

Table 76. Extended LUT Configuration (ELUTCF) (0138h)

Name	Bit Pos.	Type	Reset	Description
lut_rec_form	1:0	RW	0	**LUT Record Format.** These bits indicate the format of the LUT records as follows: "00”: 8 byte records. "01”: 16 byte record with extended monitoring. "10”. reserved. "11”: reserved.

14 Registers (continued)

Table 77. Misrouted Cell LUT 3 (MLUT3) (013Ch)

Name	Bit Pos.	Type	Reset	Description
mis_cell_lut_sel[63:48]	15:0	RW	FFFFh	**Misrouted Cell LUT Select.** Each bit in this field represents one of the 48—63 PHY ports. The least significant bit is PHY port 48. If the corresponding bit is '1,' misrouted cells from a PHY port are monitored.

Table 78. Misrouted Cell LUT 2 (MLUT2) (013Eh)

Name	Bit Pos.	Type	Reset	Description
mis_cell_lut_sel[47:32]	15:0	RW	FFFFh	**Misrouted Cell LUT Select.** Each bit in this field represents one of the 32—47 PHY ports. The least significant bit is PHY port 32. If the corresponding bit is '1,' misrouted cells from a PHY port are monitored.

Table 79. Misrouted Cell LUT 1 (MLUT1) (0140h)

Name	Bit Pos.	Type	Reset	Description
mis_cell_lut_sel[31:16]	15:0	RW	FFFFh	**Misrouted Cell LUT Select.** Each bit in this field represents one of the 16—31 PHY ports. The least significant bit is PHY port 16. If the corresponding bit is '1,' misrouted cells from a PHY port are monitored.

Table 80. Misrouted Cell LUT 0 (MLUT0) (0142h)

Name	Bit Pos.	Type	Reset	Description
mis_cell_lut_sel[15:0]	15:0	RW	FFFFh	**Misrouted Cell LUT Select.** Each bit in this field represents one of the 0—15 PHY ports. The least significant bit is PHY port 0. If the corresponding bit is '1,' misrouted cells from a PHY port are monitored.

14 Registers (continued)

Table 81. Misrouted Cell LUT 4 (MLUT4) (0144h)

Name	Bit Pos.	Type	Reset	Description
mis_cell_clr	0	WO	0	**Misrouted Cell Header Clear.** Write ‘1’ to this bit to clear the previously latched misrouted cell header. The ‘1’ will pulse for one clock cycle and will clear to ‘0’ automatically.
mis_cell_latch	1	RO	0	**Misrouted Cell Header Latched.** If this bit is set to ‘1,’ a misrouted cell was detected and is stored to the mis_cell_header bits.
Reserved	3:2	RO	0	**Reserved.**
lst_mis_cell_lut	9:4	RO	0	**Last Misrouted Cell LUT.** These bits indicate the PHY port from which the last misrouted cell was latched.
Reserved	15:10	RO	0	**Reserved.**

Table 82. Misrouted Cell Header High (MCHH) (0146h)

Name	Bit Pos.	Type	Reset	Description
mis_cell_header[31:16]	15:0	RO	0	**Misrouted Cell Header Bits [31:16].** These bits are cell header bits [31:16] from the first misrouted cell received after the mis_cell_clr bit was set. A cell is considered misrouted if its A and I bits are “00,” if its VCI is out of range, or if the lutX_vpi_chk bit is ‘1’ and the unused VPI bits in the incoming cell header are not all zero.

Table 83. Misrouted Cell Header Low (MCHL) (0148h)

Name	Bit Pos.	Type	Reset	Description
mis_cell_header[15:0]	15:0	RO	0	**Misrouted Cell Header Bits [15:0].** These bits are cell header bits [15:0] from the first misrouted cell received after the mis_cell_clr bit was set. A cell is considered misrouted if its A and I bits are “00,” if its VCI is out of range, or if the lutX_vpi_chk bit is ‘1’ and the unused VPI bits in the incoming cell header are not all zero.

14 Registers (continued)

14.3.2 UTOPIA Registers

Table 84. HEC Interrupt Status 3 (HIS3) (0300h)

Name	Bit Pos.	Type	Reset	Description
hec_err[63:48]	15:0	ROL	0	**HEC Error.** Each bit in this field represents one of the 48—63 PHY ports where the least significant bit is port 48. The associated bit is set when an HEC error is detected on the PHY port. An interrupt is generated if the corresponding enable bit is set. When a HEC error occurs, the cell is still counted as received and is translated and routed.

Table 85. HEC Interrupt Status 2 (HIS2) (0302h)

Name	Bit Pos.	Type	Reset	Description
hec_err[47:32]	15:0	ROL	0	**HEC Error.** Each bit in this field represents one of the 32—47 PHY ports where the least significant bit is port 32. The associated bit is set when an HEC error is detected on the PHY port. An interrupt is generated if the corresponding enable bit is set. When a HEC error occurs, the cell is still counted as received and is translated and routed.

Table 86. HEC Interrupt Status 1 (HIS1) (0304h)

Name	Bit Pos.	Type	Reset	Description
hec_err[31:16]	15:0	ROL	0	**HEC Error.** Each bit in this field represents one of the 16—31 PHY ports where the least significant bit is port 16. The associated bit is set when an HEC error is detected on the PHY port. An interrupt is generated if the corresponding enable bit is set. When a HEC error occurs, the cell is still counted as received and is translated and routed.

Table 87. HEC Interrupt Status 0 (HIS0) (0306h)

Name	Bit Pos.	Type	Reset	Description
hec_err[15:0]	15:0	ROL	0	**HEC Error.** Each bit in this field represents one of the 0—15 PHY ports where the least significant bit is port 0. The associated bit is set when an HEC error is detected on the PHY port. An interrupt is generated if the corresponding enable bit is set. When a HEC error occurs, the cell is still counted as received and is translated and routed.

14 Registers (continued)

Table 88. HEC Interrupt Enable 3 (HIE3) (0308h)

Name	Bit Pos.	Type	Reset	Description
hec_err_ie[63:48]	15:0	RW	0	**HEC Error Interrupt Enable.** An interrupt is generated if this bit and the corresponding status bit are set. The interrupt is generated until this bit or the corresponding status bit is reset.

Table 89. HEC Interrupt Enable 2 (HIE2) (030Ah)

Name	Bit Pos.	Type	Reset	Description
hec_err_ie[47:32]	15:0	RW	0	**HEC Error Interrupt Enable.** An interrupt is generated if this bit and the corresponding status bit are set. The interrupt is generated until this bit or the corresponding status bit is reset.

Table 90. HEC Interrupt Enable 1 (HIE1) (030Ch)

Name	Bit Pos.	Type	Reset	Description
hec_err_ie[31:16]	15:0	RW	0	**HEC Error Interrupt Enable.** An interrupt is generated if this bit and the corresponding status bit are set. The interrupt is generated until this bit or the corresponding status bit is reset.

Table 91. HEC Interrupt Enable 0 (HIE0) (030Eh)

Name	Bit Pos.	Type	Reset	Description
hec_err_ie[15:0]	15:0	RW	0	**HEC Error Interrupt Enable.** An interrupt is generated if this bit and the corresponding status bit are set. The interrupt is generated until this bit or the corresponding status bit is reset.

14 Registers (continued)

Table 92. LUT Interrupt Service Request 3 (LUTISR3) (0310h)

Name	Bit Pos.	Type	Reset	Description
lut_int_serv[63:48]	15:0	RO	0	**LUT Interrupt Service.** Each bit in this field represents one of the 48—63 LUT configuration/status registers. The least significant bit represents LUT 48 configuration/status register. If the corresponding bit is '1,' the specific LUT configuration/status register has interrupt status bits that need servicing.

Table 93. LUT Interrupt Service Request 2 (LUTISR2) (0312h)

Name	Bit Pos.	Type	Reset	Description
lut_int_serv[47:32]	15:0	RO	0	**LUT Interrupt Service.** Each bit in this field represents one of the 32—47 LUT configuration/status registers. The least significant bit represents LUT 32 configuration/status register. If the corresponding bit is '1,' the specific LUT configuration/status register has interrupt status bits that need servicing.

Table 94. LUT Interrupt Service Request 1 (LUTISR1) (0314h)

Name	Bit Pos.	Type	Reset	Description
lut_int_serv[31:16]	15:0	RO	0	**LUT Interrupt Service.** Each bit in this field represents one of the 16—31 LUT configuration/status registers. The least significant bit represents LUT 16 configuration/status register. If the corresponding bit is '1,' the specific LUT configuration/status register has interrupt status bits that need servicing.

Table 95. LUT Interrupt Service Request 0 (LUTISR0) (0316h)

Name	Bit Pos.	Type	Reset	Description
lut_int_serv[15:0]	15:0	RO	0	**LUT Interrupt Service.** Each bit in this field represents one of the 0—15 LUT configuration/status registers. The least significant bit represents LUT 0 configuration/status register. If the corresponding bit is '1,' the specific LUT configuration/status register has interrupt status bits that need servicing.

14 Registers (continued)

Table 96. LUT X Configuration/Status (LUTXCFS) (0320h to 039Eh)

Name	Bit Pos.	Type	Reset	Description
lut_en	0	RW	0	**LUT Memory Space Enable.** If this bit is '1,' the LUT memory space is enabled. When this bit is '0,' cells from the associated PHY port are discarded, are not flagged as misrouted, and are not counted as a received cell.
Reserved	3:1	RO	0	**Reserved.**
mis_cell	4	ROL	0	**Misrouted Cell to LUT.** This bit is set when a cell's translation record has its A and I bits equal to '0.' An interrupt is generated if the corresponding enable bit is set.
vci_or	5	ROL	0	**VCI Out of Range.** This bit is set when an incoming cell's VCI is greater than the allowed range. An interrupt is generated if the corresponding enable bit is set.
vpi_or	6	ROL	0	**VPI Out of Range.** This bit is set when one of the incoming cell's unmasked VPI bits is not '0' and the lutX_vpi_chk bit equals '1.' An interrupt is generated if the corresponding enable bit is set.
Reserved	9:7	RO	0	**Reserved.**
mis_cell_ie	10	RW	0	**Misrouted Cell to LUT Interrupt Enable.** An interrupt is generated if this bit and the corresponding status bit are set. The interrupt is generated until this bit or the corresponding status bit is reset.
vci_or_ie	11	RW	0	**VCI Out of Range Interrupt Enable.** An interrupt is generated if this bit and the corresponding status bit are set. The interrupt is generated until this bit or the corresponding status bit is reset.
vpi_or_ie	12	RW	0	**VPI Out of Range Interrupt Enable.** An interrupt is generated if this bit and the corresponding status bit are set. The interrupt is generated until this bit or the corresponding status bit is reset.
Reserved	15:13	RO	0	**Reserved.**

The letter X in the register name represents the 64 PHY port look-up tables. The addresses of the 64 configuration/status registers are shown below.

Register Name	Register Address	Register Name	Register Address
LUT 0 Configuration/Status	(0320h)	LUT 13 Configuration/Status	(033Ah)
LUT 1 Configuration/Status	(0322h)	LUT 14 Configuration/Status	(033Ch)
LUT 2 Configuration/Status	(0324h)	LUT 15 Configuration/Status	(033Eh)
LUT 3 Configuration/Status	(0326h)	LUT 16 Configuration/Status	(0340h)
LUT 4 Configuration/Status	(0328h)	LUT 17 Configuration/Status	(0342h)
LUT 5 Configuration/Status	(032Ah)	LUT 18 Configuration/Status	(0344h)
LUT 6 Configuration/Status	(032Ch)	LUT 19 Configuration/Status	(0346h)
LUT 7 Configuration/Status	(032Eh)	LUT 20 Configuration/Status	(0348h)
LUT 8 Configuration/Status	(0330h)	LUT 21 Configuration/Status	(034Ah)
LUT 9 Configuration/Status	(0332h)	LUT 22 Configuration/Status	(034Ch)
LUT 10 Configuration/Status	(0334h)	LUT 23 Configuration/Status	(034Eh)
LUT 11 Configuration/Status	(0336h)	LUT 24 Configuration/Status	(0350h)
LUT 12 Configuration/Status	(0338h)	LUT 25 Configuration/Status	(0352h)

14 Registers (continued)

Table 96. LUT X Configuration/Status (LUTXCFS) (0320h to 039Eh) (continued)

Register Name	Register Address	Register Name	Register Address
LUT 26 Configuration/Status	(0354h)	LUT 45 Configuration/Status	(037Ah)
LUT 27 Configuration/Status	(0356h)	LUT 46 Configuration/Status	(037Ch)
LUT 28 Configuration/Status	(0358h)	LUT 47 Configuration/Status	(037Eh)
LUT 29 Configuration/Status	(035Ah)	LUT 48 Configuration/Status	(0380h)
LUT 30 Configuration/Status	(035Ch)	LUT 49 Configuration/Status	(0382h)
LUT 31 Configuration/Status	(035Eh)	LUT 50 Configuration/Status	(0384h)
LUT 32 Configuration/Status	(0360h)	LUT 51 Configuration/Status	(0386h)
LUT 33 Configuration/Status	(0362h)	LUT 52 Configuration/Status	(0388h)
LUT 34 Configuration/Status	(0364h)	LUT 53 Configuration/Status	(038Ah)
LUT 35 Configuration/Status	(0366h)	LUT 54 Configuration/Status	(038Ch)
LUT 36 Configuration/Status	(0368h)	LUT 55 Configuration/Status	(038Eh)
LUT 37 Configuration/Status	(036Ah)	LUT 56 Configuration/Status	(0390h)
LUT 38 Configuration/Status	(036Ch)	LUT 57 Configuration/Status	(0392h)
LUT 39 Configuration/Status	(036Eh)	LUT 58 Configuration/Status	(0394h)
LUT 40 Configuration/Status	(0370h)	LUT 59 Configuration/Status	(0396h)
LUT 41 Configuration/Status	(0372h)	LUT 60 Configuration/Status	(0398h)
LUT 42 Configuration/Status	(0374h)	LUT 61 Configuration/Status	(039Ah)
LUT 43 Configuration/Status	(0376h)	LUT 62 Configuration/Status	(039Ch)
LUT 44 Configuration/Status	(0378h)	LUT 63 Configuration/Status	(039Eh)

14 Registers (continued)

14.3.2.1 TX UTOPIA Configuration

Table 97. Master Queue 7 (MQ7) (0150h)

These bits indicate which queues in the master device are enabled for shared UTOPIA mode.

Name	Bit Pos.	Type	Reset	Description
mast_queue_in[127:112]	15:0	RW	0	**Master Queue Indication [127:112].** Each bit in this field represents one of the 112—127 queues in the master device, where the least significant bit is queue 112, and most significant bit is queue 127. These bits indicate which queues in the master device are enabled for shared UTOPIA mode. If the associated bit is ‘1,’ it indicates that the queue is enabled. **Note:** These bits must be programmed even when the device is not used in shared UTOPIA mode.

Table 98. Master Queue 6 (MQ6) (0152h)

These bits indicate which queues in the master device are enabled for shared UTOPIA mode.

Name	Bit Pos.	Type	Reset	Description
mast_queue_in[111:96]	15:0	RW	0	**Master Queue Indication [111:96].** Each bit in this field represents one of the 96—111 queues in the master device, where the least significant bit is queue 96, and most significant bit is queue 111. These bits indicate which queues in the master device are enabled for shared UTOPIA mode. If the associated bit is ‘1,’ it indicates that the queue is enabled. **Note:** These bits must be programmed even when the device is not used in shared UTOPIA mode.

Table 99. Master Queue 5 (MQ5) (0154h)

These bits indicate which queues in the master device are enabled for shared UTOPIA mode.

Name	Bit Pos.	Type	Reset	Description
mast_queue_in[95:80]	15:0	RW	0	**Master Queue Indication [95:80].** Each bit in this field represents one of the 80—95 queues in the master device, where the least significant bit is queue 80, and most significant bit is queue 95. These bits indicate which queues in the master device are enabled for shared UTOPIA mode. If the associated bit is ‘1,’ it indicates that the queue is enabled. **Note:** These bits must be programmed even when the device is not used in shared UTOPIA mode.

14 Registers (continued)

Table 100. Master Queue 4 (MQ4) (0156h)

These bits indicate which queues in the master device are enabled for shared UTOPIA mode.

Name	Bit Pos.	Type	Reset	Description
mast_queue_in[79:64]	15:0	RW	0	**Master Queue Indication [79:64].** Each bit in this field represents one of the 64—79 queues in the master device, where the least significant bit is queue 64, and most significant bit is queue 79. These bits indicate which queues in the master device are enabled for shared UTOPIA mode. If the associated bit is '1,' it indicates that the queue is enabled. **Note:** These bits must be programmed even when the device is not used in shared UTOPIA mode.

Table 101. Master Queue 3 (MQ3) (0158h)

These bits indicate which queues in the master device are enabled for shared UTOPIA mode.

Name	Bit Pos.	Type	Reset	Description
mast_queue_in[63:48]	15:0	RW	0	**Master Queue Indication [63:48].** Each bit in this field represents one of the 48—63 queues in the master device, where the least significant bit is queue 48, and most significant bit is queue 63. These bits indicate which queues in the master device are enabled for shared UTOPIA mode. If the associated bit is '1,' it indicates that the queue is enabled. **Note:** These bits must be programmed even when the device is not used in shared UTOPIA mode.

Table 102. Master Queue 2 (MQ2) (015Ah)

These bits indicate which queues in the master device are enabled for shared UTOPIA mode.

Name	Bit Pos.	Type	Reset	Description
mast_queue_in[47:32]	15:0	RW	0	**Master Queue Indication [47:32].** Each bit in this field represents one of the 32—47 queues in the master device, where the least significant bit is queue 32, and most significant bit is queue 47. These bits indicate which queues in the master device are enabled for shared UTOPIA mode. If the associated bit is '1,' it indicates that the queue is enabled. **Note:** These bits must be programmed even when the device is not used in shared UTOPIA mode.

14 Registers (continued)

Table 103. Master Queue 1 (MQ1) (015Ch)

These bits indicate which queues in the master device are enabled for shared UTOPIA mode.

Name	Bit Pos.	Type	Reset	Description
mast_queue_in[31:16]	15:0	RW	0	**Master Queue Indication [31:16].** Each bit in this field represents one of the 16—31 queues in the master device, where the least significant bit is queue 16, and most significant bit is queue 31. These bits indicate which queues in the master device are enabled for shared UTOPIA mode. If the associated bit is '1,' it indicates that the queue is enabled. **Note:** These bits must be programmed even when the device is not used in shared UTOPIA mode.

Table 104. Master Queue 0 (MQ0) (015Eh)

These bits indicate which queues in the master device are enabled for shared UTOPIA mode.

Name	Bit Pos.	Type	Reset	Description
mast_queue_in[15:0]	15:0	RW	0	**Master Queue Indication [15:0].** Each bit in this field represents one of the 0—15 queues in the master device, where the least significant bit is queue 0, and most significant bit is queue 15. These bits indicate which queues in the master device are enabled for shared UTOPIA mode. If the associated bit is '1,' it indicates that the queue is enabled. **Note:** These bits must be programmed even when the device is not used in shared UTOPIA mode.

14 Registers (continued)

Table 105. Slave Queue 7 (SQ7) (0160h)

Name	Bit Pos.	Type	Reset	Description
slav_queue_in[127:112]	15:0	RW	0	**Slave Queue Indication [127:112].** Each bit in this field represents one of the 112—127 queues in the slave device, where the least significant bit is queue 112, and most significant bit is queue 127. These bits indicate which queues in the slave device are enabled for shared UTOPIA mode. If the associated bit is '1,' it indicates to the master that the queue is enabled. These bits are only meaningful in shared UTOPIA mode and must be programmed in the master device.

Table 106. Slave Queue 6 (SQ6) (0162h)

Name	Bit Pos.	Type	Reset	Description
slav_queue_in[111:96]	15:0	RW	0	**Slave Queue Indication [111:96].** Each bit in this field represents one of the 96—111 queues in the slave device, where the least significant bit is queue 96, and most significant bit is queue 111. These bits indicate which queues in the slave device are enabled for shared UTOPIA mode. If the associated bit is '1,' it indicates to the master that the queue is enabled. These bits are only meaningful in shared UTOPIA mode and must be programmed in the master device.

14 Registers (continued)

Table 107. Slave Queue 5 (SQ5) (0164h)

Name	Bit Pos.	Type	Reset	Description
slav_queue_in[95:80]	15:0	RW	0	**Slave Queue Indication [95:80].** Each bit in this field represents one of the 80—95 queues in the slave device, where the least significant bit is queue 80, and most significant bit is queue 95. These bits indicate which queues in the slave device are enabled for shared UTOPIA mode. If the associated bit is '1,' it indicates to the master that the queue is enabled. These bits are only meaningful in shared UTOPIA mode and must be programmed in the master device.

Table 108. Slave Queue 4 (SQ4) (0166h)

Name	Bit Pos.	Type	Reset	Description
slav_queue_in[79:64]	15:0	RW	0	**Slave Queue Indication [79:64].** Each bit in this field represents one of the 64—79 queues in the slave device, where the least significant bit is queue 64, and most significant bit is queue 79. These bits indicate which queues in the slave device are enabled for shared UTOPIA mode. If the associated bit is '1,' it indicates to the master that the queue is enabled. These bits are only meaningful in shared UTOPIA mode and must be programmed in the master device.

Table 109. Slave Queue 3 (SQ3) (0168h)

Name	Bit Pos.	Type	Reset	Description
slav_queue_in[63:48]	15:0	RW	0	**Slave Queue Indication [63:48].** Each bit in this field represents one of the 48—63 queues in the slave device, where the least significant bit is queue 48, and most significant bit is queue 63. These bits indicate which queues in the slave device are enabled for shared UTOPIA mode. If the associated bit is '1,' it indicates to the master that the queue is enabled. These bits are only meaningful in shared UTOPIA mode and must be programmed in the master device.

14 Registers (continued)

Table 110. Slave Queue 2 (SQ2) (016Ah)

Name	Bit Pos.	Type	Reset	Description
slav_queue_in[47:32]	15:0	RW	0	**Slave Queue Indication [47:32].** Each bit in this field represents one of the 32—47 queues in the slave device, where the least significant bit is queue 32, and most significant bit is queue 47. These bits indicate which queues in the slave device are enabled for shared UTOPIA mode. If the associated bit is '1,' it indicates to the master that the queue is enabled. These bits are only meaningful in shared UTOPIA mode and must be programmed in the master device.

Table 111. Slave Queue 1 (SQ1) (016Ch)

Name	Bit Pos.	Type	Reset	Description
slav_queue_in[31:16]	15:0	RW	0	**Slave Queue Indication [31:16].** Each bit in this field represents one of the 16—31 queues in the slave device, where the least significant bit is queue 16, and most significant bit is queue 31. These bits indicate which queues in the slave device are enabled for shared UTOPIA mode. If the associated bit is '1,' it indicates to the master that the queue is enabled. These bits are only meaningful in shared UTOPIA mode and must be programmed in the master device.

Table 112. Slave Queue 0 (SQ0) (016Eh)

Name	Bit Pos.	Type	Reset	Description
slav_queue_in[15:0]	15:0	RW	0	**Slave Queue Indication [15:0].** Each bit in this field represents one of the 0—15 queues in the slave device, where the least significant bit is queue 0, and most significant bit is queue 15. These bits indicate which queues in the slave device are enabled for shared UTOPIA mode. If the associated bit is '1,' it indicates to the master that the queue is enabled. These bits are only meaningful in shared UTOPIA mode and must be programmed in the master device.

14 Registers (continued)

Table 113. TX PHY FIFO Routing 7 (TXPFR7) (0170h)

Name	Bit Pos.	Type	Reset	Description
port_rte[127:112]	15:0	RW	0	**Port Route [127:112].** These port routing bits are only used when 64 PHY ports are used. Each bit in this field represents one of the 112—127 queues in the device, where the least significant bit is queue 112, and most significant bit is queue 127. These 128 queues are divided into 32 groups of four queues each. The four queues of each group are divided between two PHY ports, as follows: Group 0—queues 0 to 3—ports 0 and 1 Group 1—queues 4 to 7—ports 2 and 3 Group 2—queues 8 to 11—ports 4 and 5 Group 3—queues 12 to 15—ports 6 and 7 Group 4—queues 16 to 19—ports 8 and 9 Group 5—queues 20 to 23—ports 10 and 11 Group 6—queues 24 to 27—ports 12 and 13 Group 7—queues 28 to 31—ports 14 and 15 Group 8—queues 32 to 35—ports 16 and 17 Group 9—queues 36 to 39—ports 18 and 19 Group 10—queues 40 to 43—ports 20 and 21 Group 11—queues 44 to 47—ports 22 and 23 Group 12—queues 48 to 51—ports 24 and 25 Group 13—queues 52 to 55—ports 26 and 27 Group 14—queues 56 to 59—ports 28 and 29 Group 15—queues 60 to 63—ports 30 and 31 Group 16—queues 64 to 67—ports 32 and 33 Group 17—queues 68 to 71—ports 34 and 35 Group 18—queues 72 to 75—ports 36 and 37 Group 19—queues 76 to 79—ports 38 and 39 Group 20—queues 80 to 83—ports 40 and 41 Group 21—queues 84 to 87—ports 42 and 43 Group 22—queues 88 to 91—ports 44 and 45 Group 23—queues 92 to 95—ports 46 and 47 Group 24—queues 96 to 99—ports 48 and 49 Group 25—queues 100 to 103—ports 50 and 51 Group 26—queues 104 to 107—ports 52 and 53 Group 27—queues 108 to 111—ports 54 and 55 Group 28—queues 112 to 115—ports 56 and 57 Group 29—queues 116 to 119—ports 58 and 59 Group 30—queues 120 to 123—ports 60 and 61 Group 31—queues 124 to 127—ports 62 and 63 The bits in this field assign each queue in the group to either the odd- or even-numbered PHY port in the group. If a bit is cleared to ‘0,’ the corresponding queue is assigned to the even-numbered port. If the bit is set to ‘1,’ the corresponding queue is assigned to the odd-numbered port. For 64 PHY ports, if the device is configured in **normal** 64-port mode, as described in Section 9.2.2, Outgoing ATM Mode (cells sent by T8208) and in Section 11.4, Queuing, this register is programmed to “1010101010101010.”

14 Registers (continued)

Table 114. TX PHY FIFO Routing 6 (TXPFR6) (0172h)

Name	Bit Pos.	Type	Reset	Description
port_rte[111:96]	15:0	RW	0	**Port Route [111:96].** These port routing bits are only used when 64 PHY ports are used. Each bit in this field represents one of the 96—111 queues in the device, where the least significant bit is queue 96, and most significant bit is queue 111. These 128 queues are divided into 32 groups of four queues each. The four queues of each group are divided between two PHY ports, as follows: Group 0—queues 0 to 3—ports 0 and 1 Group 1—queues 4 to 7—ports 2 and 3 Group 2—queues 8 to 11—ports 4 and 5 Group 3—queues 12 to 15—ports 6 and 7 Group 4—queues 16 to 19—ports 8 and 9 Group 5—queues 20 to 23—ports 10 and 11 Group 6—queues 24 to 27—ports 12 and 13 Group 7—queues 28 to 31—ports 14 and 15 Group 8—queues 32 to 35—ports 16 and 17 Group 9—queues 36 to 39—ports 18 and 19 Group 10—queues 40 to 43—ports 20 and 21 Group 11—queues 44 to 47—ports 22 and 23 Group 12—queues 48 to 51—ports 24 and 25 Group 13—queues 52 to 55—ports 26 and 27 Group 14—queues 56 to 59—ports 28 and 29 Group 15—queues 60 to 63—ports 30 and 31 Group 16—queues 64 to 67—ports 32 and 33 Group 17—queues 68 to 71—ports 34 and 35 Group 18—queues 72 to 75—ports 36 and 37 Group 19—queues 76 to 79—ports 38 and 39 Group 20—queues 80 to 83—ports 40 and 41 Group 21—queues 84 to 87—ports 42 and 43 Group 22—queues 88 to 91—ports 44 and 45 Group 23—queues 92 to 95—ports 46 and 47 Group 24—queues 96 to 99—ports 48 and 49 Group 25—queues 100 to 103—ports 50 and 51 Group 26—queues 104 to 107—ports 52 and 53 Group 27—queues 108 to 111—ports 54 and 55 Group 28—queues 112 to 115—ports 56 and 57 Group 29—queues 116 to 119—ports 58 and 59 Group 30—queues 120 to 123—ports 60 and 61 Group 31—queues 124 to 127—ports 62 and 63 The bits in this field assign each queue in the group to either the odd- or even-numbered PHY port in the group. If a bit is cleared to ‘0,’ the corresponding queue is assigned to the even-numbered port. If the bit is set to ‘1,’ the corresponding queue is assigned to the odd-numbered port. For 64 PHY ports, if the device is configured in **normal** 64-port mode, as described in Section 9.2.2, Outgoing ATM Mode (cells sent by T8208) and in Section 11.4, Queuing, this register is programmed to “1010101010101010.”

14 Registers (continued)

Table 115. TX PHY FIFO Routing 5 (TXPFR5) (0174h)

Name	Bit Pos.	Type	Reset	Description
port_rte[95:80]	15:0	RW	0	**Port Route [95:80].** These port routing bits are only used when 64 PHY ports are used. Each bit in this field represents one of the 80—95 queues in the device, where the least significant bit is queue 80, and most significant bit is queue 95. These 128 queues are divided into 32 groups of four queues each. The four queues of each group are divided between two PHY ports, as follows: Group 0—queues 0 to 3—ports 0 and 1 Group 1—queues 4 to 7—ports 2 and 3 Group 2—queues 8 to 11—ports 4 and 5 Group 3—queues 12 to 15—ports 6 and 7 Group 4—queues 16 to 19—ports 8 and 9 Group 5—queues 20 to 23—ports 10 and 11 Group 6—queues 24 to 27—ports 12 and 13 Group 7—queues 28 to 31—ports 14 and 15 Group 8—queues 32 to 35—ports 16 and 17 Group 9—queues 36 to 39—ports 18 and 19 Group 10—queues 40 to 43—ports 20 and 21 Group 11—queues 44 to 47—ports 22 and 23 Group 12—queues 48 to 51—ports 24 and 25 Group 13—queues 52 to 55—ports 26 and 27 Group 14—queues 56 to 59—ports 28 and 29 Group 15—queues 60 to 63—ports 30 and 31 Group 16—queues 64 to 67—ports 32 and 33 Group 17—queues 68 to 71—ports 34 and 35 Group 18—queues 72 to 75—ports 36 and 37 Group 19—queues 76 to 79—ports 38 and 39 Group 20—queues 80 to 83—ports 40 and 41 Group 21—queues 84 to 87—ports 42 and 43 Group 22—queues 88 to 91—ports 44 and 45 Group 23—queues 92 to 95—ports 46 and 47 Group 24—queues 96 to 99—ports 48 and 49 Group 25—queues 100 to 103—ports 50 and 51 Group 26—queues 104 to 107—ports 52 and 53 Group 27—queues 108 to 111—ports 54 and 55 Group 28—queues 112 to 115—ports 56 and 57 Group 29—queues 116 to 119—ports 58 and 59 Group 30—queues 120 to 123—ports 60 and 61 Group 31—queues 124 to 127—ports 62 and 63 The bits in this field assign each queue in the group to either the odd- or even-numbered PHY port in the group. If a bit is cleared to ‘0,’ the corresponding queue is assigned to the even-numbered port. If the bit is set to ‘1,’ the corresponding queue is assigned to the odd-numbered port. For 64 PHY ports, if the device is configured in **normal** 64-port mode, as described in Section 9.2.2, Outgoing ATM Mode (cells sent by T8208) and in Section 11.4, Queuing, this register is programmed to “1010101010101010.”

14 Registers (continued)

Table 116. TX PHY FIFO Routing 4 (TXPFR4) (0176h)

Name	Bit Pos.	Type	Reset	Description
port_rte[79:64]	15:0	RW	0	**Port Route [79:64].** These port routing bits are only used when 64 PHY ports are used. Each bit in this field represents one of the 64—79 queues in the device, where the least significant bit is queue 64, and most significant bit is queue 79. These 128 queues are divided into 32 groups of four queues each. The four queues of each group are divided between two PHY ports, as follows: Group 0—queues 0 to 3—ports 0 and 1 Group 1—queues 4 to 7—ports 2 and 3 Group 2—queues 8 to 11—ports 4 and 5 Group 3—queues 12 to 15—ports 6 and 7 Group 4—queues 16 to 19—ports 8 and 9 Group 5—queues 20 to 23—ports 10 and 11 Group 6—queues 24 to 27—ports 12 and 13 Group 7—queues 28 to 31—ports 14 and 15 Group 8—queues 32 to 35—ports 16 and 17 Group 9—queues 36 to 39—ports 18 and 19 Group 10—queues 40 to 43—ports 20 and 21 Group 11—queues 44 to 47—ports 22 and 23 Group 12—queues 48 to 51—ports 24 and 25 Group 13—queues 52 to 55—ports 26 and 27 Group 14—queues 56 to 59—ports 28 and 29 Group 15—queues 60 to 63—ports 30 and 31 Group 16—queues 64 to 67—ports 32 and 33 Group 17—queues 68 to 71—ports 34 and 35 Group 18—queues 72 to 75—ports 36 and 37 Group 19—queues 76 to 79—ports 38 and 39 Group 20—queues 80 to 83—ports 40 and 41 Group 21—queues 84 to 87—ports 42 and 43 Group 22—queues 88 to 91—ports 44 and 45 Group 23—queues 92 to 95—ports 46 and 47 Group 24—queues 96 to 99—ports 48 and 49 Group 25—queues 100 to 103—ports 50 and 51 Group 26—queues 104 to 107—ports 52 and 53 Group 27—queues 108 to 111—ports 54 and 55 Group 28—queues 112 to 115—ports 56 and 57 Group 29—queues 116 to 119—ports 58 and 59 Group 30—queues 120 to 123—ports 60 and 61 Group 31—queues 124 to 127—ports 62 and 63 The bits in this field assign each queue in the group to either the odd- or even-numbered PHY port in the group. If a bit is cleared to ‘0,’ the corresponding queue is assigned to the even-numbered port. If the bit is set to ‘1,’ the corresponding queue is assigned to the odd-numbered port. For 64 PHY ports, if the device is configured in **normal** 64-port mode, as described in Section 9.2.2, Outgoing ATM Mode (cells sent by T8208) and in Section 11.4, Queuing, this register is programmed to “1010101010101010.”

14 Registers (continued)

Table 117. TX PHY FIFO Routing 3 (TXPFR3) (0178h)

Name	Bit Pos.	Type	Reset	Description
port_rte[63:48]	15:0	RW	0	**Port Route [48:63].** These port routing bits are only used when 64 PHY ports are used. Each bit in this field represents one of the 48—63 queues in the device, where the least significant bit is queue 48, and most significant bit is queue 63. These 128 queues are divided into 32 groups of four queues each. The four queues of each group are divided between two PHY ports, as follows: Group 0—queues 0 to 3—ports 0 and 1 Group 1—queues 4 to 7—ports 2 and 3 Group 2—queues 8 to 11—ports 4 and 5 Group 3—queues 12 to 15—ports 6 and 7 Group 4—queues 16 to 19—ports 8 and 9 Group 5—queues 20 to 23—ports 10 and 11 Group 6—queues 24 to 27—ports 12 and 13 Group 7—queues 28 to 31—ports 14 and 15 Group 8—queues 32 to 35—ports 16 and 17 Group 9—queues 36 to 39—ports 18 and 19 Group 10—queues 40 to 43—ports 20 and 21 Group 11—queues 44 to 47—ports 22 and 23 Group 12—queues 48 to 51—ports 24 and 25 Group 13—queues 52 to 55—ports 26 and 27 Group 14—queues 56 to 59—ports 28 and 29 Group 15—queues 60 to 63—ports 30 and 31 Group 16—queues 64 to 67—ports 32 and 33 Group 17—queues 68 to 71—ports 34 and 35 Group 18—queues 72 to 75—ports 36 and 37 Group 19—queues 76 to 79—ports 38 and 39 Group 20—queues 80 to 83—ports 40 and 41 Group 21—queues 84 to 87—ports 42 and 43 Group 22—queues 88 to 91—ports 44 and 45 Group 23—queues 92 to 95—ports 46 and 47 Group 24—queues 96 to 99—ports 48 and 49 Group 25—queues 100 to 103—ports 50 and 51 Group 26—queues 104 to 107—ports 52 and 53 Group 27—queues 108 to 111—ports 54 and 55 Group 28—queues 112 to 115—ports 56 and 57 Group 29—queues 116 to 119—ports 58 and 59 Group 30—queues 120 to 123—ports 60 and 61 Group 31—queues 124 to 127—ports 62 and 63 The bits in this field assign each queue in the group to either the odd- or even-numbered PHY port in the group. If a bit is cleared to ‘0,’ the corresponding queue is assigned to the even-numbered port. If the bit is set to ‘1,’ the corresponding queue is assigned to the odd-numbered port. For 64 PHY ports, if the device is configured in **normal** 64-port mode, as described in Section 9.2.2, Outgoing ATM Mode (cells sent by T8208) and in Section 11.4, Queuing, this register is programmed to “1010101010101010.”

14 Registers (continued)

Table 118. TX PHY FIFO Routing 2 (TXPFR2) (017Ah)

Name	Bit Pos.	Type	Reset	Description
port_rte[47:32]	15:0	RW	0	**Port Route [32:47].** These port routing bits are only used when 64 PHY ports are used. Each bit in this field represents one of the 32—47 queues in the device, where the least significant bit is queue 32, and most significant bit is queue 47. These 128 queues are divided into 32 groups of four queues each. The four queues of each group are divided between two PHY ports, as follows: Group 0—queues 0 to 3—ports 0 and 1 Group 1—queues 4 to 7—ports 2 and 3 Group 2—queues 8 to 11—ports 4 and 5 Group 3—queues 12 to 15—ports 6 and 7 Group 4—queues 16 to 19—ports 8 and 9 Group 5—queues 20 to 23—ports 10 and 11 Group 6—queues 24 to 27—ports 12 and 13 Group 7—queues 28 to 31—ports 14 and 15 Group 8—queues 32 to 35—ports 16 and 17 Group 9—queues 36 to 39—ports 18 and 19 Group 10—queues 40 to 43—ports 20 and 21 Group 11—queues 44 to 47—ports 22 and 23 Group 12—queues 48 to 51—ports 24 and 25 Group 13—queues 52 to 55—ports 26 and 27 Group 14—queues 56 to 59—ports 28 and 29 Group 15—queues 60 to 63—ports 30 and 31 Group 16—queues 64 to 67—ports 32 and 33 Group 17—queues 68 to 71—ports 34 and 35 Group 18—queues 72 to 75—ports 36 and 37 Group 19—queues 76 to 79—ports 38 and 39 Group 20—queues 80 to 83—ports 40 and 41 Group 21—queues 84 to 87—ports 42 and 43 Group 22—queues 88 to 91—ports 44 and 45 Group 23—queues 92 to 95—ports 46 and 47 Group 24—queues 96 to 99—ports 48 and 49 Group 25—queues 100 to 103—ports 50 and 51 Group 26—queues 104 to 107—ports 52 and 53 Group 27—queues 108 to 111—ports 54 and 55 Group 28—queues 112 to 115—ports 56 and 57 Group 29—queues 116 to 119—ports 58 and 59 Group 30—queues 120 to 123—ports 60 and 61 Group 31—queues 124 to 127—ports 62 and 63 The bits in this field assign each queue in the group to either the odd- or even-numbered PHY port in the group. If a bit is cleared to ‘0,’ the corresponding queue is assigned to the even-numbered port. If the bit is set to ‘1,’ the corresponding queue is assigned to the odd-numbered port. For 64 PHY ports, if the device is configured in **normal** 64-port mode, as described in Section 9.2.2, Outgoing ATM Mode (cells sent by T8208) and in Section 11.4, Queuing, this register is programmed to “1010101010101010.”

14 Registers (continued)

Table 119. TX PHY FIFO Routing 1 (TXPFR1) (017Ch)

Name	Bit Pos.	Type	Reset	Description
port_rte[31:16]	15:0	RW	0	**Port Route [31:16].** These port routing bits are only used when 64 PHY ports are used. Each bit in this field represents one of the 16—31 queues in the device, where the least significant bit is queue 16, and most significant bit is queue 31. These 128 queues are divided into 32 groups of four queues each. The four queues of each group are divided between two PHY ports, as follows: Group 0—queues 0 to 3—ports 0 and 1 Group 1—queues 4 to 7—ports 2 and 3 Group 2—queues 8 to 11—ports 4 and 5 Group 3—queues 12 to 15—ports 6 and 7 Group 4—queues 16 to 19—ports 8 and 9 Group 5—queues 20 to 23—ports 10 and 11 Group 6—queues 24 to 27—ports 12 and 13 Group 7—queues 28 to 31—ports 14 and 15 Group 8—queues 32 to 35—ports 16 and 17 Group 9—queues 36 to 39—ports 18 and 19 Group 10—queues 40 to 43—ports 20 and 21 Group 11—queues 44 to 47—ports 22 and 23 Group 12—queues 48 to 51—ports 24 and 25 Group 13—queues 52 to 55—ports 26 and 27 Group 14—queues 56 to 59—ports 28 and 29 Group 15—queues 60 to 63—ports 30 and 31 Group 16—queues 64 to 67—ports 32 and 33 Group 17—queues 68 to 71—ports 34 and 35 Group 18—queues 72 to 75—ports 36 and 37 Group 19—queues 76 to 79—ports 38 and 39 Group 20—queues 80 to 83—ports 40 and 41 Group 21—queues 84 to 87—ports 42 and 43 Group 22—queues 88 to 91—ports 44 and 45 Group 23—queues 92 to 95—ports 46 and 47 Group 24—queues 96 to 99—ports 48 and 49 Group 25—queues 100 to 103—ports 50 and 51 Group 26—queues 104 to 107—ports 52 and 53 Group 27—queues 108 to 111—ports 54 and 55 Group 28—queues 112 to 115—ports 56 and 57 Group 29—queues 116 to 119—ports 58 and 59 Group 30—queues 120 to 123—ports 60 and 61 Group 31—queues 124 to 127—ports 62 and 63 The bits in this field assign each queue in the group to either the odd- or even-numbered PHY port in the group. If a bit is cleared to ‘0,’ the corresponding queue is assigned to the even-numbered port. If the bit is set to ‘1,’ the corresponding queue is assigned to the odd-numbered port. For 64 PHY ports, if the device is configured in **normal** 64-port mode, as described in Section 9.2.2, Outgoing ATM Mode (cells sent by T8208) and in Section 11.4, Queuing, this register is programmed to “1010101010101010.”

14 Registers (continued)

Table 120. TX PHY FIFO Routing 0 (TXPFR0) (017Eh)

Name	Bit Pos.	Type	Reset	Description
port_rte[15:0]	15:0	RW	0	**Port Route [15:0].** These port routing bits are only used when 64 PHY ports are used. Each bit in this field represents one of the 0—15 queues in the device, where the least significant bit is queue 0, and most significant bit is queue 15. These 128 queues are divided into 32 groups of four queues each. The four queues of each group are divided between two PHY ports, as follows: Group 0—queues 0 to 3—ports 0 and 1 Group 1—queues 4 to 7—ports 2 and 3 Group 2—queues 8 to 11—ports 4 and 5 Group 3—queues 12 to 15—ports 6 and 7 Group 4—queues 16 to 19—ports 8 and 9 Group 5—queues 20 to 23—ports 10 and 11 Group 6—queues 24 to 27—ports 12 and 13 Group 7—queues 28 to 31—ports 14 and 15 Group 8—queues 32 to 35—ports 16 and 17 Group 9—queues 36 to 39—ports 18 and 19 Group 10—queues 40 to 43—ports 20 and 21 Group 11—queues 44 to 47—ports 22 and 23 Group 12—queues 48 to 51—ports 24 and 25 Group 13—queues 52 to 55—ports 26 and 27 Group 14—queues 56 to 59—ports 28 and 29 Group 15—queues 60 to 63—ports 30 and 31 Group 16—queues 64 to 67—ports 32 and 33 Group 17—queues 68 to 71—ports 34 and 35 Group 18—queues 72 to 75—ports 36 and 37 Group 19—queues 76 to 79—ports 38 and 39 Group 20—queues 80 to 83—ports 40 and 41 Group 21—queues 84 to 87—ports 42 and 43 Group 22—queues 88 to 91—ports 44 and 45 Group 23—queues 92 to 95—ports 46 and 47 Group 24—queues 96 to 99—ports 48 and 49 Group 25—queues 100 to 103—ports 50 and 51 Group 26—queues 104 to 107—ports 52 and 53 Group 27—queues 108 to 111—ports 54 and 55 Group 28—queues 112 to 115—ports 56 and 57 Group 29—queues 116 to 119—ports 58 and 59 Group 30—queues 120 to 123—ports 60 and 61 Group 31—queues 124 to 127—ports 62 and 63 The bits in this field assign each queue in the group to either the odd- or even-numbered PHY port in the group. If a bit is cleared to ‘0,’ the corresponding queue is assigned to the even-numbered port. If the bit is set to ‘1,’ the corresponding queue is assigned to the odd-numbered port. For 64 PHY ports, if the device is configured in **normal** 64-port mode, as described in Section 9.2.2, Outgoing ATM Mode (cells sent by T8208, and in Section 11.4, Queuing, this register is programmed to “1010101010101010.”

14 Registers (continued)

Table 121. Global Bypass SDRAM Control Register (GBSCR) (01B0h)

Name	Bit Pos.	Type	Reset	Description
Reserved	9:0	RO	0	**Reserved.** Program to ‘0.’
ovrn_ie	10	RW	0	**Overrun Interrupt Enable.** An interrupt is generated if this bit and any of the overrun status bits in registers 01C0h—01DEh are set. The interrupt is generated until this bit or the corresponding status bit is reset.
Reserved	15:11	RO	0	**Reserved.** Program to ‘0.’

14 Registers (continued)

Table 122. Bypass SDRAM Service Request Register (BSSR) (01BEh)

Name	Bit Pos.	Type	Reset	Description
Queue_serv[7:0]	0	RO	0	**Queue Service[7:0].** This bit represents interrupt status (register 01C0h) of queues 7 to 0 of the TX UTOPIA cell buffer. If this bit is set, at least one of the queues 7 to 0 has interrupt status bits that need servicing.
Queue_serv[15:8]	1	RO	0	**Queue Service[15:8].** This bit represents interrupt status (register 01C2h) of queues 15 to 8 of the TX UTOPIA cell buffer. If this bit is set, at least one of the queues 15 to 8 has interrupt status bits that need servicing.
Queue_serv[23:16]	2	RO	0	**Queue Service[23:16].** This bit represents interrupt status (register 01C4h) of queues 23 to 16 of the TX UTOPIA cell buffer. If this bit is set, at least one of the queues 23 to 16 has interrupt status bits that need servicing.
Queue_serv[31:24]	3	RO	0	**Queue Service[31:24].** This bit represents interrupt status (register 01C6h) of queues 31 to 24 of the TX UTOPIA cell buffer. If this bit is set, at least one of the queues 31 to 24 has interrupt status bits that need servicing.
Queue_serv[39:32]	4	RO	0	**Queue Service[39:32].** This bit represents interrupt status (register 01C8h) of queues 39 to 32 of the TX UTOPIA cell buffer. If this bit is set, at least one of the queues 39 to 32 has interrupt status bits that need servicing.
Queue_serv[47:40]	5	RO	0	**Queue Service[47:40].** This bit represents interrupt status (register 01CAh) of queues 47 to 40 of the TX UTOPIA cell buffer. If this bit is set, at least one of the queues 47 to 40 has interrupt status bits that need servicing.
Queue_serv[55:48]	6	RO	0	**Queue Service[55:48].** This bit represents interrupt status (register 01CCh) of queues 55 to 48 of the TX UTOPIA cell buffer. If this bit is set, at least one of the queues 55 to 48 has interrupt status bits that need servicing.
Queue_serv[63:56]	7	RO	0	**Queue Service[63:56].** This bit represents interrupt status (register 01CEh) of queues 63 to 56 of the TX UTOPIA cell buffer. If this bit is set, at least one of the queues 63 to 56 has interrupt status bits that need servicing.
Queue_serv[71:64]	8	RO	0	**Queue Service[71:64].** This bit represents interrupt status (register 01D0h) of queues 71 to 64 of the TX UTOPIA cell buffer. If this bit is set, at least one of the queues 71 to 64 has interrupt status bits that need servicing.
Queue_serv[79:72]	9	RO	0	**Queue Service[79:72].** This bit represents interrupt status (register 01D2h) of queues 79 to 72 of the TX UTOPIA cell buffer. If this bit is set, at least one of the queues 79 to 72 has interrupt status bits that need servicing.
Queue_serv[87:80]	10	RO	0	**Queue Service[87:80].** This bit represents interrupt status (register 01D4h) of queues 87 to 80 of the TX UTOPIA cell buffer. If this bit is set, at least one of the queues 87 to 80 has interrupt status bits that need servicing.
Queue_serv[95:88]	11	RO	0	**Queue Service[95:88].** This bit represents interrupt status (register 01D6h) of queues 95 to 88 of the TX UTOPIA cell buffer. If this bit is set, at least one of the queues 95 to 88 has interrupt status bits that need servicing.

14 Registers (continued)

Table 122. Bypass SDRAM Service Request Register (BSSR) (01BEh) (continued)

Name	Bit Pos.	Type	Reset	Description
Queue_serv[103:96]	12	RO	0	**Queue Service[103:96].** This bit represents interrupt status (register 01D8h) of queues 103 to 96 of the TX UTOPIA cell buffer. If this bit is set, at least one of the queues 103 to 96 has interrupt status bits that need servicing.
Queue_serv[111:104]	13	RO	0	**Queue Service[111:104].** This bit represents interrupt status (register 01DAh) of queues 111 to 104 of the TX UTOPIA cell buffer. If this bit is set, at least one of the queues 111 to 104 has interrupt status bits that need servicing.
Queue_serv[119:112]	14	RO	0	**Queue Service[119:112].** This bit represents interrupt status (register 01DCh) of queues 119 to 112 of the TX UTOPIA cell buffer. If this bit is set, at least one of the queues 119 to 112 has interrupt status bits that need servicing.
Queue_serv[127:120]	15	RO	0	**Queue Service[127:120].** This bit represents interrupt status (register 01DEh) of queues 127 to 120 of the TX UTOPIA cell buffer. If this bit is set, at least one of the queues 127 to 120 has interrupt status bits that need servicing.

14 Registers (continued)

Table 123. Bypass SDRAM Queue Interrupt Status Register 0 (BSQISR0) (01C0h)

Name	Bit Pos.	Type	Reset	Description
Reserved	0	RO	0	**Reserved.**
q0_ovrn	1	RO	0	**Queue 0 Overrun.** This bit is set when queue 0 overruns. An interrupt is generated if the corresponding enable bit is set.
Reserved	2	RO	0	**Reserved.**
q1_ovrn	3	RO	0	**Queue 1 Overrun.** This bit is set when queue 1 overruns. An interrupt is generated if the corresponding enable bit is set.
Reserved	4	RO	0	**Reserved.**
q2_ovrn	5	RO	0	**Queue 2 Overrun.** This bit is set when queue 2 overruns. An interrupt is generated if the corresponding enable bit is set.
Reserved	6	RO	0	**Reserved.**
q3_ovrn	7	RO	0	**Queue 3 Overrun.** This bit is set when queue 3 overruns. An interrupt is generated if the corresponding enable bit is set.
Reserved	8	RO	0	**Reserved.**
q4_ovrn	9	RO	0	**Queue 4 Overrun.** This bit is set when queue 4 overruns. An interrupt is generated if the corresponding enable bit is set.
Reserved	10	RO	0	**Reserved.**
q5_ovrn	11	RO	0	**Queue 5 Overrun.** This bit is set when queue 5 overruns. An interrupt is generated if the corresponding enable bit is set.
Reserved	12	RO	0	**Reserved.**
q6_ovrn	13	RO	0	**Queue 6 Overrun.** This bit is set when queue 6 overruns. An interrupt is generated if the corresponding enable bit is set.
Reserved	14	RO	0	**Reserved.**
q7_ovrn	15	RO	0	**Queue 7 Overrun.** This bit is set when queue 7 overruns. An interrupt is generated if the corresponding enable bit is set.

14 Registers (continued)

Table 124. Bypass SDRAM Queue Interrupt Status Register 1 (BSQISR1) (01C2h)

Name	Bit Pos.	Type	Reset	Description
Reserved	0	RO	0	**Reserved.**
q8_ovrn	1	RO	0	**Queue 8 Overrun.** This bit is set when queue 8 overruns. An interrupt is generated if the corresponding enable bit is set.
Reserved	2	RO	0	**Reserved.**
q9_ovrn	3	RO	0	**Queue 9 Overrun.** This bit is set when queue 9 overruns. An interrupt is generated if the corresponding enable bit is set.
Reserved	4	RO	0	**Reserved.**
q10_ovrn	5	RO	0	**Queue 10 Overrun.** This bit is set when queue 10 overruns. An interrupt is generated if the corresponding enable bit is set.
Reserved	6	RO	0	**Reserved.**
q11_ovrn	7	RO	0	**Queue 11 Overrun.** This bit is set when queue 11 overruns. An interrupt is generated if the corresponding enable bit is set.
Reserved	8	RO	0	**Reserved.**
q12_ovrn	9	RO	0	**Queue 12 Overrun.** This bit is set when queue 12 overruns. An interrupt is generated if the corresponding enable bit is set.
Reserved	10	RO	0	**Reserved.**
q13_ovrn	11	RO	0	**Queue 13 Overrun.** This bit is set when queue 13 overruns. An interrupt is generated if the corresponding enable bit is set.
Reserved	12	RO	0	**Reserved.**
q14_ovrn	13	RO	0	**Queue 14 Overrun.** This bit is set when queue 14 overruns. An interrupt is generated if the corresponding enable bit is set.
Reserved	14	RO	0	**Reserved.**
q15_ovrn	15	RO	0	**Queue 15 Overrun.** This bit is set when queue 15 overruns. An interrupt is generated if the corresponding enable bit is set.

14 Registers (continued)

Table 125. Bypass SDRAM Queue Interrupt Status Register 2 (BSQISR2) (01C4h)

Name	Bit Pos.	Type	Reset	Description
Reserved	0	RO	0	**Reserved.**
q16_ovrn	1	RO	0	**Queue 16 Overrun.** This bit is set when queue 16 overruns. An interrupt is generated if the corresponding enable bit is set.
Reserved	2	RO	0	**Reserved.**
q17_ovrn	3	RO	0	**Queue 17 Overrun.** This bit is set when queue 17 overruns. An interrupt is generated if the corresponding enable bit is set.
Reserved	4	RO	0	**Reserved.**
q18_ovrn	5	RO	0	**Queue 18 Overrun.** This bit is set when queue 18 overruns. An interrupt is generated if the corresponding enable bit is set.
Reserved	6	RO	0	**Reserved.**
q19_ovrn	7	RO	0	**Queue 19 Overrun.** This bit is set when queue 19 overruns. An interrupt is generated if the corresponding enable bit is set.
Reserved	8	RO	0	**Reserved.**
q20_ovrn	9	RO	0	**Queue 20 Overrun.** This bit is set when queue 20 overruns. An interrupt is generated if the corresponding enable bit is set.
Reserved	10	RO	0	**Reserved.**
q21_ovrn	11	RO	0	**Queue 21 Overrun.** This bit is set when queue 21 overruns. An interrupt is generated if the corresponding enable bit is set.
Reserved	12	RO	0	**Reserved.**
q22_ovrn	13	RO	0	**Queue 22 Overrun.** This bit is set when queue 22 overruns. An interrupt is generated if the corresponding enable bit is set.
Reserved	14	RO	0	**Reserved.**
q23_ovrn	15	RO	0	**Queue 23 Overrun.** This bit is set when queue 23 overruns. An interrupt is generated if the corresponding enable bit is set.

14 Registers (continued)

Table 126. Bypass SDRAM Queue Interrupt Status Register 3 (BSQIS30) (01C6h)

Name	Bit Pos.	Type	Reset	Description
Reserved	0	RO	0	**Reserved.**
q24_ovrn	1	RO	0	**Queue 24 Overrun.** This bit is set when queue 24 overruns. An interrupt is generated if the corresponding enable bit is set.
Reserved	2	RO	0	**Reserved.**
q25_ovrn	3	RO	0	**Queue 25 Overrun.** This bit is set when queue 25 overruns. An interrupt is generated if the corresponding enable bit is set.
Reserved	4	RO	0	**Reserved.**
q26_ovrn	5	RO	0	**Queue 26 Overrun.** This bit is set when queue 26 overruns. An interrupt is generated if the corresponding enable bit is set.
Reserved	6	RO	0	**Reserved.**
q27_ovrn	7	RO	0	**Queue 27 Overrun.** This bit is set when queue 27 overruns. An interrupt is generated if the corresponding enable bit is set.
Reserved	8	RO	0	**Reserved.**
q28_ovrn	9	RO	0	**Queue 28 Overrun.** This bit is set when queue 28 overruns. An interrupt is generated if the corresponding enable bit is set.
Reserved	10	RO	0	**Reserved.**
q29_ovrn	11	RO	0	**Queue 29 Overrun.** This bit is set when queue 29 overruns. An interrupt is generated if the corresponding enable bit is set.
Reserved	12	RO	0	**Reserved.**
q30_ovrn	13	RO	0	**Queue 30 Overrun.** This bit is set when queue 30 overruns. An interrupt is generated if the corresponding enable bit is set.
Reserved	14	RO	0	**Reserved.**
q31_ovrn	15	RO	0	**Queue 31 Overrun.** This bit is set when queue 31 overruns. An interrupt is generated if the corresponding enable bit is set.

14 Registers (continued)

Table 127. Bypass SDRAM Queue Interrupt Status Register 4 (BSQISR4) (01C8h)

Name	Bit Pos.	Type	Reset	Description
Reserved	0	RO	0	**Reserved.**
q32_ovrn	1	RO	0	**Queue 32 Overrun.** This bit is set when queue 32 overruns. An interrupt is generated if the corresponding enable bit is set.
Reserved	2	RO	0	**Reserved.**
q33_ovrn	3	RO	0	**Queue 33 Overrun.** This bit is set when queue 33 overruns. An interrupt is generated if the corresponding enable bit is set.
Reserved	4	RO	0	**Reserved.**
q34_ovrn	5	RO	0	**Queue 34 Overrun.** This bit is set when queue 34 overruns. An interrupt is generated if the corresponding enable bit is set.
Reserved	6	RO	0	**Reserved.**
q35_ovrn	7	RO	0	**Queue 35 Overrun.** This bit is set when queue 35 overruns. An interrupt is generated if the corresponding enable bit is set.
Reserved	8	RO	0	**Reserved.**
q36_ovrn	9	RO	0	**Queue 36 Overrun.** This bit is set when queue 36 overruns. An interrupt is generated if the corresponding enable bit is set.
Reserved	10	RO	0	**Reserved.**
q37_ovrn	11	RO	0	**Queue 37 Overrun.** This bit is set when queue 37 overruns. An interrupt is generated if the corresponding enable bit is set.
Reserved	12	RO	0	**Reserved.**
q38_ovrn	13	RO	0	**Queue 38 Overrun.** This bit is set when queue 38 overruns. An interrupt is generated if the corresponding enable bit is set.
Reserved	14	RO	0	**Reserved.**
q39_ovrn	15	RO	0	**Queue 39 Overrun.** This bit is set when queue 39 overruns. An interrupt is generated if the corresponding enable bit is set.

14 Registers (continued)

Table 128. Bypass SDRAM Queue Interrupt Status Register 5 (BSQISR5) (01CAh)

Name	Bit Pos.	Type	Reset	Description
Reserved	0	RO	0	**Reserved.**
q40_ovrn	1	RO	0	**Queue 40 Overrun.** This bit is set when queue 40 overruns. An interrupt is generated if the corresponding enable bit is set.
Reserved	2	RO	0	**Reserved.**
q41_ovrn	3	RO	0	**Queue 41 Overrun.** This bit is set when queue 41 overruns. An interrupt is generated if the corresponding enable bit is set.
Reserved	4	RO	0	**Reserved.**
q42_ovrn	5	RO	0	**Queue 42 Overrun.** This bit is set when queue 42 overruns. An interrupt is generated if the corresponding enable bit is set.
Reserved	6	RO	0	**Reserved.**
q43_ovrn	7	RO	0	**Queue 43 Overrun.** This bit is set when queue 43 overruns. An interrupt is generated if the corresponding enable bit is set.
Reserved	8	RO	0	**Reserved.**
q44_ovrn	9	RO	0	**Queue 44 Overrun.** This bit is set when queue 44 overruns. An interrupt is generated if the corresponding enable bit is set.
Reserved	10	RO	0	**Reserved.**
q45_ovrn	11	RO	0	**Queue 45 Overrun.** This bit is set when queue 45 overruns. An interrupt is generated if the corresponding enable bit is set.
Reserved	12	RO	0	**Reserved.**
q46_ovrn	13	RO	0	**Queue 46 Overrun.** This bit is set when queue 46 overruns. An interrupt is generated if the corresponding enable bit is set.
Reserved	14	RO	0	**Reserved.**
q47_ovrn	15	RO	0	**Queue 47 Overrun.** This bit is set when queue 47 overruns. An interrupt is generated if the corresponding enable bit is set.

14 Registers (continued)

Table 129. Bypass SDRAM Queue Interrupt Status Register 6 (BSQISR6) (01CCh)

Name	Bit Pos.	Type	Reset	Description
Reserved	0	RO	0	**Reserved.**
q48_ovrn	1	RO	0	**Queue 48 Overrun.** This bit is set when queue 48 overruns. An interrupt is generated if the corresponding enable bit is set.
Reserved	2	RO	0	**Reserved.**
q49_ovrn	3	RO	0	**Queue 49 Overrun.** This bit is set when queue 49 overruns. An interrupt is generated if the corresponding enable bit is set.
Reserved	4	RO	0	**Reserved.**
q50_ovrn	5	RO	0	**Queue 50 Overrun.** This bit is set when queue 50 overruns. An interrupt is generated if the corresponding enable bit is set.
Reserved	6	RO	0	**Reserved.**
q51_ovrn	7	RO	0	**Queue 51 Overrun.** This bit is set when queue 51 overruns. An interrupt is generated if the corresponding enable bit is set.
Reserved	8	RO	0	**Reserved.**
q52_ovrn	9	RO	0	**Queue 52 Overrun.** This bit is set when queue 52 overruns. An interrupt is generated if the corresponding enable bit is set.
Reserved	10	RO	0	**Reserved.**
q53_ovrn	11	RO	0	**Queue 53 Overrun.** This bit is set when queue 53 overruns. An interrupt is generated if the corresponding enable bit is set.
Reserved	12	RO	0	**Reserved.**
q54_ovrn	13	RO	0	**Queue 54 Overrun.** This bit is set when queue 54 overruns. An interrupt is generated if the corresponding enable bit is set.
Reserved	14	RO	0	**Reserved.**
q55_ovrn	15	RO	0	**Queue 55 Overrun.** This bit is set when queue 55 overruns. An interrupt is generated if the corresponding enable bit is set.

14 Registers (continued)

Table 130. Bypass SDRAM Queue Interrupt Status Register 7 (BSQISR7) (01CEh)

Name	Bit Pos.	Type	Reset	Description
Reserved	0	RO	0	**Reserved.**
q56_ovrn	1	RO	0	**Queue 56 Overrun.** This bit is set when queue 56 overruns. An interrupt is generated if the corresponding enable bit is set.
Reserved	2	RO	0	**Reserved.**
q57_ovrn	3	RO	0	**Queue 57 Overrun.** This bit is set when queue 57 overruns. An interrupt is generated if the corresponding enable bit is set.
Reserved	4	RO	0	**Reserved.**
q58_ovrn	5	RO	0	**Queue 58 Overrun.** This bit is set when queue 58 overruns. An interrupt is generated if the corresponding enable bit is set.
Reserved	6	RO	0	**Reserved.**
q59_ovrn	7	RO	0	**Queue 59 Overrun.** This bit is set when queue 59 overruns. An interrupt is generated if the corresponding enable bit is set.
Reserved	8	RO	0	**Reserved.**
q60_ovrn	9	RO	0	**Queue 60 Overrun.** This bit is set when queue 60 overruns. An interrupt is generated if the corresponding enable bit is set.
Reserved	10	RO	0	**Reserved.**
q61_ovrn	11	RO	0	**Queue 61 Overrun.** This bit is set when queue 61 overruns. An interrupt is generated if the corresponding enable bit is set.
Reserved	12	RO	0	**Reserved.**
q62_ovrn	13	RO	0	**Queue 62 Overrun.** This bit is set when queue 62 overruns. An interrupt is generated if the corresponding enable bit is set.
Reserved	14	RO	0	**Reserved.**
q63_ovrn	15	RO	0	**Queue 63 Overrun.** This bit is set when queue 63 overruns. An interrupt is generated if the corresponding enable bit is set.

14 Registers (continued)

Table 131. Bypass SDRAM Queue Interrupt Status Register 8 (BSQISR8) (01D0h)

Name	Bit Pos.	Type	Reset	Description
Reserved	0	RO	0	**Reserved.**
q64_ovrn	1	RO	0	**Queue 64 Overrun.** This bit is set when queue 64 overruns. An interrupt is generated if the corresponding enable bit is set.
Reserved	2	RO	0	**Reserved.**
q65_ovrn	3	RO	0	**Queue 65 Overrun.** This bit is set when queue 65 overruns. An interrupt is generated if the corresponding enable bit is set.
Reserved	4	RO	0	**Reserved.**
q66_ovrn	5	RO	0	**Queue 66 Overrun.** This bit is set when queue 66 overruns. An interrupt is generated if the corresponding enable bit is set.
Reserved	6	RO	0	**Reserved.**
q67_ovrn	7	RO	0	**Queue 67 Overrun.** This bit is set when queue 67 overruns. An interrupt is generated if the corresponding enable bit is set.
Reserved	8	RO	0	**Reserved.**
q68_ovrn	9	RO	0	**Queue 68 Overrun.** This bit is set when queue 68 overruns. An interrupt is generated if the corresponding enable bit is set.
Reserved	10	RO	0	**Reserved.**
q69_ovrn	11	RO	0	**Queue 69 Overrun.** This bit is set when queue 69 overruns. An interrupt is generated if the corresponding enable bit is set.
Reserved	12	RO	0	**Reserved.**
q70_ovrn	13	RO	0	**Queue 70 Overrun.** This bit is set when queue 70 overruns. An interrupt is generated if the corresponding enable bit is set.
Reserved	14	RO	0	**Reserved.**
q71_ovrn	15	RO	0	**Queue 71 Overrun.** This bit is set when queue 71 overruns. An interrupt is generated if the corresponding enable bit is set.

14 Registers (continued)

Table 132. Bypass SDRAM Queue Interrupt Status Register 9 (BSQISR9) (01D2h)

Name	Bit Pos.	Type	Reset	Description
Reserved	0	RO	0	**Reserved.**
q72_ovrn	1	RO	0	**Queue 72 Overrun.** This bit is set when queue 72 overruns. An interrupt is generated if the corresponding enable bit is set.
Reserved	2	RO	0	**Reserved.**
q73_ovrn	3	RO	0	**Queue 73 Overrun.** This bit is set when queue 73 overruns. An interrupt is generated if the corresponding enable bit is set.
Reserved	4	RO	0	**Reserved.**
q74_ovrn	5	RO	0	**Queue 74 Overrun.** This bit is set when queue 74 overruns. An interrupt is generated if the corresponding enable bit is set.
Reserved	6	RO	0	**Reserved.**
q75_ovrn	7	RO	0	**Queue 75 Overrun.** This bit is set when queue 75 overruns. An interrupt is generated if the corresponding enable bit is set.
Reserved	8	RO	0	**Reserved.**
q76_ovrn	9	RO	0	**Queue 76 Overrun.** This bit is set when queue 76 overruns. An interrupt is generated if the corresponding enable bit is set.
Reserved	10	RO	0	**Reserved.**
q77_ovrn	11	RO	0	**Queue 77 Overrun.** This bit is set when queue 77 overruns. An interrupt is generated if the corresponding enable bit is set.
Reserved	12	RO	0	**Reserved.**
q78_ovrn	13	RO	0	**Queue 78 Overrun.** This bit is set when queue 78 overruns. An interrupt is generated if the corresponding enable bit is set.
Reserved	14	RO	0	**Reserved.**
q79_ovrn	15	RO	0	**Queue 79 Overrun.** This bit is set when queue 79 overruns. An interrupt is generated if the corresponding enable bit is set.

14 Registers (continued)

Table 133. Bypass SDRAM Queue Interrupt Status Register 10 (BSQISR10) (01D4h)

Name	Bit Pos.	Type	Reset	Description
Reserved	0	RO	0	**Reserved.**
q80_ovrn	1	RO	0	**Queue 80 Overrun.** This bit is set when queue 80 overruns. An interrupt is generated if the corresponding enable bit is set.
Reserved	2	RO	0	**Reserved.**
q81_ovrn	3	RO	0	**Queue 81 Overrun.** This bit is set when queue 81 overruns. An interrupt is generated if the corresponding enable bit is set.
Reserved	4	RO	0	**Reserved.**
q82_ovrn	5	RO	0	**Queue 82 Overrun.** This bit is set when queue 82 overruns. An interrupt is generated if the corresponding enable bit is set.
Reserved	6	RO	0	**Reserved.**
q83_ovrn	7	RO	0	**Queue 83 Overrun.** This bit is set when queue 83 overruns. An interrupt is generated if the corresponding enable bit is set.
Reserved	8	RO	0	**Reserved.**
q84_ovrn	9	RO	0	**Queue 84 Overrun.** This bit is set when queue 84 overruns. An interrupt is generated if the corresponding enable bit is set.
Reserved	10	RO	0	**Reserved.**
q85_ovrn	11	RO	0	**Queue 85 Overrun.** This bit is set when queue 85 overruns. An interrupt is generated if the corresponding enable bit is set.
Reserved	12	RO	0	**Reserved.**
q86_ovrn	13	RO	0	**Queue 86 Overrun.** This bit is set when queue 86 overruns. An interrupt is generated if the corresponding enable bit is set.
Reserved	14	RO	0	**Reserved.**
q87_ovrn	15	RO	0	**Queue 87 Overrun.** This bit is set when queue 87 overruns. An interrupt is generated if the corresponding enable bit is set.

14 Registers (continued)

Table 134. Bypass SDRAM Queue Interrupt Status Register 11 (BSQIS11) (01D6h)

Name	Bit Pos.	Type	Reset	Description
Reserved	0	RO	0	**Reserved.**
q88_ovrn	1	RO	0	**Queue 88 Overrun.** This bit is set when queue 88 overruns. An interrupt is generated if the corresponding enable bit is set.
Reserved	2	RO	0	**Reserved.**
q89_ovrn	3	RO	0	**Queue 89 Overrun.** This bit is set when queue 89 overruns. An interrupt is generated if the corresponding enable bit is set.
Reserved	4	RO	0	**Reserved.**
q90_ovrn	5	RO	0	**Queue 90 Overrun.** This bit is set when queue 90 overruns. An interrupt is generated if the corresponding enable bit is set.
Reserved	6	RO	0	**Reserved.**
q91_ovrn	7	RO	0	**Queue 91 Overrun.** This bit is set when queue 91 overruns. An interrupt is generated if the corresponding enable bit is set.
Reserved	8	RO	0	**Reserved.**
q92_ovrn	9	RO	0	**Queue 92 Overrun.** This bit is set when queue 92 overruns. An interrupt is generated if the corresponding enable bit is set.
Reserved	10	RO	0	**Reserved.**
q93_ovrn	11	RO	0	**Queue 93 Overrun.** This bit is set when queue 93 overruns. An interrupt is generated if the corresponding enable bit is set.
Reserved	12	RO	0	**Reserved.**
q94_ovrn	13	RO	0	**Queue 94 Overrun.** This bit is set when queue 94 overruns. An interrupt is generated if the corresponding enable bit is set.
Reserved	14	RO	0	**Reserved.**
q95_ovrn	15	RO	0	**Queue 95 Overrun.** This bit is set when queue 95 overruns. An interrupt is generated if the corresponding enable bit is set.

14 Registers (continued)

Table 135. Bypass SDRAM Queue Interrupt Status Register 12 (BSQISR12) (01D8h)

Name	Bit Pos.	Type	Reset	Description
Reserved	0	RO	0	**Reserved.**
q96_ovrn	1	RO	0	**Queue 96 Overrun.** This bit is set when queue 96 overruns. An interrupt is generated if the corresponding enable bit is set.
Reserved	2	RO	0	**Reserved.**
q97_ovrn	3	RO	0	**Queue 97 Overrun.** This bit is set when queue 97 overruns. An interrupt is generated if the corresponding enable bit is set.
Reserved	4	RO	0	**Reserved.**
q98_ovrn	5	RO	0	**Queue 98 Overrun.** This bit is set when queue 98 overruns. An interrupt is generated if the corresponding enable bit is set.
Reserved	6	RO	0	**Reserved.**
q99_ovrn	7	RO	0	**Queue 99 Overrun.** This bit is set when queue 99 overruns. An interrupt is generated if the corresponding enable bit is set.
Reserved	8	RO	0	**Reserved.**
q100_ovrn	9	RO	0	**Queue 100 Overrun.** This bit is set when queue 100 overruns. An interrupt is generated if the corresponding enable bit is set.
Reserved	10	RO	0	**Reserved.**
q101_ovrn	11	RO	0	**Queue 101 Overrun.** This bit is set when queue 101 overruns. An interrupt is generated if the corresponding enable bit is set.
Reserved	12	RO	0	**Reserved.**
q102_ovrn	13	RO	0	**Queue 102 Overrun.** This bit is set when queue 102 overruns. An interrupt is generated if the corresponding enable bit is set.
Reserved	14	RO	0	**Reserved.**
q103_ovrn	15	RO	0	**Queue 103 Overrun.** This bit is set when queue 103 overruns. An interrupt is generated if the corresponding enable bit is set.

14 Registers (continued)

Table 136. Bypass SDRAM Queue Interrupt Status Register 13 (BSQISR13) (01DAh)

Name	Bit Pos.	Type	Reset	Description
Reserved	0	RO	0	**Reserved.**
q104_ovrn	1	RO	0	**Queue 104 Overrun.** This bit is set when queue 104 overruns. An interrupt is generated if the corresponding enable bit is set.
Reserved	2	RO	0	**Reserved.**
q105_ovrn	3	RO	0	**Queue 105 Overrun.** This bit is set when queue 105 overruns. An interrupt is generated if the corresponding enable bit is set.
Reserved	4	RO	0	**Reserved.**
q106_ovrn	5	RO	0	**Queue 106 Overrun.** This bit is set when queue 106 overruns. An interrupt is generated if the corresponding enable bit is set.
Reserved	6	RO	0	**Reserved.**
q107_ovrn	7	RO	0	**Queue 107 Overrun.** This bit is set when queue 107 overruns. An interrupt is generated if the corresponding enable bit is set.
Reserved	8	RO	0	**Reserved.**
q108_ovrn	9	RO	0	**Queue 108 Overrun.** This bit is set when queue 108 overruns. An interrupt is generated if the corresponding enable bit is set.
Reserved	10	RO	0	**Reserved.**
q109_ovrn	11	RO	0	**Queue 109 Overrun.** This bit is set when queue 109 overruns. An interrupt is generated if the corresponding enable bit is set.
Reserved	12	RO	0	**Reserved.**
q110_ovrn	13	RO	0	**Queue 110 Overrun.** This bit is set when queue 110 overruns. An interrupt is generated if the corresponding enable bit is set.
Reserved	14	RO	0	**Reserved.**
q111_ovrn	15	RO	0	**Queue 111 Overrun.** This bit is set when queue 111 overruns. An interrupt is generated if the corresponding enable bit is set.

14 Registers (continued)

Table 137. Bypass SDRAM Queue Interrupt Status Register 14 (BSQISR14) (01DCh)

Name	Bit Pos.	Type	Reset	Description
Reserved	0	RO	0	**Reserved.**
q112_ovrn	1	RO	0	**Queue 112 Overrun.** This bit is set when queue 112 overruns. An interrupt is generated if the corresponding enable bit is set.
Reserved	2	RO	0	**Reserved.**
q113_ovrn	3	RO	0	**Queue 113 Overrun.** This bit is set when queue 113 overruns. An interrupt is generated if the corresponding enable bit is set.
Reserved	4	RO	0	**Reserved.**
q114_ovrn	5	RO	0	**Queue 114 Overrun.** This bit is set when queue 114 overruns. An interrupt is generated if the corresponding enable bit is set.
Reserved	6	RO	0	**Reserved.**
q115_ovrn	7	RO	0	**Queue 115 Overrun.** This bit is set when queue 115 overruns. An interrupt is generated if the corresponding enable bit is set.
Reserved	8	RO	0	**Reserved.**
q116_ovrn	9	RO	0	**Queue 116 Overrun.** This bit is set when queue 116 overruns. An interrupt is generated if the corresponding enable bit is set.
Reserved	10	RO	0	**Reserved.**
q117_ovrn	11	RO	0	**Queue 117 Overrun.** This bit is set when queue 117 overruns. An interrupt is generated if the corresponding enable bit is set.
Reserved	12	RO	0	**Reserved.**
q118_ovrn	13	RO	0	**Queue 118 Overrun.** This bit is set when queue 118 overruns. An interrupt is generated if the corresponding enable bit is set.
Reserved	14	RO	0	**Reserved.**
q119_ovrn	15	RO	0	**Queue 119 Overrun.** This bit is set when queue 119 overruns. An interrupt is generated if the corresponding enable bit is set.

14 Registers (continued)

Table 138. Bypass SDRAM Queue Interrupt Status Register 15 (BSQISR15) (01DEh)

Name	Bit Pos.	Type	Reset	Description
Reserved	0	RO	0	**Reserved.**
q120_ovrn	1	RO	0	**Queue 120 Overrun.** This bit is set when queue 120 overruns. An interrupt is generated if the corresponding enable bit is set.
Reserved	2	RO	0	**Reserved.**
q121_ovrn	3	RO	0	**Queue 121 Overrun.** This bit is set when queue 121 overruns. An interrupt is generated if the corresponding enable bit is set.
Reserved	4	RO	0	**Reserved.**
q122_ovrn	5	RO	0	**Queue 122 Overrun.** This bit is set when queue 122 overruns. An interrupt is generated if the corresponding enable bit is set.
Reserved	6	RO	0	**Reserved.**
q123_ovrn	7	RO	0	**Queue 123 Overrun.** This bit is set when queue 123 overruns. An interrupt is generated if the corresponding enable bit is set.
Reserved	8	RO	0	**Reserved.**
q124_ovrn	9	RO	0	**Queue 124 Overrun.** This bit is set when queue 124 overruns. An interrupt is generated if the corresponding enable bit is set.
Reserved	10	RO	0	**Reserved.**
q125_ovrn	11	RO	0	**Queue 125 Overrun.** This bit is set when queue 125 overruns. An interrupt is generated if the corresponding enable bit is set.
Reserved	12	RO	0	**Reserved.**
q126_ovrn	13	RO	0	**Queue 126 Overrun.** This bit is set when queue 126 overruns. An interrupt is generated if the corresponding enable bit is set.
Reserved	14	RO	0	**Reserved.**
q127_ovrn	15	RO	0	**Queue 127 Overrun.** This bit is set when queue 127 overruns. An interrupt is generated if the corresponding enable bit is set.

14 Registers (continued)

Table 139. Routing Information 1 (RI1) (0200h)

Name	Bit Pos.	Type	Reset	Description
mphy1_sel[5:0]	5:0	RW	X	**Multi-PHY 1 Select [5:0].** The mphy1_sel[5:0] bit field selects which bit of the cell header, the cell bus routing header, or the tandem routing header is used as this queue group address bit.
mphy2_sel[5:0]	11:6	RW	X	**Multi-PHY 2 Select [5:0].** The mphy2_sel[5:0] bit field selects which bit of the cell header, the cell bus routing header, or the tandem routing header is used as this queue group address bit. **Multi-PHY 1 and 2 Select [5:0].** The multi-PHY select bits are used to determine the queue group to which the cell is directed. The priority select bits are used to determine the queue in the queue group to which the cell is directed. The mphy4_sel[5:0] bits select the most significant bit of the queue group address, and the mphy0_sel[5:0] bits select the least significant bit of the queue group address. A value of zero to 31 selects bits in the cell header where zero is the CLP bit and 31 is the most significant bit of the GFC/VPI field. A value of 32 to 47 selects bits in the tandem routing header where 32 is the least significant bit and 47 is the most significant bit. A value of 48 to 63 selects bits in the cell bus header where 48 is the least significant bit and 63 is the most significant bit. The value “110000” is a special case and may be used to force the value of this bit to ‘0.’ If this bit is forced to zero, the bit position in the resultant pointer is always ‘0’ and is not extracted from the received cell.
Reserved	15:12	RO	0	**Reserved.**

14 Registers (continued)

Table 140. Routing Information 2 (RI2) (0202h)

Name	Bit Pos.	Type	Reset	Description
reserved_sel[5:0]	5:0	RW	X	**Reserved Select [5:0].** Program these bits to zero.
mphy0_sel[5:0]	11:6	RW	X	**Multi-PHY 0 Select [5:0].** The mphy0_sel[5:0] bit field selects which bit of the cell header, the cell bus routing header, or the tandem routing header is used as this queue group address bit. The multi-PHY select bits are used to determine the queue group to which the cell is directed. The priority select bits are used to determine the queue in the queue group to which the cell is directed. The mphy4_sel[5:0] bits select the most significant bit of the queue group address, and the mphy0_sel[5:0] bits select the least significant bit of the queue group address. A value of zero to 31 selects bits in the cell header where zero is the CLP bit and 31 is the most significant bit of the GFC/VPI field. A value of 32 to 47 selects bits in the tandem routing header where 32 is the least significant bit and 47 is the most significant bit. A value of 48 to 63 selects bits in the cell bus header where 48 is the least significant bit and 63 is the most significant bit. The value “110000” is a special case and may be used to force the value of this bit to ‘0.’ If this bit is forced to zero, the bit position in the resultant pointer is always ‘0’ and is not extracted from the received cell.
Reserved	15:12	RO	0	**Reserved.**

14 Registers (continued)

Table 141. Routing Information 3 (RI3) (0204h)

Name	Bit Pos.	Type	Reset	Description
prior0_sel[5:0]	5:0	RW	X	**Priority 0 Select.** The prior0_sel[5:0] bit field selects which bit of the cell header, the cell bus routing header, or the tandem routing header is used as this priority bit.
prior1_sel[5:0]	11:6	RW	X	**Priority 1 Select.** The prior1_sel[5:0] bit field selects which bit of the cell header, the cell bus routing header, or the tandem routing header is used as this priority bit. **Priority 0 and 1 Select.** The multi-PHY select bits are used to determine the queue group to which the cell is directed. The priority select bits are used to determine the queue in the queue group to which the cell is directed. The prior1_sel[5:0] bits select the most significant bit of the priority number in the specified group, and the prior0_sel[5:0] bits select the least significant bit of the priority number. A value of zero to 31 selects bits in the cell header where zero is the CLP bit and 31 is the most significant bit of the GFC/VPI field. A value of 32 to 47 selects bits in the tandem routing header where 32 is the least significant bit and 47 is the most significant bit. A value of 48 to 63 selects bits in the cell bus header where 48 is the least significant bit and 63 is the most significant bit. The value “110000” is a special case and may be used to force the value of this bit to ‘0.’ If this bit is forced to zero, the bit position in the resultant pointer is always ‘0’ and is not extracted from the received cell.
Reserved	15:12	RO	0	**Reserved.**

14 Registers (continued)

Table 142. PPD Information 1 (PPDI1) (0206h)

Name	Bit Pos.	Type	Reset	Description
ppd_pnt12_sel[5:0]	5:0	RW	X	**PPD Pointer 12 Select.** The ppd_pnt12_sel[5:0] bit field selects which bit of the cell header, the cell bus routing header, or the tandem routing header is used as this offset bit. The PPD pointer select bits are used to create an offset into the PPD state memory. The PPD state memory is used to keep track of AAL5 virtual channels for partial packet discard. Up to 8192 virtual channels may be supported with these select fields. The ppd_pnt12_sel[5:0] bits select the most significant bit of the PPD state memory offset, and the ppd_pnt0_sel[5:0] bits select the least significant bit of the offset. A value of zero to 31 selects bits in the cell header where zero is the CLP bit and 31 is the most significant bit of the GFC/VPI field. A value of 32 to 47 selects bits in the tandem routing header where 32 is the least significant bit and 47 is the most significant bit. A value of 48 to 63 selects bits in the cell bus header where 48 is the least significant bit and 63 is the most significant bit. The value “110000” is a special case and may be used to force the value of this bit to ‘0.’ If this bit is forced to zero, the bit position in the resultant pointer is always ‘0’ and is not extracted from the received cell.
ppd_en_sel[5:0]	11:6	RW	X	**PPD Enable Select.** The ppd_en_sel[5:0] bit field selects which bit of the cell header, the cell bus routing header, or the tandem routing header is used as this enable bit. The PPD enable select bits are used to identify the AAL5 virtual channel and to enable PPD. A value of zero to 31 selects bits in the cell header where zero is the CLP bit and 31 is the most significant bit of the GFC/VPI field. A value of 32 to 47 selects bits in the tandem routing header where 32 is the least significant bit and 47 is the most significant bit. A value of 48 to 63 selects bits in the cell bus header where 48 is the least significant bit and 63 is the most significant bit. The value “110000” is a special case and may be used to force the value of this bit to ‘0.’ If this selected bit in the received cell is one, the partial packet discard feature is enabled.
Reserved	15:12	RO	0	**Reserved.**

14 Registers (continued)

Table 143. PPD Information 2 (PPDI2) (0208h)

Name	Bit Pos.	Type	Reset	Description
ppd_pnt10_sel[5:0]	5:0	RW	X	**PPD Pointer 10 Select.** The ppd_pnt10_sel[5:0] bit field selects which bit of the cell header, the cell bus routing header, or the tandem routing header is used as this offset bit.
ppd_pnt11_sel[5:0]	11:6	RW	X	**PPD Pointer 11 Select.** The ppd_pnt11_sel[5:0] bit field selects which bit of the cell header, the cell bus routing header, or the tandem routing header is used as this offset bit. **PPD Pointer 10 and 11 Select.** The ppd pointer select bits are used to create an offset into the PPD state memory. The PPD state memory is used to keep track of AAL5 virtual channels for partial packet discard. Up to 8192 virtual channels may be supported with these select fields. The ppd_pnt12_sel[5:0] bits select the most significant bit of the PPD state memory offset, and the ppd_pnt0_sel[5:0] bits select the least significant bit of the offset. A value of zero to 31 selects bits in the cell header where zero is the CLP bit and 31 is the most significant bit of the GFC/VPI field. A value of 32 to 47 selects bits in the tandem routing header where 32 is the least significant bit and 47 is the most significant bit. A value of 48 to 63 selects bits in the cell bus header where 48 is the least significant bit and 63 is the most significant bit. The value “110000” is a special case and may be used to force the value of this bit to ‘0.’ If this bit is forced to zero, the bit position in the resultant pointer is always ‘0’ and is not extracted from the received cell.
Reserved	15:12	RO	0	**Reserved.**

14 Registers (continued)

Table 144. PPD Information 3 (PPDI3) (020Ah)

Name	Bit Pos.	Type	Reset	Description
ppd_pnt8_sel[5:0]	5:0	RW	X	**PPD Pointer 8 Select.** The ppd_pnt8_sel[5:0] bit field selects which bit of the cell header, the cell bus routing header, or the tandem routing header is used as this offset bit.
ppd_pnt9_sel[5:0]	11:6	RW	X	**PPD Pointer 9 Select.** The ppd_pnt9_sel[5:0] bit field selects which bit of the cell header, the cell bus routing header, or the tandem routing header is used as this offset bit. **PPD Pointer 8 and 9 Select.** The ppd pointer select bits are used to create an offset into the PPD state memory. The PPD state memory is used to keep track of AAL5 virtual channels for partial packet discard. Up to 8192 virtual channels may be supported with these select fields. The ppd_pnt12_sel[5:0] bits select the most significant bit of the PPD state memory offset, and the ppd_pnt0_sel[5:0] bits select the least significant bit of the offset. A value of zero to 31 selects bits in the cell header where zero is the CLP bit and 31 is the most significant bit of the GFC/VPI field. A value of 32 to 47 selects bits in the tandem routing header where 32 is the least significant bit and 47 is the most significant bit. A value of 48 to 63 selects bits in the cell bus header where 48 is the least significant bit and 63 is the most significant bit. The value “110000” is a special case and may be used to force the value of this bit to ‘0.’ If this bit is forced to zero, the bit position in the resultant pointer is always ‘0’ and is not extracted from the received cell.
Reserved	15:12	RO	0	**Reserved.**

14 Registers (continued)

Table 145. PPD Information 4 (PPDI4) (020Ch)

Name	Bit Pos.	Type	Reset	Description
ppd_pnt6_sel[5:0]	5:0	RW	X	**PPD Pointer 6 Select.** The ppd_pnt6_sel[5:0] bit field selects which bit of the cell header, the cell bus routing header, or the tandem routing header is used as this offset bit.
ppd_pnt7_sel[5:0]	11:6	RW	X	**PPD Pointer 7 Select.** The ppd_pnt7_sel[5:0] bit field selects which bit of the cell header, the cell bus routing header, or the tandem routing header is used as this offset bit. **PPD Pointer 6 and 7 Select.** The ppd pointer select bits are used to create an offset into the PPD state memory. The PPD state memory is used to keep track of AAL5 virtual channels for partial packet discard. Up to 8192 virtual channels may be supported with these select fields. The ppd_pnt12_sel[5:0] bits select the most significant bit of the PPD state memory offset, and the ppd_pnt0_sel[5:0] bits select the least significant bit of the offset. A value of zero to 31 selects bits in the cell header where zero is the CLP bit and 31 is the most significant bit of the GFC/VPI field. A value of 32 to 47 selects bits in the tandem routing header where 32 is the least significant bit and 47 is the most significant bit. A value of 48 to 63 selects bits in the cell bus header where 48 is the least significant bit and 63 is the most significant bit. The value “110000” is a special case and may be used to force the value of this bit to ‘0.’ If this bit is forced to zero, the bit position in the resultant pointer is always ‘0’ and is not extracted from the received cell.
Reserved	15:12	RO	0	**Reserved.**

14 Registers (continued)

Table 146. PPD Information 5 (PPDI5) (020Eh)

Name	Bit Pos.	Type	Reset	Description
ppd_pnt4_sel[5:0]	5:0	RW	X	**PPD Pointer 4 Select.** The ppd_pnt4_sel[5:0] bit field selects which bit of the cell header, the cell bus routing header, or the tandem routing header is used as this offset bit.
ppd_pnt5_sel[5:0]	11:6	RW	X	**PPD Pointer 5 Select.** The ppd_pnt5_sel[5:0] bit field selects which bit of the cell header, the cell bus routing header, or the tandem routing header is used as this offset bit. **PPD Pointer 4 and 5 Select.** The ppd pointer select bits are used to create an offset into the PPD state memory. The PPD state memory is used to keep track of AAL5 virtual channels for partial packet discard. Up to 8192 virtual channels may be supported with these select fields. The ppd_pnt12_sel[5:0] bits select the most significant bit of the PPD state memory offset, and the ppd_pnt0_sel[5:0] bits select the least significant bit of the offset. A value of zero to 31 selects bits in the cell header where zero is the CLP bit and 31 is the most significant bit of the GFC/VPI field. A value of 32 to 47 selects bits in the tandem routing header where 32 is the least significant bit and 47 is the most significant bit. A value of 48 to 63 selects bits in the cell bus header where 48 is the least significant bit and 63 is the most significant bit. The value “110000” is a special case and may be used to force the value of this bit to ‘0.’ If this bit is forced to zero, the bit position in the resultant pointer is always ‘0’ and is not extracted from the received cell.
Reserved	15:12	RO	0	**Reserved.**

14 Registers (continued)

Table 147. PPD Information 6 (PPDI6) (0210h)

Name	Bit Pos.	Type	Reset	Description
ppd_pnt2_sel[5:0]	5:0	RW	X	**PPD Pointer 2 Select.** The ppd_pnt2_sel[5:0] bit field selects which bit of the cell header, the cell bus routing header, or the tandem routing header is used as this offset bit.
ppd_pnt3_sel[5:0]	11:6	RW	X	**PPD Pointer 3 Select.** The ppd_pnt3_sel[5:0] bit field selects which bit of the cell header, the cell bus routing header, or the tandem routing header is used as this offset bit. **PPD Pointer 2 and 3 Select.** The ppd pointer select bits are used to create an offset into the PPD state memory. The PPD state memory is used to keep track of AAL5 virtual channels for partial packet discard. Up to 8192 virtual channels may be supported with these select fields. The ppd_pnt12_sel[5:0] bits select the most significant bit of the PPD state memory offset, and the ppd_pnt0_sel[5:0] bits select the least significant bit of the offset. A value of zero to 31 selects bits in the cell header where zero is the CLP bit and 31 is the most significant bit of the GFC/VPI field. A value of 32 to 47 selects bits in the tandem routing header where 32 is the least significant bit and 47 is the most significant bit. A value of 48 to 63 selects bits in the cell bus header where 48 is the least significant bit and 63 is the most significant bit. The value “110000” is a special case and may be used to force the value of this bit to ‘0.’ If this bit is forced to zero, the bit position in the resultant pointer is always ‘0’ and is not extracted from the received cell.
Reserved	15:12	RO	0	**Reserved.**

14 Registers (continued)

Table 148. PPD Information 7 (PPDI7) (0212h)

Name	Bit Pos.	Type	Reset	Description
ppd_pnt0_sel[5:0]	5:0	RW	X	**PPD Pointer 0 Select.** The ppd_pnt0_sel[5:0] bit field selects which bit of the cell header, the cell bus routing header, or the tandem routing header is used as this queue group offset bit.
ppd_pnt1_sel[5:0]	11:6	RW	X	**PPD Pointer 1 Select.** The ppd_pnt1_sel[5:0] bit field selects which bit of the cell header, the cell bus routing header, or the tandem routing header is used as this queue group offset bit. **PPD Pointer 0 and 1 Select.** The PPD pointer select bits are used to create an offset into the PPD state memory. The PPD state memory is used to keep track of AAL5 virtual channels for partial packet discard. Up to 8192 virtual channels may be supported with these select fields. The ppd_pnt12_sel[5:0] bits select the most significant bit of the PPD state memory offset, and the ppd_pnt0_sel[5:0] bits select the least significant bit of the offset. A value of zero to 31 selects bits in the cell header where zero is the CLP bit and 31 is the most significant bit of the GFC/VPI field. A value of 32 to 47 selects bits in the tandem routing header where 32 is the least significant bit and 47 is the most significant bit. A value of 48 to 63 selects bits in the cell bus header where 48 is the least significant bit and 63 is the most significant bit. The value “110000” is a special case and may be used to force the value of this bit to ‘0.’ If this bit is forced to zero, the bit position in the resultant pointer is always ‘0’ and is not extracted from the received cell.
Reserved	15:12	RO	0	**Reserved.**

14 Registers (continued)

Table 149. Routing Information 4 (RI4) (0214h)

Name	Bit Pos.	Type	Reset	Description
mphy3_sel[5:0]	5:0	RW	X	**Multi-PHY 3 Select [5:0].** The mphy3_sel[5:0] bit field selects which bit of the cell header, the cell bus routing header, or the tandem routing header is used as this queue group address bit.
mphy4_sel[5:0]	11:6	RW	X	**Multi-PHY 4 Select [5:0].** The mphy4_sel[5:0] bit field selects which bit of the cell header, the cell bus routing header, or the tandem routing header is used as this queue group address bit. **Multi-PHY 3 and 4 Select [5:0].** The multi-PHY select bits are used to determine the queue group to which the cell is directed. The priority select bits are used to determine the queue in the queue group to which the cell is directed. The mphy4_sel[5:0] bits select the most significant bit of the queue group address, and the mphy0_sel[5:0] bits select the least significant bit of the queue group address. A value of zero to 31 selects bits in the cell header where zero is the CLP bit and 31 is the most significant bit of the GFC/VPI field. A value of 32 to 47 selects bits in the tandem routing header where 32 is the least significant bit and 47 is the most significant bit. A value of 48 to 63 selects bits in the cell bus header where 48 is the least significant bit and 63 is the most significant bit. The value “110000” is a special case and may be used to force the value of this bit to ‘0.’ If this bit is forced to zero, the bit position in the resultant pointer is always ‘0’ and is not extracted from the received cell.
Reserved	15:12	RO	0	**Reserved.**

14 Registers (continued)

Table 150. PPD Memory Write (PPDMW) (0418h)

Name	Bit Pos.	Type	Reset	Description
write_pul	0	RW	0	**Write Pulse.** If a '1' is written to this bit, a single bit will be written to the PPD memory. The value of the bit is obtained from the write_val bit, and the address in the PPD memory is obtained from the write_addr bits. The write_pul bit is cleared by hardware when the write is complete.
write_val	1	RW	0	**Write Value.** This bit contains the value to be written to the PPD state memory bit.
write_addr	14:2	RW	0	**Write Address.** These bits contain the address of the bit in PPD memory. This address will be used when a write is performed. This address corresponds to the offset from the cell header, cell bus header, and tandem routing header as determined from the PPD point select bits. An address of all zeros will point to the most significant bit of word 0, and an address of all ones will point to the least significant bit of word 1FF.
Reserved	15	RO	0	**Reserved.**

14 Registers (continued)

14.3.2.2 TX UTOPIA Monitoring

Table 151. PHY Port X Transmit Count Structure (PPXTXCNT) (0600h to 06FEh)

Name	Offset	Type	Reset	Description
out_cnt_phyX[31:16]	00h	RW	X	**Outgoing Cell Count for PHY Port X [31:16].** The out_cnt_phyX[31:16] and out_cnt_phyX[15:0] fields together are a free-running counter of cells transmitted on UTOPIA PHY port X.
out_cnt_phyX[15:0]	02h	RW	X	**Outgoing Cell Count for PHY Port X [15:0].** The out_cnt_phyX[31:16] and out_cnt_phyX[15:0] fields together are a free-running counter of cells transmitted on UTOPIA PHY port X.

The letter X in the data structure name and in the bit names represents the values of 0 through 63 for the 64 PHY ports. The base addresses of the 64 data structures are shown below.

Data Structure	Base Address	Data Structure	Base Address
PHY Port 0 Transmit Count 0	(0600h)	PHY Port 32 Transmit Count 0	(0680h)
PHY Port 1 Transmit Count 0	(0604h)	PHY Port 33 Transmit Count 0	(0684h)
PHY Port 2 Transmit Count 0	(0608h)	PHY Port 34 Transmit Count 0	(0688h)
PHY Port 3 Transmit Count 0	(060Ch)	PHY Port 35 Transmit Count 0	(068Ch)
PHY Port 4 Transmit Count 0	(0610h)	PHY Port 36 Transmit Count 0	(0690h)
PHY Port 5 Transmit Count 0	(0614h)	PHY Port 37 Transmit Count 0	(0694h)
PHY Port 6 Transmit Count 0	(0618h)	PHY Port 38 Transmit Count 0	(0698h)
PHY Port 7 Transmit Count 0	(061Ch)	PHY Port 39 Transmit Count 0	(069Ch)
PHY Port 8 Transmit Count 0	(0620h)	PHY Port 40 Transmit Count 0	(06A0h)
PHY Port 9 Transmit Count 0	(0624h)	PHY Port 41 Transmit Count 0	(06A4h)
PHY Port 10 Transmit Count 0	(0628h)	PHY Port 42 Transmit Count 0	(06A8h)
PHY Port 11 Transmit Count 0	(062Ch)	PHY Port 43 Transmit Count 0	(06ACh)
PHY Port 12 Transmit Count 0	(0630h)	PHY Port 44 Transmit Count 0	(06B0h)
PHY Port 13 Transmit Count 0	(0634h)	PHY Port 45 Transmit Count 0	(06B4h)
PHY Port 14 Transmit Count 0	(0638h)	PHY Port 46 Transmit Count 0	(06B8h)
PHY Port 15 Transmit Count 0	(063Ch)	PHY Port 47 Transmit Count 0	(06BCh)
PHY Port 16 Transmit Count 0	(0640h)	PHY Port 48 Transmit Count 0	(06C0h)
PHY Port 17 Transmit Count 0	(0644h)	PHY Port 49 Transmit Count 0	(06C4h)
PHY Port 18 Transmit Count 0	(0648h)	PHY Port 50 Transmit Count 0	(06C8h)
PHY Port 19 Transmit Count 0	(064Ch)	PHY Port 51 Transmit Count 0	(06CCh)
PHY Port 20 Transmit Count 0	(0650h)	PHY Port 52 Transmit Count 0	(06D0h)
PHY Port 21 Transmit Count 0	(0654h)	PHY Port 53 Transmit Count 0	(06D4h)
PHY Port 22 Transmit Count 0	(0658h)	PHY Port 54 Transmit Count 0	(06D8h)
PHY Port 23 Transmit Count 0	(065Ch)	PHY Port 55 Transmit Count 0	(06DCh)
PHY Port 24 Transmit Count 0	(0660h)	PHY Port 56 Transmit Count 0	(06E0h)
PHY Port 25 Transmit Count 0	(0664h)	PHY Port 57 Transmit Count 0	(06E4h)
PHY Port 26 Transmit Count 0	(0668h)	PHY Port 58 Transmit Count 0	(06E8h)
PHY Port 27 Transmit Count 0	(066Ch)	PHY Port 59 Transmit Count 0	(06ECh)
PHY Port 28 Transmit Count 0	(0670h)	PHY Port 60 Transmit Count 0	(06F0h)
PHY Port 29 Transmit Count 0	(0674h)	PHY Port 61 Transmit Count 0	(06F4h)
PHY Port 30 Transmit Count 0	(0678h)	PHY Port 62 Transmit Count 0	(06F8h)
PHY Port 31 Transmit Count 0	(067Ch)	PHY Port 63 Transmit Count 0	(06FCh)

14 Registers (continued)

14.3.2.3 RX UTOPIA Count Monitoring

Table 152. PHY Port X Receive Count Structure (PPXRXCNT) (4000h to 40FEh)

Name	Offset	Bit Pos.	Type	Reset	Description
in_cnt_phyX[31:16]	00h	15:0	RW	X	**Incoming Cell Count for PHY Port X [31:16].** The in_cnt_phyX[31:16] and in_cnt_phyX[15:0] fields together are a free-running counter of cells from PHY port X. Both valid and misrouted cells are counted. Incoming cells are not counted if they encounter an ignore (I) bit in their translation records that is '1' or if their VPI and/or VCI are out of range.
in_cnt_phyX[15:0]	02h	15:0			**Incoming Cell Count for PHY Port X [15:0].** The in_cnt_phyX[31:16] and in_cnt_phyX[15:0] fields together are a free-running counter of cells from PHY port X. Both valid and misrouted cells are counted. Incoming cells are not counted if they encounter an ignore (I) bit in their translation records that is '1' or if their VPI and/or VCI are out of range.

The letter X in the data structure name and in the bit names represents the values 0 through 63 for the 64 PHY ports. The base addresses of the 64 data structures are shown below.

Structure Name	Base Address	Structure Name	Base Address
PHY Port 0 Receive Count 0	(4000h)	PHY Port 32 Receive Count 0	(4080h)
PHY Port 1 Receive Count 0	(4004h)	PHY Port 33 Receive Count 0	(4084h)
PHY Port 2 Receive Count 0	(4008h)	PHY Port 34 Receive Count 0	(4088h)
PHY Port 3 Receive Count 0	(400Ch)	PHY Port 35 Receive Count 0	(408Ch)
PHY Port 4 Receive Count 0	(4010h)	PHY Port 36 Receive Count 0	(4090h)
PHY Port 5 Receive Count 0	(4014h)	PHY Port 37 Receive Count 0	(4094h)
PHY Port 6 Receive Count 0	(4018h)	PHY Port 38 Receive Count 0	(4098h)
PHY Port 7 Receive Count 0	(401Ch)	PHY Port 39 Receive Count 0	(409Ch)
PHY Port 8 Receive Count 0	(4020h)	PHY Port 40 Receive Count 0	(40A0h)
PHY Port 9 Receive Count 0	(4024h)	PHY Port 41 Receive Count 0	(40A4h)
PHY Port 10 Receive Count 0	(4028h)	PHY Port 42 Receive Count 0	(40A8h)
PHY Port 11 Receive Count 0	(402Ch)	PHY Port 43 Receive Count 0	(40ACh)
PHY Port 12 Receive Count 0	(4030h)	PHY Port 44 Receive Count 0	(40B0h)
PHY Port 13 Receive Count 0	(4034h)	PHY Port 45 Receive Count 0	(40B4h)
PHY Port 14 Receive Count 0	(4038h)	PHY Port 46 Receive Count 0	(40B8h)
PHY Port 15 Receive Count 0	(403Ch)	PHY Port 47 Receive Count 0	(40BCh)
PHY Port 16 Receive Count 0	(4040h)	PHY Port 48 Receive Count 0	(40C0h)
PHY Port 17 Receive Count 0	(4044h)	PHY Port 49 Receive Count 0	(40C4h)
PHY Port 18 Receive Count 0	(4048h)	PHY Port 50 Receive Count 0	(40C8h)
PHY Port 19 Receive Count 0	(404Ch)	PHY Port 51 Receive Count 0	(40CCh)
PHY Port 20 Receive Count 0	(4050h)	PHY Port 52 Receive Count 0	(40D0h)
PHY Port 21 Receive Count 0	(4054h)	PHY Port 53 Receive Count 0	(40D4h)
PHY Port 22 Receive Count 0	(4058h)	PHY Port 54 Receive Count 0	(40D8h)
PHY Port 23 Receive Count 0	(405Ch)	PHY Port 55 Receive Count 0	(40DCh)
PHY Port 24 Receive Count 0	(4060h)	PHY Port 56 Receive Count 0	(40E0h)
PHY Port 25 Receive Count 0	(4064h)	PHY Port 57 Receive Count 0	(40E4h)
PHY Port 26 Receive Count 0	(4068h)	PHY Port 58 Receive Count 0	(40E8h)
PHY Port 27 Receive Count 0	(406Ch)	PHY Port 59 Receive Count 0	(40ECh)
PHY Port 28 Receive Count 0	(4070h)	PHY Port 60 Receive Count 0	(40F0h)
PHY Port 29 Receive Count 0	(4074h)	PHY Port 61 Receive Count 0	(40F4h)
PHY Port 30 Receive Count 0	(4078h)	PHY Port 62 Receive Count 0	(40F8h)
PHY Port 31 Receive Count 0	(407Ch)	PHY Port 63 Receive Count 0	(40FCh)

14 Registers (continued)

14.3.2.4 RX UTOPIA Configuration Monitoring

Table 153. PHY Port X Configuration Structure (PPXCF) (4200h to 42FEh)

Name	Offset	Bit Pos.	Type	Reset	Description
lutX_vpi_base	00h	15:0	RW	X	**PHY Port X VPI Base Address.** These bits define bits 3 through 18 of the VPI base address offset in the look-up table for PHY port X. The offset may be a maximum of 19 bits. If 16-byte records are used, the least significant bit of this word is ignored.
lutX_vpi_mask	02h	11:0			**PHY Port X VPI Mask.** This 12-bit field is used to mask the incoming VPI bits. If a bit in the field is set to ‘1,’ the value of the corresponding bit in the incoming VPI will be meaningful. All other bits of the incoming VPI will be forced to zero.
lutX_vpi_chk		12			**PHY Port X VPI Check.** If this bit is set to ‘1,’ the unused incoming VPI bits must be ‘0,’ or the cell will be counted as misrouted. Unused bits are bits whose corresponding lutX_vpi_mask bit equal zero.
lutX_uni_en		13			**PHY Port X User Network Interface (UNI) Enable.** If this bit is set to ‘1,’ the port is identified as UNI, and the GFC field of the cell header will not be used in the look-up table. If this bit is ‘0,’ the port is identified as NNI.
Reserved		15:14			**Reserved.**

The letter X in the data structure name and in the bit names represents the values 0 through 63 for the 64 PHY ports. The base addresses of the 64 data structures are shown below.

Structure Name	Base Address	Structure Name	Base Address
PHY Port 0 Configuration	(4200h)	PHY Port 21 Configuration	(4254h)
PHY Port 1 Configuration	(4204h)	PHY Port 22 Configuration	(4258h)
PHY Port 2 Configuration	(4208h)	PHY Port 23 Configuration	(425Ch)
PHY Port 3 Configuration	(420Ch)	PHY Port 24 Configuration	(4260h)
PHY Port 4 Configuration	(4210h)	PHY Port 25 Configuration	(4264h)
PHY Port 5 Configuration	(4214h)	PHY Port 26 Configuration	(4268h)
PHY Port 6 Configuration	(4218h)	PHY Port 27 Configuration	(426Ch)
PHY Port 7 Configuration	(421Ch)	PHY Port 28 Configuration	(4270h)
PHY Port 8 Configuration	(4220h)	PHY Port 29 Configuration	(4274h)
PHY Port 9 Configuration	(4224h)	PHY Port 30 Configuration	(4278h)
PHY Port 10 Configuration	(4228h)	PHY Port 31 Configuration	(427Ch)
PHY Port 11 Configuration	(422Ch)	PHY Port 32 Configuration	(4280h)
PHY Port 12 Configuration	(4230h)	PHY Port 33 Configuration	(4284h)
PHY Port 13 Configuration	(4234h)	PHY Port 34 Configuration	(4288h)
PHY Port 14 Configuration	(4238h)	PHY Port 35 Configuration	(428Ch)
PHY Port 15 Configuration	(423Ch)	PHY Port 36 Configuration	(4290h)
PHY Port 16 Configuration	(4240h)	PHY Port 37 Configuration	(4294h)
PHY Port 17 Configuration	(4244h)	PHY Port 38 Configuration	(4298h)
PHY Port 18 Configuration	(4248h)	PHY Port 39 Configuration	(429Ch)
PHY Port 19 Configuration	(424Ch)	PHY Port 40 Configuration	(42A0h)
PHY Port 20 Configuration	(4250h)	PHY Port 41 Configuration	(42A4h)

14 Registers (continued)

Table 153. PHY Port X Configuration Structure (PPXCF) (4200h to 42FEh) (continued)

Structure Name	Base Address	Structure Name	Base Address
PHY Port 42 Configuration	(42A8h)	PHY Port 53 Configuration	(42D4h)
PHY Port 43 Configuration	(42ACh)	PHY Port 54 Configuration	(42D8h)
PHY Port 44 Configuration	(42B0h)	PHY Port 55 Configuration	(42DCh)
PHY Port 45 Configuration	(42B4h)	PHY Port 56 Configuration	(42E0h)
PHY Port 46 Configuration	(42B8h)	PHY Port 57 Configuration	(42E4h)
PHY Port 47 Configuration	(42BCh)	PHY Port 58 Configuration	(42E8h)
PHY Port 48 Configuration	(42C0h)	PHY Port 59 Configuration	(42ECh)
PHY Port 49 Configuration	(42C4h)	PHY Port 60 Configuration	(42F0h)
PHY Port 50 Configuration	(42C8h)	PHY Port 61 Configuration	(42F4h)
PHY Port 51 Configuration	(42CCh)	PHY Port 62 Configuration	(42F8h)
PHY Port 52 Configuration	(42D0h)	PHY Port 63 Configuration	(42FCh)

14 Registers (continued)

14.3.3 SDRAM Registers

Table 154. SDRAM Control (SCT) (0400h)

Name	Bit Pos.	Type	Reset	Description
sdram_en	0	RW	0	**SDRAM Enable.** If this bit is set to '1,' the SDRAM becomes active. If '0,' the SDRAM is in the idle state.
gen_man_acc	1	WO	0	**Generate Manual Access.** If the sdram_en bit is '0,' writing a '1' to this bit will take the SDRAM out of its idle state and activate the manual values programmed in the cas_man, ras_man, we_man, bs_man, and addr_man bits. The '1' pulses for one clock cycle and clears to '0' automatically. The SDRAM then returns to its idle state. This special mode is used in the start-up sequence for the SDRAM.
Reserved	14:2	RO	0	**Reserved.**
Reserved	15	RW	0	**Reserved.** Program this bit to '0.'

Table 155. SDRAM Interrupt Status (SIS) (0402h)

Name	Bit Pos.	Type	Reset	Description
ref_late	0	ROL	0	**Refresh Late.** This bit is set when the refresh cycle for the SDRAM is greater than the value programmed in the late_lim bits. An interrupt is generated if the corresponding enable bit is set.
crc8_err_even	1	ROL	0	**CRC8 Error on Even Data Byte.** This bit is set when an error is detected on the even byte (sd_d[15:8]) of the SDRAM data bus. An interrupt is generated if the corresponding enable bit is set.
crc8_err_odd	2	ROL	0	**CRC8 Error on Odd Data Byte.** This bit is set when an error is detected on the odd byte (sd_d[7:0]) of the SDRAM data bus. An interrupt is generated if the corresponding enable bit is set.
Reserved	15:3	RO	0	**Reserved.**

Table 156. SDRAM Interrupt Enable (SIE) (0404h)

Name	Bit Pos.	Type	Reset	Description
ref_late_ie	0	RW	0	**Refresh Late Interrupt Enable.** An interrupt is generated if this bit and the corresponding status bit are set. The interrupt is generated until this bit or the corresponding status bit is reset.
crc8_err_even_ie	1	RW	0	**CRC8 Error on Even Data Byte Interrupt Enable.** An interrupt is generated if this bit and the corresponding status bit are set. The interrupt is generated until this bit or the corresponding status bit is reset.
crc8_err_odd_ie	2	RW	0	**CRC8 Error on Odd Data Byte Interrupt Enable.** An interrupt is generated if this bit and the corresponding status bit are set. The interrupt is generated until this bit or the corresponding status bit is reset.
Reserved	15:3	RO	0	**Reserved.**

14 Registers (continued)

Table 157. SDRAM Configuration (SCF) (0408h)

Name	Bit Pos.	Type	Reset	Description
col_num	1:0	RW	0	**Column Number.** These bits are used to indicate the number of columns in the SDRAM. “100” = 256 columns “01” = 512 columns “10” = 1024 columns “11” = reserved
cas_lat	2	RW	0	**CAS Latency.** This bit is used to indicate the CAS latency of the SDRAM based on the clock frequency and speed grade of the device. ‘0’ = 2 cycles ‘1’ = 3 cycles
ras2cas	4:3	RW	2h	**RAS Inactive to CAS Active Delay.** These bits specify the minimum time in SDRAM clock cycles from RAS going inactive to CAS going active. “01” = 2 clock cycles “10” = 2 clock cycles “11” = 3 clock cycles “00” = 4 clock cycles
cas2pre	6:5	RW	1	**CAS Inactive to Precharge Active Delay.** These bits specify the minimum time in SDRAM clock cycles from CAS going inactive to the precharge command going active. “01” = 1 clock cycles “10” = 2 clock cycles “11” = 3 clock cycles “00” = 4 clock cycles
pre2cmd	8:7	RW	2h	**Precharge Inactive to Next Command Active Delay.** These bits specify the minimum time in SDRAM clock cycles from the precharge command going inactive to next command going active. “01” = 1 clock cycles “10” = 2 clock cycles “11” = 3 clock cycles “00” = 4 clock cycles
ref2cmd	10:9	RW	0	**CBR Refresh Inactive to Next Command Active Delay.** These bits specify the minimum time in SDRAM clock cycles from the refresh command going inactive to next refresh command going active. “00” = 15 clock cycles “01” = reserved “10” = 3 clock cycles “11” = 7 clock cycles
Reserved	15:11	RO	0	**Reserved.**

14 Registers (continued)

Table 158. Refresh (RFRSH) (0410h)

Name	Bit Pos.	Type	Reset	Description
ref_cnt	15:0	RW	0400h	**Refresh Count.** These bits are used to program the refresh cycle in SDRAM clock cycles. The number of clock cycles programmed in this register should be less than one half the worst-case refresh period.

Table 159. Refresh Lateness (RFRSHL) (0412h)

Name	Bit Pos.	Type	Reset	Description
late_lim	15:0	RW	0400h	**Lateness Limit.** These bits are used to program how late a refresh cycle may occur. This limit is in refresh cycles. When this limit is reached, the ref_late status bit will be set.

Table 160. Idle State 1 (IS1) (0420h)

Name	Bit Pos.	Type	Reset	Description
cas_idle	0	RW	1	**SDRAM CAS Idle Value.** This is the value that will be placed on the sd_cas* pin while the SDRAM is idle (sdram_en = ‘0’).
ras_idle	1	RW	1	**SDRAM RAS Idle Value.** This is the value that will be placed on the sd_ras* pin while the SDRAM is idle (sdram_en = ‘0’).
we_idle	2	RW	1	**SDRAM Write Enable Idle Value.** This is the value that will be placed on the sd_we* pin while the SDRAM is idle (sdram_en = ‘0’).
bs_idle[1:0]	4:3	RW	3h	**SDRAM Bank Select Idle Value.** This is the value that will be placed on the sd_bs[1:0] pins while the SDRAM is idle (sdram_en = ‘0’).
Reserved	15:5	RO	0	**Reserved.**

Table 161. Idle State 2 (IS2) (0422h)

Name	Bit Pos.	Type	Reset	Description
addr_idle[11:0]	11:0	RW	0	**SDRAM Address Idle Value.** This is the value that will be placed on the sd_a[11:0] pins while the SDRAM is idle (sdram_en = ‘0’).
Reserved	15:12	RO	0	**Reserved.**

14 Registers (continued)

Table 162. Manual Access State 1 (MAS1) (0424h)

Name	Bit Pos.	Type	Reset	Description
cas_ man	0	RW	1	**SDRAM CAS Manual Value.** This is the value that will be placed on the sd_cas* pin for one clock cycle when the gen_man_acc bit is written to ‘1.’
ras_ man	1	RW	1	**SDRAM RAS Manual Value.** This is the value that will be placed on the sd_ras* pin for one clock cycle when the gen_man_acc bit is written to ‘1.’
we_ man	2	RW	1	**SDRAM Write Enable Manual Value.** This is the value that will be placed on the sd_we* pin for one clock cycle when the gen_man_acc bit is written to ‘1.’
bs_ man[1:0]	4:3	RW	3h	**SDRAM Band Select Manual Value.** This is the value that will be placed on the sd_bs[1:0] pins for one clock cycle when the gen_man_acc bit is written to ‘1.’
Reserved	15:5	RO	0	**Reserved.**

Table 163. Manual Access State 2 (MAS2) (0426h)

Name	Bit Pos.	Type	Reset	Description
addr_man[11:0]	11:0	RW	0	**SDRAM Address Manual Value.** This is the value that will be placed on the sd_a[11:0] pins for one clock cycle when the gen_man_acc bit is written to ‘1.’
Reserved	15:12	RO	0	**Reserved.**

14 Registers (continued)

Table 164. SDRAM Interrupt Service Request 7 (SISR7) (0430h)

Name	Bit Pos.	Type	Reset	Description
queue_serv[127:112]	15:0	RO	0	**Queue Service [127:112].** Each bit in this field represents one of 16 queue X registers from the 128 queue X registers. The least significant bit represents the queue 112 register. If the corresponding bit is ‘1,’ the specific queue register has interrupt status bits that need servicing.

Table 165. SDRAM Interrupt Service Request 6 (SISR6) (0432h)

Name	Bit Pos.	Type	Reset	Description
queue_serv[111:96]	15:0	RO	0	**Queue Service [111:96].** Each bit in this field represents one of 16 queue X registers from the 128 queue X registers. The least significant bit represents the queue 96 register. If the corresponding bit is ‘1,’ the specific queue register has interrupt status bits that need servicing.

Table 166. SDRAM Interrupt Service Request 5 (SISR5) (0434h)

Name	Bit Pos.	Type	Reset	Description
queue_serv[95:80]	15:0	RO	0	**Queue Service [95:80].** Each bit in this field represents one of 16 queue X registers from the 128 queue X registers. The least significant bit represents the queue 80 register. If the corresponding bit is ‘1,’ the specific queue register has interrupt status bits that need servicing.

Table 167. SDRAM Interrupt Service Request 4 (SISR4) (0436h)

Name	Bit Pos.	Type	Reset	Description
queue_serv[79:64]	15:0	RO	0	**Queue Service [79:64].** Each bit in this field represents one of 16 queue X registers from the 128 queue X registers. The least significant bit represents the queue 64 register. If the corresponding bit is ‘1,’ the specific queue register has interrupt status bits that need servicing.

14 Registers (continued)

Table 168. SDRAM Interrupt Service Request 3 (SISR3) (0438h)

Name	Bit Pos.	Type	Reset	Description
queue_serv[63:48]	15:0	RO	0	**Queue Service [63:48].** Each bit in this field represents one of 16 queue X registers from the 128 queue X registers. The least significant bit represents the queue 48 register. If the corresponding bit is ‘1,’ the specific queue register has interrupt status bits that need servicing.

Table 169. SDRAM Interrupt Service Request 2 (SISR2) (043Ah)

Name	Bit Pos.	Type	Reset	Description
queue_serv[47:32]	15:0	RO	0	**Queue Service [47:32].** Each bit in this field represents one of 16 queue X registers from the 128 queue X registers. The least significant bit represents the queue 32 register. If the corresponding bit is ‘1,’ the specific queue register has interrupt status bits that need servicing.

Table 170. SDRAM Interrupt Service Request 1 (SISR1) (043Ch)

Name	Bit Pos.	Type	Reset	Description
queue_serv[31:16]	15:0	RO	0	**Queue Service [31:16].** Each bit in this field represents one of 16 queue X registers from the 128 queue X registers. The least significant bit represents the queue 16 register. If the corresponding bit is ‘1,’ the specific queue register has interrupt status bits that need servicing.

Table 171. SDRAM Interrupt Service Request 0 (SISR0) (043Eh)

Name	Bit Pos.	Type	Reset	Description
queue_serv[15:0]	15:0	RO	0	**Queue Service [15:0].** Each bit in this field represents one of 16 queue X registers from the 128 queue X registers. The least significant bit represents the queue 0 register. If the corresponding bit is ‘1,’ the specific queue register has interrupt status bits that need servicing.

14 Registers (continued)

Table 172. Queue X (QX) (0440h to 053Eh)

Name	Bit Pos.	Type	Reset	Description
queueX_rd_en	0	RW	0	**Queue X Read Enable.** If this bit is '1,' the queue is enabled for read operations. When any configuration bits are changed, this bit must be '0.' **Note:** To prevent corruption of data, this bit must be cleared in unused queues.
queueX_wr_en	1	RW	0	**Queue X Write Enable.** If this bit is '1,' the queue is enabled for write operations. When any configuration bits are changed, this bit must be '0.' **Note:** To prevent corruption of data, this bit must be cleared in unused queues.
queueX_fecn_en	2	RW	0	**Queue X FECN Enable.** If this bit is '1,' the forward explicit congestion notification (FECN) feature is enabled.
queueX_clp_en	3	RW	0	**Queue X CLP Enable.** If this bit is '1,' the cell loss priority (CLP) feature is enabled.
Reserved	7:4	RO	0	**Reserved.**
queueX_fecn_lim	8	ROL	0	**Queue X FECN Limit Reached.** This bit is set when the FECN limit has been reached in the queue. An interrupt is generated if the corresponding enable bit is set.
queueX_clp_lim	9	ROL	0	**Queue X CLP Limit Reached.** This bit is set when the CLP limit has been reached in the queue. An interrupt is generated if the corresponding enable bit is set.
queueX_ovrn	10	ROL	0	**Queue X Overrun.** This bit is set when the queue overruns. An interrupt is generated if the corresponding enable bit is set.
queueX_emp	11	ROL	0	**Queue X Empty.** This bit is set when the queue is empty. An interrupt is generated if the corresponding enable bit is set.
queueX_fecn_lim_ie	12	RW	0	**Queue X FECN Limit Reached Interrupt Enable.** An interrupt is generated if this bit and the corresponding status bit are set. The interrupt is generated until this bit or the corresponding status bit is reset.
queueX_clp_lim_ie	13	RW	0	**Queue X CLP Limit Reached Interrupt Enable.** An interrupt is generated if this bit and the corresponding status bit are set. The interrupt is generated until this bit or the corresponding status bit is reset.
queueX_ovrn_ie	14	RW	0	**Queue X Overrun Interrupt Enable.** An interrupt is generated if this bit and the corresponding status bit are set. The interrupt is generated until this bit or the corresponding status bit is reset.

14 Registers (continued)

Table 172. Queue X (QX) (0440h to 053Eh) (continued)

Name	Bit Pos.	Type	Reset	Description
queueX_emp_ie	15	RW	0	**Queue X Empty Interrupt Enable.** An interrupt is generated if this bit and the corresponding status bit are set. The interrupt is generated until this bit or the corresponding status bit is reset.

The letter X in the register name and in the bit names represents the values of 0 through 127 for the 128 queues shown below.

Register Name	Register Address	Register Name	Register Address	Register Name	Register Address	Register Name	Register Address
Queue 0 (Q0)	(0440h)	Queue 32 (Q32)	(0480h)	Queue 64 (Q64)	(04C0h)	Queue 96 (Q96)	(0500h)
Queue 1 (Q1)	(0442h)	Queue 33 (Q33)	(0482h)	Queue 65 (Q65)	(04C2h)	Queue 97 (Q97)	(0502h)
Queue 2 (Q2)	(0444h)	Queue 34 (Q34)	(0484h)	Queue 66 (Q66)	(04C4h)	Queue 98 (Q98)	(0504h)
Queue 3 (Q3)	(0446h)	Queue 35 (Q35)	(0486h)	Queue 67 (Q67)	(04C6h)	Queue 99 (Q99)	(0506h)
Queue 4 (Q4)	(0448h)	Queue 36 (Q36)	(0488h)	Queue 68 (Q68)	(04C8h)	Queue 100 (Q100)	(0508h)
Queue 5 (Q5)	(044Ah)	Queue 37 (Q37)	(048Ah)	Queue 69 (Q69)	(04CAh)	Queue 101 (Q101)	(050Ah)
Queue 6 (Q6)	(044Ch)	Queue 38 (Q38)	(048Ch)	Queue 70 (Q70)	(04CCh)	Queue 102 (Q102)	(050Ch)
Queue 7 (Q7)	(044Eh)	Queue 39 (Q39)	(048Eh)	Queue 71 (Q71)	(04CEh)	Queue 103 (Q103)	(050Eh)
Queue 8 (Q8)	(0450h)	Queue 40 (Q40)	(0490h)	Queue 72 (Q72)	(04D0h)	Queue 104 (Q104)	(0510h)
Queue 9 (Q9)	(0452h)	Queue 41 (Q41)	(0492h)	Queue 73 (Q73)	(04D2h)	Queue 105 (Q105)	(0512h)
Queue 10 (Q10)	(0454h)	Queue 42 (Q42)	(0494h)	Queue 74 (Q74)	(04D4h)	Queue 106 (Q106)	(0514h)
Queue 11 (Q11)	(0456h)	Queue 43 (Q43)	(0496h)	Queue 75 (Q75)	(04D6h)	Queue 107 (Q107)	(0516h)
Queue 12 (Q12)	(0458h)	Queue 44 (Q44)	(0498h)	Queue 76 (Q76)	(04D8h)	Queue 108 (Q108)	(0518h)
Queue 13 (Q13)	(045Ah)	Queue 45 (Q45)	(049Ah)	Queue 77 (Q77)	(04DAh)	Queue 109 (Q109)	(051Ah)
Queue 14 (Q14)	(045Ch)	Queue 46 (Q46)	(049Ch)	Queue 78 (Q78)	(04DCh)	Queue 110 (Q110)	(051Ch)
Queue 15 (Q15)	(045Eh)	Queue 47 (Q47)	(049Eh)	Queue 79 (Q79)	(04DEh)	Queue 111 (Q111)	(051Eh)
Queue 16 (Q16)	(0460h)	Queue 48 (Q48)	(04A0h)	Queue 80 (Q80)	(04E0h)	Queue 112 (Q112)	(0520h)
Queue 17 (Q17)	(0462h)	Queue 49 (Q49)	(04A2h)	Queue 81 (Q81)	(04E2h)	Queue 113 (Q113)	(0522h)
Queue 18 (Q18)	(0464h)	Queue 50 (Q50)	(04A4h)	Queue 82 (Q82)	(04E4h)	Queue 114 (Q114)	(0524h)
Queue 19 (Q19)	(0466h)	Queue 51 (Q51)	(04A6h)	Queue 83 (Q83)	(04E6h)	Queue 115 (Q115)	(0526h)
Queue 20 (Q20)	(0468h)	Queue 52 (Q52)	(04A8h)	Queue 84 (Q84)	(04E8h)	Queue 116 (Q116)	(0528h)
Queue 21 (Q21)	(046Ah)	Queue 53 (Q53)	(04AAh)	Queue 85 (Q85)	(04EAh)	Queue 117 (Q117)	(052Ah)
Queue 22 (Q22)	(046Ch)	Queue 54 (Q54)	(04ACh)	Queue 86 (Q86)	(04ECh)	Queue 118 (Q118)	(052Ch)
Queue 23 (Q23)	(046Eh)	Queue 55 (Q55)	(04AEh)	Queue 87 (Q87)	(04EEh)	Queue 119 (Q119)	(052Eh)
Queue 24 (Q24)	(0470h)	Queue 56 (Q56)	(04B0h)	Queue 88 (Q88)	(04F0h)	Queue 120 (Q120)	(0530h)
Queue 25 (Q25)	(0472h)	Queue 57 (Q57)	(04B2h)	Queue 89 (Q89)	(04F2h)	Queue 121 (Q121)	(0532h)
Queue 26 (Q26)	(0474h)	Queue 58 (Q58)	(04B4h)	Queue 90 (Q90)	(04F4h)	Queue 122 (Q122)	(0534h)
Queue 27 (Q27)	(0476h)	Queue 59 (Q59)	(04B6h)	Queue 91 (Q91)	(04F6h)	Queue 123 (Q123)	(0536h)
Queue 28 (Q28)	(0478h)	Queue 60 (Q60)	(04B8h)	Queue 92 (Q92)	(04F8h)	Queue 124 (Q124)	(0538h)
Queue 29 (Q29)	(047Ah)	Queue 61 (Q61)	(04BAh)	Queue 93 (Q93)	(04FAh)	Queue 125 (Q125)	(053Ah)
Queue 30 (Q30)	(047Ch)	Queue 62 (Q62)	(04BCh)	Queue 94 (Q94)	(04FCh)	Queue 126 (Q126)	(053Ch)
Queue 31 (Q31)	(047Eh)	Queue 63 (Q63)	(04BEh)	Queue 95 (Q95)	(04FEh)	Queue 127 (Q127)	(053Eh)

14 Registers (continued)

14.3.3.1 SDRAM Control Memory

Table 173. Queue X Definition Structure (QXDEF) (2000h to 2FFEh)

Name	Offset	Bit Pos.	Type	Reset	Description
base_addrX[24:9]	00h	15:0	RW	X	**Base Address Queue X [24:9].** These bits configure the upper 16 bits of the queue's base address in increments of one cell (64 bytes).
base_addrX[8:6]	02h	15:13	RW		**Base Address Queue X [8:6].** These bits configure bits 6 through 8 of the queue's base address offset in increments of one cell (64 bytes).
Reserved		12:0	RO		**Reserved.**
end_addrX[24:9]	04h	15:0	RW		**End Address Queue X [24:9].** These bits configure the upper 16 bits of the queue's end address in increments of one cell. The total number of cells held by the queue may be calculated by subtracting the base_addr from the end_addr and adding one to the difference. The minimum size of any queue is four cells.
end_addrX[8:6]	06h	15:13	RW		**End Address Queue X [8:6].** These bits configure bits 6 through 8 of the queue's end address in increments of one cell. The total number of cells held by the queue may be calculated by subtracting the base_addr from the end_addr and adding one to the difference. The minimum size of any queue is four cells.
Reserved		12:0	RO		**Reserved.**
wr_pntX[24:9]	08h	15:0	RW		**Write Pointer for Queue X [24:9].** These bits must be initialized to the base_addrX[24:9] before the queue is enabled.
wr_pntX[8:6]	0Ah	15:13	RW		**Write Pointer for Queue X [8:6].** These bits must be initialized to the base_addrX[8:6] before the queue is enabled.
Reserved		12:0	RO		**Reserved.**
rd_pntX[24:9]	0Ch	15:0	RW		**Read Pointer for Queue X [24:9].** These bits must be initialized to the base_addrX[24:9] before the queue is enabled.
rd_pntX[8:6]	0Eh	15:13	RW		**Read Pointer for Queue X [8:6].** These bits must be initialized to the base_addrX[8:6] before the queue is enabled.
Reserved		12:0	RO		**Reserved.**
fecn_fillX[24:9]	10h	15:0	RW	X	**FECN Fill for Queue X [24:9].** These bits with fecn_fillX[8:6] determine the queue's fill level in cells (64 bytes) where the FECN bit is set in outgoing cells. The FECN bit is set only when the queueX_fecn_en bit is '1.'
fecn_fillX[8:6]	12h	15:13	RW		**FECN Fill for Queue X [8:6].** These bits with fecn_fillX[24:9] determine the queue's fill level in cells (64 bytes) where the FECN bit is set in outgoing cells. The FECN bit is set only when the queueX_fecn_en bit is '1.'
Reserved		12:0	RO		**Reserved.**
clp_fillX[24:9]	14h	15:0	RW		**CLP Fill for Queue X [24:9].** These bits with clp_fillX[8:6] determine the queue's fill level in cells (64 bytes) where incoming cells with their CLP bit set will be discarded. The incoming cell is dropped at this fill level only when the queueX_clp_en bit is '1.'
clp_fillX[8:6]	16h	15:13	RW		**CLP Fill for Queue X [8:6].** These bits with clp_fillX[24:9] determine the queue's fill level in cells (64 bytes) where incoming cells with their CLP bit set will be discarded. The incoming cell is dropped at this fill level only when the queueX_clp_en bit is '1.'
Reserved		12:0	RO		**Reserved.**

14 Registers (continued)

Table 173. Queue X Definition Structure (QXDEF) (2000h to 2FFEh) (continued)

Name	Offset	Bit Pos.	Type	Reset	Description
The letter X in the data structure name and in the bit names represents the values of 0 through 127 for the 128 queues shown below.					

Structure Name	Base Address	Structure Name	Base Address
Queue 0 Base Address High	(2000h)	Queue 32 Base Address High	(2400h)
Queue 1 Base Address High	(2020h)	Queue 33 Base Address High	(2420h)
Queue 2 Base Address High	(2040h)	Queue 34 Base Address High	(2440h)
Queue 3 Base Address High	(2060h)	Queue 35 Base Address High	(2460h)
Queue 4 Base Address High	(2080h)	Queue 36 Base Address High	(2480h)
Queue 5 Base Address High	(20A0h)	Queue 37 Base Address High	(24A0h)
Queue 6 Base Address High	(20C0h)	Queue 38 Base Address High	(24C0h)
Queue 7 Base Address High	(20E0h)	Queue 39 Base Address High	(24E0h)
Queue 8 Base Address High	(2100h)	Queue 40 Base Address High	(2500h)
Queue 9 Base Address High	(2120h)	Queue 41 Base Address High	(2520h)
Queue 10 Base Address High	(2140h)	Queue 42 Base Address High	(2540h)
Queue 11 Base Address High	(2160h)	Queue 43 Base Address High	(2560h)
Queue 12 Base Address High	(2180h)	Queue 44 Base Address High	(2580h)
Queue 13 Base Address High	(21A0h)	Queue 45 Base Address High	(25A0h)
Queue 14 Base Address High	(21C0h)	Queue 46 Base Address High	(25C0h)
Queue 15 Base Address High	(21E0h)	Queue 47 Base Address High	(25E0h)
Queue 16 Base Address High	(2200h)	Queue 48 Base Address High	(2600h)
Queue 17 Base Address High	(2220h)	Queue 49 Base Address High	(2620h)
Queue 18 Base Address High	(2240h)	Queue 50 Base Address High	(2640h)
Queue 19 Base Address High	(2260h)	Queue 51 Base Address High	(2660h)
Queue 20 Base Address High	(2280h)	Queue 52 Base Address High	(2680h)
Queue 21 Base Address High	(22A0h)	Queue 53 Base Address High	(26A0h)
Queue 22 Base Address High	(22C0h)	Queue 54 Base Address High	(26C0h)
Queue 23 Base Address High	(22E0h)	Queue 55 Base Address High	(26E0h)
Queue 24 Base Address High	(2300h)	Queue 56 Base Address High	(2700h)
Queue 25 Base Address High	(2320h)	Queue 57 Base Address High	(2720h)
Queue 26 Base Address High	(2340h)	Queue 58 Base Address High	(2740h)
Queue 27 Base Address High	(2360h)	Queue 59 Base Address High	(2760h)
Queue 28 Base Address High	(2380h)	Queue 60 Base Address High	(2780h)
Queue 29 Base Address High	(23A0h)	Queue 61 Base Address High	(27A0h)
Queue 30 Base Address High	(23C0h)	Queue 62 Base Address High	(27C0h)
Queue 31 Base Address High	(23E0h)	Queue 63 Base Address High	(27E0h)

14 Registers (continued)

Table 173. Queue X Definition Structure (QXDEF) (2000h to 2FFEh) (continued)

Name	Offset	Bit Pos.	Type	Reset	Description
The letter X in the data structure name and in the bit names represents the values of 0 through 127 for the 128 queues shown below.					

Structure Name	Base Address	Structure Name	Base Address
Queue 64 Base Address High	(2800h)	Queue 96 Base Address High	(2C00h)
Queue 65 Base Address High	(2820h)	Queue 97 Base Address High	(2C20h)
Queue 66 Base Address High	(2840h)	Queue 98 Base Address High	(2C40h)
Queue 67 Base Address High	(2860h)	Queue 99 Base Address High	(2C60h)
Queue 68 Base Address High	(2880h)	Queue 100 Base Address High	(2C80h)
Queue 69 Base Address High	(28A0h)	Queue 101 Base Address High	(2CA0h)
Queue 70 Base Address High	(28C0h)	Queue 102 Base Address High	(2CC0h)
Queue 71 Base Address High	(28E0h)	Queue 103 Base Address High	(2CE0h)
Queue 72 Base Address High	(2900h)	Queue 104 Base Address High	(2D00h)
Queue 73 Base Address High	(2920h)	Queue 105 Base Address High	(2D20h)
Queue 74 Base Address High	(2940h)	Queue 106 Base Address High	(2D40h)
Queue 75 Base Address High	(2960h)	Queue 107 Base Address High	(2D60h)
Queue 76 Base Address High	(2980h)	Queue 108 Base Address High	(2D80h)
Queue 77 Base Address High	(29A0h)	Queue 109 Base Address High	(2DA0h)
Queue 78 Base Address High	(29C0h)	Queue 110 Base Address High	(2DC0h)
Queue 79 Base Address High	(29E0h)	Queue 111 Base Address High	(2DE0h)
Queue 80 Base Address High	(2A00h)	Queue 112 Base Address High	(2E00h)
Queue 81 Base Address High	(2A20h)	Queue 113 Base Address High	(2E20h)
Queue 82 Base Address High	(2A40h)	Queue 114 Base Address High	(2E40h)
Queue 83 Base Address High	(2A60h)	Queue 115 Base Address High	(2E60h)
Queue 84 Base Address High	(2A80h)	Queue 116 Base Address High	(2E80h)
Queue 85 Base Address High	(2AA0h)	Queue 117 Base Address High	(2EA0h)
Queue 86 Base Address High	(2AC0h)	Queue 118 Base Address High	(2EC0h)
Queue 87 Base Address High	(2AE0h)	Queue 119 Base Address High	(2EE0h)
Queue 88 Base Address High	(2B00h)	Queue 120 Base Address High	(2F00h)
Queue 89 Base Address High	(2B20h)	Queue 121 Base Address High	(2F20h)
Queue 90 Base Address High	(2B40h)	Queue 122 Base Address High	(2F40h)
Queue 91 Base Address High	(2B60h)	Queue 123 Base Address High	(2F60h)
Queue 92 Base Address High	(2B80h)	Queue 124 Base Address High	(2F80h)
Queue 93 Base Address High	(2BA0h)	Queue 125 Base Address High	(2FA0h)
Queue 94 Base Address High	(2BC0h)	Queue 126 Base Address High	(2FC0h)
Queue 95 Base Address High	(2BE0h)	Queue 127 Base Address High	(2FE0h)

14 Registers (continued)

14.3.4 Various Internal Memories

14.3.4.1 Control Cell Memories

Table 174. Control Cell Receive Extended Memory (CCRXEM) (07FCh to 0832h)

The control cell receive memory may also be accessed from direct memory. See Table 51.

Name	Offset	Type	Reset	Description
cell_bus_routing_header	0	RO	X	These 56 bytes are the control cell received from the cell bus. When present, the control cell may be read from this extended memory space.
tandem_routing_header	2			
header[31:16]	4			
header[15:0]	6			
payload_bytes 0—1	8			
. . .	. . .			
payload_bytes 46—47	36h			

Table 175. Control Cell Transmit Extended Memory (CCTXEM) (0900h to 0936h)

The control cell transmit memory may also be accessed from direct memory. See Table 52.

Name	Offset	Type	Reset	Description
cell_bus_routing_header	0	RW	X	These 56 bytes are the cell routing header, the tandem routing header, and the control cell to be transmitted onto the cell bus. A control cell to be transmitted may be written to this extended memory space.
tandem_routing_header	2			
header[31:16]	4			
header[15:0]	6			
payload_bytes 0—1	8			
. . .	. . .			
payload_bytes 46—47	36h			

14 Registers (continued)

14.3.4.2 Multicast Number Memories

Table 176. PHY Port 0 and Control Cells Multicast Extended Memory (PP0MEM) (0C00h to 0C1Eh)

The PHY port 0 and control cells multicast memory may also be accessed from direct memory (see Table 53).

Name	Offset	Type	Reset	Description
multicast_receive_enable[15:0]	00h	RW	X	This memory space contains 256 active-high enable bits. Each bit represents a multicast net number from 0 through 255. If a bit is set, the corresponding multicast net number data cell is sent to the queue group for PHY port 0, or the corresponding multicast control cell is sent to the control cell receive direct and extended memory. The least significant bit is multicast net number 0.
multicast_receive_enable[31:16]	02h			
multicast_receive_enable[47:32]	04h			
. . .	. . .			
multicast_receive_enable[191:176]	16h			
multicast_receive_enable[207:192]	18h			
multicast_receive_enable[223:208]	1Ah			
multicast_receive_enable[239:224]	1Ch			
multicast_receive_enable[255:240]	1Eh			

14 Registers (continued)

Table 177. PHY Port X Multicast Memory (PPXMM) (0C20h to 0FFEh)

Name	Offset	Type	Reset	Description
multicast_receive_enable[15:0]	00h	RW	X	This memory space contains 256 active-high enable bits. Each bit represents a multicast net number from 0 through 255. If a bit is set, the corresponding multicast net number data cell is sent to the queue group for PHY port X. The least significant bit is multicast net number 0.
multicast_receive_enable[31:16]	02h			
multicast_receive_enable[47:32]	04h			
. . .	. . .			
multicast_receive_enable[239:224]	1Ch			
multicast_receive_enable[255:240]	1Eh			

The letter X in the data structure and in the bit names represents the values of 1 through 31 for 31 of the 32 PHY ports. The base addresses of the 31 multicast memory locations are shown below.

Memory Name	Base Address
PHY Port 1 Multicast Memory	(0C20h)
PHY Port 2 Multicast Memory	(0C40h)
PHY Port 3 Multicast Memory	(0C60h)
PHY Port 4 Multicast Memory	(0C80h)
PHY Port 5 Multicast Memory	(0CA0h)
PHY Port 6 Multicast Memory	(0CC0h)
PHY Port 7 Multicast Memory	(0CE0h)
PHY Port 8 Multicast Memory	(0D00h)
PHY Port 9 Multicast Memory	(0D20h)
PHY Port 10 Multicast Memory	(0D40h)
PHY Port 11 Multicast Memory	(0D60h)
PHY Port 12 Multicast Memory	(0D80h)
PHY Port 13 Multicast Memory	(0DA0h)
PHY Port 14 Multicast Memory	(0DC0h)
PHY Port 15 Multicast Memory	(0DE0h)
PHY Port 16 Multicast Memory	(0E00h)
PHY Port 17 Multicast Memory	(0E20h)
PHY Port 18 Multicast Memory	(0E40h)
PHY Port 19 Multicast Memory	(0E60h)
PHY Port 20 Multicast Memory	(0E80h)
PHY Port 21 Multicast Memory	(0EA0h)
PHY Port 22 Multicast Memory	(0EC0h)
PHY Port 23 Multicast Memory	(0EE0h)
PHY Port 24 Multicast Memory	(0F00h)
PHY Port 25 Multicast Memory	(0F20h)
PHY Port 26 Multicast Memory	(0F40h)
PHY Port 27 Multicast Memory	(0F60h)
PHY Port 28 Multicast Memory	(0F80h)
PHY Port 29 Multicast Memory	(0FA0h)
PHY Port 30 Multicast Memory	(0FC0h)
PHY Port 31 Multicast Memory	(0FE0h)

14 Registers (continued)

14.3.4.3 PPD State Memory

Table 178. PPD Memory (PPDM) (1000h to 13FEh)

Name	Offset	Type	Reset	Description
word0	00h	RW	X	This memory space contains 8192 AAL5 virtual channel PPD bits. The PPD pointer bits in the cell header, cell bus routing header, and tandem routing header, which are selected by the PPD pointer select bits, point to a single bit in this memory space. If the bit for a corresponding AAL5 virtual channel is '0,' no cells are dropped. If the bit is '1,' all remaining cells in the packet, except the last cell, are dropped. A PPD bit becomes set when a cell in an AAL5 virtual channel packet is dropped. The last cell of a packet is identified by the least significant bit of the PTI field in the cell header, which is set to '1.' The most significant bit of the PTI field is also checked to be '0' (user data). The final cell of the packet is sent, and the corresponding PPD bit is cleared. The most significant bit of word0 corresponds to AAL5 virtual channel zero, and the least significant bit of word1FF corresponds to AAL5 virtual channel 8191.
word1	02h			
word2	04h			
word3	06h			
word4	08h			
word5	0Ah			
word6	0Ch			
word7	0Eh			
. . .	. . .			
word1F9	3F2h			
word1FA	3F4h			
word1FB	3F6h			
word 1FC	3F8h			
word1FD	3FAh			
word1FE	3FCh			
word1FF	3FEh			

14 Registers (continued)

14.3.5 Dropped Cell Count

These registers count only cells dropped on SDRAM or TX UTOPIA CELL BUFFER (256 cells). They cannot count cells dropped at TX PHY FIFO.

Table 179. Queue X Dropped Cell Count (QXDCC) (3000h to 31FEh)

Name	Offset	Bit Pos.	Type	Reset	Description
queueX_drop_cell_cnt[23:16]	00h	7:0	RW	0	**Queue X Drop Cell Count[23:16].** The queueX_drop_cell_cnt[23:16] and queueX_drop_cell_cnt[15:0] fields together are a free-running counter of cells dropped on queue X of the SDRAM or TX UTOPIA cell buffer.
queueX_drop_cell_ovrfl[23:16]	00h	8	RW	0	**Queue X Drop Cell Counter Overflow.** If this bit is set to ‘1’ by the T8208 logic, it indicates that the dropped cell counter for queue X has overflowed. Once this bit is set, it stays set until it is cleared by the customer (this bit is cleared automatically after a read operation if clear_on_read, bit 12 in register 0112h is set to ‘1’). If this bit is ‘0,’ it indicates that the dropped cell counter for queue X has not overflowed.
queueX_drop_clp0_cell_dis	00h	9	RW	0	**Queue X clp0 Cells Discarded.** If this bit is set to ‘1’ by the T8208 logic, it indicates that cells with clp = 0 have been discarded for queue X. Once this bit is set, it stays set until it is cleared by the customer (this bit is cleared automatically after a read operation if clear_on_read, bit 12 in register 0112h is set to ‘1’). If this bit is ‘0,’ it indicates that cells with clp = 0 have not been discarded.
Reserved	00h	15:10	RW	0	**Reserved.** Program to ‘0.’
queueX_drop_cell_cnt[15:0]	02h	15:0	RW	0	**Queue X Drop Cell Count[15:0].** The queueX_drop_cell_cnt[23:16] and queueX_drop_cell_cnt[15:0] fields together are a free-running counter of cells dropped on queue X of the SDRAM or TX UTOPIA cell buffer.

14 Registers (continued)

Table 179. Queue X Dropped Cell Count (QXDCC) (3000h to 31FEh) (continued)

Name	Offset	Bit Pos.	Type	Reset	Description
The letter X in the data structure name and in the bit names represents the values of 0 through 127 for the 128 queues shown below.					

Structure Name	Base Address	Structure Name	Base Address
Queue 0 Base Address	(3000h)	Queue 32 Base Address	(3080h)
Queue 1 Base Address	(3004h)	Queue 33 Base Address	(3084h)
Queue 2 Base Address	(3008h)	Queue 34 Base Address	(3088h)
Queue 3 Base Address	(300Ch)	Queue 35 Base Address	(308Ch)
Queue 4 Base Address	(3010h)	Queue 36 Base Address	(3090h)
Queue 5 Base Address	(3014h)	Queue 37 Base Address	(3094h)
Queue 6 Base Address	(3018h)	Queue 38 Base Address	(3098h)
Queue 7 Base Address	(301Ch)	Queue 39 Base Address	(309Ch)
Queue 8 Base Address	(3020h)	Queue 40 Base Address	(30A0h)
Queue 9 Base Address	(3024h)	Queue 41 Base Address	(30A4h)
Queue 10 Base Address	(3028h)	Queue 42 Base Address	(30A8h)
Queue 11 Base Address	(302Ch)	Queue 43 Base Address	(30ACh)
Queue 12 Base Address	(3030h)	Queue 44 Base Address	(30B0h)
Queue 13 Base Address	(3034h)	Queue 45 Base Address	(30B4h)
Queue 14 Base Address	(3038h)	Queue 46 Base Address	(30B8h)
Queue 15 Base Address	(303Ch)	Queue 47 Base Address	(30BCh)
Queue 16 Base Address	(3040h)	Queue 48 Base Address	(30C0h)
Queue 17 Base Address	(3044h)	Queue 49 Base Address	(30C4h)
Queue 18 Base Address	(3048h)	Queue 50 Base Address	(30C8h)
Queue 19 Base Address	(304Ch)	Queue 51 Base Address	(30CCh)
Queue 20 Base Address	(3050h)	Queue 52 Base Address	(30D0h)
Queue 21 Base Address	(3054h)	Queue 53 Base Address	(30D4h)
Queue 22 Base Address	(3058h)	Queue 54 Base Address	(30D8h)
Queue 23 Base Address	(305Ch)	Queue 55 Base Address	(30DCh)
Queue 24 Base Address	(3060h)	Queue 56 Base Address	(30E0h)
Queue 25 Base Address	(3064h)	Queue 57 Base Address	(30E4h)
Queue 26 Base Address	(3068h)	Queue 58 Base Address	(30E8h)
Queue 27 Base Address	(306Ch)	Queue 59 Base Address	(30ECh)
Queue 28 Base Address	(3070h)	Queue 60 Base Address	(30F0h)
Queue 29 Base Address	(3074h)	Queue 61 Base Address	(30F4h)
Queue 30 Base Address	(3078h)	Queue 62 Base Address	(30F8h)
Queue 31 Base Address	(307Ch)	Queue 63 Base Address	(30FCh)

14 Registers (continued)

Table 179. Queue X Dropped Cell Count (QXDCC) (3000h to 31FEh) (continued)

Name	Offset	Bit Pos.	Type	Reset	Description
The letter X in the data structure name and in the bit names represents the values of 0 through 127 for the 128 queues shown below.					

Structure Name	Base Address	Structure Name	Base Address
Queue 64 Base Address	(3100h)	Queue 96 Base Address	(3180h)
Queue 65 Base Address	(3104h)	Queue 97 Base Address	(3184h)
Queue 66 Base Address	(3108h)	Queue 98 Base Address	(3188h)
Queue 67 Base Address	(310Ch)	Queue 99 Base Address	(318Ch)
Queue 68 Base Address	(3110h)	Queue 100 Base Address	(3190h)
Queue 69 Base Address	(3114h)	Queue 101 Base Address	(3194h)
Queue 70 Base Address	(3118h)	Queue 102 Base Address	(3198h)
Queue 71 Base Address	(311Ch)	Queue 103 Base Address	(319Ch)
Queue 72 Base Address	(3120h)	Queue 104 Base Address	(31A0h)
Queue 73 Base Address	(3124h)	Queue 105 Base Address	(31A4h)
Queue 74 Base Address	(3128h)	Queue 106 Base Address	(31A8h)
Queue 75 Base Address	(312Ch)	Queue 107 Base Address	(31ACh)
Queue 76 Base Address	(3130h)	Queue 108 Base Address	(31B0h)
Queue 77 Base Address	(3134h)	Queue 109 Base Address	(31B4h)
Queue 78 Base Address	(3138h)	Queue 110 Base Address	(31B8h)
Queue 79 Base Address	(313Ch)	Queue 111 Base Address	(31BCh)
Queue 80 Base Address	(3140h)	Queue 112 Base Address	(31C0h)
Queue 81 Base Address	(3144h)	Queue 113 Base Address	(31C4h)
Queue 82 Base Address	(3148h)	Queue 114 Base Address	(31C8h)
Queue 83 Base Address	(314Ch)	Queue 115 Base Address	(31CCh)
Queue 84 Base Address	(3150h)	Queue 116 Base Address	(31D0h)
Queue 85 Base Address	(3154h)	Queue 117 Base Address	(31D4h)
Queue 86 Base Address	(3158h)	Queue 118 Base Address	(31D8h)
Queue 87 Base Address	(315Ch)	Queue 119 Base Address	(31DCh)
Queue 88 Base Address	(3160h)	Queue 120 Base Address	(31E0h)
Queue 89 Base Address	(3164h)	Queue 121 Base Address	(31E4h)
Queue 90 Base Address	(3168h)	Queue 122 Base Address	(31E8h)
Queue 91 Base Address	(316Ch)	Queue 123 Base Address	(31ECh)
Queue 92 Base Address	(3170h)	Queue 124 Base Address	(31F0h)
Queue 93 Base Address	(3174h)	Queue 125 Base Address	(31F4h)
Queue 94 Base Address	(3178h)	Queue 126 Base Address	(31F8h)
Queue 95 Base Address	(317Ch)	Queue 127 Base Address	(31FCh)

14 Registers (continued)

14.3.6 External Memories

14.3.6.1 Look-Up Translation Memory

Table 180. Translation RAM Memory (TRAM) (100000h to 17FFFEh)

Name	Offset	Type	Reset	Description
word0	00h	RW	X	This memory space is used to access the translation RAM memory.
. . .	. . .			
word3FFFF	7FFFEh			

14.3.6.2 SDRAM Buffer Memory

Table 181. SDRAM (SDRAM) (2000000h to 3FFFFFEh)

Name	Offset	Type	Reset	Description
word0	00h	RW	X	This memory space is used to access the SDRAM memory.
. . .	. . .			
wordFFFFFE	1FFFFFEh			

15 Absolute Maximum Ratings

Stresses in excess of the absolute maximum ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of the data sheet. Exposure to absolute maximum ratings for extended periods can adversely affect device reliability.

Table 182. Maximum Rating Parameters and Values

Parameter	Symbol	Min	Typ	Max	Unit
dc Supply Voltage with Respect to Ground	V_{DD}	—	—	4.2	V
Input Voltage Range[1]	V_{I1}	V_{SS} – 0.3	—	V_{DD} + 0.3	V
Junction Temperature Range	T_J	–40	—	125	°C
Storage Temperature	T_{stg}	–60	—	160	°C
Maximum Power Dissipation (package limit)[2]	P_D	—	—	2.44	W

1. Except for 5 V tolerant buffers where V_{IHmax} = 5.5 V + 0.3 V.
2. Maximum power dissipation may be determined from the following equation: $P_D = (125\ °C – T_A)/22.5\ °C/W$.

16 Recommended Operating Conditions

Table 183. Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
dc Supply Voltage with Respect to Ground	V_{DD}	3.0	—	3.6	V
Ambient Operating Temperature Range	T_A	–40	—	85	°C

17 Handling Precautions

Although protection circuitry has been designed into this device, proper precautions should be taken to avoid exposure to electrostatic discharge (ESD) during handling and mounting. Agere employs a human-body model (HBM) and a charged-device model (CDM) for ESD-susceptibility testing and protection design evaluation. ESD voltage thresholds are dependent on the circuit parameters used to define the model. No industry-wide standard has been adopted for the CDM. A standard HBM (resistance = 1500 Ω, capacitance = 100 pF) is widely accepted and can be used for comparison. The HBM ESD threshold presented here was obtained by using these circuit parameters.

Table 184. HBM ESD Threshold

Device	Voltage (V)
T8208	2000

18 Electrical Requirements and Characteristics

18.1 Crystal Information

The *CelXpres* T8208 device requires a crystal or external clock source. The crystal may have a frequency from 5 MHz to 40 MHz and is connected between xtalin and xtalout. External 5% capacitors must be connected from xtalin and xtalout to V_{SS}. The value of the external capacitors is determined from the crystal data sheet using the crystal specification requirements shown below.

Table 185. Crystal Specifications

Parameter	Value
Frequency	5 MHz to 40 MHz.
Oscillation Mode	Fundamental parallel resonant.
Effective Series Resistance	See Figure 19 below.
Frequency Tolerance and Stability	5%.

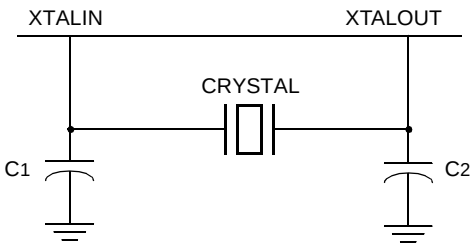


Figure 18. Crystal

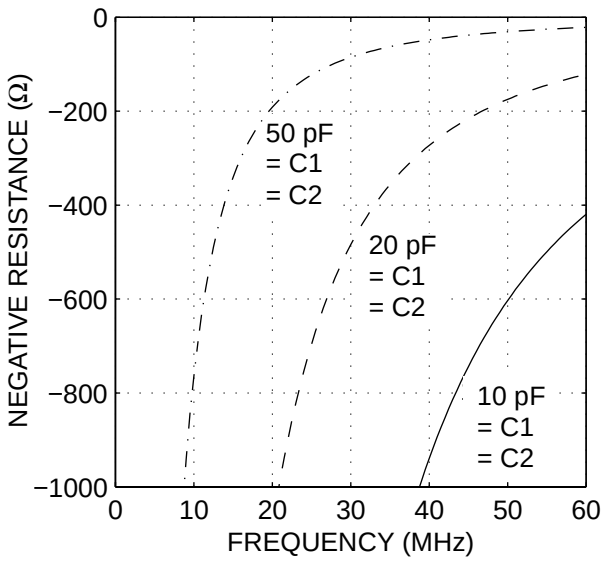


Figure 19. Negative Resistance Plot

The xtalin input may be driven by an external clock instead of a crystal. The frequency of the external source may be 5 MHz to 50 MHz. The external clock must meet the requirements shown below.

Table 186. External Clock Requirements

Parameter	Min	Max
Frequency	5 MHz	50 MHz
Maximum Rise or Fall Time	—	5 ns
Duty Cycle	40%	60%

The frequency of the T8208's main clock (mclk) is derived from the clock at the xtalin input (pclk). See Section 5, PLL Configuration, for more information on these clocks.

18 Electrical Requirements and Characteristics (continued)

18.2 dc Electrical Characteristics

The following conditions apply except where noted: T_A = –40 °C to +85 °C, V_{DD} = 3.3 V ± 10%, 15 pF each output.

Table 187. dc Electrical Characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Current	I_{DD}	—	—	—	—	mA
Input Voltage (TTL):						
Low	V_{IL}	—	—	—	0.8	V
High	V_{IH}	—	2.0	—	—	V
Input Voltage (TTL 5 V tolerant):						
Low	V_{IL}	—	—	—	0.8	V
High	V_{IH}	—	2.0	—	5.5	V
Input Voltage (GTL+):						
Low	V_{IL}	—	—	—	0.8	V
High	V_{IH}	—	1.2	—	—	V
Input Voltage (xtalin):						
Low	V_{IL}	—	—	—	0.2 V_{DD}	V
High	V_{IH}	—	0.7 V_{DD}	—	—	V
Output Voltage (TTL 4 mA):						
Low	V_{OL}	I_{OL} = 4 mA	—	—	0.4	V
High	V_{OH}	I_{OH} = –4 mA	2.4	—	—	V
Output Voltage (TTL 6 mA):						
Low	V_{OL}	I_{OL} = 6 mA	—	—	0.4	V
High	V_{OH}	I_{OH} = –6 mA	2.4	—	—	V
Output Voltage (TTL 7 mA):						
Low	V_{OL}	I_{OL} = 7 mA	—	—	0.4	V
High	V_{OH}	I_{OH} = –7 mA	2.4	—	—	V
Output Voltage (TTL 10 mA):						
Low	V_{OL}	I_{OL} = 10 mA	—	—	0.4	V
High	V_{OH}	I_{OH} = –10 mA	2.4	—	—	V
Output Current (GTL+)	I_{OL}	—	65	—	75	mA
Output Voltage (GTL+)	V_{OL}	—	—	0.3	0.5	V
Input Leakage Current (TTL)	—	—	—	—	1	µA
Input Leakage Current (TTL with pull-ups)	—	V_{IL} = V_{SS}	—	—	67	µA
Input Leakage Current (cb_vref)	—	—	—	—	40	µA
Power Dissipation	P_D	—	—	—	1.5*	W

* This is the power consumed by the device under the following conditions: V_{DD} = 3.3 V, pclk = 20 MHz, mclk = 100 MHz, UTOPIA clock = 20 MHz, cell bus clock = 30 MHz, nominal slew rate (register 2Eh).

19 Timing Requirements

The following section describes the timing requirements. Capacitve loading is in the range of 10 pF to 50 pF, unless otherwise specified.

Some timing requirements are dependent on the frequency of pclk or mclk. The terms mclkp and pclkp refer to the period of their respective clocks in ns when used in the following tables.

Table 188. Input Clocks

Clock Name	Frequency (Max)	Voltage Level		Rise Time (Max)	Fall Time (Max)	Pulse Width (Min)	
		High	Low			High	Low
cb_wc*	66 MHz	—	—	—	—	6.06 ns	6.06 ns
cb_rc*	66 MHz	—	—	—	—	6.06 ns	6.06 ns
u_rxclk	50 MHz	2.0 V	0.8 V	4.0 ns	4.0 ns	8.0 ns	8.0 ns
u_txclk	50 MHz	2.0 V	0.8 V	4.0 ns	4.0 ns	8.0 ns	8.0 ns

Note: The cell bus write clock (cb_wc*) should be delayed 1.5 ns to 4 ns relative to the cell bus read clock (cb_rc*) to ensure sufficient data hold time.

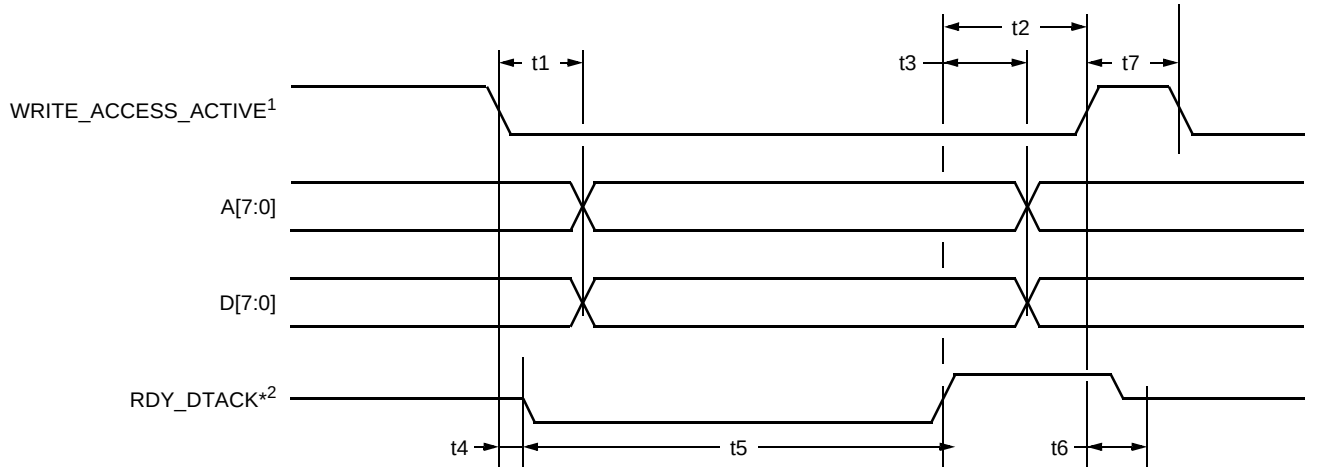
Table 189. Output Clocks

Clock Name	Frequency (Max)	Rise Time (Max)	Fall Time (Max)	Pulse Width (Min)		Load
				High	Low	
sd_clk	100 MHz	1.0 ns	1.0 ns	4.0 ns	4.0 ns	15 pF
u_rxclk	50 MHz	2.0 ns	2.0 ns	8.0 ns	8.0 ns	40 pF
u_txclk	50 MHz	2.0 ns	2.0 ns	8.0 ns	8.0 ns	40 pF
cb_gen_wc*	66 MHz	1.5 ns	1.5 ns	6.0 ns	6.0 ns	—
cb_gen_rc*	66 MHz	1.5 ns	1.5 ns	6.0 ns	6.0 ns	—

19 Timing Requirements (continued)

19.1 Microprocessor Interface Timing

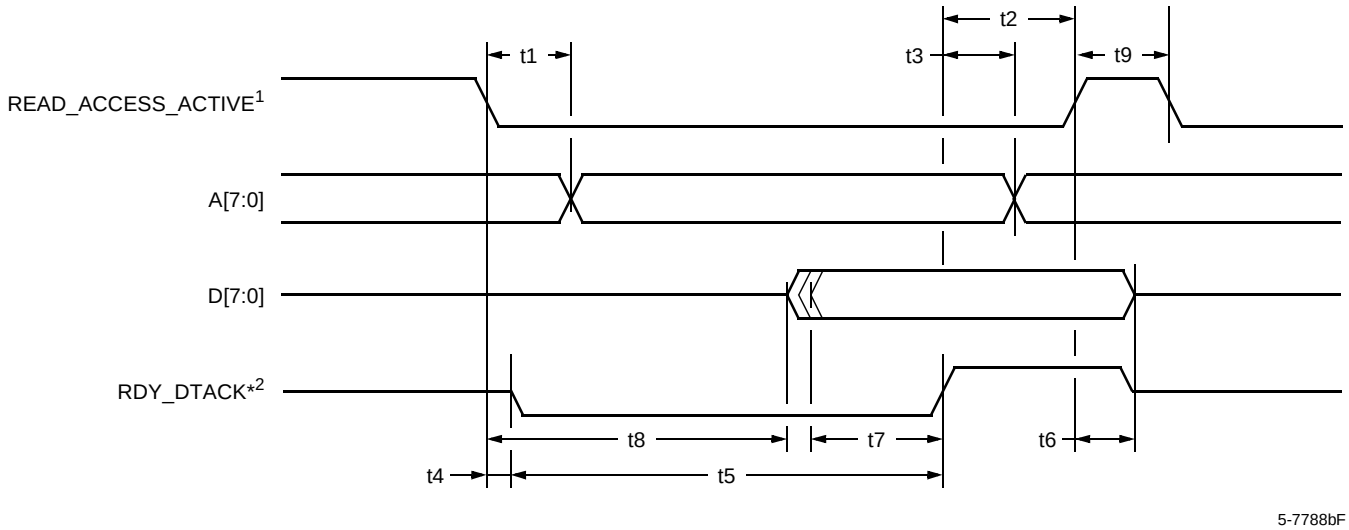
For access time information, see Section 6.3.2, *CelXpres* T8208 Access Performance.



1. write_access_active is the logical OR function of sel* and wr*_ds*.
2. Load is 15 pF.

Note: sel* and wr*_ds* must not have coinciding edges in opposite directions to prevent glitches on the write_access_active signal.

Figure 20. Nonmultiplexed *Intel* Mode Write Access Timing



1. read_access_active is the logical OR function of sel* and rd*_wr*.
2. Load is 15 pF.

Note: sel* and rd*_wr* must not have coinciding edges in opposite directions to prevent glitches on the read_access_active signals.

Figure 21. Nonmultiplexed *Intel* Mode Read Access Timing

19 Timing Requirements (continued)

Table 190. Nonmultiplexed *Intel* Mode Write Access Timing

Symbol	Parameter	Min	Typ	Max	Unit
t1	write_access_active Falling Edge to a[7:0] and d[7:0] Valid	—	—	2 x pclkp – 4	ns
t2	rdy_dtack* Rising Edge to write_access_active Rising Edge	0	—	—	ns
t3	rdy_dtack* Rising Edge to a[7:0] and d[7:0] Invalid	0	—	—	ns
t4	write_access_active Falling Edge to rdy_dtack* Falling Edge	0	—	12	ns
t5	rdy_dtack* Low Pulse Width[1]	—	—	—	—
t6	write_access_active Rising Edge to rdy_dtack* 3_state	0	—	5	ns
t7	write_access_active Rising Edge to write_access_active Falling Edge	25	—	—	ns

1. See access times in Table 11.

Note: The term pclkp in the table represents the period of pclk in ns.

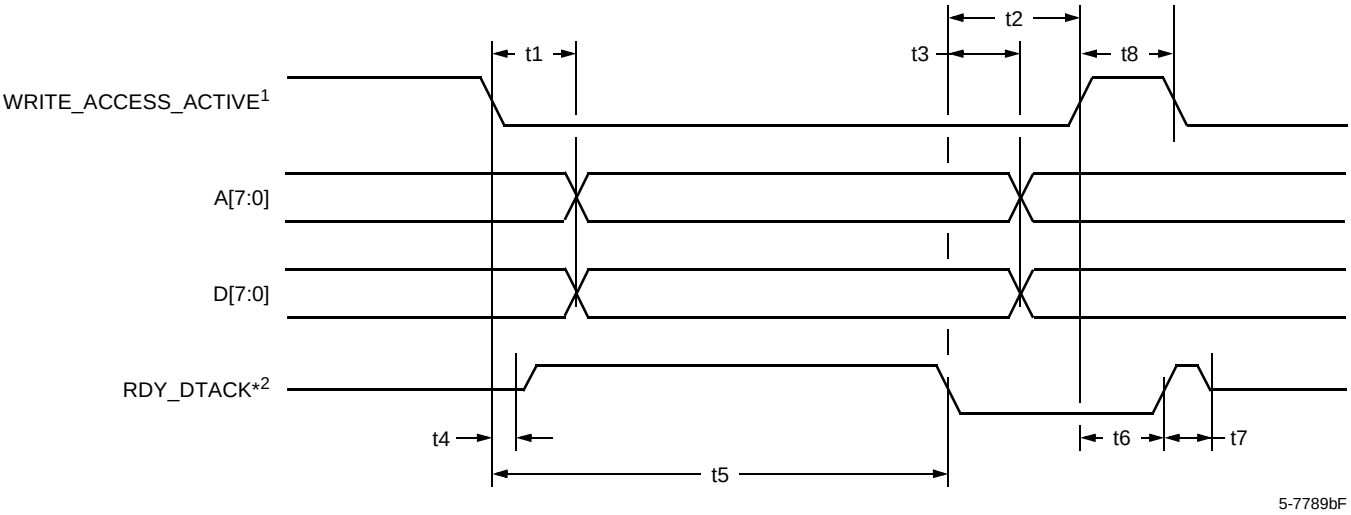
Table 191. Nonmultiplexed *Intel* Mode Read Access Timing

Symbol	Parameter	Min	Typ	Max	Unit
t1	read_access_active Falling Edge to a[7:0]	—	—	2 x pclkp – 4	ns
t2	rdy_dtack* Rising Edge to read_access_active Rising Edge	0	—	—	ns
t3	rdy_dtack* Rising Edge to a[7:0] Invalid	0	—	—	ns
t4	read_access_active Falling Edge to rdy_dtack* Falling Edge	0	—	12	ns
t5	rdy_dtack* Low Pulse Width[1]	—	—	—	—
t6	read_access_active Rising Edge to d[7:0] Invalid	0	—	5	ns
t7	d[7:0] Valid to rdy_dtack* Rising Edge	pclkp – 4	—	—	ns
t8	read_access_active Falling Edge to d[7:0] Drive	3 x pclkp – 4	—	—	ns
t9	read_access_active Rising Edge to read_access_active Falling Edge	25	—	—	ns

1. See access times in Table 11.

Note: The term pclkp in the table represents the period of pclk in ns.

19 Timing Requirements (continued)

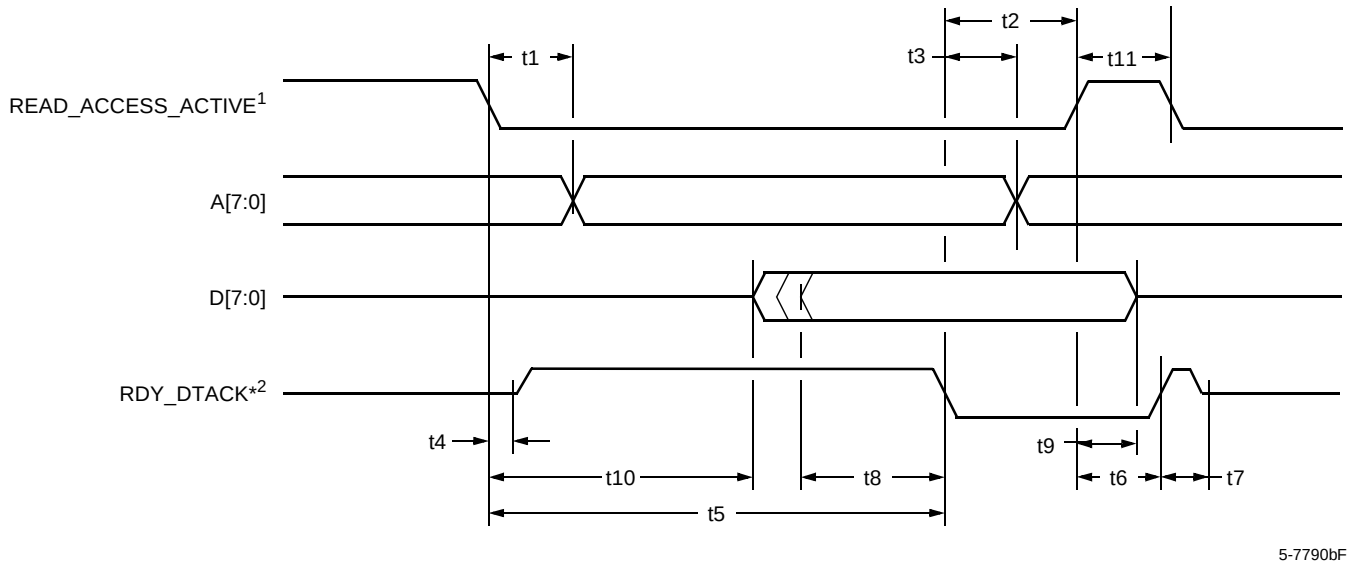


1. write_access_active is the logical OR function of sel*, wr*_ds*, and rd*_wr*.
2. Load is 50 pF.

Notes:
sel* and wr*_ds* must not have coinciding edges in opposite directions to prevent glitches on the write_access_active signal.

rd*_wr* must be stable any time both sel* and wr*_ds* are low to prevent glitches on the write_access_active signals.

Figure 22. *Motorola* Mode Write Access Timing



1. read_access_active is the logical OR function of sel*, wr*_ds*, and $\overline{\text{rd*\_wr*}}$.
2. Load is 50 pF.

Notes:
sel* and wr*_ds* must not have coinciding edges in opposite directions to prevent glitches on the read_access_active signal.

rd*_wr* must be stable any time both sel* and wr*_ds* are low to prevent glitches on the read_access_active signals.

Figure 23. *Motorola* Mode Read Access Timing

19 Timing Requirements (continued)

Table 192. *Motorola* Mode Write Access Timing

Symbol	Parameter	Min	Typ	Max	Unit
t1	write_access_active Falling Edge to a[7:0] and d[7:0] Valid	—	—	2 x pclkp – 4	ns
t2	rdy_dtack* Falling Edge to write_access_active Rising Edge	0	—	—	ns
t3	rdy_dtack* Falling Edge to a[7:0] and d[7:0] Invalid	0	—	—	ns
t4	write_access_active Falling Edge to rdy_dtack* Drive	0	—	12	ns
t5	write_access_active Falling Edge to rdy_dtack* Falling Edge[1]	—	—	—	—
t6	write_access_active Rising Edge to rdy_dtack* Rising Edge	0	—	5	ns
t7	rdy_dtack* Rising Edge to rdy_dtack* 3-state	1	—	5	ns
t8	write_access_active Rising Edge to write_access_active Falling Edge	25	—	—	ns

1. See access times in Table 11.

Note: The term pclkp in the table represents the period of pclk in ns.

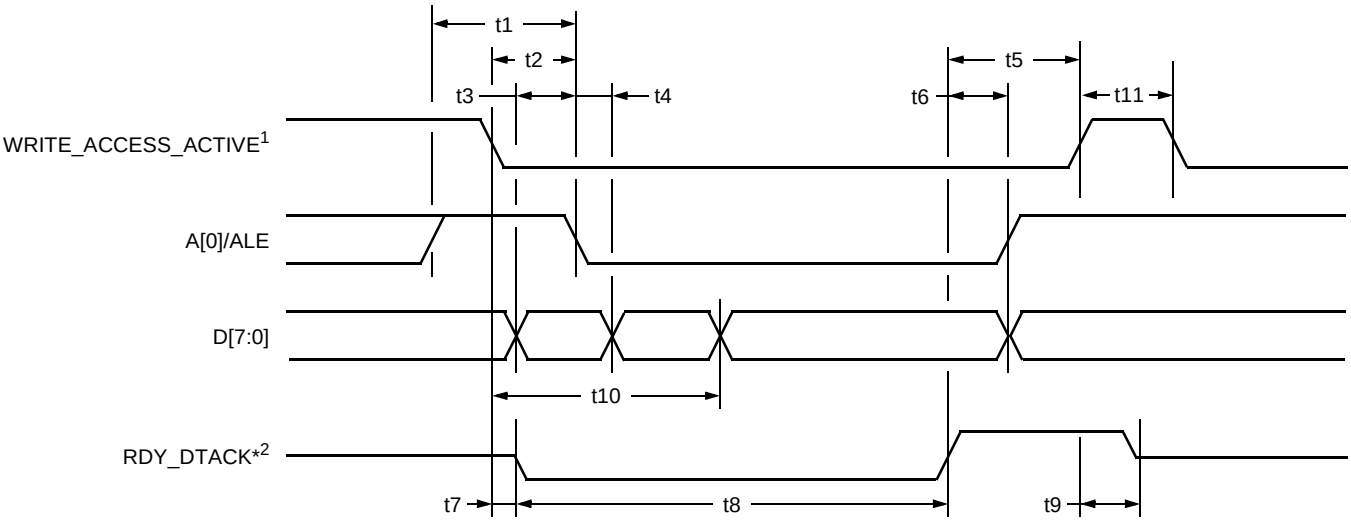
Table 193. *Motorola* Mode Read Access Timing

Symbol	Parameter	Min	Typ	Max	Unit
t1	read_access_active Falling Edge to a[7:0] Valid	—	—	2 x pclkp – 4	ns
t2	rdy_dtack* Falling Edge to read_access_active Rising Edge	0	—	—	ns
t3	rdy_dtack* Falling Edge to a[7:0] Invalid	0	—	—	ns
t4	read_access_active Falling Edge to rdy_dtack* Drive	0	—	12	ns
t5	read_access_active Falling Edge to rdy_dtack* Falling Edge[1]	—	—	—	—
t6	read_access_active Rising Edge to rdy_dtack* Rising Edge	0	—	5	ns
t7	rdy_dtack* Rising Edge to rdy_dtack* 3-state	1	—	5	ns
t8	d[7:0] Valid to rdy_dtack* Falling Edge	pclkp – 4	—	—	ns
t9	read_access_active Rising Edge to d[7:0] Invalid	0	—	5	ns
t10	read_access_active Falling Edge to d[7:0] Drive	3 x pclkp – 4	—	—	ns
t11	read_access_active Rising Edge to read_access_active Falling Edge	25	—	—	ns

1. See access times in Table 11.

Note: The term pclkp in the table represents the period of pclk in ns.

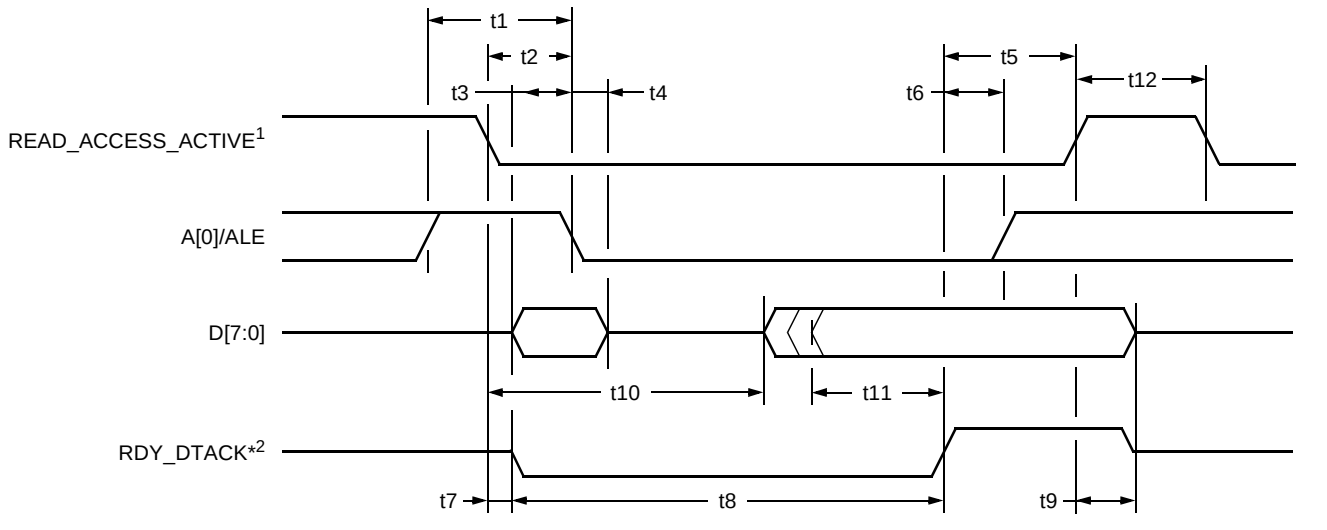
19 Timing Requirements (continued)



1. write_access_active is the logical OR function of sel* and wr*_ds*.
2. Load is 50 pF.

Note: sel* and wr*_ds* must not have coinciding edges in opposite directions to prevent glitches on the write_access_active signal.

Figure 24. Multiplexed *Intel* Mode Write Access Timing



1. read_access_active is the logical OR function of sel* and rd*_wr*.
2. Load is 50 pF.

Note: sel* and rd*_wr* must not have coinciding edges in opposite directions prevent glitches on the read_access_active signals.

Figure 25. Multiplexed *Intel* Mode Read Access Timing

19 Timing Requirements (continued)

Table 194. Multiplexed *Intel* Mode Write Access Timing

Symbol	Parameter	Min	Typ	Max	Unit
t1	a[0]/ale High Pulse Width	5	—	—	ns
t2	write_access_active Falling Edge to a[0]/ale Falling Edge	—	—	2 x pclkp – 4	ns
t3	d[7:0] Valid to a[0]/ale Falling Edge	5	—	—	ns
t4	a[0]/ale Falling Edge to d[7:0] Invalid	0	—	—	ns
t5	rdy_dtack* Rising Edge to write_access_active Rising Edge	0	—	—	ns
t6	rdy_dtack* Rising Edge to d[7:0] Invalid and a[0]/ale Rising Edge	0	—	—	ns
t7	write_access_active Falling Edge to rdy_dtack* Falling Edge	0	—	12	ns
t8	rdy_dtack* Low Pulse Width[1]	—	—	—	—
t9	write_access_active Rising Edge to rdy_dtack* 3-state	0	—	5	ns
t10	write_access_active Falling Edge to d[7:0] Valid	—	—	2 x pclkp – 4	ns
t11	write_access_active Rising Edge to write_access_active Falling Edge	25	—	—	ns

1. See access times in Table 11.

Note: The term pclkp in the table represents the period of pclk in ns.

Table 195. Multiplexed *Intel* Mode Read Access Timing

Symbol	Parameter	Min	Typ	Max	Unit
t1	a[0]/ale High Pulse Width	5	—	—	ns
t2	read_access_active Falling Edge to a[0]/ale Falling Edge	—	—	2 x pclkp – 4	ns
t3	d[7:0] Valid to a[0]/ale Falling Edge	5	—	—	ns
t4	a[0]/ale Falling Edge to d[7:0] Invalid	0	—	—	ns
t5	rdy_dtack* Rising Edge to read_access_active Rising Edge	0	—	—	ns
t6	rdy_dtack* Rising Edge to a[0]/ale Rising Edge	0	—	—	ns
t7	read_access_active Falling Edge to rdy_dtack* Falling Edge	0	—	12	ns
t8	rdy_dtack* Low Pulse Width[1]	—	—	—	—
t9	read_access_active Rising Edge to d[7:0] Invalid and rdy_dtack* 3-state	0	—	5	ns
t10	read_access_active Falling Edge to d[7:0] Drive	3 x pclkp – 4	—	—	ns
t11	d[7:0] Valid to rdy_dtack* Rising Edge	pclkp – 4	—	—	ns
t12	read_access_active Rising Edge to read_access_active Falling Edge	25	—	—	ns

1. See access times in Table 11.

Note: The term pclkp in the table represents the period of pclk in ns.

19 Timing Requirements (continued)

19.2 UTOPIA Timing

Table 196. TX UTOPIA Timing (70 pF Load on Outputs)

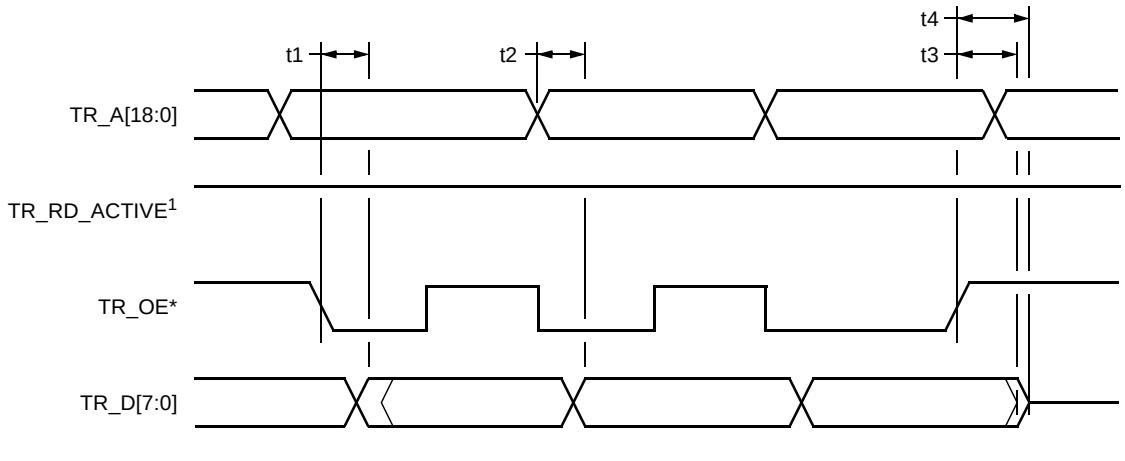
Parameter	Min	Typ	Max	Unit
u_txclk Frequency	0	—	50	MHz
u_txclk Duty Cycle	40	—	60	%
Output Delay from u_txclk, Applies to the Following Signals:				
u_txaddr[4:0]	1	—	10.6	ns
u_txdata[15:0], u_txsoc, u_txprty, u_txenb*[3:0]	1	—	10	ns
u_txclav[0],	1	—	7.66	ns
u_shr_grant[1:0], u_shr_req[3:0]	1	—	12.6	ns
Input Setup Time to u_txclk, Applies to the Following Signals: u_shr_req[3:0], u_shr_grant[1:0], u_txclav[3:0], u_txenb*[0], u_txaddr[4:0]	4	—	—	ns
Input Hold Time from u_txclk, Applies to the Following Signals: u_shr_req[3:0], u_shr_grant[1:0], u_txclav[3:0], u_txenb*[0], u_txaddr[4:0]	1	—	—	ns

Table 197. RX UTOPIA Timing (70 pF Load on Outputs)

Parameter	Min	Typ	Max	Unit
u_rxclk Frequency	0	—	50	MHz
u_rxclk Duty Cycle	40	—	60	%
Output Delay from u_rxclk, Applies to the Following Signals:				
u_rxaddr[4:0],	1	—	9.01	ns
u_rxenb*[3:0],	1	—	8.36	ns
u_rxclav[0]	1	—	7.19	ns
Input Setup Time to u_rxclk, Applies to the Following Signals: u_rxenb*[3:0], u_rxclav[3:0], u_rxdata[15:0], u_rxparity, u_rxsoc, u_rxaddr[4:0]	4	—	—	ns
Input Hold Time from u_rxclk, Applies to the Following Signals: u_rxenb*[3:0], u_rxclav[3:0], u_rxdata[15:0], u_rxprty, u_rxsoc, u_rxaddr[4:0]	1	—	—	ns

19 Timing Requirements (continued)

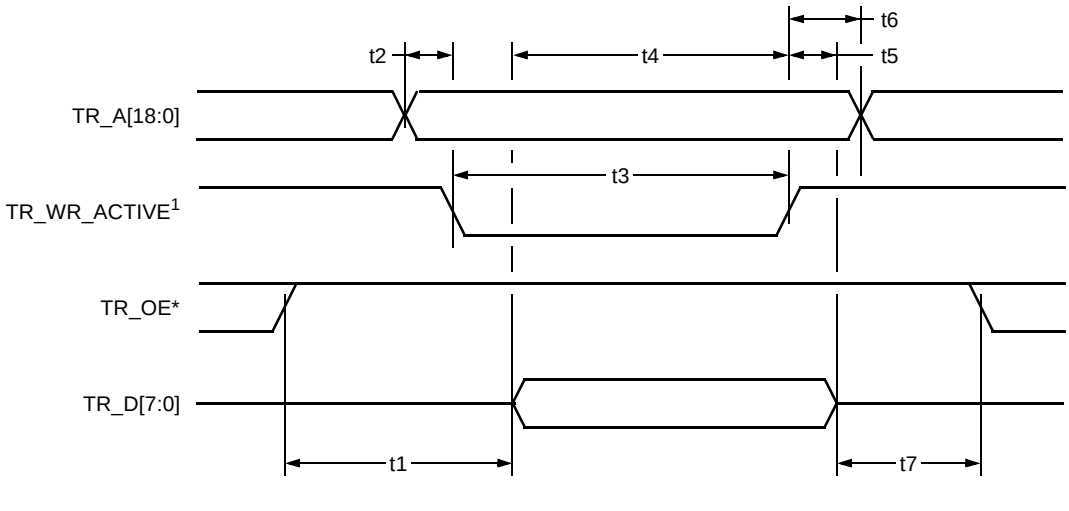
19.3 External LUT Memory Timing



Note: 30 pF load on outputs.

1. TR_RD_ACTIVE is the logical OR function of TR_CS*[1:0] and TR_WE*.
2. When a single SRAM of 512K bytes is used (bit 5 in register 100h must be set to '1'), TR_CS0 is used as TR_A[18].

Figure 26. External LUT Memory Read Timing (cyc_per_acc = 2 and cyc_per_acc = 3)



Note: 30 pF load on outputs.

1. TR_WR_ACTIVE is the logical OR function of TR_CS*[1:0] and TR_WE*.
2. When a single SRAM of 512K bytes is used (bit 5 in register 100h must be set to '1'), TR_CS0 is used as TR_A[18].

Figure 27. External LUT Memory Write Timing (cyc_per_acc = 2 and cyc_per_acc = 3)

19 Timing Requirements (continued)

The term mclkp in Tables 198, 199, 200, and 201, represents the period of mclk in ns.

Table 198. External LUT Memory Read Timing (cyc_per_acc = 2)

Symbol	Parameter	Min	Typ	Max	Unit
t1	tr_oe* Low to tr_d[7:0] Driven by SRAM Chip	0	—	2 x mclkp – 11	ns
t2	tr_a[17:0] & tr_cs*[1:0] Valid to tr_d[7:0] Valid	0	—	2 x mclkp – 11	ns
t3	tr_oe* High to tr_d[7:0] Invalid	0	—	—	ns
t4	tr_oe* High to tr_d[7:0] 3-State	—	—	mclkp	ns

Table 199. External LUT Memory Read Timing (cyc_per_acc = 3)

Symbol	Parameter	Min	Typ	Max	Unit
t1	tr_oe* Low to tr_d[7:0] Driven by SRAM Chip	0	—	3 x mclkp – 11	ns
t2	tr_a[17:0] & tr_cs*[1:0] Valid to tr_d[7:0] Valid	0	—	3 x mclkp – 11	ns
t3	tr_oe* High to tr_d[7:0] Invalid	0	—	—	ns
t4	tr_oe* High to tr_d[7:0] 3-State	—	—	mclkp	ns

Table 200. External LUT Memory Write Timing (cyc_per_acc = 2)

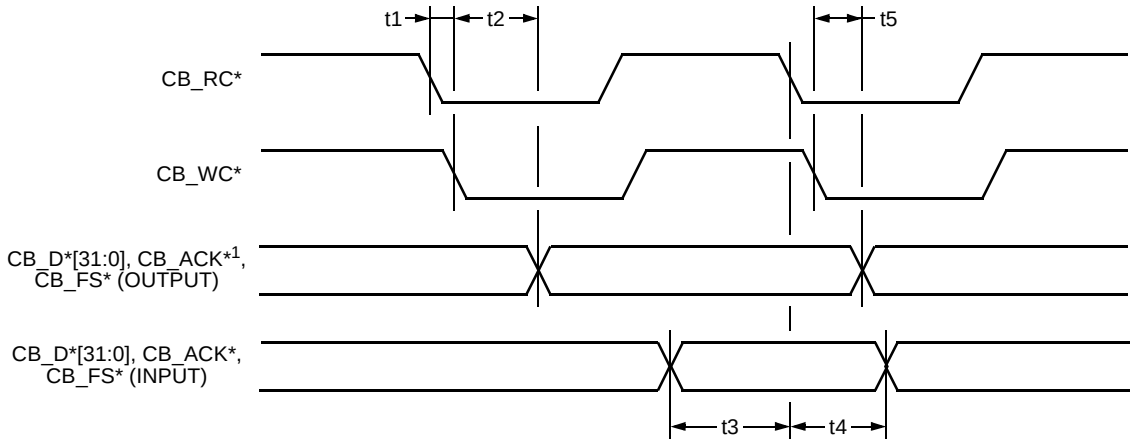
Symbol	Parameter	Min	Typ	Max	Unit
t1	tr_oe* High to tr_d[7:0] Driven	mclkp – 4	—	—	ns
t2	tr_a[17:0] Setup to tr_we* Falling Edge	2	—	—	ns
t3	tr_we* Low Pulse Width	mclkp – 1	—	—	ns
t4	tr_d[7:0] Setup to tr_we* Rising Edge	mclkp	—	—	ns
t5	tr_d[7:0] Hold from tr_we* Rising Edge	2	—	—	ns
t6	tr_a[17:0] Hold from tr_we* Rising Edge	2	—	—	ns
t7	tr_d[7:0] 3-State to tr_oe* Low	0	—	—	ns

Table 201. External LUT Memory Write Timing (cyc_per_acc = 3)

Symbol	Parameter	Min	Typ	Max	Unit
t1	tr_oe* High to tr_d[7:0] Driven	mclkp – 4	—	—	ns
t2	tr_a[17:0] Setup to tr_we* Falling Edge	2	—	—	ns
t3	tr_we* Low Pulse Width	2 x mclkp – 1	—	—	ns
t4	tr_d[7:0] Setup to tr_we* Rising Edge	2 x mclkp	—	—	ns
t5	tr_d[7:0] Hold from tr_we* Rising Edge	2	—	—	ns
t6	tr_a[17:0] Hold from tr_we* Rising Edge	2	—	—	ns
t7	tr_d[7:0] 3-State to tr_oe* Low	0	—	—	ns

19 Timing Requirements (continued)

19.4 Cell Bus Timing



1. 25 pF load.

Figure 28. Cell Bus Timing

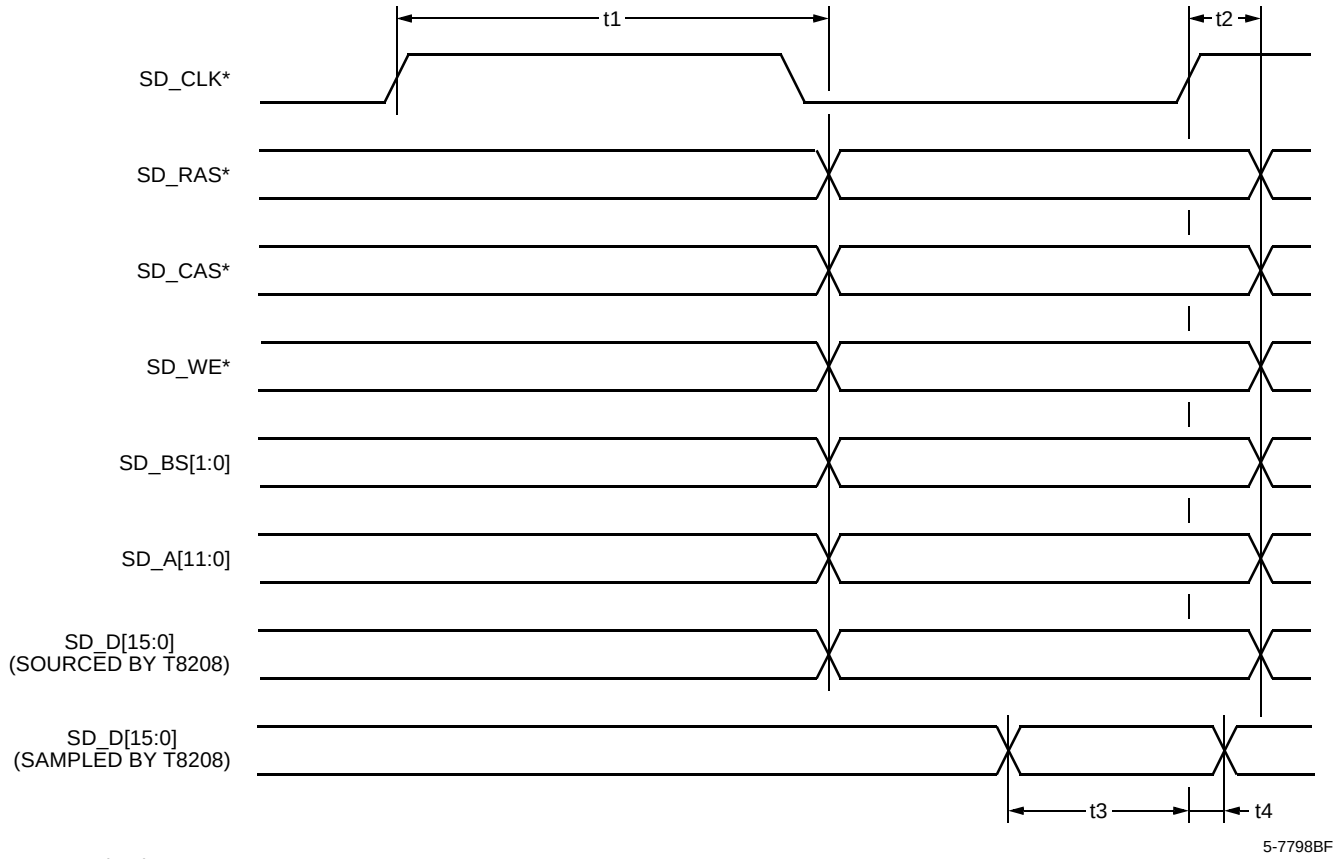
Table 202. Cell Bus Timing

Symbol	Parameter	Min	Typ	Max	Unit
t1	cb_rc* Falling Edge to cb_wc* Falling Edge	1.5	—	4.0	ns
t2	cb_wc* Falling Edge to Output Valid[1]	—	—	11.5	ns
t3	Input Setup to cb_rc* Falling Edge	1.0	—	—	ns
t4	Input Hold from cb_rc* Falling Edge	2.0	—	—	ns
t5	cb_wc* Falling Edge to Output Invalid[1]	3.0	—	—	ns

1. Pin loading = 25 pF.

19 Timing Requirements (continued)

19.5 SDRAM Interface Timing



Note: 15 pF load on outputs.

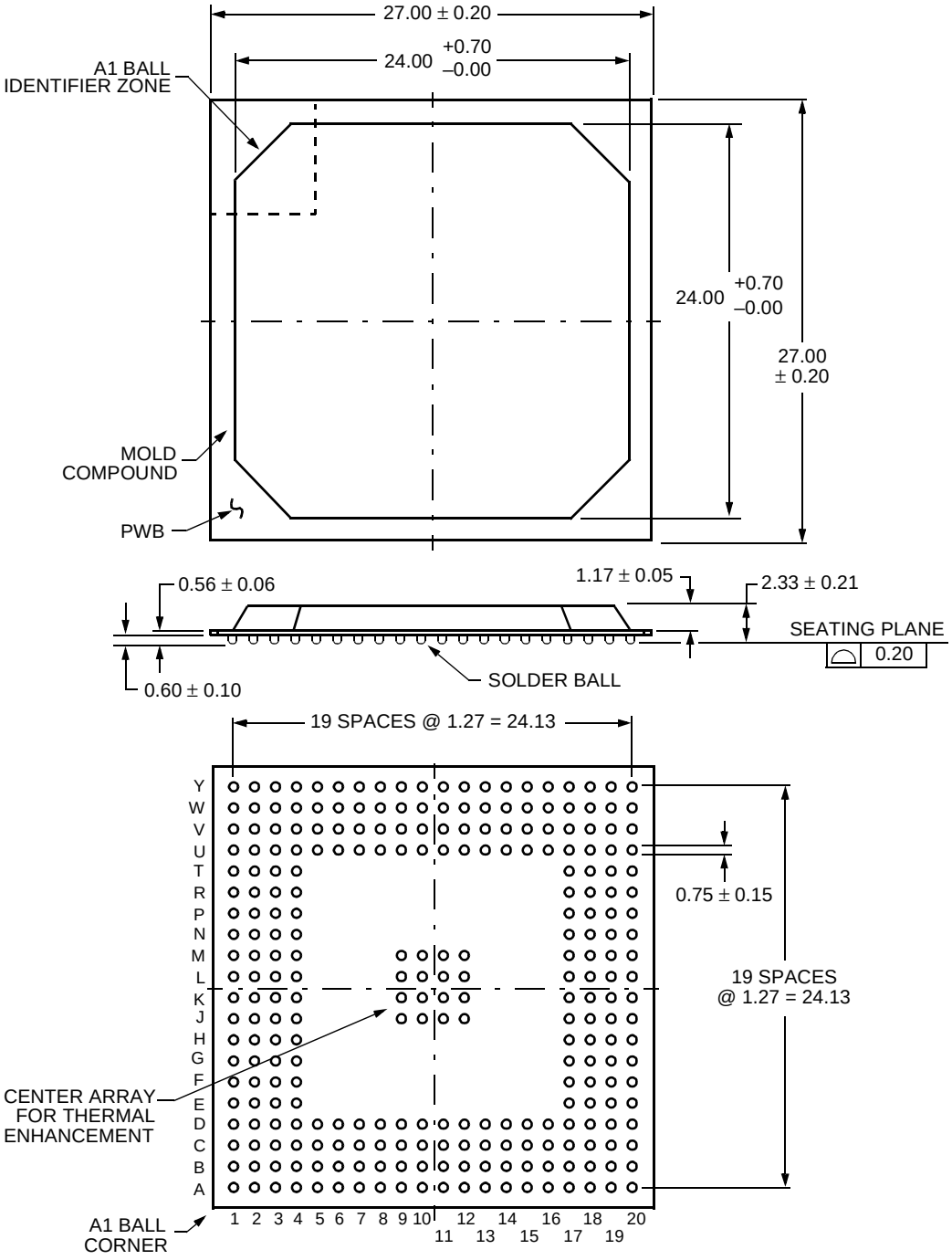
Figure 29. SDRAM Interface Timing

Table 203. SDRAM Interface Timing

Symbol	Parameter	Min	Typ	Max	Unit
t1	sd_clk Rising to Outputs Valid	—	—	7	ns
t2	sd_clk Rising to Outputs Invalid	1.5	—	—	ns
t3	sd_d[15:0] Input Setup to sd_clk Rising Edge	3	—	—	ns
t4	sd_d[15:0] Input Hold from sd_clk Rising Edge	0	—	—	ns

20 Outline Diagram

All dimensions shown are in millimeters.



5-4406.c

21 Ordering Information

Part Number	Package	Comcode
T-8208---BAL-DB	272-pin PBGAM, Dry Pack Tray	108888876
T-8208---BAL-DT	272-pin PBGAM Dry-bagged, Tape & Reel	700001513

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