T7234, T7237, and T7256
Compliance with the New ETSI PSD Requirement

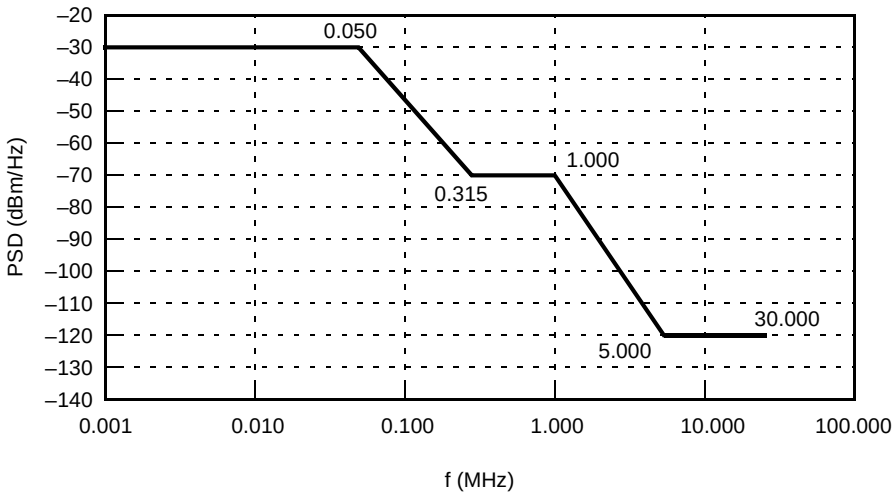
(Refer to the T7234, T7237, and T7256 ISDN transceiver data sheets.)

Telecommunication Standard

The European Telecommunications Standards Institute (ETSI) has identified a change in the requirement of the power spectral density (PSD) for Basic Rate Interface ISDN.

Section A.12.4, Power Spectral Density, of ETSI TS080 states the following:

- The upper boundary of the power spectral density of the transmitted signal shall be as shown in Figure 1, below.
- Measurements to verify compliance with this requirement are to use a noise power bandwidth of 1.0 kHz.
- Systems deployed before January 1, 2000 do not have to meet this PSD requirement but shall meet the PSD requirements as defined in ETR 080 edition 2. It is, however, expected that these systems will also meet the PSD requirements of TS080 edition 3. Some narrowband violations could occur and should be tolerated.



5-7388F

Figure 1. Upper Boundary of Power Spectral Density from NT1 and LT

The existing SCNT1 family (T7234A, T7237A, and T7256A) of U-interface transceivers fully comply with this standard.

Conformance to the above requirement has been fully verified, and test reports are available upon request.

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November 1998
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(Must accompany DS97-410ISDN, DS97-411ISDN, DS97-412ISDN, and AY98-025ISDN)

microelectronics group

Lucent Technologies
Bell Labs Innovations

Advisory
July 1998

microelectronics group

Lucent Technologies
Bell Labs Innovations

T7234, T7237, and T7256 Data Sheet Advisory

(Refer to the T7234, T7237, and T7256 ISDN transceiver data sheets.)

The Technology and Telecommunications Standard sections below denote the differences between the T7234, T7237, and T7256 and the T7234A, T7237A, and T7256A.

Technology

- The T-7234- - -ML, T-7237- - -ML, and T-7256- - -ML2 are 0.9 µm CMOS technology devices.
- The T-7234A- -ML, T-7237A- -ML, and T-7256A- -ML are 0.6 µm CMOS technology devices.

Telecommunication Standard

In 1996, the European Telecommunications Standards Institute (ETSI) added a microinterruption immunity requirement to ETR 080 (Sections 5.4.5 and 6.2.5).

Section 5.4.5 in ETSI ETR 080 states the following:

- A microinterruption is a temporary line interruption due to external mechanical activity on the copper wires constituting the transmission path.
- The effect of a microinterruption on the transmission system can be a failure of the digital transmission link.
- The objective of this requirement is that the presence of a microinterruption of specified maximum length shall not deactivate the system, and the system shall activate if it has deactivated due to longer interruption.

Section 6.2.5 in ETSI ETR 080 states that:

- A system shall tolerate a microinterruption up to t = 5 ms, when simulated with a repetition interval of t = 5 ms.

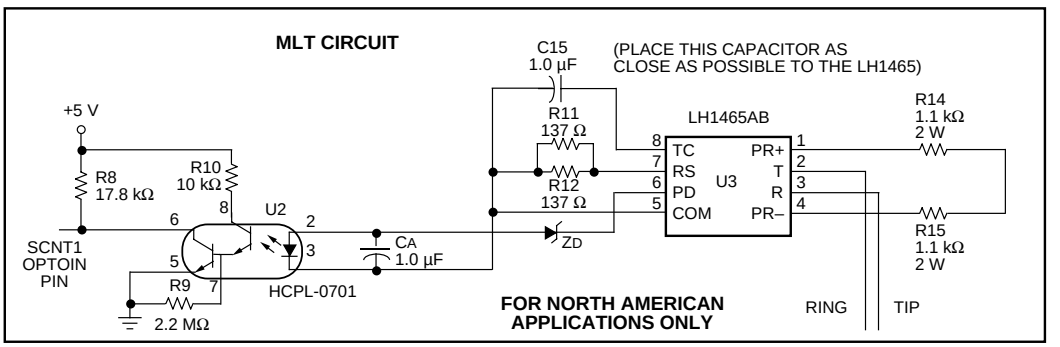
The SCNT1 family of U-interface transceivers was upgraded to fully comply with this standard. The devices have been given an A suffix (T7234A, T7237A, and T7256A).

A proposal was added to the Living List (which is intended to collect issues and observations for a possible future update of ETSI ETR 080) to change the value of the microinterruption from 5 ms to 10 ms. The current SCNT1 family of U-interface transceivers (T7234A/T7237A/T7256A) from Lucent Technologies Microelectronics Group meets and exceeds this new requirement.

The above change to the SCNT1 family of transceivers has been fully verified, and test reports are available upon request.

Application Circuit

Please change the value of capacitor C15 from 0.1 µF to 1.0 µF in Figure 11 of the T7234 data sheet, Figure 17 of the T7237 data sheet, and Figure 20 of the T7256 data sheet. The following schematic shows the correct value (1.0 µF) for C15.



5-7034(C)

Figure 1. MLT Circuit Showing New Placement of Zener Diode (Z_D) and Capacitor (C_A)

In the ILOSS mode (refer to ANSI T1.601 1992, Section 6.5.2), the NT generates a scrambled, framed, 2B1Q signal such as SN1 and SN2. When the ILOSS mode is applied to circuits with the LH1465, it was observed that for some short loop lengths, the NT, once in the ILOSS mode, would not respond to further maintenance pulses until the ILOSS timer expired. It was discovered that there is some portion of the transmitted 2B1Q signal from the NT that passes through the LH1465 to the optoisolator. This causes the optoisolator to report incorrect dial pulses at its output, and thus prevent the NT from properly exiting the ILOSS mode.

To correct this situation, the dropout voltage (voltage at the Tip/Ring needed to turn on the optoisolator) of the optoisolator driver on the LH1465 is raised using the 3.6 V zener diode Z_D (for example, *Motorola** MMSZ4685T1). Capacitor C_A is a 1.0 µF ±10% tantalum chip capacitor, with a voltage rating of at least 16 V. C_A is added to provide a level of filtering for the transition points (turn-on or turn-off) of the optoisolator input voltage, which increases the robustness of the circuit.

* *Motorola* is a registered trademark of Motorola Inc.

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Data Sheet
January 1998

microelectronics group

Lucent Technologies
Bell Labs Innovations

T7256 Single-Chip NT1 (SCNT1) Transceiver

Features

- U- to S/T-interface conversion for ISDN basic rate (2B+D) systems
  - — Integrated U- and S/T-interfaces
  - — Operates in stand-alone mode to provide U- and S/T-interface activation, control, and maintenance functions
  - — Serial microprocessor and time-division multiplexed (TDM) bus interfaces for enhanced NT1 operation and voice/data ports
  - — Automatic embedded operations channel (eoc) processing for ANSI T1.601 systems
  - — Low power consumption supporting line-powered NT1 (See table 45 on page 102, Question and Answers section, #53 for detailed power consumption information.)
  - — Idle-mode support (35 mW typical)
  - — Board-level testability support
- U-interface
  - — Conforms to ANSI T1.601 standard and ETSI ETR 080 technical report
  - — 2B1Q four-level line code
  - — Automatic ANSI maintenance functions (quiet mode and insertion loss mode)
- S/T-interface
  - — Conforms to ANSI T1.605 standard, ITU-T I.430 recommendation, and ETSI ETS 300 012 for NT operation
  - — Supports point-to-point and point-to-multipoint (passive bus) arrangements
  - — Supports S- and Q-channel multiframing operations (an external microprocessor is required for S- and Q-channel multiframing support)
- Serial microprocessor and TDM bus interfaces
  - — Supports inexpensive serial microprocessor
  - — Supports direct codec connection and voice/data ports
  - — Allows access to 2B+D data on TDM bus
- Other
  - — Single +5 V (±5%) supply
  - — –40 °C to +85 °C
  - — 44-pin PLCC

Description

The Lucent Technologies Microelectronics Group T7256 Single-Chip NT1 (SCNT1) Transceiver integrated circuit provides data (2B+D) and control information conversion between 2-wire (U-interface) and 4-wire (S/T-interface) digital subscriber loops on the integrated services digital network (ISDN). The T7256 conforms to the ANSI T1.601 standard and ETSI ETR 080 technical report for the U-interface and the ITU-T I.430 recommendation, ANSI T1.605 standard, and ETSI ETS 300 012 for the S/T-interface. The T7256 also supports digital pair gain and terminal adapter applications. The single +5 V CMOS device is packaged in a 44-pin plastic leaded chip carrier (PLCC).

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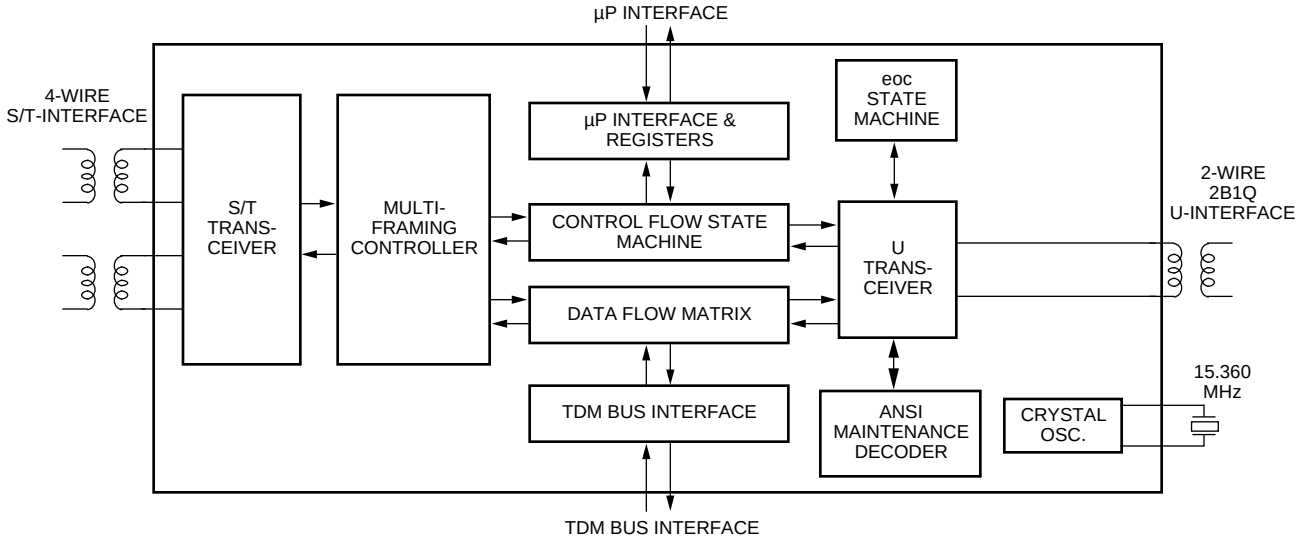
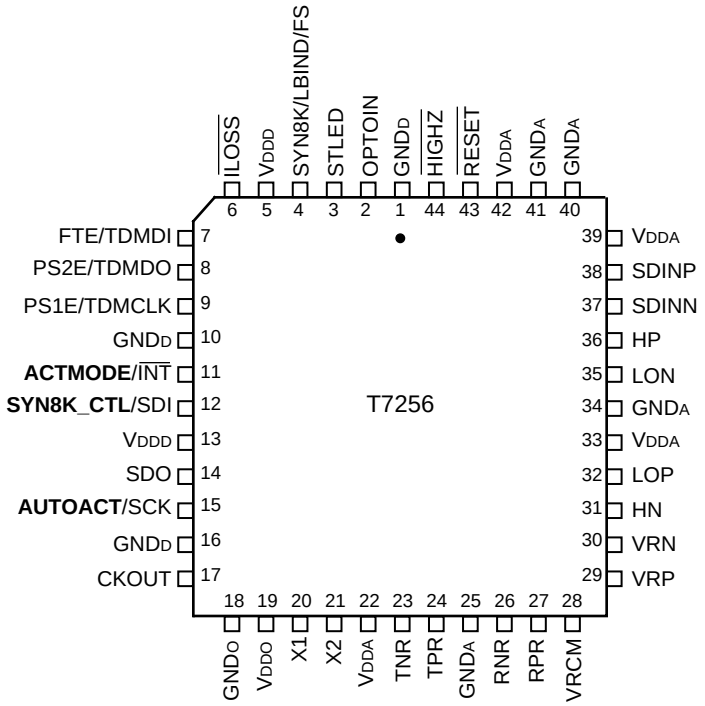
Description (continued)



5-2292 (C)

Figure 1. Block Diagram

Pin Information



Note: Pin labels shown in bold (pins 11, 12, and 15) represent chip configuration controls that are sampled on the rising edge of $\overline{\text{RESET}}$ (see Table 1, Pin Descriptions).

5-2296 (C)

Figure 2. Pin Diagram

Pin Information (continued)

Table 1. Pin Descriptions

Pin	Symbol	Type*	Name/Function
1, 10, 16	GND_D	—	**Digital Ground.** Ground leads for digital circuitry.
2	OPTOIN	I^u	**Optoisolator Input.** Pin accepts CMOS logic level maintenance pulse streams. These pulse streams typically are generated by an optoisolator that is monitoring the U loop. Pulse patterns on this pin are digitally filtered for 20 ms before being considered valid and are then decoded and interpreted using the ANSI maintenance state machine requirements. If AUTOCTL = 1 (register GR0, bit 3, default), the internal state machine decodes pulse trains and implements the required maintenance states automatically. If AUTOCTL = 0, the pulse trains are decoded internally, but the microprocessor must implement the maintenance state as indicated by the maintenance interrupts (register MIR0). If the OPTOIN pin is being used for implementing maintenance functions, the $\overline{\text{ILOSS}}$ pin should not be used (i.e., it should be held high). Instead, the $\overline{\text{ILOSS}}$ register bit should be used (register CFR0, bit 0). An internal 100 kΩ pull-up resistor is on this pin.
3	STLED	O	**Status LED Driver.** Output pin for driving an LED (source/sink 4.0 mA) that indicates the device status. The four defined states are low, high, 1 Hz flashing, and 8 Hz flashing (flashing occurs at 50% duty cycle). See the STLED Description section for a detailed explanation of these states. Also, this pin indicates device sanity upon power on/RESET, as follows: ■ If AUTOACT/SCK = 0 (pin 15) after a device RESET (which sets AUTOACT = 0 in register GR0 bit 6, turning on autoactivation), STLED will toggle at an 8 Hz rate for at least 0.5 s, signifying an activation attempt. If the activation attempt succeeds, it will continue to flash per the normal start-up sequence (see STLED Description section). ■ If AUTOACT/SCK = 1 (pin 15) after a device RESET, STLED will go low for 1 s (flash of life), indicating that the device is operational, and no activation attempt will be made.
4	SYN8K/LBIND/FS	O	**Synchronous 8 kHz Clock or Loopback Indicator.** If TDMEN = 1 (register GR2, bit 5, default), the pin function is determined based on the state of pin 12 (SYN8K_CTL/SDI) at the most recent rising edge of $\overline{\text{RESET}}$. As SYN8K (SYN8K_CTL/SDI = 0 at $\overline{\text{RESET}}$ rising edge), this pin is an 8 kHz 50% duty cycle clock that is synchronous with the recovered timing from the U-interface. When U-interface synchronization is not present, SYN8K is free-running. As LBIND (SYN8K_CTL/SDI = 1 at $\overline{\text{RESET}}$ rising edge), this pin indicates a 2B+D loopback: 0—No loopback. 1—eoc requested 2B+D loopback in progress. **Frame Strobe.** If TDMEN = 0, this pin is a programmable strobe output used to indicate appearance of B- and/or D-channel data on the TDM bus. Polarity, offset, and duration of FS are programmable through the microprocessor interface (see register TDR0). FS will be disabled until at least one of bits 2—7 in register DFR1 is enabled.

* I^u = input with internal pull-up.

Pin Information (continued)

Table 1. Pin Descriptions (continued)

Pin	Symbol	Type*	Name/Function
5, 13	V_{DDD}	—	**Digital Power.** 5 V ± 5% power supply pins for digital circuitry.
6	$\overline{\text{ILOSS}}$	I^u	**Insertion Loss Test Control (Active-Low)**. The $\overline{\text{ILOSS}}$ pin is used to control SN1 tone transmission for maintenance. The OPTOIN and $\overline{\text{ILOSS}}$ pins should not be used at the same time (i.e., OPTOIN should be held high when $\overline{\text{ILOSS}}$ is active). This pin would typically be used if an external ANSI maintenance decoder is being used, in which case the decoder output drives the $\overline{\text{ILOSS}}$ pin. The $\overline{\text{ILOSS}}$ pin is ignored, and the functionality is controlled by the ILOSS bit (register CFR0, bit 0) if AUTOCTL = 0 (register GR0, bit 3). Internal 100 kΩ pull-up resistor on this pin. 0—U transmitter sends SN1 tone continuously. 1—No effect on device operation.
7	FTE/ TDMDI	I^u	**Fixed/Adaptive Timing Mode Select.** If TDMEN = 1 (register GR2, bit 5, default), selects S/T-interface timing recovery mode: 0—Fixed timing recovery mode. 1—Adaptive timing recovery mode. **TDM Data In.** If TDMEN = 0, this pin is the TDM bus 2B+D data input synchronous with TDMCLK, and the S/T-interface timing mode is controlled via the FT bit (register GR2, bit 0). An internal 100 kΩ pull-up resistor is on this pin.
8	PS2E/ TDMDO	I^d/O	**Power Status #2.** If TDMEN = 1 (register GR2, bit 5, default), this is an input for the PS2 bit in transmit U-interface data stream. See PS2 bit description (register GR1, bit 1) for PS1 and PS2 message definition. An internal 100 kΩ pull-down resistor is on this pin. **TDM Data Out.** If TDMEN = 0, this pin is the 2.048 MHz TDM bus 2B+D data output synchronous with TDMCLK, and PS2 is controlled via the PS2 (register GR1, bit 1) microprocessor register bit.
9	PS1E/ TDMCLK	I^d/O	**Power Status #1.** If TDMEN = 1 (register GR2, bit 5, default), this is an input for the PS1 bit in transmit U-interface data stream. See PS2 bit description (register GR1, bit 1) for PS1 and PS2 message definition. If PS1E is not driven by an external control circuit, it must be pulled up externally with a 10 kΩ or less resistor to indicate the presence of primary power. An internal 100 kΩ pull-down resistor is on this pin. **TDM Clock.** If TDMEN = 0, this pin is the 2.048 MHz TDM clock output synchronous with U-interface (if active) or is free-running, and PS1 is controlled via the PS1 microprocessor register bit. TDMCLK will be disabled until at least one of bits 2—7 in register DFR1 is enabled.

* I^u = input with internal pull-up; I^d = input with internal pull-down.

Pin Information (continued)

Table 1. Pin Descriptions (continued)

Pin	Symbol	Type*	Name/Function
11	ACTMODE/ $\overline{\text{INT}}$	I^u/O	**ACT Bit Mode.** Upon exiting $\overline{\text{RESET}}$, the state of ACTMODE/$\overline{\text{INT}}$ is read and if ACTMODE/$\overline{\text{INT}}$ = 1 (default), bit ACTSEL = 1 (register GR2, bit 6). If ACTMODE/ $\overline{\text{INT}}$= 0 (externally pulled down), then ACTSEL = 0. An internal 100 kΩ pull-up resistor is on this pin. **Serial Interface Microprocessor Interrupt (Active-Low).** Interrupt output for microprocessor. Any active, unmasked bit in interrupt registers UIR0, SIR0, or MIR0 will cause $\overline{\text{INT}}$ to go low. The bits in the interrupt registers UIR0, SIR0, and MIR0 will be set on a true condition, independent of the state of the corresponding mask bits. If a masked, active interrupt bit is subsequently unmasked, the $\overline{\text{INT}}$ pin will go low to indicate an interrupt for that condition. Reading UIR0, SIR0, or MIR0 clears the entire register and forces $\overline{\text{INT}}$ high for 50 µs. After this interval, $\overline{\text{INT}}$ will again reflect the state of any unmasked bit in these registers. The global interrupt register (GIRO) provides a summary status of the UIR0, SIR0, and MIR0 interrupt registers and indicates if one of the registers currently has an active, unmasked interrupt bit.
12	SYN8K_CTL /SDI	I^d	**SYN8K/LBIND Control.** If this pin is low at the rising edge of $\overline{\text{RESET}}$, the SYN8K/ LBIND/FS pin performs the SYN8K function. Otherwise, the pin performs the LBIND function. An internal 100 kΩ pull-down resistor is on this pin. **Serial Interface Data Input.** Data input for microprocessor interface.
14	SDO	O	**Serial Interface Data Output.** Data output for microprocessor interface. This pin is 3-stated at all times except for when a microprocessor read from the T7256 is taking place.
15	AUTOACT/ SCK	I^d	**Automatic Activation.** If this pin is low at the rising edge of $\overline{\text{RESET}}$, the AUTOACT bit is written to 0, creating an activation attempt (see AUTOACT [register GR0, bit 6] description in Table 4). If pin is held high during external $\overline{\text{RESET}}$, no activation is attempted. An internal 100 kΩ pull-down resistor is on this pin. **Serial Interface Clock.** Clock input for microprocessor interface.
17	CKOUT	O	**Clock Output.** Clock output function to drive other board components. Powerup default state is high-impedance to minimize power consumption. Programmable via microprocessor register (register GR0, bits 1 and 2) to provide 15.36 MHz output or 10.24 MHz output. If U-interface is active, the 10.24 MHz output is synchronous with U-interface timing.
18	GND_O	—	**Crystal Oscillator Ground.** Ground lead for crystal oscillator.
19	V_{DDO}	—	**Crystal Oscillator Power.** Power supply lead for crystal oscillator.
20	X1	O	**Crystal #1.** Crystal connection #1 for 15.36 MHz oscillator.
21	X2	I	**Crystal #2.** Crystal connection #2 for 15.36 MHz oscillator.
22, 33, 39, 42	V_{DDA}	—	**Analog Power.** 5 V ± 5% power supply leads for analog circuitry.
23	TNR	O	**Transmit Negative Rail for S/T-Interface.** Negative output of S/T-interface analog transmitter. Connect to transformer through a 121 Ω ± 1% resistor.
24	TPR	O	**Transmit Positive Rail for S/T-Interface.** Positive output of S/T-interface analog transmitter. Connect to transformer through a 121 Ω ± 1% resistor.

* I^u = input with internal pull-up; I^d = input with internal pull-down.

Pin Information (continued)

Table 1. Pin Description (continued)

Pin	Symbol	Type*	Name/Function
25, 34, 40, 41	GND_A	—	**Analog Ground.** Ground leads for analog circuitry.
26	RNR	I	**Receive Negative Rail for S/T-Interface.** Negative input of S/T-interface analog receiver. Connect to transformer through a 10 kΩ ± 10% resistor.
27	RPR	I	**Receive Positive Rail for S/T-Interface.** Positive input of S/T-interface analog receiver. Connect to transformer through a 10 kΩ ± 10% resistor.
28	VRCM	—	**Common-Mode Voltage Reference for U-Interface Circuits.** Connect a 0.1 µF ± 20% capacitor to GND_A (as close to the device pins as possible).
29	VRP	—	**Positive Voltage Reference for U-Interface Circuits.** Connect a 0.1 µF ± 20% capacitor to GND_A (as close to the device pins as possible).
30	VRN	—	**Negative Voltage Reference for U-Interface Circuits.** Connect a 0.1 µF ± 20% capacitor to GND_A (as close to the device pins as possible).
31	HN	I	**Hybrid Negative Input for U-Interface.** Connect directly to negative side of U-interface transformer.
32	LOP	O	**Line Driver Positive Output for U-Interface.** Connect to the U-interface transformer through a 16.9 Ω ± 1% resistor.
35	LON	O	**Line Driver Negative Output for U-Interface.** Connect to the U-interface transformer through a 16.9 Ω ± 1% resistor.
36	HP	I	**Hybrid Positive Input for U-Interface.** Connect directly to positive side of U-interface transformer.
37	SDINN	I	**Sigma-Delta A/D Negative Input for U-Interface.** Connect via an 820 pF ± 5% capacitor to SDINP.
38	SDINP	I	**Sigma-Delta A/D Positive Input for U-Interface.** Connect via an 820 pF ± 5% capacitor to SDINN.
43	$\overline{\text{RESET}}$	I^d	**Reset (Active-Low).** Asynchronous Schmitt trigger input. Reset halts data transmission, clears adaptive filter coefficients, resets the U-transceiver timing recovery circuitry, resets the S/T-interface transceiver, and sets all microprocessor register bits to their default state. During reset, the U-interface transmitter produces 0 V and the output impedance is 135 Ω at tip and ring. The $\overline{\text{RESET}}$ pin can be used to implement quiet mode maintenance testing (refer to pin 2 for more description). The states of pins 11, 12, and 15 (ACTMODE/$\overline{\text{INT}}$, SYN8K_CTL/SDI, and AUTOACT/SCK, respectively) are latched on the rising edge of $\overline{\text{RESET}}$. (See corresponding pin descriptions.) An internal 100 kΩ pull-down resistor is on this pin. $\overline{\text{RESET}}$ must be held low for 1.5 ms after power on. Device is fully functional after an additional 1 ms.
44	$\overline{\text{HIGHZ}}$	I^u	**High-Impedance Control (Active-Low).** Control of the high-impedance function. An internal 100 kΩ pull-up resistor is on this pin. **Note:** This pin does not 3-state the analog outputs. 0—All digital outputs enter high-impedance state. 1—No effect on device operation.

* I^u = input with internal pull-up; I^d = input with internal pull-down.

Application Overview

The T7256 is intended for use in ISDN networks as part of a 2-wire to 4-wire converter (NT1) or as part of a terminal adapter (TA), providing 2-wire termination of the network with available voice and/or data ports. Local switching of terminal voice/data is also supported by the T7256. Figure 3 shows the NT1 and TA applications. See Using the T7256 in a Combination TE/TA Environment in the Application Briefs section for a detailed explanation of an application that has both TE and TA functions.

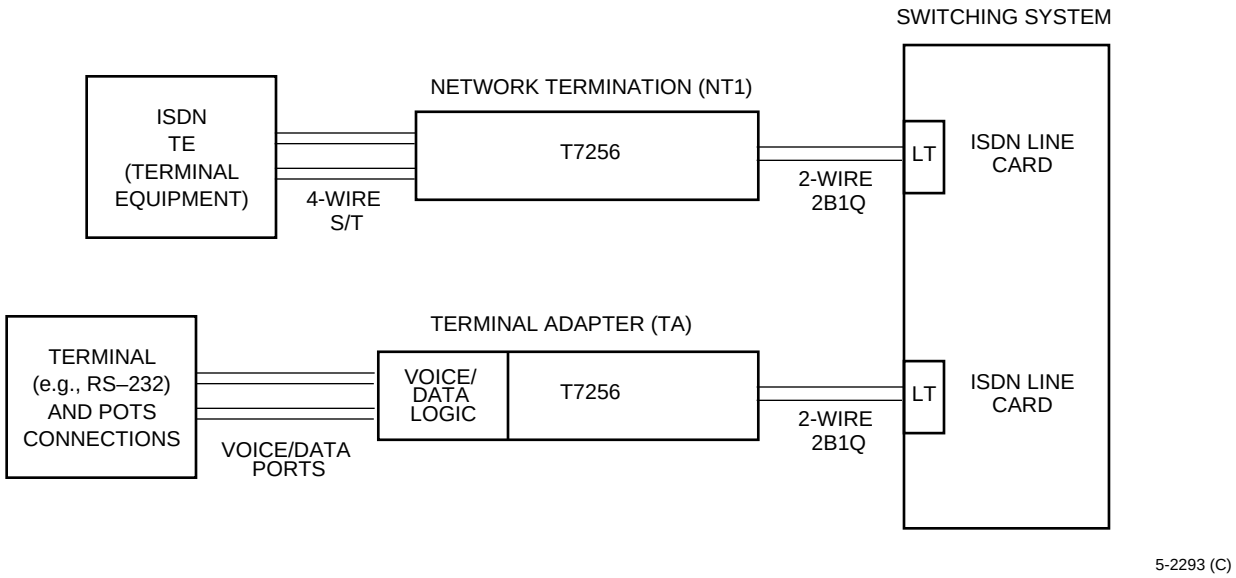


Figure 3. Applications of T7256

Functional Overview

The T7256 device provides four major interfaces for information transfer: the U-interface, the S/T-interface, the microprocessor interface, and the time-division multiplexed (TDM) bus interface (see Figure 1). Use of the microprocessor and TDM bus interface is optional.

If the microprocessor and TDM interfaces aren't required, the T7234 SCNT1 Euro-LITE may be a more cost-effective solution (see the T7234 SCNT1 Euro-LITE Single-Chip NT1 Data Sheet). Similarly, if an S/T-interface is not required, the T7237 may be a more cost-effective solution (see the T7237 ISDN U-Interface Transceiver Data Sheet). These devices are pin-compatible with the T7256, but have a reduced feature set for cost-sensitive applications that don't require the full feature set of the T7256.

Routing of data between the S/T, U, and TDM interfaces is controlled by the data flow matrix that uses register settings accessible via the microprocessor port. The data flow matrix circuitry routes 2B+D information between the appropriate interfaces, under direction of the microprocessor register settings. Routing between the T7256 interfaces allows configurations to support both NT1 and TA applications.

The architecture of the T7256 allows for a flexible combination of automatically and manually controlled functions. A control flow state machine, eoc state machine, and multiframing controller can be independently enabled or disabled. When enabled, these circuit blocks automatically perform their functions while ignoring the associated control bits in the microprocessor registers. When disabled, the control bits are made available to the microprocessor for manipulation. At all times, the status bits are available to the microprocessor and the 2B+D data can be routed via the data flow matrix.

The microprocessor interface is a serial communications port consisting of input data (SDI), output data (SDO), input clock (SCK), and an output interrupt pin ($\overline{\text{INT}}$). The microprocessor interface supports synchronous communication between the T7256 and an inexpensive microprocessor with a serial port. The interrupt is maskable via the onboard microprocessor interrupt mask registers. The internal register set controls various functions including information routing between interfaces, auto-eoc processing, maintenance testing, S/T-interface timing recovery mode, S- and Q-channel processing, microprocessor interrupt masks, activation of the TDM bus, and frame strobe timing.

The TDM interface consists of a TDM bus data clock (TDMCLK), input data (TDMDI), output data (TDMDO), and frame strobe (FS). The 2B+D data is transmitted and received in fixed time slots on the TDM bus; however, the frame strobe output lead is programmable to support a wide variety of devices (codecs, HDLC processors, asynchronous interfaces) for direct connection on the TDM bus. The TDM bus exists as a selectable option via the microprocessor interface. When the TDM bus is activated, pins 4, 7, 8, and 9 are reconfigured to form the bus interface.

The eoc state machine, when enabled, automatically performs the eoc channel functions as described in the ANSI requirements. When disabled, control of the eoc channel is passed to the microprocessor via the appropriate microprocessor register bits.

The ANSI maintenance controller can operate in fully automatic or in fully manual mode. In automatic mode, the device decodes and responds to maintenance states according to the ANSI requirements. In manual mode, the device is controlled by an external maintenance decoder that drives the $\overline{\text{RESET}}$ and $\overline{\text{ILOSS}}$ pins to implement the required maintenance states.

The multiframing controller, when enabled, allows the S and Q channels on the S/T-interface to be manipulated by the microprocessor. When disabled, the S- and Q-channel bits are automatically loaded with their default values for applications not supporting multiframing.

The control flow state machine performs the functions of reserved bit insertion, automatic implementation of the ANSI maintenance state machine, and automatic prioritization of multiple requests, such as reset, activation, maintenance, etc. Some bits that are normally controlled by the control flow state machine can be forced to their active state by writing the appropriate register (i.e., register GR1). When the control flow state machine is disabled (via the AUTOCTL bit in register GR0), the only change in the operation is that reserved bit control and ANSI maintenance control are passed directly to the microprocessor via register CFR0.

Functional Overview (continued)

When the T7256 is powered on and there is no activity on the S/T- or U-interfaces (i.e., no pending activation request), it automatically enters a low-power IDLE mode in which it consumes an average of 35 mW.

This mode is exited automatically when an activation or U maintenance request occurs from either the microprocessor or the S/T- or U-interfaces. The T7256 provides a board-level test capability that allows functional verification. Finally, an LED driver output indicates the status of the device during operation.

U-Interface Frame Structure

Data is transmitted over the U-interface in 240-bit groups called U frames. Each U frame consists of an 18-bit synchronization word or inverted synchronization word (SW or ISW), 12 blocks of 2B+D data (216 bits), and six overhead bits (M bits). A U-interface superframe consists of eight U frames grouped together. The beginning of a U superframe is indicated by the inverted sync word (ISW). The six overhead bits (M1—M6) from each of the eight U frames, when taken together, form the 48 M bits. Figure 4 shows how U frames, superframes, and M bits are arranged.

Of the 48 M bits, 24 bits form the embedded operations channel (eoc) for sending messages from the LT to the NT and responses from the NT to the LT. There are two eoc messages per superframe with 12 bits per eoc message (eoc1 and eoc2). Another 12 bits serve as U-interface control and status bits (UCS). The last 12 bits form the cyclic redundancy check (CRC) which is calculated over the 2B+D data and the M4 bits of the previous superframe. Figure 5 and Table 2 show the different groups of bits in the superframe.

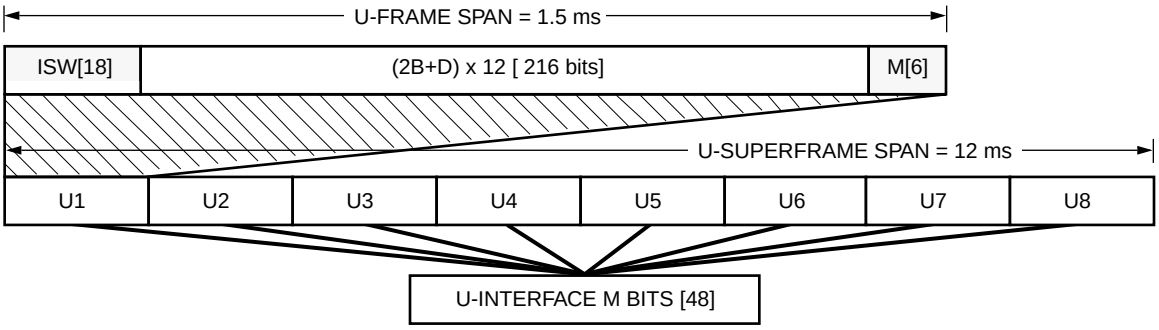


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Figure 4. U-Interface Frame and Superframe

U-Interface Frame Structure (continued)

<table>
<tr><th>Bit #</th><th>1—18</th><th>19—234</th><th>235</th><th>236</th><th>237</th><th>238</th><th>239</th><th>240</th></tr>
<tr><th>Frame #</th><th>Sync</th><th>12(2B+D)</th><th>M1</th><th>M2</th><th>M3</th><th>M4</th><th>M5</th><th>M6</th></tr>
<tr><td>1</td><td>ISW</td><td rowspan="8">2B+D</td><td colspan="3" rowspan="4">eoc1</td><td colspan="3" rowspan="2">CONTROL & STATUS (UCS)</td></tr>
<tr><td>2</td><td rowspan="7">SW</td></tr>
<tr><td>3</td><td rowspan="5">crc</td></tr>
<tr><td>4</td></tr>
<tr><td>5</td><td colspan="3" rowspan="4">eoc2</td><td rowspan="4"></td></tr>
<tr><td>6</td></tr>
<tr><td>7</td></tr>
<tr><td>8</td></tr>
</table>

Figure 5. U-Interface Superframe Bit Groups

Bit Assignments

Table 2. U-Interface Bit Assignment

Bit #	1—18	19—234	235	236	237	238	239	240
Frame #	Sync	12(2B+D)	M1	M2	M3	M4	M5	M6
1	ISW	2B+D	eoc_{a1}	eoc_{a2}	eoc_{a3}	act	$R_{1,5}$	$R_{1,6}$
2	SW	2B+D	eoc_{dm}	eoc_{i1}	eoc_{i2}	dea (ps1)*	$R_{2,5}$	febe
3	SW	2B+D	eoc_{i3}	eoc_{i4}	eoc_{i5}	$R_{3,4}$ (ps2)*	crc_1	crc_2
4	SW	2B+D	eoc_{i6}	eoc_{i7}	eoc_{i8}	$R_{4,4}$ (ntm)*	crc_3	crc_4
5	SW	2B+D	eoc_{a1}	eoc_{a2}	eoc_{a3}	$R_{5,4}$ (cso)*†	crc_5	crc_6
6	SW	2B+D	eoc_{dm}	eoc_{i1}	eoc_{i2}	$R_{6,4}$	crc_7	crc_8
7	SW	2B+D	eoc_{i3}	eoc_{i4}	eoc_{i5}	uoa (sai)*	crc_9	crc_{10}
8	SW	2B+D	eoc_{i6}	eoc_{i7}	eoc_{i8}	aib (nib)*‡	crc_{11}	crc_{12}

* LT(NT). Values in parentheses () indicate meaning at the NT.
† cso is fixed at 0 by the device to indicate both cold and warm start capability.
‡ nib is fixed at 1 by the device to indicate the link is normal.

S/T-Interface Frame Structure

The S/T-interface transfers its subscriber line 2B+D information as a 192 kbits/s full-duplex signal grouped into frames of 48 bits with a period of 250 µs, as specified in the ITU-T I.430/ANSI T1.605 standard. Thirty-six of the 48 bits sent in each direction convey user information (two 8-bit occurrences of each of the two B channels, and four D-channel bits). The remaining 12 bits per frame are used for framing, control, dc balance, and maintenance. The frame structures are shown in each direction in Figure 6.

In the bit stream transmitted from the terminal endpoint (TE) to the network termination (NT), 4 bits are used for framing (F and FA, each with a dc balancing bit L), eight additional L bits are used to balance the 32 B-channel bits, and 4 bits are D-channel bits.

For the NT-to-TE transmission, 4 bits (F with dc balancing bit L, FA, and N) are used for framing, one M bit marks the start of a 20-frame multiframe, four E bits form an echo channel for retransmission of the D-channel bits received from the TE, one additional L bit is used to balance the contents of the entire frame, and 1 bit (A) is set to one when bit synchronization is achieved between TE and NT as part of the INFO 4 state. One S bit is used for transmitting S subchannel messages in an NT-to-TE multiframe.

The framing procedure uses bipolar line-code violations to establish synchronization. Since the last binary 0 of any frame is a positive pulse and the F bit is also defined to be a positive pulse (see Figure 7), the first bit of each frame represents a coding violation. In addition, the second bit of each frame, a balance bit, is a negative pulse, and the next binary 0 in the frame is forced to be negative, causing another violation. Both bipolar violations allow framing and provide dc balance. All other pulses follow the alternating convention.

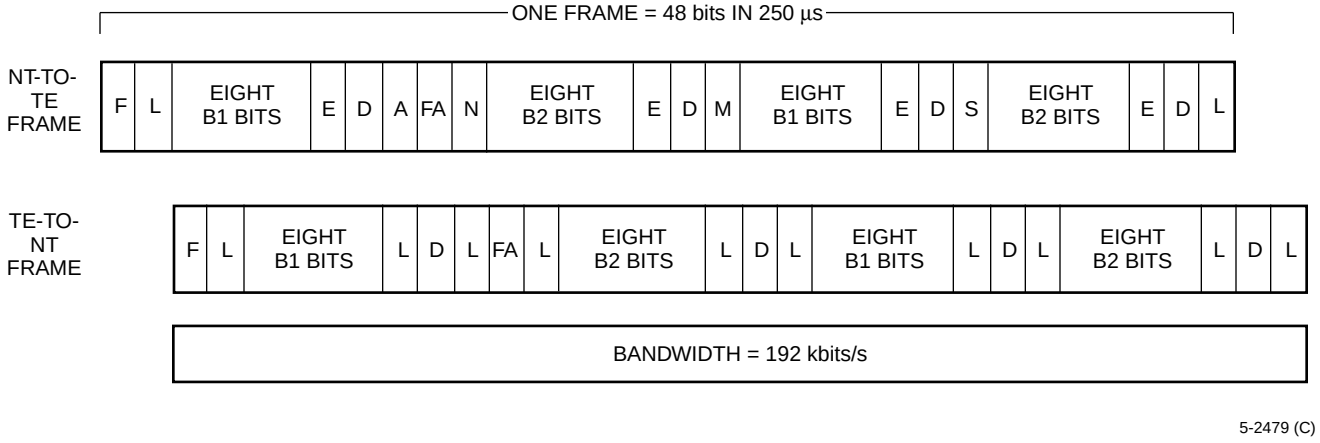
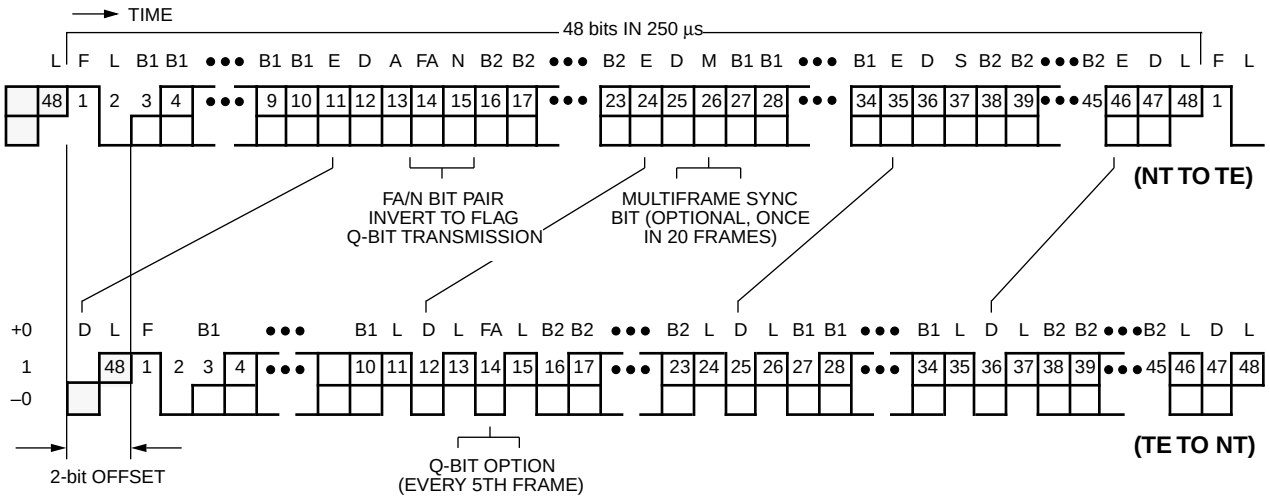


Figure 6. Frame Structures of NT and TE Frames

S/T-Interface Frame Structure (continued)

In the TE-to-NT direction, in at least four of five frames, this second violation occurs within 13 bits of the F bit. If this coding algorithm is not maintained, the receiver loses synchronization, but the T7256 continues transmitting.



F = Framing bit
L = dc balancing bit
D = D-channel bit
E = Echo D-channel bit
FA = Auxiliary framing bit or Q-channel bit
N = Bit set to binary value N = $\overline{FA}$
A = Activation bit
S = S-channel bit
M = Multiframe synchronization bit
B1 = Bit within B channel 1
B2 = Bit within B channel 2

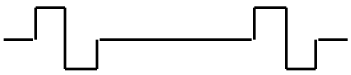
Signals from NT to TE		Signals from TE to NT	
INFO 0	No signal.	INFO 0	No signal.
INFO 2	Frame with all bits of B, D, and D echo (E) channels set to binary ZERO; bit A set to binary ZERO; N and L bits set according to the normal coding rules.	INFO 1	A continuous signal with the following pattern: positive ZERO, negative ZERO, six ONEs. 
INFO 4	Frames with operational data on B, D, and E channels; bit A set to binary ONE.	INFO 3	Synchronized frames with operational data on B and D channels.

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Figure 7. Details of NT and TE Frames

S/T-Interface Frame Structure (continued)

The T7256 supports multiframing on the S/T-interface in conjunction with an external microprocessor that is used to enable multiframing and transmit and receive S- and Q-channel messages. When multiframing is enabled, the M bit in the NT-to-TE direction is set to a one every 20 frames and the FA bit is set to one every five frames. The TE recognizes these states and, in returned frames immediately corresponding to those in which the NT set the FA bit, replaces the FA bit it sends to the NT with a Q bit (Q1 through Q4). Q1 is returned for each frame in which both the M and FA bits were set to one by the NT, with Q2 through Q4 following at five-frame intervals. (See Figure 8.)

The S-bit position in the NT-to-TE direction is divided into five 4-bit subchannels during multiframing: SC1—SC5. Message sets for subchannels SC3—SC5 are not currently defined, and a message set for SC2 is defined only in ANSI T1.605, but not ITU I.430 (see the S/T-Interface Multiframing Controller Description section for more details). Figure 8 indicates the location of the various S-subchannel bits during multiframing.

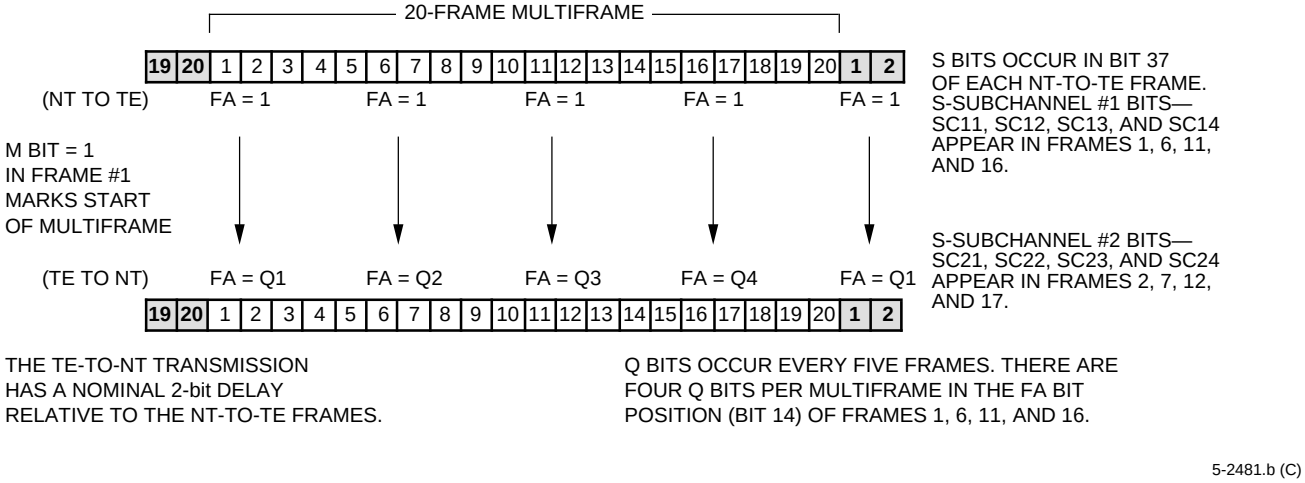

Figure 8. Multiframing—S Subchannels and Q Subchannels

U-Interface Description

At the U-interface, the T7256 conforms to ANSI T1.601 and ETSI ETR 080 when used with the proper line interface circuitry. The T7256 Reference Circuit description in the Application Briefs section of this document describes a detailed example of a U-interface circuit design.

The 2B1Q line code provides a four-level (quaternary) pulse amplitude modulation code with no redundancy. Data is grouped into pairs of bits for conversion to quaternary (quat) symbols. Figure 9 shows an example of this coding method.

The U-interface transceiver section provides the 2B1Q line coder (D/A conversion), pulse shaper, line driver, first-order line balance network, clock regeneration, and sigma-delta A/D conversion. The line driver, when connected to the proper transformer and interface circuitry, generates pulses which meet the required 2B1Q templates. The A/D converter is implemented by using a double-loop, sigma-delta modulator.

The U transceiver block also takes input from the data flow matrix and formats this information for the U-interface (see Figure 1). During this formatting, synchronization bits for U framing are added and a scrambling algorithm is applied. This data is then transferred to the 2B1Q encoder for transmission over the U-interface. Signals received from the U-interface are first passed through the sigma-delta A/D converter, and then sent to the digital signal processor for more extensive signal processing. The block provides decimation of the sigma-delta output, linear and nonlinear echo cancellation, automatic gain control, signal detection, phase shift interpolation, decision feedback equalization, timing recovery, descrambling, and line-code polarity detection. The decision feedback equalizer circuit provides the functionality necessary for proper operation on subscriber loops with bridged taps.

A crystal oscillator provides the 15.36 MHz master clock for the device. The on-chip, phase-locked loop provides the ability to synchronize the chip to the line rate.

The U-interface provides rapid cold start and warm start operation. From a cold start, the device is typically operational within four seconds. The interface supports activation/deactivation, and when properly deactivated, it stores the adaptive filter coefficients permitting a warm start on the next activation request. A warm start typically requires 200 ms for the device to become operational.

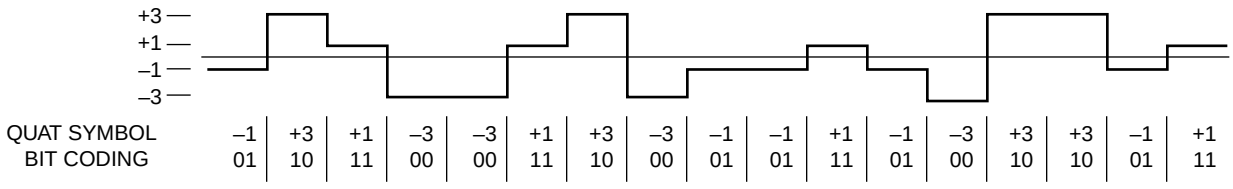

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Figure 9. U-Interface Quat Example

S/T-Interface Description

At the S/T-interface, the 4-wire line transceiver meets the ANSI T1.605 standard, ITU-T I.430 recommendation, and ETSI ETS 300 012 when used with the proper line interface circuitry. Refer to the March 1996, T7903 ISA Multiport Wide Area Connection (ISA-MWAC) Device Data Sheet (DS96-084ISDN). Appendix F of the ISA-MWAC data sheet is an application brief that contains detailed information concerning guidelines for S/T line interface circuit design.

The S/T transceiver interprets the frames received from the line and generates frames to be transmitted onto the S/T link. It exchanges full-duplex 2B+D information with the data flow matrix. The transceiver consists of two sections, the transmitter and the receiver. The transmitter is a voltage-limited current source. The transmitted bits are timed by an internal 192 kHz clock derived from the U-interface.

The transmitter employs a line coding technique referred to in the standards as “pseudo-ternary coding with 100% pulse width,” which is often referred to as alternate space inversion (ASI) coding. ASI coding represents a logical 1 by the absence of a pulse and a logical 0 by alternating positive and negative pulses. ASI is a differential strategy, with positive and negative rails connecting to the transformer. Current flows through the transformer only when there is a voltage difference on the two rails. When a logical one or mark is being sent, meaning no current is desired, both rails go to a high-impedance condition. When a positive logical zero (space) is transmitted, the positive rail forces current to the negative rail through the transformer. The reverse occurs for a negative zero. Table 3 and Figure 10 illustrate the ASI coding method.

Table 3. Line Transmission Code

Positive Rail	Negative Rail	Current	Logic
Z*	Z*	0	1
1	0	+1	+0
0	1	–1	–0

* Z = high impedance.

The line receiver is more complex. Since the loop length to the subscriber(s) is variable, as is the number of TEs on the loop (1 to 8), the receiver must be sufficiently intelligent to adjust for widely varying input waveforms. The receiver uses a self-adjusting voltage threshold comparator to adapt to various loop lengths. It also features a digital timing recovery circuit employing either adaptive or fixed timing modes.

The adaptive timing mode can be used on any loop configuration (point-to-point, extended passive bus, short passive bus) in which round trip delays are between 0 µs and 42 µs and differential delays between TEs are between 0 µs and 3.1 µs. This exceeds the requirement in the standards, which is 0—2 µs (see, for example, ITU-T I.430 section A.2.1.3 (p. 58). A differential delay of 0 µs is meaningful in the case of a line transmitter and line receiver directly connected externally in a loopback configuration, so the receiver can extract the 2B+D information correctly from the transmitted stream.

A short passive bus configuration permits TEs to be connected anywhere along the full length of the cable, with the restriction that the total round trip delay must be between 10 µs and 14 µs for all TEs. Thus, worst-case differential delay between TEs can be as much as 4 µs. If the differential delay is more than 3.1 µs, adaptive timing mode cannot be used. A fixed timing mode is available for this case. When using fixed timing, the input stream is sampled 4.2 µs after the leading edge of each 192 kHz transmit bit interval. The fixed/adaptive timing mode is controlled via the FTE pin if the TDM highway is not enabled (TDMEN = 0 in register GR2, bit 5). Otherwise, it is controlled via the FT microprocessor bit (register GR2, bit 0).

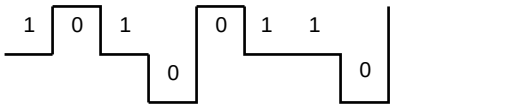


Figure 10. S/T-Interface ASI Example

Microprocessor Interface Description

The microprocessor interface, used to control and monitor the device, is compatible with most general-purpose serial microprocessor interfaces using a synchronous mode of transmission. A detailed description of the operation follows, and detailed timing information is given in the Timing Characteristics section.

Registers

The on-chip registers are divided by major circuit block and by status and control function. Microprocessor register control bits associated with the control flow state machine, eoc state machine, and multiframing controller are ignored when those blocks are enabled (the device controls the blocks automatically). When the blocks are disabled, the control bits are used to drive device operations. The functional summary of the registers and bits is shown in Figure 11.

Microprocessor Interface Description (continued)

Registers (continued)

FUNCTION	ADDRESS	REGISTER	R/W	BIT							
				7	6	5	4	3	2	1	0
GLOBAL DEVICE CONTROL—DEVICE CONFIGURATION	00h	GR0	R/W	RSV	AUTOACT	MULTIF	AUTOEOC	AUTOCTL	CRATE1	CRATE0	RESET
GLOBAL DEVICE CONTROL—U-INTERFACE	01h	GR1	R/W	SAI1	SAI0	XPCY	ACTT	NTM	PS1	PS2	LPBK
GLOBAL DEVICE CONTROL—S/T-INTERFACE	02h	GR2	R/W	STOA	ACTSEL	TDMEN	U2BDLN	SXE	SRESET	SPWRUD	FT
DATA FLOW CONTROL—U & S/T B CHANNELS	03h	DFR0	R/W	SXB21	SXB20	SXB11	SXB10	UXB21	UXB20	UXB11	UXB10
DATA FLOW CONTROL—D CHANNELS & TDM BUS	04h	DFR1	R/W	TDMDU	TDMB2U	TDMB1U	TDMDS	TDMB2S	TDMB1S	SXD	UXD
TDM BUS TIMING CONTROL	05h	TDR0	R/W	—	—	—	—	FSP	FSC2	FSC1	FSC0
CONTROL FLOW ST. MACH. CONTROL—MAINTEN./RSV. BITS	06h	CFR0	R/W	—	—	R64T	R25T	R16T	R15T	AFRST	ILOSS
CONTROL FLOW ST. MACH. STATUS	07h	CFR1	R	I4I	AIB	FEBE	NEBE	UOA	OOF	XACT	ACTR
CONTROL FLOW ST. MACH. STATUS—RESERVED BITS	08h	CFR2	R	—	R64R	R54R	R44R	R34R	R25R	R16R	R15R
eoc STATE MACHINE CONTROL—ADDRESS	09h	ECR0	R/W	CCRC	U2BDLT	UB2LP	UB1LP	DMT	A1T	A2T	A3T
eoc STATE MACHINE CONTROL—INFORMATION	0Ah	ECR1	R/W	I1T	I2T	I3T	I4T	I5T	I6T	I7T	I8T
eoc STATE MACHINE STATUS—ADDRESS	0Bh	ECR2	R	—	—	—	—	DMR	A1R	A2R	A3R
eoc STATE MACHINE STATUS—INFORMATION	0Ch	ECR3	R	I1R	I2R	I3R	I4R	I5R	I6R	I7R	I8R
Q CHANNEL BITS	0Dh	MCR0	R	—	—	—	—	Q1	Q2	Q3	Q4
S SUBCHANNEL 1	0Eh	MCR1	R/W	—	—	—	—	SC11	SC12	SC13	SC14
S SUBCHANNEL 2	0Fh	MCR2	R/W	—	—	—	—	SC21	SC22	SC23	SC24
S SUBCHANNEL 3	10h	MCR3	R/W	—	—	—	—	SC31	SC32	SC33	SC34
S SUBCHANNEL 4	11h	MCR4	R/W	—	—	—	—	SC41	SC42	SC43	SC44
S SUBCHANNEL 5	12h	MCR5	R/W	—	—	—	—	SC51	SC52	SC53	SC54
U-INTERFACE INTERRUPT REGISTER	13h	UIR0	R	—	—	TSFINT	RSFINT	OUSC	BERR	ACTSC	EOCSC
U-INTERFACE INTERRUPT MASK REGISTER	14h	UIR1	R/W	—	—	TSFINTM	RSFINTM	OUSCM	BERRM	ACTSCM	EOCSCM
S/T-INTERFACE INTERRUPT REGISTER	15h	SIR0	R	—	—	—	—	I4C	SFECV	QSC	SOM
S/T-INTERFACE INTERRUPT MASK REGISTER	16h	SIR1	R/W	—	—	—	—	I4CM	SFECVM	QSCM	SOMM
MAINTENANCE INTERRUPT REGISTER	17h	MIR0	R	—	—	—	—	—	EMINT	ILINT	QMINT
MAINTENANCE INTERRUPT MASK REGISTER	18h	MIR1	R/W	—	—	—	—	—	EMINTM	ILINTM	QMINTM
GLOBAL INTERRUPT REGISTER	19h	GIR0	R	—	—	—	—	—	MINT	SINT	UINT

Figure 11. Functional Register Map (Addresses and Bit Assignments)

Microprocessor Interface Description (continued)

Registers (continued)

Table 4. Global Device Control—Device Configuration (Address 00h)

Reg	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
GR0	R/W	Rsv.	AUTOACT	MULTIF	AUTOEOC	AUTOCTL	CRATE1	CRATE0	RESET
Default State on $\overline{\text{RESET}}$		1	AUTOACT/ SCK	1	1	1	1	1	1

Register	Bit	Symbol	Name/Description
GR0	0	RESET	**Reset.** Same function as external $\overline{\text{RESET}}$ pin, except the state of the AUTOACT/ SCK, ACTMODE/$\overline{\text{INT}}$, and SYN8K_CTL/SDI pins are not checked. Assertion of this bit halts data transmission, clears adaptive filter coefficients, resets the S/T-interface transceiver, and sets all microprocessor register bits (except itself) to their default state. The microprocessor must write this bit back to a 1 to bring the T7256 out of its RESET state. During reset, the U-interface transmitter produces 0 V and the output impedance is 135 Ω at tip and ring. 0—Reset. 1—No effect on device operation (default).
GR0	2—1	CRATE[1:0]	**CKOUT Rate Control.** 00—Not used. 01—10.24 MHz synchronous with U-interface (if active); otherwise, free-running. 10—15.36 MHz free-running. 11—3-state (default).
GR0	3	AUTOCTL	**Auto Control Enable.** Enables automatic control of ANSI maintenance and reserved bit insertion. When AUTOCTL = 1, register CFR0 is ignored and the control flow state machine automatically controls ANSI maintenance functions and reserved bit insertion. When AUTOCTL = 0, the microprocessor controls ANSI maintenance functions and reserved bit insertion via register CFR0. 0—CFR0 functions controlled manually by microprocessor. 1—CFR0 functions controlled automatically.
GR0	4	AUTOEOC	**Automatic eoc Processor Enable.** Enables eoc state machine which implements eoc processing per the ANSI standard. When AUTOEOC = 1, registers ECR0—ECR1 are ignored. The eoc state machine only responds to addresses 000 and 111 as valid addresses. 0—eoc state machine disabled. 1—eoc state machine enabled (default).
GR0	5	MULTIF	**Multiframing Control.** Enables the multiframing controller and allows the microprocessor to access the S and Q channels. When disabled, multiframing is not implemented (the NT transmits all 0s in the FA and M bit positions and all 1s in the S bit positions to the TE). Also, register bits 3—0 in MCR0 are forced to 1 and register bits 3—0 in MCR1—5 are forced to 0 when multiframing is disabled. 0—Multiframing controller enabled. 1—Multiframing controller disabled (default).

Microprocessor Interface Description (continued)

Registers (continued)

Table 4. Global Device Control—Device Configuration (Address 00h) (continued)

Register	Bit	Symbol	Name/Description
GR0	6	AUTOACT	**Automatic Activation Control.** Upon a 1-to-0 transition of the AUTOACT bit, the control flow state machine attempts one activation of the U-interface. After the activation attempt, this bit is internally set to 1, automatically. If the AUTOACT/SCK pin is low on the rising edge of $\overline{\text{RESET}}$, AUTOACT is written to 0 and one activation attempt is made (see AUTOACT/SCK pin description in Table 1). Multiple activation attempts can be made by repeatedly writing 0s to this bit. 1—No activation attempt. 0—One activation attempt.
GR0	7	—	**Reserved.** Set to 1. 1—Default.

Microprocessor Interface Description (continued)

Registers (continued)

Table 5. Global Device Control—U-Interface (Address 01h)

Reg	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
GR1	R/W	SAI1	SAI0	XPCY	ACTT	NTM	PS1	PS2	LPBK
Default State on $\overline{\text{RESET}}$		1	1	1	0	1	1	1	1

Register	Bit	Symbol	Name/Description
GR1	0	LPBK	**U-Interface Analog Loopback.** Controls loopback of U-interface data stream at the line interface. Loopback turns off the echo canceler and reconfigures the receive scrambler to match the transmit scrambler. The line should be disconnected before this loopback test. This ensures that a sufficiently large echo is generated so that the device can detect the echo as received data and synchronize to it. 0—U-interface analog loopback. 1—No effect on device operation (default).
GR1	1	PS2	**Power Status #2.** Controls PS2 bit in transmit U-interface data stream if TDMEN = 0 (register GR2, bit 5). If TDMEN = 1, PS2 bit is ignored. For ANSI T1.601 applications, PS1 and PS2 indicate the NT power status via the following messages: **PS1 PS2 Power Status** 0 0 Dying gasp. 0 1 Primary power out. 1 0 Secondary power out. 1 1 All power normal (default).
GR1	2	PS1	**Power Status #1.** Controls PS1 bit in transmit U-interface data stream if TDMEN = 0 (register GR2, bit 5). If TDMEN = 1, PS1 bit is ignored. See PS2 bit definition.
GR1	3	NTM	**NT Test Mode.** Controls ntm bit in transmit U-interface data stream and indicates if the NT is in a customer-initiated test mode. 0—NT is currently in a customer-initiated test mode. 1—No effect on device operation (default).
GR1	4	ACTT	**Transmit Activation.** Controls act bit in transmit U-interface data stream. 0—No effect on device operation (default). 1—Ready to transmit.
GR1	5	XPCY	**Transparency.** Controls data being transmitted at U-interface. 0—Enable data transparency. 1—No effect on device operation (default).
GR1	7—6	SAI[1:0]	**S/T-Interface Activity Indicator Control.** Controls sai bit in transmit U-interface data stream. For ANSI T1.601 applications, the sai bit is set to 1 to indicate to the network that there is activity (INFO 1 or INFO 3) at the S/T reference point. Otherwise, it is set to 0. The SAI[1:0] bits provide the following options for controlling the sai bit: 00—Forces sai to 0 on the U-interface. 01—Forces sai to 1 on the U-interface. 1X—sai is set internally according to S-interface activity (default = 11).

Microprocessor Interface Description (continued)

Registers (continued)

Table 6. Global Device Control—S/T-Interface (Address 02h)

Reg	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
GR2	R/W	STOA	ACTSEL	TDMEN	U2BDLN	SXE	SRESET	SPWRUD	FT
Default State on $\overline{\text{RESET}}$		1	ACTMODE/ $\overline{\text{INT}}$ pin	1	1	1	1	1	1

Register	Bit	Symbol	Name/Description
GR2	0	FT	**Fixed/Adaptive Timing Control.** Controls mode of timing recovery on S/T-interface if TDMEN = 0 (register GR2, bit 5). If TDMEN = 1, FT is ignored. 0—Fixed timing. 1—Adaptive timing (default).
GR2	1	SPWRUD	**S/T-Interface Powerdown Control.** When 0, this bit forces the S/T-interface to remain in a powerdown mode. This is the same low-power mode the S/T-interface is in when the T7256 is in its IDLE state with no activity on the U- or S/T-interfaces. In this mode, all S/T-interface circuits are powered down, except for circuits required to detect an activation request from a TE. 0—Powerdown. 1—Normal (default).
GR2	2	SRESET	**S/T-Interface Reset.** While 0, this bit causes a reset of the S/T-interface, initializing the interface in the same manner as the external $\overline{\text{RESET}}$ pin. Must be set to 1 for normal operation. 0—Reset. 1—Normal (default).
GR2	3	SXE	**S/T-Interface D-Channel Echo Bit Control.** Controls data in E channel from NT to TE on S/T-interface. This bit must be cleared during 2B+D loopbacks to meet ITU-T I.430 requirements. 0—All 0s. 1—Echoes D channel from S/T receive path (default).
GR2	4	U2BDLN	**Nontransparent 2B+D Loopback Control.** When 0, this bit causes a nontransparent loopback of 2B+D data from U receiver to U transmitter upstream of the data flow matrix. Note that this loopback path is not as close to the S/T-interface as the transparent loopback initiated by U2BDLT (register ECR0, bit 6). This loopback may be useful for test purposes. When this bit is set, the upstream data (NT to LT direction) will be forced to all 1s until either ACTR = 1 (register CFR1, bit 0) or XPCY = 0 (register GR1, bit 5). 0—2B+D loopback. All 1s 2B+D data is automatically generated towards the TE. 1—No loopback (default).
GR2	5	TDMEN	**TDM Bus Select.** Selects functions of pins 4, 7, 8, and 9. 0—TDM bus functions. Pins 4, 7, 8, and 9 configured as FS, TDMDI, TDMDO, and TDMCLK, respectively. See DFR1 and TDR0 registers for TDM bus programming details. Microprocessor register bits GR11, GR12, and GR20 control the PS2, PS1, and FT functions. 1—No TDM bus. Pins 4, 7, 8, and 9 configured as SYN8K/LBIND, FTE, PS2E, and PS1E, respectively (default).

Microprocessor Interface Description (continued)

Registers (continued)

Table 6. Global Device Control—S/T-Interface (Address 02h) (continued)

Reg	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
GR2	R/W	STOA	ACTSEL	TDMEN	U2BDLN	SXE	SRESET	SPWRUD	FT
Default State on $\overline{\text{RESET}}$		1	ACTMODE/ $\overline{\text{INT}}$ pin	1	1	1	1	1	1

Register	Bit	Symbol	Name/Description
GR2	6	ACTSEL	**ACT Mode Select.** Controls the state of the transmitted ACT bit when an eoc loopback 2 (2B+D loopback) is requested. The loopback 2 occurs automatically if AUTOEOC = 1 (register GR0, bit 4). Otherwise, bit U2BDLT (register ECR0, bit 6) must be set to 0. The loopback is accomplished in the device by looping the output of the S/T transmitter back to the input of the S/T receiver at the device pins (i.e., as close to the S/T-interface as possible). The S/T transceiver will ignore any signals transmitted by the TE, and the T7256 will synchronize to its own transmit signal causing INFO 3 to be reported. The initial state of ACTSEL is determined by the state of the ACTMODE/$\overline{\text{INT}}$ pin on the rising edge of $\overline{\text{RESET}}$. 0—act = 0 during loopback 2 (per ANSI T1.601). The data received at the NT is looped back towards the LT as soon as the 2B+D loopback is enabled. 1—act = 1 during loopback 2 after INFO 3 is recognized at the S/T-interface (per ETSI ETR 080). The data received by the NT is not looped back towards the LT until after ACT = 1 is received from the LT. Prior to this time, 2B+D data toward the LT is all 1s.
GR2	7	STOA	**S/T Only Activation.** Set to 0 to force an S/T activation when the U-interface is inactive. When the U-interface is active, this bit is ignored. STOA is reset to 1 upon the receipt of a U-interface tone, an INFO1 or INFO3 signal, or a 1-to-0 transition of AUTOACT (register GR0, bit 6). 0—Attempt an S/T only activation. 1—No effect on device operation (default).

Microprocessor Interface Description (continued)

Registers (continued)

Table 7. Data Flow Control—U and S/T B Channels (Address 03h)

Reg	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DFR0	R/W	SXB21	SXB20	SXB11	SXB10	UXB21	UXB20	UXB11	UXB10
Default State on $\overline{\text{RESET}}$		1	1	1	1	1	1	1	1

Register	Bit	Symbol	Name/Description
DFR0	1—0	UXB1[1:0]	**U-Interface Transmit Path Source for B1 Channel.** Refer to point #1 in Figure 16. 00—Not used. 01—TDM bus. 10—All 1s. 11—S/T-interface receive (default).
DFR0	3—2	UXB2[1:0]	**U-Interface Transmit Path Source for B2 Channel.** Refer to point #1 in Figure 16. 00—Not used. 01—TDM bus. 10—All 1s. 11—S/T-interface receive (default).
DFR0	5—4	SXB1[1:0]	**S/T-Interface Transmit Path Source for B1 Channel.** Refer to point #2 in Figure 16. 00—Not used. 01—TDM bus. 10—S/T-interface receive (ITU-T I.430 Loop C for B1 channel). 11—U-interface receive (default).
DFR0	7—6	SXB2[1:0]	**S/T-Interface Transmit Path Source for B2 Channel.** Refer to point #2 in Figure 16. 00—Not used. 01—TDM bus. 10—S/T-interface receive (ITU-T I.430 Loop C for B2 channel). 11—U-Interface receive (default).

Microprocessor Interface Description (continued)

Registers (continued)

Table 8. Data Flow Control—D Channels and TDM Bus (Address 04h)

Bits 2—7 are enabled only if TDMEN = 0 (register GR2, bit 5). The TDMCLK and FS outputs are activated if any one of bits 2—7 is enabled. The TDMDO output is activated during time slots enabled by programming bits 2—7.

Reg	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DFR1	R/W	TDMDU	TDMB2U	TDMB1U	TDMDS	TDMB2S	TDMB1S	SXD	UXD
Default State on $\overline{\text{RESET}}$		1	1	1	1	1	1	1	1

Register	Bit	Symbol	Name/Description
DFR1	0	UXD	**U-Interface Transmit Path Source for D Channel.** Refer to point #1 in Figure 16. 0—TDM bus. 1—S/T-interface receive (default).
DFR1	1	SXD	**S/T-Interface Transmit Path Source for D Channel.** Refer to point #2 in Figure 16. 0—TDM bus. 1—U-interface receive (default).
DFR1	2	TDMB1S	**TDM Bus Transmit Control for B1 Channel from S/T-Interface.** Refer to point #3 in Figure 16. Controls transmit time slot allocated on TDM bus for B1 channel derived from S/T-interface receiver. 0—Time slot enabled. 1—Time slot disabled (high impedance) (default).
DFR1	3	TDMB2S	**TDM Bus Transmit Control for B2 Channel from S/T-Interface.** Refer to point #3 in Figure 16. Controls transmit time slot allocated on TDM bus for B2 channel derived from S/T-interface receiver. 0—Time slot enabled. 1—Time slot disabled (high impedance) (default).
DFR1	4	TDMDS	**TDM Bus Transmit Control for D Channel from S/T-Interface.** Refer to point #3 in Figure 16. Controls transmit time slot allocated on TDM bus for D channel derived from S/T-interface receiver. 0—Time slot enabled. 1—Time slot disabled (high impedance) (default).
DFR1	5	TDMB1U	**TDM Bus Transmit Control for B1 Channel from U-Interface.** Refer to point #3 in Figure 16. Controls transmit time slot allocated on TDM bus for B1 channel derived from U-interface receiver. 0—Time slot enabled. 1—Time slot disabled (high impedance) (default).
DFR1	6	TDMB2U	**TDM Bus Transmit Control for B2 Channel from U-Interface.** Refer to point #3 in Figure 16. Controls transmit time slot allocated on TDM bus for B2 channel derived from U-interface receiver. 0—Time slot enabled. 1—Time slot disabled (high impedance) (default).
DFR1	7	TDMDU	**TDM Bus Transmit Control for D Channel from U-Interface.** Refer to point #3 in Figure 16. Controls transmit time slot allocated on TDM bus for D channel derived from U-interface receiver. 0—Time slot enabled. 1—Time slot disabled (high impedance) (default).

Microprocessor Interface Description (continued)

Registers (continued)

Table 9. TDM Bus Timing Control (Address 05h)

Bits 0—4 are enabled only if TDMEN = 0 (register GR2, bit 5) and one or more of bits DFR1[2:7] are set to 0.

Reg	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TDR0	R/W	—	—	—	—	FSP	FSC2	FSC1	FSC0
Default State on $\overline{\text{RESET}}$		—	—	—	—	1	1	1	1

Register	Bit	Symbol	Name/Description
TDR0	2—0	FSC[2:0]	**Frame Strobe (FS) Control.** Selects location of strobe envelope within TDM bus time slots. 000—S/T-interface 2B+D channel strobe (18-bit envelope). 001—U-interface 2B+D channel strobe (18-bit envelope). 010—S/T-interface B2 channel strobe (8-bit envelope). 011—U-interface B2 channel strobe (8-bit envelope). 100—S/T-interface D channel strobe (2-bit envelope). 101—U-interface D channel strobe (2-bit envelope). 110—S/T-interface B1 channel strobe (8-bit envelope). 111—U-interface B1 channel strobe (8-bit envelope) (default).
TDR0	3	FSP	**Frame Strobe (FS) Polarity.** 0—Active-low envelope. 1—Active-high envelope (default).

Microprocessor Interface Description (continued)

Registers (continued)

Table 10. Control Flow State Machine Control—Maintenance/Reserved Bits (Address 06h)

This register has no effect on device operation if AUTOCTL = 1 (register GR0, bit 3).

Reg	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CFR0	R/W	—	—	R64T	R25T	R16T	R15T	AFRST	ILOSS
Default State on $\overline{\text{RESET}}$		—	—	1	1	1	1	1	1

Register	Bit	Symbol	Name/Description
CFR0	0	ILOSS	**Insertion Loss Test Control.** The insertion loss test mode is initiated by setting AFRST = 0 and ILOSS = 0, and then setting AFRST = 1. When enabled, the U-interface transmitter continuously transmits the sequence SN1. The U-interface receiver remains reset. The U-interface transceiver performs an internal reset when the ILOSS bit returns to its inactive state. 0—U-transmitter sends SN1 tone continuously. 1—No effect on device operation (default).
CFR0	1	AFRST	**Adaptive Filter Reset.** U-transceiver reset. Assertion of this bit halts U-interface data transmission and clears adaptive filter coefficients. During AFRST, the U transmitter produces 0 V and has an output impedance of 135 Ω. If the microprocessor interface is being used, the AFRST bit should be used to place the device in quiet mode for U-interface maintenance procedures. Assertion of AFRST does not reset the S/T transceiver, microprocessor register bits, or the U-interface timing recovery. 0—U-transceiver reset. 1—No effect on device operation (default).
CFR0	3—2	R[16:15]T	**Transmit Reserved Bits.** Controls $R_{1, 6}$ and $R_{1, 5}$ in transmit U-interface data stream. 11—(Default.)
CFR0	4	R25T	**Transmit Reserved Bit.** Controls $R_{2, 5}$ in transmit U-interface data stream. 1—(Default.)
CFR0	5	R64T	**Transmit Reserved Bit.** Controls $R_{6, 4}$ in transmit U-interface data stream. 1—(Default.)

Microprocessor Interface Description (continued)

Registers (continued)

Table 11. Control Flow State Machine Status (Address 07h)

Reg	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CFR1	R	I4I	AIB	FEBE	NEBE	UOA	OOF	XACT	ACTR

Register	Bit	Symbol	Name/Description
CFR1	0	ACTR	**Receive Activation.** Follows act bit in receive U-interface data stream. 0—Pending activation. 1—Ready to transmit.
CFR1	1	XACT	**U-Transceiver Active.** 0—Transceiver not active. 1—Transceiver starting up or active.
CFR1	2	OOF	**Out of Frame.** 0—U-interface out of frame. 1—Normal.
CFR1	3	UOA	**U-Interface Only Activation.** Follows uoa bit in receive U-interface data stream. 0—U-interface only for activation. 1—U-interface and S/T-interface for activation.
CFR1	4	NEBE	**Near-End Block Error.** Follows nebe bit in receive U-interface data stream. 0—CRC error detected in previously received U frame. 1—No error.
CFR1	5	FEBE	**Far-End Block Error.** Follows febe bit in receive U-interface data stream. 0—Error detected at LT. 1—No error.
CFR1	6	AIB	**Alarm Indication Bit.** Follows aib in receive U-interface data stream. 0—Failure of intermediate 2B+D transparent element. 1—Transmission path established between LT and NT.
CFR1	7	I4I	**INFO 4 Indicator.** 0—Non-INFO 4. 1—INFO 4.

Microprocessor Interface Description (continued)

Registers (continued)

Table 12. Control Flow State Machine Status—Reserved Bits (Address 08h)

Reg	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CFR2	R	—	R64R	R54R	R44R	R34R	R25R	R16R	R15R

Register	Bit	Symbol	Name/Description
CFR2	1—0	R[16:15]R	**Receive Reserved Bits.** Follows $R_{1,5}$ and $R_{1,6}$ in receive U-interface data stream.
CFR2	2	R25R	**Receive Reserved Bits.** Follows $R_{2,5}$ in receive U-interface data stream.
CFR2	6—3	R[64:54:44:34]R	**Receive Reserved Bits.** Follows $R_{3,4}$; $R_{4,4}$; $R_{5,4}$; and $R_{6,4}$ in receive U-interface data stream.

Microprocessor Interface Description (continued)

Registers (continued)

Table 13. eoc State Machine Control—Address (Address 09h)

This register has no effect on device operation if AUTOEOC = 1 (register GR0, bit 4).

Reg	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ECR0	R/W	CCRC	U2BDLT	UB2LP	UB1LP	DMT	A1T	A2T	A3T
Default State on $\overline{\text{RESET}}$		1	1	1	1	1	0	0	0

Register	Bit	Symbol	Name/Description
ECR0	0—2	A[3:1]T	**Transmit eoc Address.** 000—NT address (default). 111—Broadcast address.
ECR0	3	DMT	**Transmit eoc Data or Message Indicator.** 0—Data. 1—Message (default).
ECR0	4	UB1LP	**U-Interface Loopback of B1 Channel Control.** Control for U-interface transparent B1 loopback. UB1LP and UB2LP may be enabled concurrently. 0—B1 channel loopback from U-interface receive to U-interface transmit upstream of data flow matrix. 1—No loopback (default).
ECR0	5	UB2LP	**U-Interface Loopback of B2 Channel Control.** Control for U-interface transparent B2 loopback. UB1LP and UB2LP may be enabled concurrently. 0—B2 channel loopback from U-interface receive to U-interface transmit upstream of data flow matrix. 1—No loopback (default).
ECR0	6	U2BDLT	**Transparent 2B+D Loopback Control.** When activated, this bit causes a transparent 2B+D loopback from S/T transmitter to S/T receiver at the device pins (i.e., as close as possible to the S/T-interface) according to ITU-T I.430 Loop2. Any signals from the TE are ignored during this loopback. 0—Transparent 2B+D loopback: The microprocessor must clear the D-channel echo bit control (SXE = 0) and data flow matrix (SXB10 = SXB11 = SXB20 = SXB21 = SXD = UXB10 = UXB11 = UXB20 = UXB21 = UXD = 1) for proper operation of the loopback. 1—No loopback (default).
ECR0	7	CCRC	**Corrupt Cyclic Redundancy Check.** Used to corrupt the CRC information transmitted at the U-interface. 0—Corrupt CRC generation. 1—Generate correct CRC (default).

Microprocessor Interface Description (continued)

Registers (continued)

Table 14. eoc State Machine Control—Information (Address 0Ah)

This register has no effect on device operation if AUTOEOC = 1 (register GR0, bit 4).

Reg	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ECR1	R/W	I1T	I2T	I3T	I4T	I5T	I6T	I7T	I8T
Default State on $\overline{\text{RESET}}$		1	1	1	1	1	1	1	1

Register	Bit	Symbol	Name/Description
ECR1	0—7	I[8:1]T	**Transmit eoc Information.** These bits are transmitted as the eoc channel message when in manual eoc mode. See eoc State Machine Description section for a list of possible eoc messages.

Table 15. eoc State Machine Status—Address (Address 0Bh)

This register contains the currently received eoc address and data/message indicator bits independent of the state of AUTOEOC (register GR0, bit 4).

Reg	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ECR2	R	—	—	—	—	DMR	A1R	A2R	A3R

Register	Bit	Symbol	Name/Description
ECR2	0—2	A[3:1]R	**Receive eoc Address.** These bits store the received eoc address. 000 = NT address. 001—110 = Intermediate element addresses. 111 = Broadcast address.
ECR2	3	DMR	**Receive eoc Data or Message Indicator.** 0—Data. 1—Message.

Table 16. eoc State Machine Status—Information (Address 0Ch)

This register contains the currently received eoc information bits independent of the state of AUTOEOC (register GR0, bit 4).

Reg	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ECR3	R	I1R	I2R	I3R	I4R	I5R	I6R	I7R	I8R

Register	Bit	Symbol	Name/Description
ECR3	0—7	I[8:1]R	**Receive eoc Information.** Receive eoc channel message or data.

Microprocessor Interface Description (continued)

Registers (continued)

Table 17. Q-Channel Bits (Address 0Dh)

These register bits are forced to 1 if MULTIF = 1 (register GR0, bit 5) and during $\overline{\text{RESET}}$.

Reg	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
MCR0	R	—	—	—	—	Q1	Q2	Q3	Q4

Register	Bit	Symbol	Name/Description
MCR0	0—3	Q[4:1]	**Q-Channel Bits.** Four bits reflecting the four Q bits (Q1—Q4) received in the last completed multiframe. Bits are loaded at the end of the multiframe.

Table 18. S Subchannels 1—5 (Address 0Eh—12h)

These register bits have no effect on device operation and are set to 0 if MULTIF = 1. Refer to the S/T-Interface Multiframing Controller Description section for more detail on using S and Q channels.

Reg	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
MCR1	R/W	—	—	—	—	SC11	SC12	SC13	SC14
MCR2	R/W	—	—	—	—	SC21	SC22	SC23	SC24
MCR3	R/W	—	—	—	—	SC31	SC32	SC33	SC34
MCR4	R/W	—	—	—	—	SC41	SC42	SC43	SC44
MCR5	R/W	—	—	—	—	SC51	SC52	SC53	SC54
Default State on $\overline{\text{RESET}}$		—	—	—	—	0	0	0	0

Register	Bit	Symbol	Name/Description
MCR1	0—3	SC1[4:1]	**S Subchannel 1.**
MCR2	0—3	SC2[4:1]	**S Subchannel 2.**
MCR3	0—3	SC3[4:1]	**S Subchannel 3.**
MCR4	0—3	SC4[4:1]	**S Subchannel 4.**
MCR5	0—3	SC5[4:1]	**S Subchannel 5.**

Microprocessor Interface Description (continued)

Registers (continued)

Table 19. U-Interface Interrupt Register (Address 13h)

These bits are cleared during $\overline{\text{RESET}}$.

Reg	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
UIR0	R	—	—	TSFINT	RSFINT	OUSC	BERR	ACTSC	EOCSC

Register	Bit	Symbol	Name/Description
UIR0	0	EOCSC	**eoc State Change on U-Interface.** Activates (set to 1) when the received eoc message changes state. Bit is cleared on read. See eoc State Machine Description section for details. 0—No change in eoc state. 1—eoc state change.
UIR0	1	ACTSC	**Activation/Deactivation State Change on U-Interface.** Activates (set to 1) during changes in the status bits monitoring U-interface activation and deactivation (ACTR and XACT, register CFR1, bits 0 and 1). Bit cleared on read. 0—No activation/deactivation activity. 1—Change in state of activation/deactivation bits.
UIR0	2	BERR	**Block Error on U-Interface.** Activates (set to 1) when received signal contains either a near-end (NEBE = 0) or a far-end (FEBE = 0) block error. Bit cleared on read. 0—No block errors. 1—Block error.
UIR0	3	OUSC	**Other U-Interface State Change.** Activates (set to 1) when any of the following bits change state: OOF, UOA, AIB, and Rx, y (all reserved U-interface status bits). Bit cleared on read. 0—No state change. 1—State change.
UIR0	4	RSFINT	**Receive Superframe Interrupt.** Activates (set to 1) when the receive superframe boundary occurs. Bit cleared on read. 0 to 1—First 2B+D data of the receive U superframe.
UIR0	5	TSFINT	**Transmit Superframe Interrupt.** Activates (set to 1) when the transmit superframe boundary occurs. Bit cleared on read. 0 to 1—First 2B+D data of the transmit U superframe.

Microprocessor Interface Description (continued)

Registers (continued)

Table 20. U-Interface Interrupt Mask Register (Address 14h)

Reg	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
UIR1	R/W	—	—	TSFINTM	RSFINTM	OUSCM	BERRM	ACTSCM	EOCSCM
Default State on $\overline{\text{RESET}}$		—	—	1	1	1	1	1	1

Register	Bit	Symbol	Name/Description
UIR1	0	EOCSCM	**eoc State Change on U-Interface Mask.** 0—EOCSC interrupt enabled. 1—EOCSC interrupt disabled (default).
UIR1	1	ACTSCM	**Activation/Deactivation State Change on U-Interface Mask.** 0—ACTSC interrupt enabled. 1—ATCSC interrupt disabled (default).
UIR1	2	BERRM	**Block Error on U-Interface Mask.** 0—BERR interrupt enabled. 1—BERR interrupt disabled (default).
UIR1	3	OUSCM	**Other U-Interface State Change Mask.** 0—OUSC interrupt enabled. 1—OUSC interrupt disabled (default).
UIR1	4	RSFINTM	**Receive Superframe Interrupt Mask.** 0—RSFINT interrupt enabled. 1—RSFINT interrupt disabled (default).
UIR1	5	TSFINTM	**Transmit Superframe Interrupt Mask.** 0—TSFINT interrupt enabled. 1—TSFINT interrupt disabled (default).

Microprocessor Interface Description (continued)

Registers (continued)

Table 21. S/T-Interface Interrupt Register (Address 15h)

These bits are cleared during $\overline{\text{RESET}}$.

Reg	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SIR0	R	—	—	—	—	I4C	SFECV	QSC	SOM

Register	Bit	Symbol	Name/Description
SIR0	0	SOM	**Start of Multiframe.** Activates (set to 1) upon transmission of the F bit that begins a multiframing interval toward the TE. Bit is cleared on read. 0 to 1—Start of multiframe.
SIR0	1	QSC	**Q-Bits State Change.** Activates (set to 1) when the set of four Q bits received in a multiframe differs from the set of Q bits received in the previous multiframe. Bit is cleared on read. 0—No state change. 1—State change.
SIR0	2	SFECV	**S-Channel Far-End Code Violation.** Activates when an illegal line code violation or extra/missing bipolar violations are detected in the S/T-interface data stream. Changes on multiframe boundary. Only active if MULTIF = 0 (register GR0, bit 5) and a transparent Loop2 is not in effect. Bit is cleared on read. 0—No code violations. 1—At least one code violation.
SIR0	3	I4C	**INFO 4 Change.** 0—No INFO 4 state change. 1—INFO 4 state change.

Table 22. S/T-Interface Interrupt Mask Register (Address 16h)

Reg	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SIR1	R/W	—	—	—	—	I4CM	SFECVM	QSCM	SOMM
Default State on $\overline{\text{RESET}}$		—	—	—	—	1	1	1	1

Register	Bit	Symbol	Name/Description
SIR1	0	SOMM	**Start of Multiframe Mask.** 0—SOM interrupt enabled. 1—SOM interrupt disabled (default).
SIR1	1	QSCM	**Q-Bits State Change Mask.** 0—QSC interrupt enabled. 1—QSC interrupt disabled (default).
SIR1	2	SFECVM	**S-Subchannel Far-End Code Violation Mask.** 0—SFECVM interrupt enabled. 1—SFECVM interrupt disabled (default).
SIR1	3	I4CM	**INFO 4 Change Mask.** 0—I4C interrupt enabled. 1—I4C interrupt disabled (default).

Microprocessor Interface Description (continued)

Registers (continued)

Table 23. Maintenance Interrupt Register (Address 17h)

These bits are cleared during $\overline{\text{RESET}}$.

Reg	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
MIR0	R	—	—	—	—	—	EMINT	ILINT	QMINT

Register	Bit	Symbol	Name/Description
MIR0	0	QMINT	**Quiet Mode Interrupt.** Activates (set to 1) when the ANSI maintenance state machine detects a request on the OPTOIN pin for the device to enter the quiet mode. Bit is cleared on read. 0—No quiet mode request. 1—Quiet mode requested.
MIR0	1	ILINT	**Insertion Loss Interrupt.** Activates (set to 1) when the ANSI maintenance state machine has detected a request on the OPTOIN pin for the device to transmit the SN1 tone on the U-interface. Bit is cleared on read. 0—No SN1 tone request. 1—SN1 tone requested.
MIR0	2	EMINT	**Exit Maintenance Mode Interrupt.** Activates (set to 1) when the ANSI maintenance state machine detects a request on the OPTOIN pin for the device to exit the current maintenance mode. Bit is cleared on read. 0—No exit request. 1—Exit requested.

Table 24. Maintenance Interrupt Mask Register (Address 18h)

Reg	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
MIR1	R/W	—	—	—	—	—	EMINTM	ILINTM	QMINTM
Default State on $\overline{\text{RESET}}$		—	—	—	—	—	1	1	1

Register	Bit	Symbol	Name/Description
MIR1	0	QMINTM	**Quiet Mode Interrupt Mask.** 0—QMINT interrupt enabled. 1—QMINT interrupt disabled (default).
MIR1	1	ILINTM	**Insertion Loss Interrupt Mask.** 0—ILINT interrupt enabled. 1—ILINT interrupt disabled (default).
MIR1	2	EMINTM	**Exit Maintenance Mode Interrupt Mask.** 0—EMINT interrupt enabled. 1—EMINT interrupt disabled (default).

Microprocessor Interface Description (continued)

Registers (continued)

Table 25. Global Interrupt Register (Address 19h)

These bits are cleared during $\overline{\text{RESET}}$.

Reg	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
GIR0	R	—	—	—	—	—	MINT	SINT	UINT

Register	Bit	Symbol	Name/Description
GIR0	0	UINT	**U-Transceiver Interrupt.** Activates (set to 1) when any of the unmasked U-transceiver interrupt bits (register UIR0) activate. 0—No U-transceiver interrupts. 1—U-transceiver interrupt active.
GIR0	1	SINT	**S/T-Transceiver Interrupt.** Activates (set to 1) when any of the unmasked S/T-transceiver interrupt bits (register SIR0) activate. 0—No S/T-transceiver interrupts. 1—S/T-transceiver interrupt active.
GIR0	2	MINT	**Maintenance Interrupt.** Activates (set to 1) when any of the unmasked maintenance interrupt bits (register MIR0) activate. 0—No maintenance interrupts. 1—Maintenance interrupt active.

Microprocessor Interface Description (continued)

Timing

The microprocessor interface is compatible with any microprocessor that supports a synchronous serial microprocessor port such as the following:

- NEC[1] 75402
- Motorola[2] MC68HC05 and MC68302 SCP port
- Intel[3] 80C51

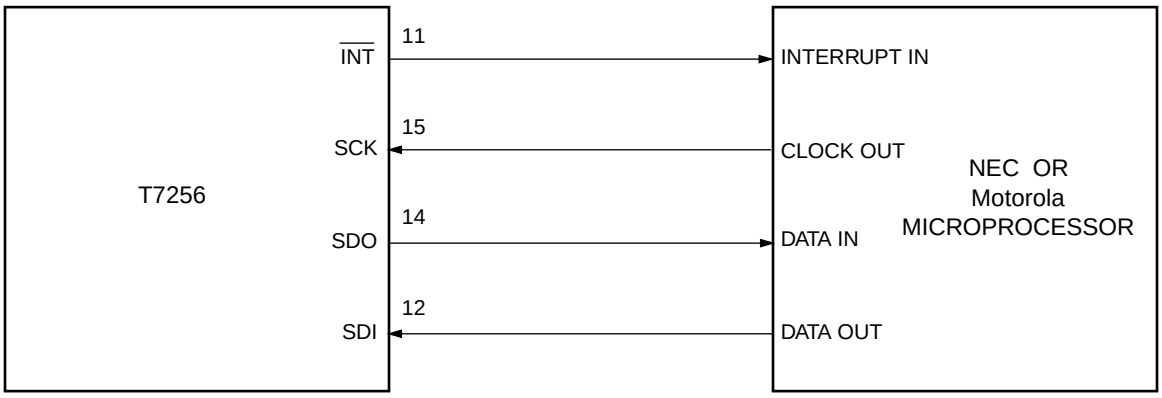


Figure 12. NEC and Motorola Microprocessor Port Connections

The synchronous interface consists of the microprocessor input clock (SCK), serial data input (SDI), and serial data output (SDO). A microprocessor interrupt lead ($\overline{INT}$) is also included. These connections are shown in Figure 12 for applications using either NEC or Motorola microprocessors. Figure 13 shows the connections for applications using a multiplexed data out/in scheme such as the Intel 80C51 or equivalent.

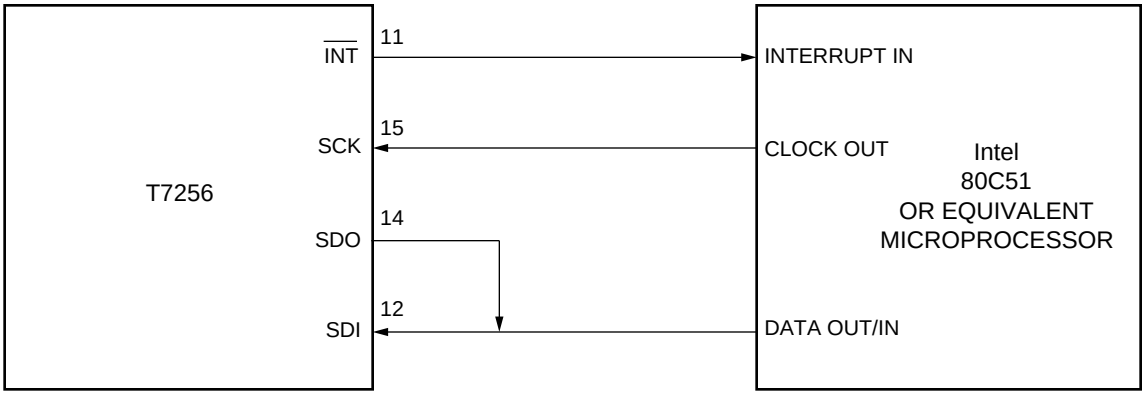
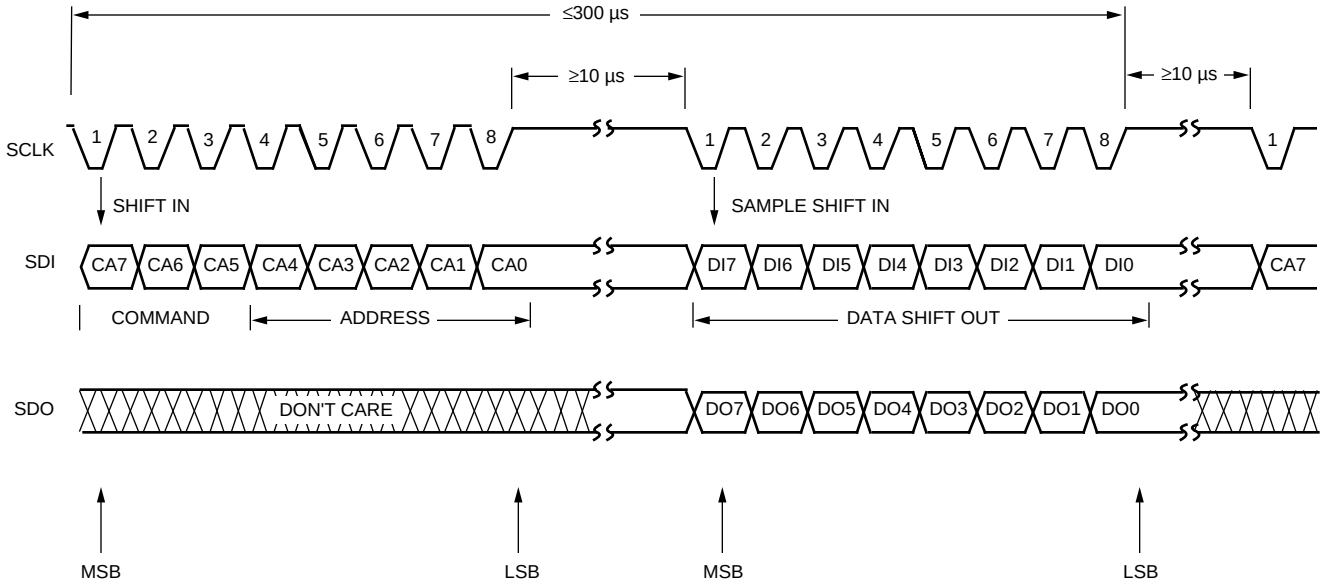


Figure 13. Intel Microprocessor Port Connections

1. NEC is a registered trademark of NEC Electronics, Inc.
2. Motorola is a registered trademark of Motorola, Inc.
3. Intel is a registered trademark of Intel Corporation.

Microprocessor Interface Description (continued)

Timing (continued)



Note: If SCLK is initially low, it must be held high for >300 µs before its first falling edge. From that point forward, the above timing applies.

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Figure 14. Synchronous Microprocessor Port Interface Format

Figure 14 shows the basic transfer format. All data transfers are initiated by the microprocessor, although the interrupt may indicate to the microprocessor that a register read or write is required. The microprocessor should normally hold the SCK pin high during inactive periods and only make transitions during register transfers. The maximum clock rate of SCK is 960 kHz. Data changes on the falling edge of SCK and is latched on the rising edge of SCK.

Each complete serial transfer consists of 2 bytes (8 bits/byte). The first byte of data received over the SDI pin from the microprocessor consists of command/address information that includes a 5-bit register address in the least significant bit positions (CA4—CA0) and a 3-bit command field in the most significant bit positions (CA7—CA5). The byte is defined as follows:

- Bits CA7—CA5: 001 = read, 010 = write, all other bit patterns will be ignored.
- Bits CA4—CA0: 00000 = register address 0, 00001 = register address 1, etc.

The second byte of data received over the SDI pin consists of write data for CA7—CA5 = 010 (write) or don't care information for CA7—CA5 = 001 (read).

The data transmitted over the SDO pin to the microprocessor during the first byte transfer is a don't care for both read and write operations. The second byte transmitted over the SDO pin consists of read data for CA7—CA5 = 001 (read) or don't care information for CA7—CA5 = 010 (write).

In order for the T7256 to recognize the identity (command/address or data) of the byte being received, it is required that the time allowed to transfer an entire instruction (time from the receipt of the first bit of the command/address byte to the last bit of the data byte) be limited to less than 300 µs. This limits the minimum SCK rate to 60 kHz. If the complete instruction is received in less than 300 µs, the T7256 accepts the instruction immediately and is ready to receive the next instruction after a 10 µs delay. If the complete instruction is not received within 300 µs, the bits received in the previous 300 µs are discarded and the interface is prepared to receive a new instruction after a 10 µs delay. In addition, a minimum 10 µs delay must exist between the command/address and data bytes.

Microprocessor Interface Description
(continued)

Timing (continued)

For microprocessors using a multiplexed data out/in pin to drive SDI and SDO (as shown in Figure 13), a read instruction to T7256 will require that the microprocessor data in/out pin be an output during the command/address byte written to T7256, and then switch to an input to read the data byte T7256 presents on the SDO pin in response to the read command. In this case, the microprocessor data in/out pin must 3-state within 1.46 μs of the final SCK rising edge of the command/address byte to ensure that there is no contention between the microprocessor data out pin and the T7256 SDO pin.

Time-Division Multiplexed (TDM) Bus Description

The TDM bus facilitates B1-, B2-, and D-channel communication between the T7256 and peripheral devices such as codecs, HDLC processors, time-slot interchangers, synchronous data interfaces, etc. The following list is a subset of the devices that can connect directly to the T7256 TDM bus:

- Lucent T7570 and T7513 Codecs
- Lucent T7270 Time-Slot Interchanger
- Lucent T7121 HDLC Formatter
- National Semiconductor*3070 Codec

The bus can be used to extract data from S/T- or U-interface receivers, process the data externally, and source data to the appropriate transmitters with the processed data. The bus can also be used to simply monitor 2B+D channel data flow within the T7256 without modifying it. The bus also supports board-level testing procedures using in-circuit techniques (see the Board-Level Testing section for more details). Upon powerup, the TDM bus is not selected. Pins 4, 7, 8, and 9 form the TDM bus when TDMEN is set to 0 (register GR2, bit 5).

The TDM bus consists of a 2.048 MHz output clock (TDMCLK), data in (TDMDI), data out (TDMDO), and a programmable frame strobe lead (FS). The frame strobe timing can be configured via the microprocessor register bits FSC and FSP in register TDR0. Data appearing and expected on the bus is controlled via the B1-, B2-, and D-channel data flow register bits (registers DFR0 and DFR1). The TDMCLK and FS outputs only become active if one or more of the TDM time slots is enabled (see register DFR1, Table 8).

Clock and Data Format

The clock and data signals for the TDM bus are TDMCLK, TDMDO, and TDMDI (see Figure 15). TDMCLK is a 2.048 MHz output clock. TDMDO is the 2B+D data output for data derived from either the S/T-interface receiver, U-interface receiver, or both. The TDMDO output driver is only active during a time slot when it is driving data off-chip; otherwise, the output driver is 3-stated (this includes the 6-bit interval in the D-channel octet). TDMDI is the 2B+D data input for data used to drive either the S/T-interface transmitter, U-interface transmitter, or both.

On both the TDMDO and TDMDI leads, six 8-bit time slots are reserved for the B1-, B2-, and D-channels associated with the S/T- and U-interfaces. The relative locations of the time slots are fixed; however, the frame strobe is programmable. The total number of time slots available within each frame strobe period is 32. During unused time slots, data on TDMDI is ignored and TDMDO is 3-stated.

Frame Strobe

The FS frame strobe is a programmable output associated with the TDM bus. FS can be configured to serve as an envelope strobe for any of the six reserved time slots available on the bus: U-interface B1, B2, and D and S/T-interface B1, B2, and D. FS can also be programmed as a 2B+D envelope for either the U-interface or S/T-interface time slots. FS can be used to directly drive a codec for voice applications or can be used to control other external devices such as HDLC controllers.

Figure 15 shows the relationship between the TDMCLK, TDMDO, and TDMDI time slots, and the FS strobe for some example programmable settings. Detailed descriptions of TDM bus interface timing are given in the Timing Characteristics section of this document.

* National Semiconductor is a registered trademark of National Semiconductor Corporation.

Time-Division Multiplexed (TDM) Bus Description (continued)

Frame Strobe (continued)

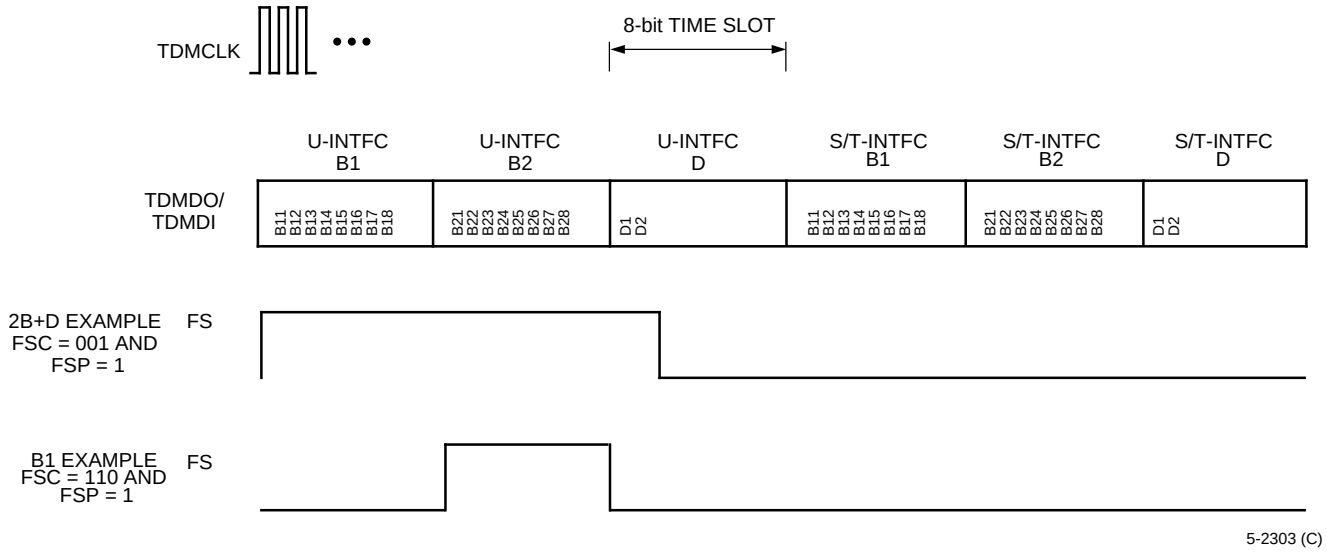

Figure 15. TDM Bus Time-Slot Format

Data Flow Matrix Description

B1-, B2-, D-Channel Routing

The T7256 supports extremely flexible B1-, B2-, and D-channel routing among major circuit blocks in order to accommodate various applications. Channel routing is controlled via the data flow control registers, DFR0 and DFR1. Figure 16 shows a block diagram of the device and the channel paths to and from the U transceiver, S/T transceiver, and TDM bus interface. Channel flow is determined by specifying the source of channel data at the three points shown in the figure: (1) U transceiver transmit input, (2) S/T transceiver transmit input, and (3) TDM bus transmit input. Channel flow at the TDM bus receive input (4) is determined, by default, from the settings at the other three points. A switch matrix within the data flow matrix block routes channels to and from the specified points.

As an example, below are the register settings required to configure the device as an NT1, with the B1 and B2 channels in both the U- to S/T- and S/T- to U-interface directions made available on the TDM bus for monitoring:

- TDMEN = 0 (enables TDM bus).
- UXB1 = 11, UXB2 = 11, UXD = 1 (routes S/T-interface receive channels to U-interface transmitter).
- SXB1 = 11, SXB2 = 11, SXD = 1 (routes U-interface receive channels to S/T-interface transmitter).
- TDMB1S = TDMB2S = 0 (brings out B1 and B2 channels in S/T- to U-interface direction to TDM bus).
- TDMDS = 1 (D channel in S/T- to U-interface direction not brought out on TDM bus).
- TDMB1U = TDMB2U = 0 (brings out B1 and B2 channels in U- to S/T-interface direction to TDM bus).
- TDMDU = 1 (D channel in U- to S/T-interface direction not brought out on TDM bus).

Refer to the Board-Level Testing section for another example of using the data flow matrix to route data.

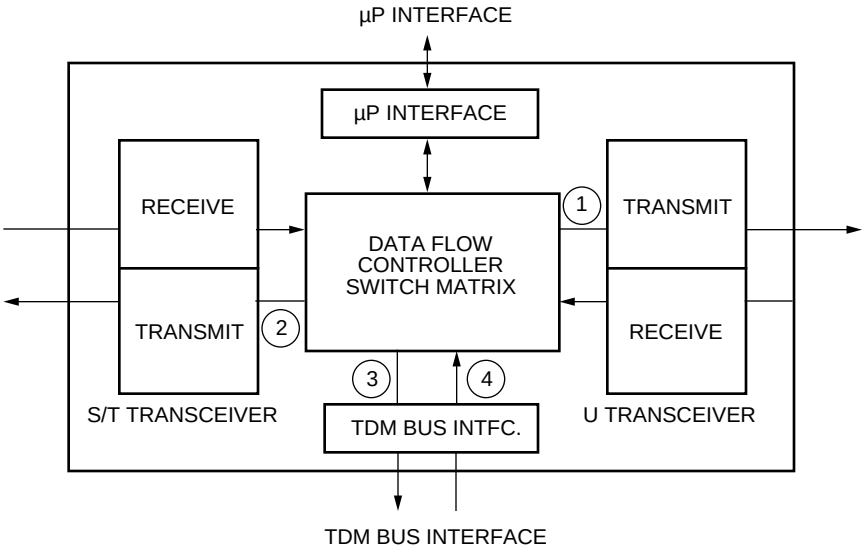

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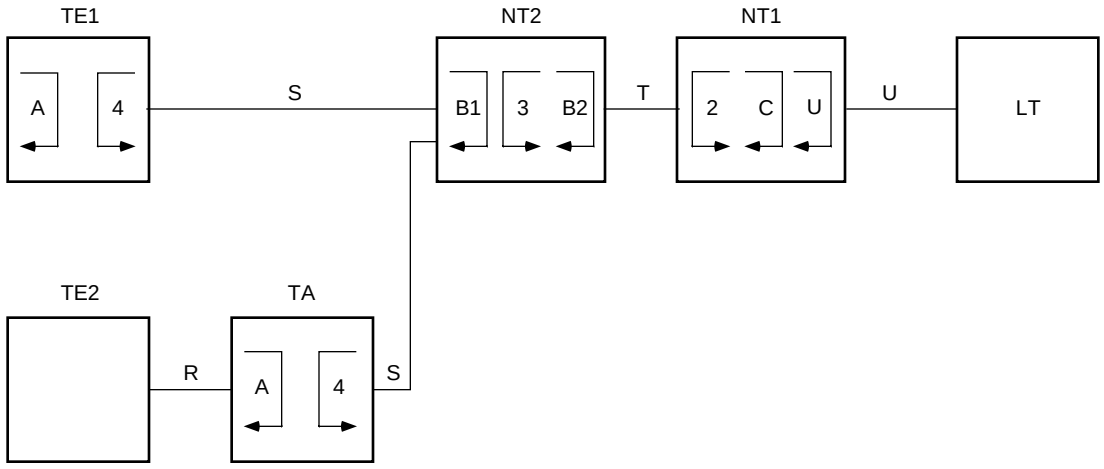
Figure 16. B1-, B2-, D-Channel Routing

Loopbacks

The figure below shows the Layer-1 loopbacks that are defined in ITU-T I.430, Appendix I and ANSI Specification T1.605, Appendix G. A complete discussion of these loopbacks is presented in ITU-T I.430, Appendix I. The T7256 supports loopbacks 2, C, and U. Loopback U is not defined in the standards, but is provided by the T7256 via register GR1, bit 0. Loopback 2 is the eoc 2B+D loopback defined in the standards.

Individual B-channel eoc loopbacks are looped upstream of the data flow matrix. Loopback C is supported via the DFR0 register, bits 4—7.

In a loopback 2, the 2B+D data is looped as close to the S/T-interface as possible (just short of the S/T-interface device pins). During this loopback, the device overrides the SXE bit to force all 0s in the echo channel and also overrides the SXB1, SXB2, SXD, UXB1, UXB2, and UXD data flow matrix bits to force a U- to S/T-interface data path. Note that the actual register bits themselves are unaffected. If AUTOEOC = 0, (register GRO, bit 4), these registers must be set up manually.



TE1 = ISDN terminal
TE2 = Non-ISDN terminal
TA = Terminal adapter
NT2 = Network termination 2
NT1 = Network termination 1
LT = Line termination

R = R reference point
S = S reference point
T = T reference point
U = U reference point

Loopback	Channel(s) Looped
2	2B+D channels
3	2B+D channels
4	B1, B2
C	B1, B2
B1 or B2	2B+D, B1, B2
A	2B+D, B1, B2

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Figure 17. Location of the Loopback Configurations (Reference ITU-T I.430 Appendix I)

Modes of Operation

To provide flexibility in the system architecture, the T7256 transceiver can operate in stand-alone mode (no microprocessor) to provide basic NT1 functionality or it can operate under microprocessor control through the serial interface to provide enhanced NT1 operation. In stand-alone mode, the T7256 automatically handles U- and S/T-interface activation, control, and maintenance according to the ANSI T1.601 and ITU-T I.430/ANSI T1.605 standards. The device is configured for this mode via internal pull-ups and pull-downs and microprocessor register default values during an external $\overline{\text{RESET}}$. Table 26 shows the transceiver control pins that may be relevant in stand-alone mode.

Table 26. Stand-Alone Mode

Pin	Symbol	Function
2	OPTOIN	Maintenance pulse streams are decoded and automatically implemented using the ANSI state machine requirements.
4	SYN8K/LBIND/FS	Performs the SYN8K or LBIND depending on the state of SYN8K_CTL/SDI (pin 12) during an external $\overline{\text{RESET}}$.
7	FTE/TDMI	Performs the FTE function. Selects the S/T-interface timing recovery mode.
8	PS2E/TDMDO	Performs the PS2E function. Controls the PS2 bit in the transmit U-interface data stream.
9	PS1E/TDMCLK	Performs the PS1E function. Controls the PS1 bit in the transmit U-interface data stream.
11	ACTMODE/$\overline{\text{INT}}$	Performs the ACTMODE function. Controls the act bit in the transmit U-interface data stream during 2B+D loopbacks.
12	SYN8K_CTL/SDI	Held high or low on powerup or RESET to control SYN8K/LBIND/FS (pin 4).
15	AUTOACT/SCK	Held high or low on powerup or RESET to control automatic activation attempt.
43	$\overline{\text{RESET}}$	Resets the device. The states of SCK, SDI, and $\overline{\text{INT}}$ are read upon exiting reset state.

In microprocessor mode, the T7256 supports all the features of stand-alone mode, plus allows enhanced control including S/Q-channel support, TDM highway access, and manual eoc and U overhead bit manipulation. The microprocessor port can be accessed at any time via the SDI, SDO, and SCK pins (see Microprocessor Interface Description and Timing Characteristics sections for details). Table 27 shows the transceiver control pins that may be relevant in microprocessor mode, or whose operation may change based on register settings.

Table 27. Microprocessor Mode

Pin	Symbol	Comment
2	OPTOIN	Controlled by microprocessor bit AUTOCTL (register GR0).
4	SYN8K/LBIND/FS	Controlled by microprocessor bit TDMEN (register GR2).
6	$\overline{\text{ILOSS}}$	Controlled by microprocessor bit AUTOCTL (register GR0).
7	FTE/TDMDI	Controlled by microprocessor bit TDMEN (register GR2).
8	PS2E/TDMDO	Controlled by microprocessor bit TDMEN (register GR2).
9	PS1E/TDMCLK	Controlled by microprocessor bit TDMEN (register GR2).
11	ACTMODE/$\overline{\text{INT}}$	Interrupt output for the microprocessor interface.
12	SYN8K_CTL/SDI	Serial data input for the microprocessor interface.
14	SDO	Serial data output for the microprocessor interface.
15	AUTOACT/SCK	Master clock input for the microprocessor interface.

STLED Description

The STLED pin is used to drive an LED and provides a visual indication of the current state of the T7256. The STLED control is typically configured to illuminate the LED when STLED is LOW. This convention will be assumed throughout this section.

Table 28 describes the four states of STLED, the list of system conditions that produce the state, and the corresponding ANSI states, as defined in ANSI T1.601-1992 (Tables C1 and C4) and ETSI ETR 080-1992 (Tables A3 and I2).

Note: The ETSI state names begin with the letters NT instead of H. Also, the ETSI state tables do not include a state NT11 because it is considered identical to state NT6. Table A3 of the ETSI standard contains the additional states NT6A, NT7A, and NT8A to describe states related to the eoc loopback 2 (2B+D loopback). The most likely ANSI state for each STLED state is shown in bold typeface below.

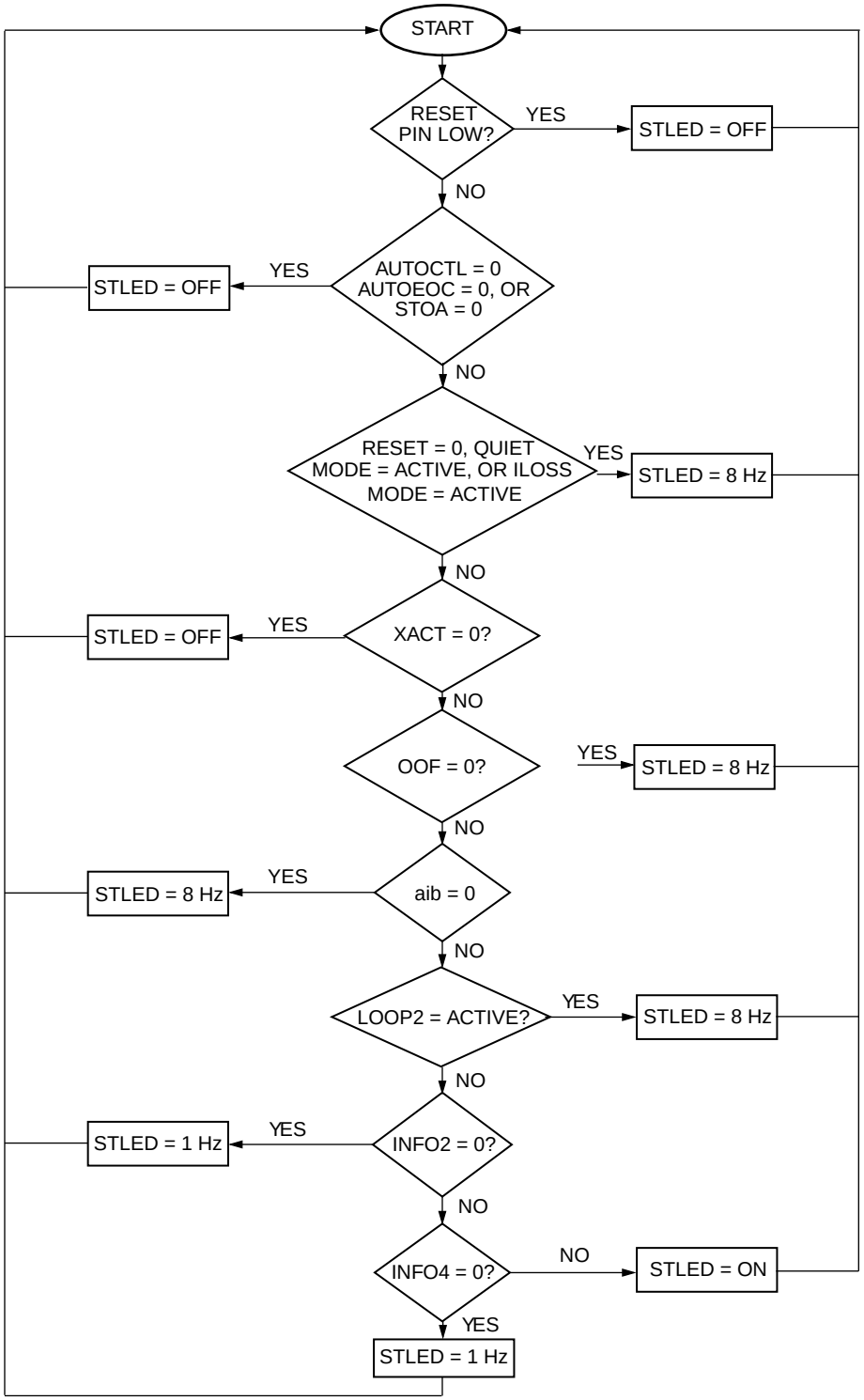
The flow chart in Figure 18 illustrates the priority of the logic signals which control the STLED pin. In the decision diamonds, those names in all capital letters denote T7256 register bit names. The RESET, AUTOCTL, AUTOEOC, and STOA are R/W bits controlled by the user via the microprocessor interface. The XACT, OOF, and AIB bits are read-only bits determined by the internal logic based on system events and can be monitored by the user via the microprocessor interface. Other names in the decision diamonds (quiet mode, ILOSS mode, Loop2, INFO 2, INFO 4) represent system conditions that cannot be directly monitored or controlled by the microprocessor interface.

Table 28. STLED States

STLED State	List of System Conditions that Can Cause STLED State	Corresponding ANSI States
High (LED off)	RESET (pin 43) = 0 AUTOCTL = 0 (register GR0, bit 3), or AUTOEOC = 0 (register GR0, bit 4), or STOA = 0 (register GR2, bit 7)	NA
	U and S/T not active	H0, **H1**, H10, H12
8 Hz Flashing	RESET = 0 (register GR0, bit 0) Quiet mode active, or ILOSS mode active	NA
	U activation attempt in progress	H2, H3, H4
	AIB = 0 (register CFR1, bit 6)	H7, **H8**
	eoc-initiated 2B+D loopback active	NT6A*, NT7A*, **NT8A***
1 Hz Flashing	U active, S/T not fully active	H6, H6(a), **H7**, H11, H8(a)†, H8(b), H8(c)
Low (LED on)	U and S/T fully active	**H8**

* These are ETSI DTR/TM-3002 states not yet defined in ANSI T1.601, although they are defined in revised ANSI tables which are currently on the living list (i.e., not yet an official part of the standards document).
† State H8(a) is most likely when U-interface bit uoa = 0.

STLED Description (continued)



5-3599d (C)

Figure 18. STLED Control Flow Diagram

eoc State Machine Description

The following list shows the eight eoc states defined in ANSI T1.601 and ETSI ETR 080. The bit pattern below represents the state of U-interface overhead bits eoci1—eoci8, respectively (see Table 2).

01010000—Operate 2B+D loopback.
01010001—Operate B1 channel loopback.
01010010—Operate B2 channel loopback.
01010011—Request corrupt CRC.
01010100—Notify of corrupted CRC.
11111111—Return to normal (default).
00000000—Hold state.
10101010—Unable to comply.

Normally, the T7256 automatically handles the eoc channel processing per the ANSI and ETSI standards. There may be some applications where manual control of the eoc channel is desired (e.g., equipment that is meant to test the eoc processing of upstream elements by writing incorrect or delayed eoc data). This can be accomplished by setting AUTOEOC = 0 (register GR0, bit 4). The eoc state change interrupt is enabled by setting EOCSCM = 0 (register UIR1, bit 0). This allows state changes in the received eoc messages (registers ECR2 and ECR3) to be indicated to the microprocessor by the assertion of UINT = 1 (register GIR0, bit 0) and EOCSC = 1 (register UIR0, bit 0). The microprocessor reads registers ECR2 and ECR3 to determine which received eoc bits changed. Then, it updates the transmit eoc values by writing registers ECR0 and ECR1 and takes appropriate action (e.g., enable a requested loopback). The total manual eoc procedure consists of the following steps:

1. Microprocessor detects $\overline{\text{INT}}$ pin going low.
2. Microprocessor reads GIR0 and determines that the UINT bit is set.
3. Microprocessor reads UIR0 and determines that the EOCSC bit is set.
4. Microprocessor reads ECR2.
5. Microprocessor reads ECR3.
6. Microprocessor interprets newly received eoc message and determines the appropriate response.
7. Microprocessor writes ECR0 based on results of step 6.
8. Microprocessor writes ECR1 based on results of step 6.

The maximum time allowed from the assertion of the $\overline{\text{INT}}$ pin (step 1) until the completion of the last write cycle to the eoc registers (step 8) is 1.5 ms.

ANSI Maintenance Control Description

The ANSI maintenance controller of the T7256 can operate in fully automatic or in fully manual mode. Automatic mode can be used in applications where autonomous control of the metallic loop termination (MLT) maintenance is desired. The MLT capability implemented with the Lucent LH1465AB and an optocoupler provides a dc signature, sealing current sink, and maintenance pulse-level translation for the testing facilities. Maintenance pulses from the U-interface MLT circuit are received by the OPTOIN pin and digitally filtered for 20 ms. The device decodes these pulses according to ANSI maintenance state machine requirements and responds to each request automatically.

For example, the T7256 will place itself in the quiet mode if six pulses are received from the MLT circuitry. Microprocessor interrupts in register MIR0 are available for tracking maintenance events if desired. Manual mode can be used in applications where an external maintenance decoder is used to drive the $\overline{\text{RESET}}$ and $\overline{\text{ILOSS}}$ pins of the T7256. In this mode, the $\overline{\text{RESET}}$ pin places the device in quiet mode and the $\overline{\text{ILOSS}}$ pin controls SN1 tone transmission. Maintenance events are not available in register MIR0 when in manual mode.

S/T-Interface Multiframing Controller Description

If an external microprocessor is available, the T7256 can provide the capability of supporting multiframing as defined in ITU-T I.430 Section 6.3.3 and ANSI T1.605 Section 7.3.3. Multiframing provides layer-1 signaling capability between the TEs and the NT in both directions through the use of extra channels referred to as the S channel for the NT-to-TE direction and the Q channel for the TE-to-NT direction (see Figure 8 in this data sheet for the location of the S and Q bits in the NT and TE frames). This signaling capability is similar to the eoc channel between the LT and NT on the U-interface. The S and Q channels exist only between the TE and NT, and there is no requirement that the NT transfers this information to the U-interface.

The requirement for multiframing capability is treated somewhat differently in ANSI T1.605, ITU-T I.430, and ETSI ETS 300 012. The ANSI standard states that the use of the S- and Q-channels is optional (Section 7.3.3). NTs that do not support these channels are not required to encode the FA and M bits as required for multiframing. TEs that do not support these channels still must provide for identification of the Q-bit positions and, if identified, must set each Q bit to a binary one. ANSI defines a set of Q-channel messages, and divides the S channel into five subchannels, defining messages for S subchannels 1 and 2 (see T1.605 Tables 8 and 9).

ITU-T I.430 contains similar requirements for the S and Q channels as T1.605, with the following exceptions:

1. There is no "far-end code violation" message for S subchannel 1 (see ITU-T I.430, Table 9).
2. S subchannel 2 is not defined.

ETSI ETS 300 012 deviates slightly from ITU-T I.430. It states that the NT1 will not provide multiframing, and therefore the FA bit from NT-to-TE must be set to zero (Table A.1, subclause A.6.3.3). An NT2, however, may optionally provide multiframing in accordance with ITU-T I.430. In either case, the TEs must provide for identification of the Q-bit positions.

The multiframing mechanism in the T7256 is controlled by the microprocessor. Normally, multiframing is disabled (the NT transmits all zeros in the FA and M bit positions and all ones in the S bit positions). To enable multiframing, set MULTIF = 0 in bit 5 of register GR0. Note that multiframing should only be enabled after the TE interface is fully active (i.e., transmitting INFO3). In order to guarantee this, the controller should implement the following procedure:

1. Initialize MULTIF = 1 (this is the default on powerup).
2. Monitor ACTR (register CFR1, bit 0) with the microprocessor to detect when the system has activated and has received INFO3. ACTR reflects the state of the U-interface act bit from the LT, and is sent by the LT in response to a reception of the act bit from the NT. The NT sets act = 1 only after receiving INFO3 on the S/T-interface; so waiting for ACTR = 1 ensures that INFO3 is being received.

   The monitoring of the ACTR bit can be interrupt-driven using the ACTSC bit in interrupt register UIR0.
3. When ACTR = 1 is detected, set MULTIF = 0 to enable multiframing.
4. Monitor for a change from XACT = 1 to XACT = 0. This can also be interrupt-driven using the ACTSC bit in interrupt register UIR0.
5. When XACT = 0 is detected, this indicates that the system has deactivated.

At this point, go back to step #1 and repeat the procedure.

S/T-Interface Multiframing Controller Description (continued)

Once multiframing has been enabled, the microprocessor can read the Q-channel data that is received and control the S subchannel data that is transmitted via registers MCR0—MCR5. The reception of a new Q-channel message is indicated to the microprocessor when interrupt bit QSC = 1 (Q-Bits State Change bit, register SIR0 bit 1). The microprocessor is informed that a new S-subchannel message may be transmitted when interrupt bit SOM = 1 (Start of Multiframe bit, register SIR0, bit 0). To enable the SOM and QSC interrupts, set SOMM = 0 and QSCM = 0 (register SIR1, bits 0 and 1). When an interrupt occurs, the global interrupt bits (register GIR0) can be read by the microprocessor to determine the source of the interrupt (register UINT, SINT, or MINT). An interrupt asserted in the SIR0 register is indicated by SINT = 1. Reading the SIR0 interrupt register clears the SOM and QSC interrupt bits in preparation for the next occurrence. It should be noted that the SOM interrupt is asserted 27 μs after the start of a multiframe and the S-subchannel bits are latched in the MCR1—MCR5 registers 3 μs prior to the start of the next multiframe. Since 30 μs (27 μs + 3 μs) of time is used by the device, the microprocessor has 4.97 ms of a total 5 ms multiframe to load the next value of S-subchannel bits. The Q-channel bits in the MCR0 register are updated every multiframe at the same time that SOM is asserted. Changes in any of the Q bits are indicated to the microprocessor by QSC = 1.

Board-Level Testing

The T7256 provides several board-level testability features. For example, the $\overline{\text{HIGHZ}}$ pin 3-states all digital outputs for bed-of-nails testing. Also, various loopbacks can be used to verify device functionality.

Stimulus/Response Testing

Data transparency of the B1, B2, and D channels can be verified by the combined use of the TDM bus and microprocessor port. Data flow within the device can be configured by the external controller through the microprocessor port, and B1-, B2-, and D-channel data can be transmitted into and received from the device via the TDM bus. Using this method, arbitrary data patterns can be used to stimulate the device and combinations of loopbacks can be exercised to help detect and isolate faults. Figure 19 illustrates this general-purpose testing configuration.

TDMDI data can be routed through the device and back to TDMDO at both the U- or S/T-interfaces. For looping at U-interface, the procedure is as follows:

- Disconnect the U-interface from the telephone network.
- Set TDMEN = 0 in register GR2, bit 5.
- Set register DFR0 to 11110101.
- Set register DFR1 to 00011110.
- Set register TDR0 as required for the desired frame strobe location and polarity.

Now, write LPBK in register GR1 to a 0. This causes the chip to enter the U-interface loopback mode. Any data entering the TDM highway on TDMDI will be looped back (with some delay) on TDMDO.

For looping of the S/T-interface, the procedure is as follows:

- Set TDMEN = 0 in register GR2, bit 5.
- Set register DFR0 to 01011111.
- Set register DFR1 to 11100001.
- Set register TDR0 as required for the desired frame strobe location and polarity.
- Set AFRST = 0 (register CFR0, bit 1) and STOA = 0 (register GR2, bit 7). This causes the S/T-interface to force activation while keeping the U-interface inactive.

Now, externally short the transmit pins to the receive pins on the S/T-interface (e.g., in Figure 21, short J2—4 to J2—3 and short J2—5 to J2—6). This causes a loopback of the S/T-interface that results in TDMDI data being looped to TDMDO.

S/T-Interface Multiframing Controller Description (continued)

Stimulus/Response Testing (continued)

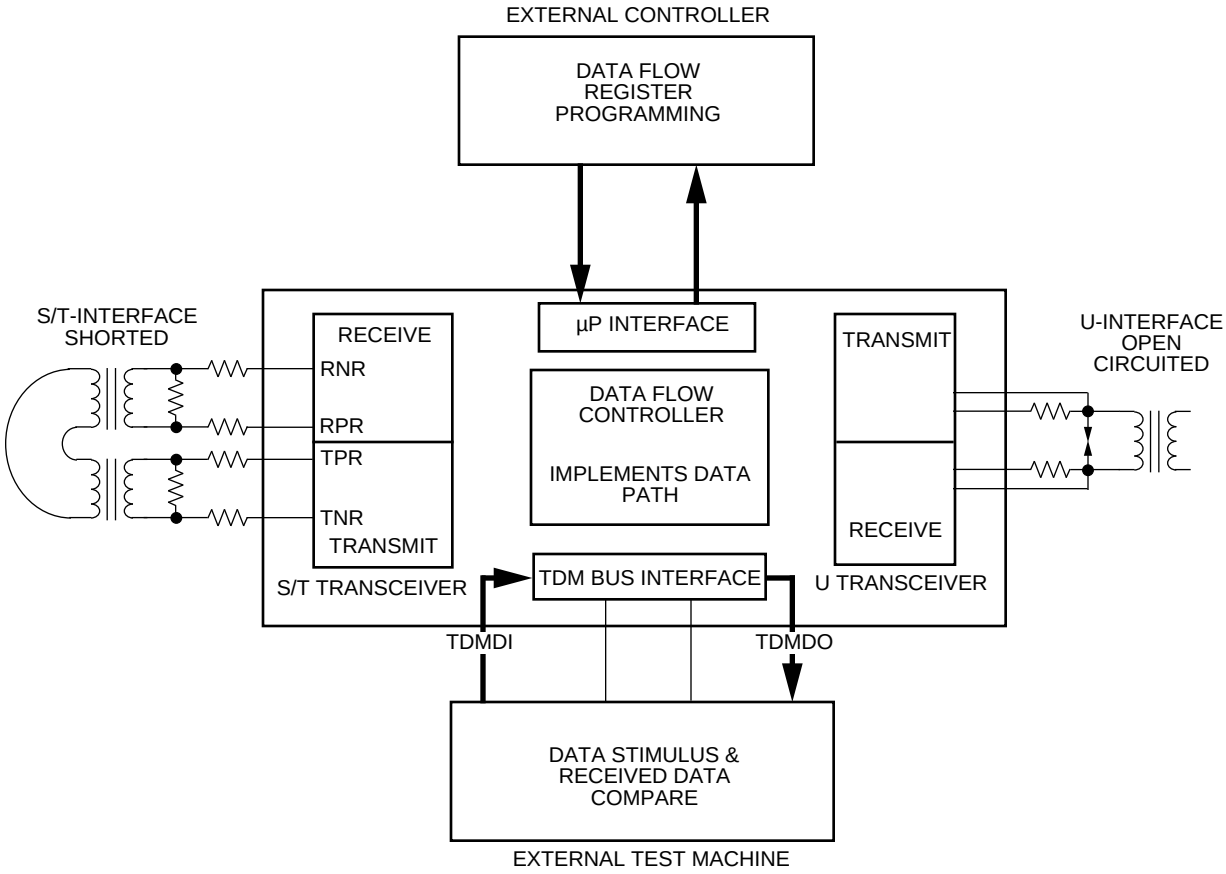


Figure 19. External Stimulus/Response Configuration

Application Briefs

T7256 Reference Circuit

A reference circuit illustrating the T7256 in a stand-alone NT1 application is shown in Figures 20 and 21. This depicts a complete stand-alone NT1 design with the exception of power supply circuitry and power status monitoring circuitry. A bill of materials for the schematic is shown in Table 29. Note that specific applications may vary depending on individual requirements.

U-Interface

The U-Interface attaches to the board at RJ-45 connector J1 (see Figure 20). F1 and VR2 provide overcurrent and overvoltage protection, respectively. These two devices in combination with transformer T1 provide protection levels required by FCC Part 68 and UL* 1459. For an in-depth discussion of protection issues, the following application notes are helpful.

1. “Overvoltage Protection of Solid-State Subscriber Loop Circuits,” Lucent Analog Line Card Components Data Book (CA94-007ALC) 800-372-2447.
2. Protection of Telecommunications Customer Premesis Equipment, Raychem† Corporation, 415-361-6900.

C16 is a 1.0 μF dc blocking capacitor that is required per ANSI T1.601, Section 7.5.2.3. The 250 V rating of C16 is governed by the maximum breakdown voltage of VR2, since the capacitor must not break down before VR2. The resistance of R13 (21 Ω) and F1 (12 Ω) provides a total line-side resistance of 33 Ω, which is required when using the Lucent 2754H2 transformer (see the note at the end of Table 29 for information on R13 values when using other transformers).

On the device side of the U-interface transformer, VR1 provides secondary overvoltage protection of 6.8 V. Optional capacitors C13 and C14 provide common-mode noise suppression for applications that are required to operate in the presence of high common-mode noise. R6 and R7 provide the necessary external hybrid resistors.

S/T-Interface

The S/T-interface attaches to the board at RJ-45 connector J2 (see Figure 21). L1 is a high-frequency common-mode choke used to minimize EMI. R24 and R25 are 100 Ω terminations required by ITU I.430 Section 8.4. Jumper-selectable resistors R26 and R27 provide for a 50 Ω termination option instead of the standard 100 Ω termination. This is useful in configurations where none of the TEs have terminating resistors. Dual-transformer T2 has a standard footprint that can accept ISDN transformers from several vendors. On the device side of the S/T-interface transformer, D2—D11 and VR3—4 provide overvoltage protection for the device pins. R20—23 provide current limiting for cases where one or more of the protection diodes conducts due to an overvoltage condition. Capacitor C17 provides suppression of common-mode noise that might otherwise be introduced onto the receiver input pins, effectively increasing the receiver's CMRR. Note that the S/T transformer must have a center tap on the device side in order to use this scheme. R16 and R17 in combination with R20 and R21, respectively, provide the 121 Ω of resistance required by the T7256 on each transmitter output pin. R18 and R19 are the 10 kΩ, 10% resistors required on the receiver input pins.

MLT Circuit

The metallic loop termination (MLT) circuit (U3 and related components in Figure 20) provides a dc termination for the loop per ANSI T1.601, Section 7.5. R14 and R15 are power resistors used to sink current during overvoltage fault conditions. The optoisolater (U2) provides signal isolation and voltage translation of the signaling pulses used for NT maintenance modes, per T1.601, Section 6.5. The T7256 interprets these pulses via an internal ANSI maintenance state machine, and responds accordingly. For applications outside North America, the MLT circuit is not required.

Status LED

D1 in Figure 20 is an LED that is controlled by the STLED pin of the T7256 and indicates the status of the device (activating, out-of-sync, etc.). Table 28 and Figure 18 of this data sheet details the possible states of the STLED pin and the meaning of each state.

* UL is a registered trademark of Underwriters Laboratories, Inc.
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Application Briefs (continued)

T7256 Reference Circuit (continued)

Power Status Leads

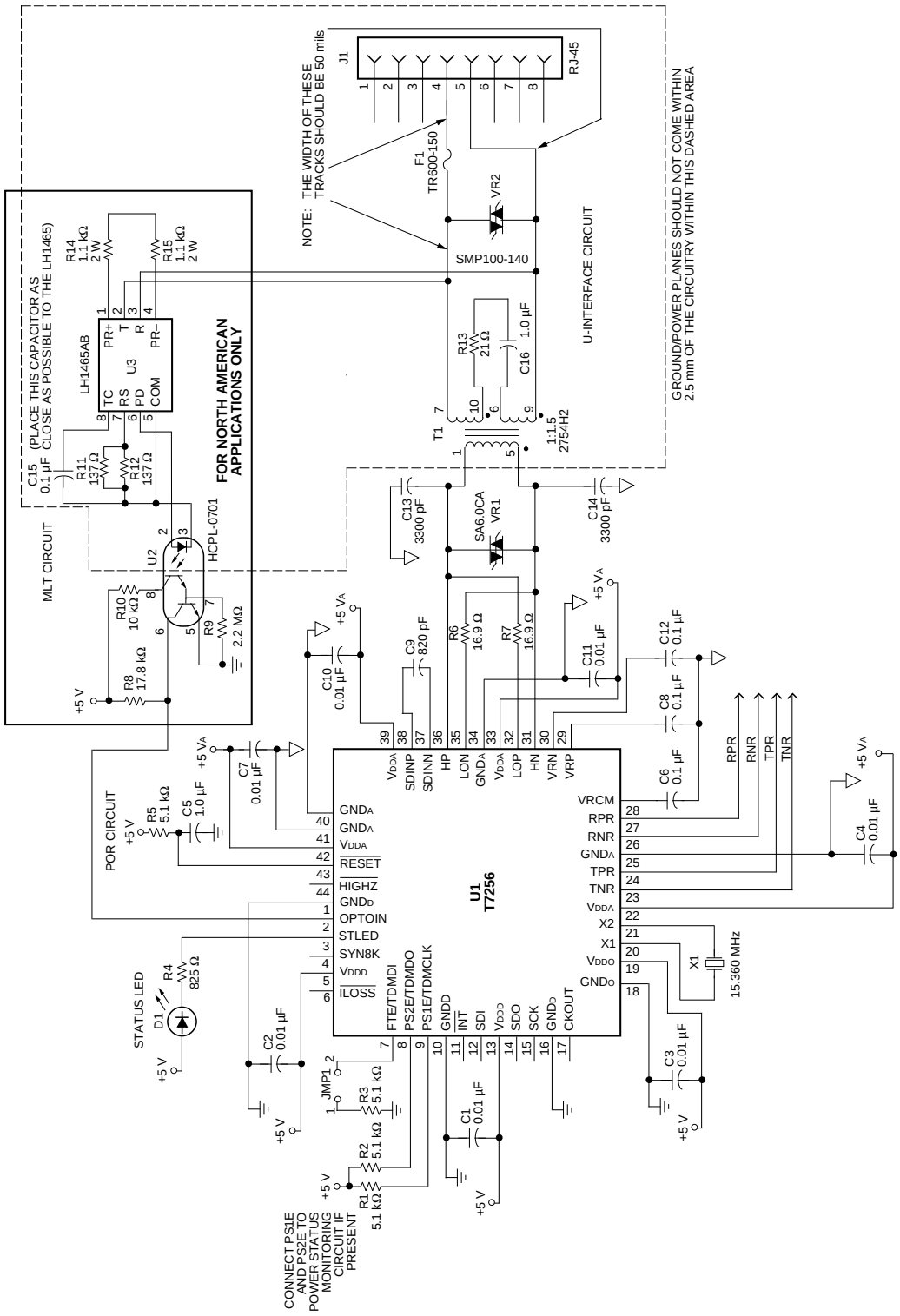
ANSI T1.601 Section 8.2.4 defines U-interface NT power status bits ps1 and ps2. These bits are transmitted across the U-Interface via the U maintenance channel. On the T7256, these bits are controlled by pins 8 and 9 (PS2E and PS1E). When the TDM highway is used (NT1+ or TA modes), the ps1/ps2 bits are controlled by internal registers that are written by an external microprocessor. An NT1 typically has circuitry that monitors the status of the power supply and sets ps1 and ps2 accordingly. In general, power status monitoring circuitry is dependent on various system parameters and requirements, and must be designed based on the specific application's requirements. For this reason, there is no power status monitoring circuitry shown in this design. Instead, pull-ups R1 and R2 in Figure 20 are provided to force a default indication of primary and secondary power good status.

Fixed/Adaptive Timing Control

As detailed in Table 1, pin 7 of the T7256 controls whether the S/T-interface will use fixed or adaptive timing recovery. When there is no connection to pin 7, an internal 100K pull-up holds the pin high, which causes the chip to default to adaptive timing recovery. JMP1 is provided (see Figure 20) to change the timing recovery mode to fixed timing by pulling pin 7 down through a 5.1 kΩ resistor.

Application Briefs (continued)

T7256 Reference Circuit (continued)

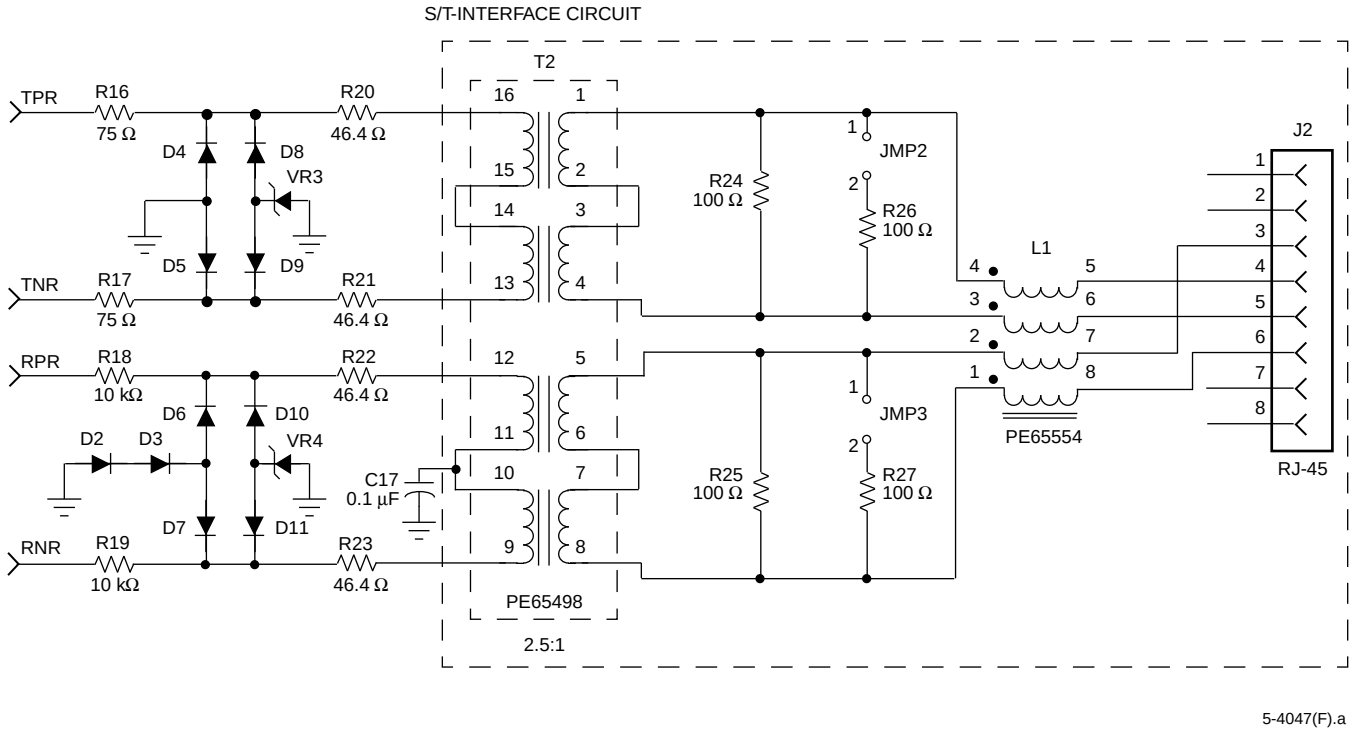


5-4048(C).d

Figure 20. T7256 Stand-Alone Reference Circuit-A

Application Briefs (continued)

T7256 Reference Circuit (continued)



5-4047(F).a

Note: See Question/Answer section, #35.

Figure 21. T7256 Stand-Alone Reference Circuit-B

Application Briefs (continued)

T7256 Reference Circuit (continued)

Table 29. T7256 Reference Schematic Parts List

Reference Designator	Description	Source	Part #
C[1—4, 7, 10, 11]	Ceramic Chip Capacitor, 0.01 µF, 10%, 50 V, X7R	Kemet[1]	C1206C103K5RAC
C5	Tantalum Chip Capacitor, 1.0 µF, 10%, 16 V	Kemet	T491A105K016AS
C[6, 8, 12, 17]	Ceramic Chip Capacitor, 0.1 µF, 10%, 50 V, X7R	Kemet	C1206C104K5RAC
C9	Ceramic Chip Capacitor, 820 pF, 5%, 50 V, NPO	Kemet	C0805C821J5GAC
C[13, 14]	Ceramic Chip Capacitor, 3300 pF, 10%, 50 V, X7R	Kemet	C1206C332F5RAC
C15	Polyester Capacitor, 0.1 µF, 63 V, 10% **Note:** Insulation resistance of this part must be >2 GΩ.	Philips [2]	2222 370 12104
C16	Capacitor, 1.0 µF, 250 V, 10% Alternate: Philips 2222 373 41105	Vitramon[3], via TMI (rep) (215) 830-8500	VJ9253Y105KXPM
D1	Green Surface-mount LED	Hewlett Packard [4]	HSMG-C650
D[2—11]	SMT Switching Diode	Philips	PMLL4151
F1	Overcurrent Protector (Polyswitch[5]) Alternate: BEL Fuse[6] MJS 1.00A, (201) 432-0463 See Note at the end of this table.	Raychem (415) 361-6900	TR600-150
J1, J2	RJ-45 8-pin Modular Jack (standard height)	Molex[7]	15-43-8588
JMP1—3	Two-position Header with Shorting Jumper	Multiple	
L1	High-frequency Common-mode Choke Alternate: Pulse PE-65854 (surface mount)	Pulse Engineering[8] (619) 674-8100	PE65554
R[1—3, 5]	SMC Resistor, 5.1 kΩ, 1/8 W, 5%	Dale[9]	CRCW1206512J
R4	SMC Resistor, 825 kΩ, 1/8 W, 1%	Dale	CRCW12068250F
R6, 7	SMC Resistor, 16.9 kΩ, 1/8 W, 1%	Dale	CRCW120616R9F
R8	SMC Resistor, 17.8 kΩ, 1/8 W, 1%	Dale	CRCW12061783F
R9	SMC Resistor, 2.2 MΩ, 1/8 W, 5%	Dale	CRCW1206225J
R[10, 18, 19]	SMC Resistor, 10 kΩ, 1/8 W, 5%	Dale	CRCW1206103J
[R11, 12]	SMC Resistor, 137 Ω, 1/8 W, 1%	Dale	CRCW12061370F
R13	SMC Resistor, 21.0 Ω, 1 W, 1%	Dale	WSC-1

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Application Briefs (continued)

T7256 Reference Circuit (continued)

Table 29. T7256 Reference Schematic Parts List (continued)

Reference Designator	Description	Source	Part #
R14, 15	SMC Resistor, 1.1 kΩ, 2 W, 5%	Dale	WSC-2
R16, 17	SMC Resistor, 75 Ω, 1/8 W, 1%	Dale	CRCW120675R0F
R20—23	SMC Resistor, 46.4 Ω, 1/8 W, 1%	Dale	CRCW120646R4F
R24—27	SMC Resistor, 100 Ω, 1/8 W, 1%	Dale	CRCW12061000F
T1	ISDN U-interface Transformer	Lucent	2754H2 Alternates (See footnote at the end of this table.): Lucent 2754K2 (1500 Vrms breakdown) Lucent 2809A (for EN60950 compliance) Valor [10] PT4084 (619) 537-2500 Midcom 671-7759 (605) 886-4385
T2	ISDN S-Interface Dual Transformer	Pulse Engineering (619) 674-8100	PE65498 Alternates: Pulse Engineering PE-68988 (single transformer, reinforced insulation) Valor PT5048 (619) 537-2500 (pin compatible) Advanced Power Components[11], LTD. APC40498 (pin compatible) APC2050S (single transformer, reinforced insulation) US: Terry Manton, Inc. (rep), (201) 447-8821 Europe: 44-634-290588 Vacuumschmelze[12] (VAC) (single transformer, reinforced insulation) T60403-L4097-X017-80 U.S.: (908) 494-3530 Europe: 49-6181-38-2026
U1	Single-chip NT1 IC, 44-pin PLCC	Lucent	T7256
U2	Optocoupler	Hewlett Packard	HCPL-0701
U3	ISDN dc Termination IC	Lucent	LH1465AB

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Application Briefs (continued)

T7256 Reference Circuit (continued)

Table 29. T7256 Reference Schematic Parts List (continued)

Reference Designator	Description	Source	Part #
VR1	Transient Voltage Suppressor	SGS-Thomson[13]	SM6T6V8CA Alternates: Motorola SA6.5CA, P6KE6.8CA, P6KE7.5CA
VR2	Transient Voltage Suppressor	SGS-Thomson	SMP100-140 Alternate: Teccor[14] P1602AB (972) 580-7777
VR[3, 4]	Transient Voltage Suppressor, 6.8 V	Motorola	1.5SMC6.8AT3 Alternate: Motorola 1N6269A
X1	15.36 Crystal	Saronix (415) 856-6900	SRX5144 Alternates: MTRON[15] 4044-001 (605) 665-9321 2B Elettronica S.D.L. TP0648 39-6-6622432

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Note: The Lucent 2754K2 and the Valor PT4084 have different winding resistances than the Lucent 2754H2, and therefore require a change to the line-side resistor (R15). In addition, if the Bel Fuse is used in place of the Raychem TR600-150 PTC at location F1 (which will sacrifice the resettable protection that the PTC provides), the line-side resistors must be adjusted to compensate for reduced resistance due to the removal of the PTC (12 Ω). The following table lists the necessary resistor values for these cases. Note that R15 is specified at 1%. This is due to the fact that the values were chosen from standard 1% resistor tables. When a PTC is used, the overall tolerance will be greater than 1%. This is acceptable, as long as the total line-side resistance is kept as close as possible to the ideal value. See Question and Answer section, #6 for more details.

Table 30. Line-Side Resistor Requirements

Transformer	When Raychem TR600-150 Is Used	When Bel Fuse Is Used
	R13	R13
Lucent 2754H2	21 Ω	33.2 Ω
Lucent 2754K2	15.4 Ω	27.4 Ω
Lucent 2809A	9.53	21.5
Valor PT4084	0 Ω	10.7 Ω

Application Briefs (continued)

Using the T7256 in a Combination TE/TA Environment (NT1/TA)

The T7256 can be used in applications requiring NT1 and terminal adapter (TA) functionality (NT1/TA). This application brief describes an NT1 that supports conventional POTS (plain old telephone service) as well as ISDN service. A block diagram of this application is shown in Figure 22. The microprocessor (µP) performs the following functions:

- Runs the ISDN call control stack (Q.931).
- Controls the HDLC formatter for performing the LAP-D protocol on the D channel.
- Controls the register configuration of the T7256.
- Controls the POTS circuitry (i.e., translates signaling such as off-hook into the correct call-control message, translates DTMF digits from a DTMF receiver, controls the ringer, etc.).
- Controls access to the B and D channels on the TDM highway for the codecs and HDLC formatter, respectively.

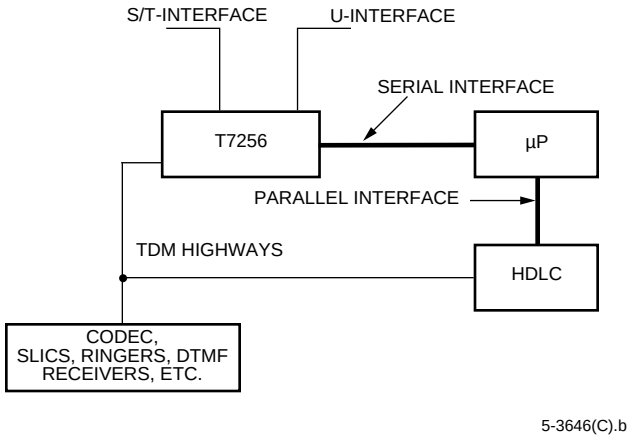


Figure 22. T7256 NT1/TA Application Block Diagram

T7256 Configuration

When the T7256 is used in the NT1/TA application, the TDM highway must be used in conjunction with the data flow control registers (DFR0 and DFR1) to control the B- and D-channel data flow. Following is a suggested procedure for properly configuring the T7256 in this application.

1. Set TDMEN = 0 (register GR2, bit 5) to enable the TDM highway. In this case, the ps1/ps2 functions must be controlled via the microprocessor (register GR1, bits 1 and 2) because pins 8 and 9 are used for TDMDO and TDMCLK. Note that when the TDM highway is enabled, TDMCLK and FS will not become active until at least one of the bits 2—7 in register DFR1 are enabled (set to 0).
2. The downstream D channel must be monitored by the TA circuit for call-control messages from the switch. This is accomplished via the TDM bus by setting TDMDU = 0 (register DFR1, bit 7). The upstream D channel (which is normally sourced from the S/T-interface) must be sourced by the POTS HDLC controller when one of the following events occurs:

   a. The switch notifies the POTS circuit of an incoming call request via a downstream D-channel message.

   b. A local POTS phone goes off-hook (i.e., a call is being placed).

   In either of these cases, the POTS HDLC controller must take control of the D-channel in order to complete the call setup for the appropriate POTS phone. This is accomplished by setting UXD = 0 (register DFR1, bit 0).
3. The frame strobe pulse envelope and polarity must be configured for correct operation with the HDLC controller and codecs using register TDR0. For example, to set an active-high FS pulse that envelopes the U-interface B1 channel data (see Figure 18), register TDR0 bits 0—3 should be set to all 1s (default on powerup). This setting can be used with the Lucent T7121 HDLC controller because the T7121 can be programmed for any time slot and bit offset from the rising or falling edge of FS.

   The codecs may require the FS pulse be in a particular position relative to the B-channel data. For example, if two Lucent T7513B codecs are used in variable timing mode in this application (one for each POTS line), each would require an FS pulse that envelopes the appropriate B-channel data. The configuration described in the preceding paragraph is adequate for allowing either codec to source or sink B1 channel data to the U-interface, but there is no separate FS pulse available for the B2 channel data. Therefore, external glue logic is necessary to generate an FS pulse for the B2 channel data.

Application Briefs (continued)

T7256 Configuration (continued)

4. The upstream B-channel source will be either the S/T-interface (if a TE has a call active) or the TDM highway (if an analog phone has a call active). Each B channel can be sourced from the TDM highway or the S/T-interface independent of the other B channel. The source of the upstream B channels is controlled by register DFR0, bits 1 and 0 (for B1) and bits 3 and 2 (for B2). These bits must be controlled dynamically depending on whether an analog phone or a TE is requesting the B channel. A suggested approach to B-channel control is to default to the S/T-interface (i.e., the TEs) and switch to the TDM highway when it is determined that a call is being placed/received on the analog phone (i.e., after call setup has been established via the D channel as described in item #2, above). For example, if a B1 call is placed on an analog phone, DFR0, bit 1 must be changed from a 1 to a 0 to allow the POTS circuitry to source the upstream B1 channel data. All the other bits in DFR0 remain set to 1.

   Register DFR1, bits 5 and 6 control B1 and B2 channel data (respectively) from the U-interface to the TDM highway. It may be necessary to keep the B1 and B2 time slots disabled (3-stated) when the analog phones are not in use to keep the codecs quiet. A 5.1 kΩ pull-up resistor on the TDMDO pin should be used to ensure that the TDM data is all 1s. Some codecs can be quieted by disabling the codec frame strobe signal.

5. When the TDM highway is enabled by setting TDMEN = 0, TDMCLK and FS will not become active until at least one of the bits 2—7 in register DFR1 are enabled (set to 0).

D-Channel Priority

One issue in this application concerns the D-channel priority mechanism because the D channel must be shared between the TA circuitry and any TEs that are connected to the S/T-interface. Below is an approach for implementing the D-channel priority mechanism.

1. Normally, the D channels from the TE should be routed directly through to the switch. Thus, the NT1/TA simply looks like an NT1, passing data directly between the S/T- and U-interfaces.
2. If a POTS phone needs to access the D channel (due to an incoming or outgoing call request as described in item #2 of the previous section), it should set SXE = 0 (register GR2, bit 3). This will cause any TEs currently accessing the D channel to relinquish the D channel due to a collision detection (i.e., the TE's outgoing D bit will differ from its incoming E bit).
3. The POTS controller should delay 1.5 ms, then set UXD = 0 (register DFR1, bit 0) to allow local control of the upstream D channel. Then it can assume control of the D channel and begin to transmit and receive call control packets via the HDLC formatter. The 1.5 ms delay guarantees that at least seven 1s will be transmitted in the upstream D-channel data stream before the local controller sends the opening flag of its first packet. Thus, if the last bit that a TE transmitted on the D channel (before SXE = 0 was set) was a 0, the transmission of at least seven 1s will cause an abort HDLC message to be recognized by the switch, which properly notifies the switch that the TE that was in the process of sending a packet aborted that transmission.
4. When the POTS controller has completed its D-channel message, it should set SXE = 1 to relinquish control of the D channel.

More intelligence can be built into the D-channel algorithm if desired. For example, since the downstream D-channel messages are always being monitored, it is possible to determine whether a call setup to a TE is in progress. If so, the POTS controller can hold off a local TA call request until the TE call setup is complete. In addition, after each D-channel access, the POTS controller can allow adequate time for a TE to exchange call control messages with a switch before taking over the D channel again. The timing for these sequences would be managed by the TA controller software.

Application Briefs (continued)

D-Channel Priority (continued)

Activation Control

Because there is no guarantee that a TE will be connected in this application, the local microprocessor must be provisioned to perform a layer-1 activation request as follows:

1. Write AUTOACT = 0 (register GR0, bit 6) to initiate start-up on the U-interface. This results in XACT = 1 (register CFR1, bit 1). The AUTOACT bit will be set to a 1 automatically after the start-up request is made. This permits another activation attempt by writing AUTOACT = 0 again (without first writing it back to 1) if the start-up attempt fails.

   A switch-initiated start-up is detected by the local microprocessor when XACT = 1 (register CFR1, bit 1). This event can be indicated by an interrupt (INT, pin 11) by writing the interrupt mask bit OUSCM = 0 (register UIR1, bit 3) and calling the interrupt routine when UINT = 1 (register GIR0, bit 0). The OUSC interrupt (register UIR0, bit 3) indicates a bit change in either CFR1 or CFR2. Read these registers to determine which of these bits has changed since the last read.

   In either of the above cases, it may be necessary to set the sai[1:0] bits in register GR1 to 01. This has the effect of indicating S/T-interface activity to the switch even when no TE is attached. Some switches require the reception of sai = 1 in order to properly establish layer 1 transparency.

2. Look for XACT = 0 or OOF = 1 (register CFR1, bits 1 and 2). These events can be indicated by an interrupt INT, pin 11) in a similar manner as described in (1) above.

3. If XACT = 0, the start-up attempt has failed and appropriate action should be taken depending on the system requirements (it may be desirable to attempt another start-up).

4. If OOF = 1, U-interface synchronization is complete. Set ACTT = 1 (register GR1, bit 4). This will set the upstream ACT = 1 on the U-interface independent of actions on the S/T-interface. It may be desirable to delay several tens of milliseconds between detecting OOF and setting ACTT = 1 to allow the S/T-interface time to activate if there is a TE present. If this is the case, the upstream act bit will automatically be set, but manually setting ACTT = 1 is permissible.

5. After setting ACTT = 1, wait for ACTR = 1 (register CFR1, bit 0). This event can be indicated by an interrupt (INT, pin 11) in a similar manner as described in (1) above. The reception of ACTR = 1, enables U-interface transparency in the upstream direction, so it is not necessary to do so explicitly by setting XPCY = 0 (register GR1, bit 5).

At this point, layer-1 activation is complete. Note that the above steps 1—5 occur automatically if there is a TE connected or if the LT starts up and sends an eoc loopback-2 request (2B+D loopback). However, having the microprocessor perform these steps ensures layer 1 activation independently of the presence of a TE. After layer 1 activation is complete, the XACT bit (register CFR1, bit 1) can be monitored for a state change to 0. This provides an indication to the local microprocessor that layer 1 has deactivated. When this occurs, set ACTT = 0 (register GR1, bit 4) to prepare for the next start-up attempt.

Application Briefs (continued)

Interfacing the T7256 to the Motorola 68302

Introduction

The Motorola MC68302 integrated multiprotocol processor (IMP) contains a 68000 core integrated with a flexible communications architecture. It has three serial communications controllers (SCCs) that can be independently programmed to support the following protocols and physical interfaces.

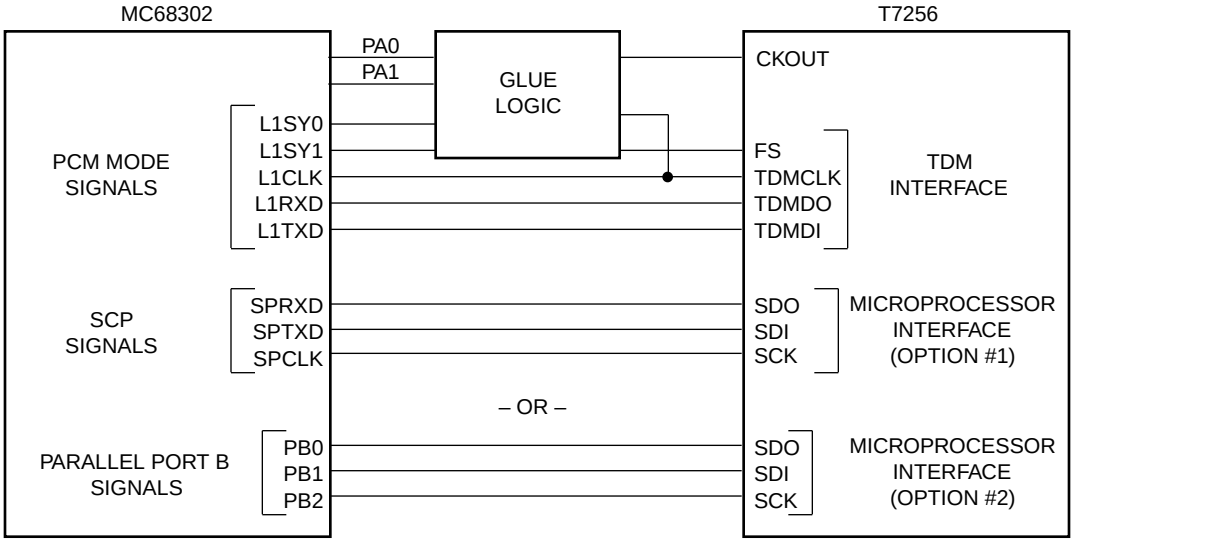
Table 31. Motorola MC68302 SCC Options

Protocols	Physical Interfaces
HDLC/SDLC	Motorola IDL
UART	GCI
BISYNC	PCM Highway
DDCMP	NMSI (nonmultiplexed serial interface)
V.110 Rate Adaption	—
Transparent	—

The PCM interface option of the SCCs is appropriate for interfacing to the T7256 TDM highway to provide access to B- and D-channel data. The SCCs allow ISDN B-channel transfers that support applications such as V.120 rate adaption (synchronous HDLC mode) and voice storage (transparent mode). However, the T7256 does not output all signals that are required to connect directly to the SCC and some external circuitry (e.g., an EPLD) is required in order to interface the T7256 TDM highway to the MC68302 SCC PCM highway. Users of the Motorola MC68360 should note that the T7256 can be connected directly to the PCM highway of the MC68360 without the use of any such glue logic.

The MC68302 contains a 3-wire serial interface called an SCP (serial communications port). The SCP may be directly connected to the T7256 serial microprocessor interface to control the T7256 register configuration. The MC68302 also has programmable ports A (16 bits) and B (12 bits) that are bit-wise programmable and can be used as an alternative to the SCP to drive the T7256 serial microprocessor interface.

Figure 23 illustrates the interface connections between the MC68302 and the T7256. A discussion of the TDM and microprocessor interfaces follows.



5-4046(C).b

Figure 23. MC68302 to T7256 Interface Diagram

Application Briefs (continued)

Interfacing the T7256 to the Motorola 68302 (continued)

Using the Motorola MC68302 PCM Mode to Interface to the T7256 TDM Highway

In PCM mode, any number of the MC68302 internal SCCs can be multiplexed to support a TDM type of interface (see Section 4.4.3, PCM Highway Mode in the MC68302 Data Book). The SCCs in PCM mode require a data-in lead (L1RXD) for receive data, a data-out lead (L1TXD) for transmit data, and a common receive and transmit data clock to clock data into and out of the SCCs (L1CLK). These signals are directly compatible with the T7256 TDM highway. In addition, the PCM-mode SCCs require two data synchronization signals, L1SY1 and L1SY0, which route specific TDM time slots to the SCCs. These signals are not directly supported by T7256, and some glue logic is required to generate them.

The L1SY0/1 signal pair combinations are used to select between PCM channels 1, 2, and 3 (or to select no PCM channel), where each channel is routed to one of the SCCs (routing is controlled by software). They can be set up in an envelope mode such that the they are active for N bits, where N determines the number of bits in a time slot. Values of N equal to 7 and 8 are required to interface to the T7256 TDM highway B-channel time slots (for 56 kbits/s or 64 kbits/s data, respectively). A value of N equal to 2 is required to interface to the D-channel time slots. Table 32 lists the L1SY0/1 channel assignments for the T7256-to-MC68302 interface circuit.

Table 32. PCM Channel Selection

L1SY0	L1SY1	Channel Accessed
0	0	None
1	0	PCM Channel 1 (U-interface B1 channel)
0	1	PCM Channel 2 (U-interface B2 channel)
1	1	PCM Channel 3 (U-interface D channel)

The interface circuit can be easily implemented in a programmable logic device. An example is presented here using the Altera* EPM7032 EPLD. The EPM7032 was selected for this example because it is used on the SCNT1 Family Reference Design Board (SCNT1-RDB) to implement this same function, so the design files presented here have already been proven on an actual hardware platform (consult Appendix B, SCNT1 Family Reference Design Board Hardware User Manual, MN96-011ISDN, for detailed design information). The design uses 43% of the EPM7032, which leaves a large portion of the device available for other glue functions that may be required. If no other system glue is required, the design can be ported to a smaller, cheaper EPLD.

The inputs to the circuit from the T7256 are FS, TDM-CLK, and CKOUT (CKOUT must be programmed to a frequency of 10 MHz via register GR0, bits 2—1 in order for the circuit to operate properly). The inputs to the circuit from the 68302 are PA0 and PA1 (parallel port A, bits 0 and 1), which are used to control the 7-bit envelope mode on the B1 and B2 channels. These two signals are called 7BIT_B1 and 7BIT_B2 in the design files and, when set high, enable the 7-bit time-slot mode (otherwise, 8-bit time-slot mode is active). The outputs from the circuit are L1SY0 and L1SY1, which drive the corresponding signals on the 68302.

The design was implemented using the Altera MAX+plus II development system. Figures 24, 25, 26, and 27 illustrate the circuit schematic, Altera high-level design language (AHDL) files, and the timing diagrams for the design.

* Altera is a registered trademark of Altera Corporation.

Application Briefs (continued)

Interfacing the T7256 to the Motorola 68302 (continued)

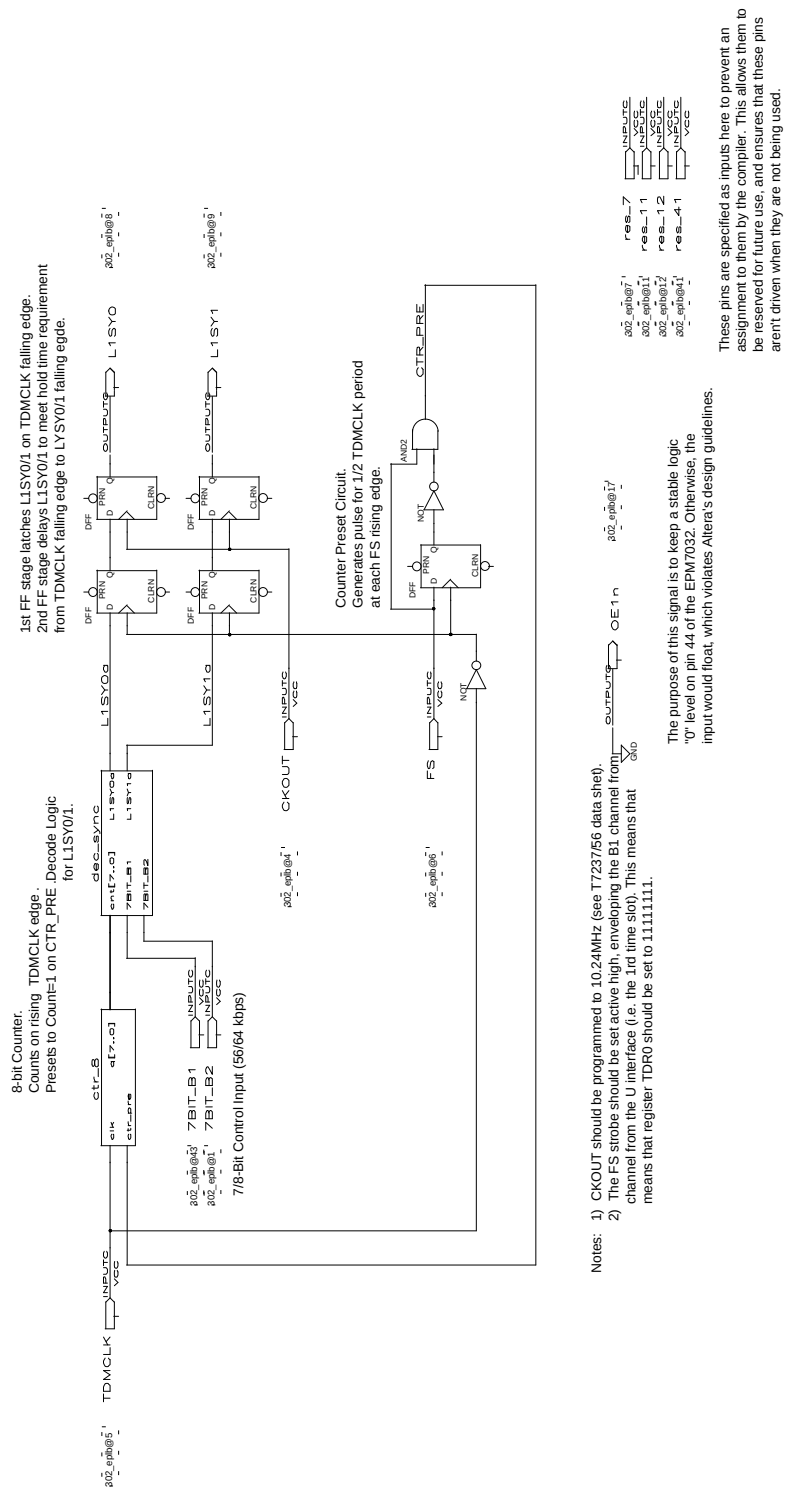


Figure 24. SCNT1-RDB EPLD Schematic

Application Briefs (continued)

Interfacing the T7256 to the Motorola 68302 (continued)

8-Bit Up Counter (T-FF Based)

8-bit up-counter with async active-high CLR.

Note: CTR_PRE sets count = 1.

```
SUBDESIGN ctr_8 (
  clk,
  ctr_pre      :INPUT;
  q[7..0]      :OUTPUT;
)
VARIABLE
  count[7..0] :DFF;
BEGIN
  count[].clk = clk;
  count[7..1].clrn = !ctr_pre;        % counter gets preset to count = 1 on clr %
  count[0].prn = !ctr_pre;
  count[] = count[] + 1;
  q[] = count[];
END;
```

Sync Decode Logic

Decode logic for frame sync. Generates L1SY0/1 logic and shifts them left by 1/2 bit relative to FS.

```
SUBDESIGN dec_sync (
  cnt[7..0],
  7BIT_B1,
  7BIT_B2      INPUT;
  L1SY0a,
  L1SY1a       OUTPUT
)
BEGIN
     L1SY0a=        (cnt[] == 0) # (cnt[] == 1) # (cnt[] == 2)
                 # (cnt[] == 3) # (cnt[] == 4) # (cnt[] == 5)
                 # (cnt[] == 6) # ((cnt[] == 7) & !7BIT_B1)
                 # (cnt[] == 16) # (cnt[] == 17);
     L1SY1a=        (cnt[] == 8)  # (cnt[] == 9) # (cnt[] == 10)
                 # (cnt[] == 11) # (cnt[] == 12) # (cnt[] == 13)
                 # (cnt[] == 14) # ((cnt[] == 15) & !7BIT_B2)
                 # (cnt[] == 16) # (cnt[] == 17);
END;
```

Figure 25. SCNT1-RDB EPLD AHDL Design Files

Application Briefs (continued)

Interfacing the T7256 to the Motorola 68302 (continued)

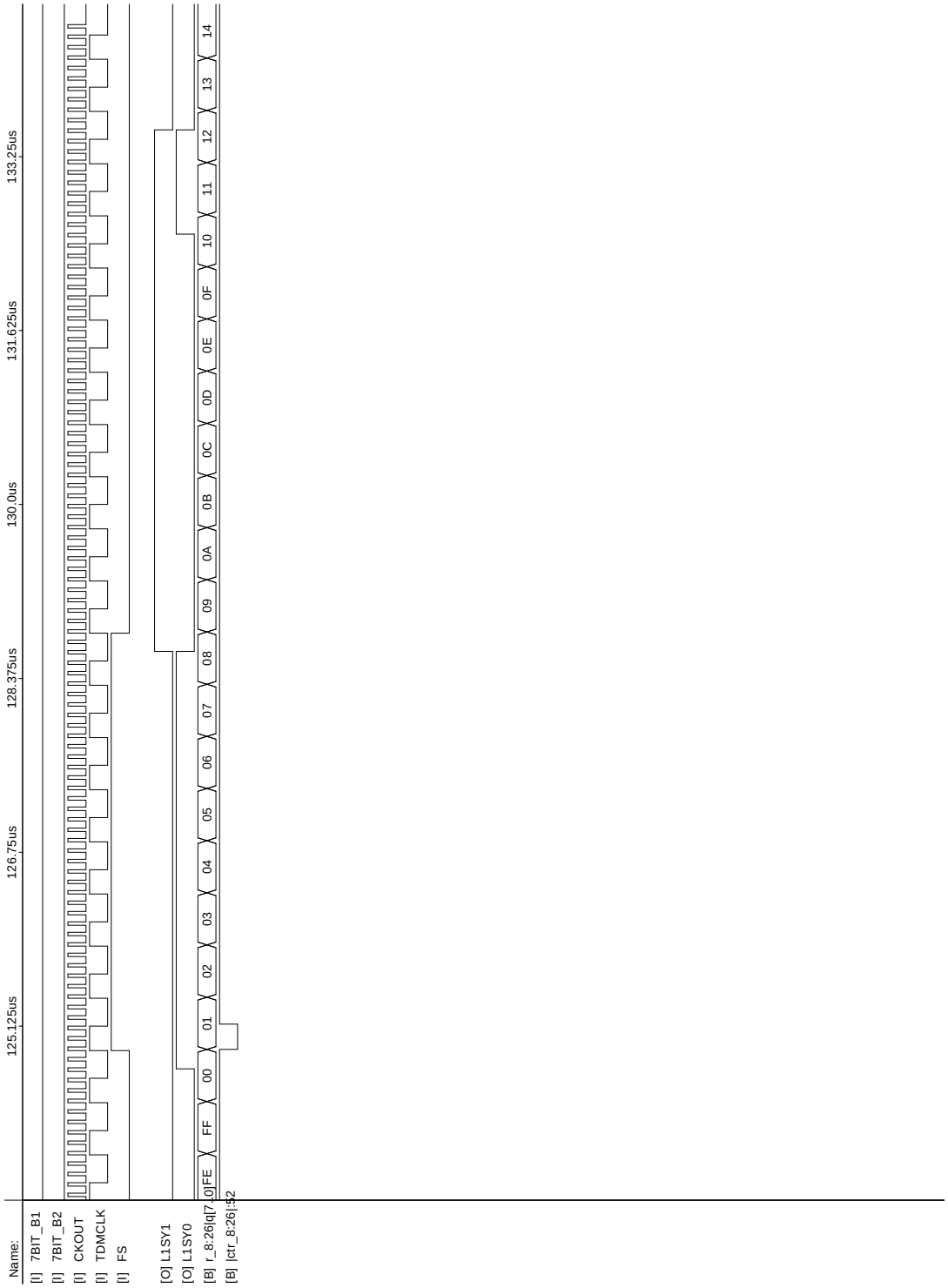


Figure 26. SCNT1-RDB EPLD Timing (8-bit)

Application Briefs (continued)

Interfacing the T7256 to the Motorola 68302 (continued)

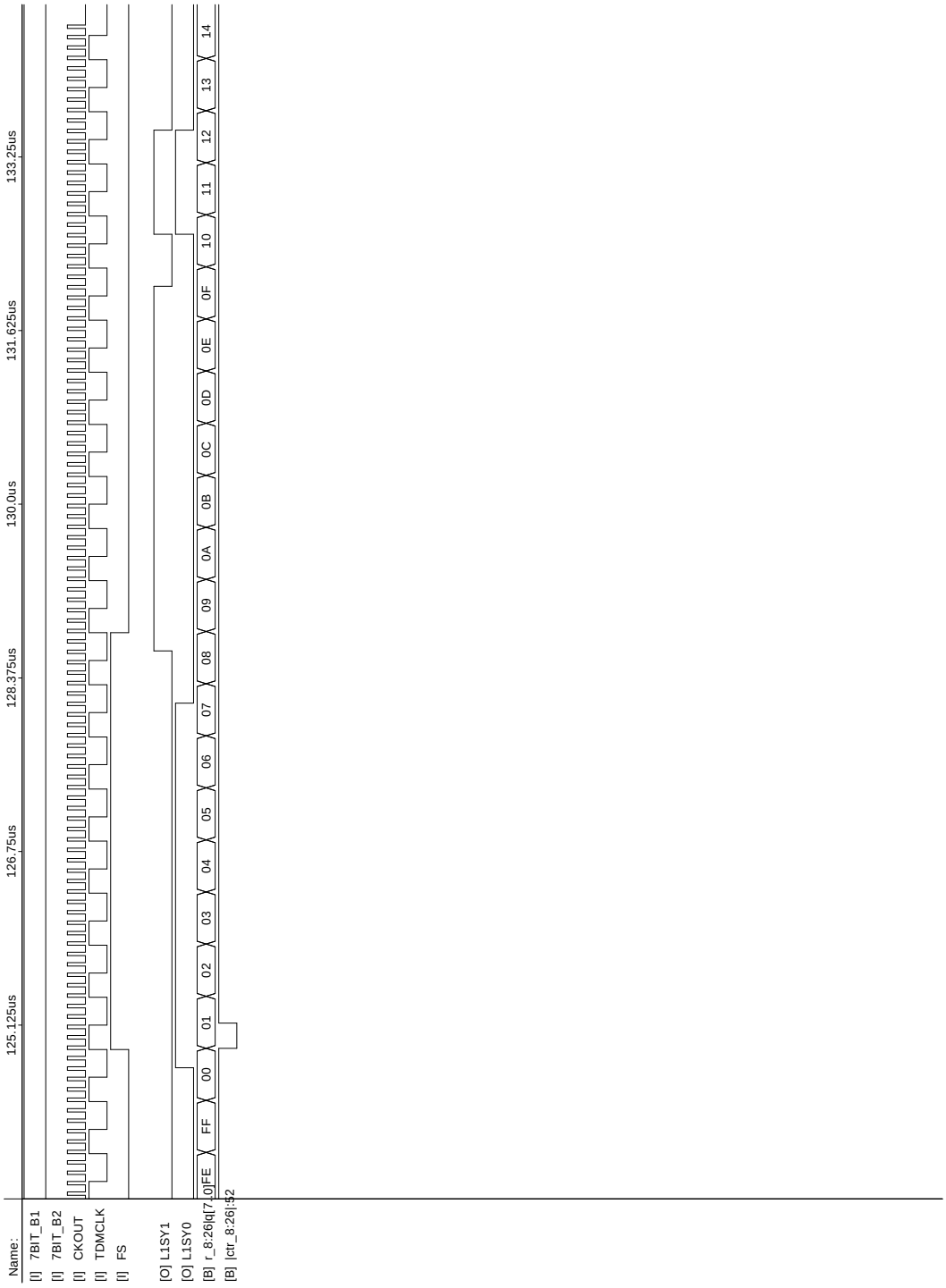


Figure 27. SCNT1-RDB EPLD Timing (7-bit)

Application Briefs (continued)

Interfacing the T7256 to the Motorola 68302 (continued)

To enable the TDMCLK and FS signals and generate the FS signal in the proper time slot, the following T7256 register bits must be programmed:

Register GR2, bit 5 (TDMEN) = 0.

Register DFR1, bits 7:5 (TDMDU, TDMB2U, TDMB1U) = 000.

Register TDR0, bit 3:0 (FSP, FSC[2:0]) = 1111 (default).

Detailed information on T7256 activation control and configuration of the microprocessor registers can be found in the Application Briefs, Using the T7256 in a Combination NT1/TA Environment section in this document.

As an example of programming the MC68302 SIMODE register bits for PCM mode, the following settings will enable PCM mode and route the B2 channel to SCC1, the B1 channel to SCC2, and the D channel to SCC3. The ISDN signaling protocol stack (Q.931 and LAPD) would communicate via SCC3, and any higher-layer data protocol such as V.120 or V.110 would communicate via SCC1 and SCC2, as required.

SETZ = 0, SYNC = 1, SDIAG1:SDIAG0 = 00, SDC2 = 0, SDC1 = 0, B2RB:B2RA = 01, B1RB:B1RA = 10, DRB:DRA = 11, MSC3 = 0, MSC2 = 0, and MS1:MS0 = 01.

T7256 Serial Microprocessor Interface Support

The MC68302 SCP interface is a 3-wire serial interface that may be directly connected to the T7256 microprocessor interface. The SCP interface is implemented in the MC68302 hardware, and the only software interaction required is to set up the SCP interface, to transmit/receive SCP bytes, and to respond to SCP events (the SCP interrupt).

There are several points to note when interfacing the T7256 to the MC68302 microprocessor interface.

1. Register bit CI (clock invert) in the MC68302 SPMODE register should be set to 1 to invert the MC68302 SCP clock in order to meet the T7256 microprocessor timing specifications.
2. The MC68302 SCP clock, SPCLK, may be programmed to run as high as 4.096 MHz. The minimum rate of the SCP SPCLK, assuming the slower 16.384 MHz version of the MC68302 with a maximum divide-down prescale of 64, is 256 kHz. The minimum and maximum rates of the T7256 SCK are 60 kHz and 960 kHz, respectively, and care should be taken to ensure that the MC68302 is programmed to a clock rate that is compatible with T7256.
3. Every T7256 access consists of two 8-bit transfers, where the first is the command/address byte and the second is the data byte. There must be a delay of 10 µs between every 8-bit register access to meet the T7256 microprocessor timing specifications. The back-to-back byte transmit delay of the MC68302 SCP at the slowest SPCLK rate of 256 kHz can be anywhere from two to eight clocks, or 7.8 µs to 31.25 µs. To ensure that the 10 µs delay requirement is met, the MC68302 software must not send the second byte of the 2-byte sequence for at least 10 µs after the SCP processor clears the DONE bit in the SCP transmit/receive buffer descriptor (refer to Section 4.6.2 of the Motorola MC68302 User Manual for further information).
4. During 2-byte data transfer over the MC68302 SCP, 8 bits will be shifted into the SCP receive buffer for every 8 bits shifted out. For a T7256 read, the first byte in the receive buffer should be discarded and the second byte will contain the read data from the T7256. For a write, both bytes should be discarded from the SCP receive buffer.
5. The T7256 microprocessor interface lacks an enable pin to permit multiple device communication on a single MC68302 SCP. In these applications, the T7256 microprocessor interface can be enabled/disabled using a microprocessor parallel port pin to control a 3-state buffer at SCK (pin 15).

An alternative method of interfacing the MC68302 to the T7256 microprocessor interface is to use three MC68302 parallel port pins (e.g., PB0, PB1, and PB2 in Figure 23) programmed as outputs and supporting the T7256 microprocessor interface in software. The timing of the SCK, SDI, and SDO signals can be implemented in software with a minimum amount of code.

Application Briefs (continued)

Available Tools for Evaluation of the T7256

SCNT1 Family Reference Design Board

The SCNT1 Family Reference Design Board (SCNT1-RDB) is a printed-circuit board platform that provides an example implementation of an ISDN NT1 circuit based on the Lucent T7256 or T7234. In addition, it can be configured as an ISDN terminal adapter (TA) based on the Lucent T7237. With the T7234 or T7256 installed, it is a fully functional NT1, with the exception of power status monitoring circuitry (which can be added by the user). It can be used as an evaluation platform as well as a reference design. With the T7237 installed, it can be used to develop U-interface terminal adapter applications (external control hardware is required in this case). For complete information, consult the SCNT1 Family Reference Design Board Hardware User Manual (document # MN96-011ISDN).

SPEC_V2 Test Board

The SPEC_V2 is a circuit board that connects to a T7256 or T7237-based product in order to provide various control and status operations. The SPEC_V2 board is controlled via an RS-232 terminal interface (DB-25 connector J2). A PC running a standard terminal emulation package can be connected to J2 via one of the PC's COM ports.

The SPEC_V2 allows the operations in Table 33 to be performed on the unit under test (i.e., the SPEC_UUT).

Table 33. SPEC_V2 Functions

Command	Function
rd ['hex-addr']	Read SCNT1 register(s)
mon ['hex-addr'] [/s]	Continuously monitor SCNT1 register(s)
wr 'hex-addr' 'hex-data'	Write SCNT1 register
spulse 'pol/mag'	Enable single pulse mode
eye	Enable EYE pattern mode
srst	Perform a h/w reset of SCNT1
help	Display a list of available commands.

Note: Optional command-line parameters are shown in brackets.

Following is an explanation of the command syntax for each command. Command-line parameters enclosed in brackets [ ] represent optional parameters.

rd ['hex-addr']

Read SCNT1 register(s).

The **rd** command, when entered with no command line parameters, reads and displays each internal register address and the corresponding contents in the following format, where the top row (beginning with A:) displays the hexadecimal address and the bottom row (beginning with D:) displays the register data corresponding to the address directly above it. For example, if each register contained its address, the resulting display would appear as follows:

```
A:00 01 02 03 04 05 06 07 08 09 0a 0b 0c 0d
0e 0f 10 11 12 13 14 15 16 17 18 19
D:00 01 02 03 04 05 06 07 08 09 0a 0b 0c 0d
0e 0f 10 11 12 13 14 15 16 17 18 19
```

When the **rd** command is entered with the optional command line parameter representing the hexadecimal address of the desired register to read (for example, **"rd c"**), the resulting display is as follows:

```
Addr: 0x0c   Data: 0xff
```

mon ['hex-addr'] [/s]

Continuously monitor SCNT1 register(s).

This command is identical to the rd command, with the following exception—the address and data of the specified register (or all registers if no 'hex-addr' parameter is specified) are continuously read and updated on the terminal screen. In addition, there is an optional parameter, /s, that can be specified. This causes each successive register refresh to appear on a new line (as opposed to the same line). Thus, the terminal display will scroll as the values are updated. This can be useful for terminal emulators that have a scrollback buffer, since a history of the register contents and changes is available on screen.

To exit this mode, press the ESC key.

wr 'hex-addr' 'hex-data'

Write SCNT1 register.

This command allows 'hex-data' to be written to the register at 'hex-addr'. For example, to write the value 0xef to register address 0x0a, the following would be entered.

wr a ef

Application Briefs (continued)

Available Tools for Evaluation of the T7256 (continued)

spulse 'pol/mag'

Enable single pulse mode.

Single pulse mode is for performing pulse template tests on the U- and S/T-interfaces. For the U-interface, the chip is placed into a mode in which it periodically (every 125 µs) outputs a single isolated pulse whose magnitude and polarity depend on the 'pol/mag' command line parameter, which can be +1, +3, –1, and –3. For the S/T-interface, the I.430-defined Loop C is set up so that S/T test equipment such as the Siemens* K1403 can transmit a fixed pattern and expect to receive the same pattern (this is a common way of performing pulse template tests on the S/T-interface).

Prior to activating this mode, the U- and S/T-interfaces should be disconnected from the SCNT1-based product until after the mode is entered, at which point they may be reconnected.

eye

Enable EYE pattern mode.

This mode is for viewing the eye pattern of the received signal at the input to the slicer. This gives a good indication of the receiver performance and shows the effect of impairments such as NEXT. The eye pattern signal is available at BNC connector J5.

srst

Performs a h/w reset of SCNT1.

help

Displays a list of available commands.

Using the SPEC_V2

To use the SPEC_V2, connect it to a terminal emulator configured for 9600 baud, 8-bit, 1 stop bit, no parity, full duplex, and XON/XOFF flow control. A +5 V supply should be connected to connector J3 using the screw-terminal block provided with the board (the +5 V lead gets connected to pin 1 of J3, and the return lead gets connected to pin 2). When power is applied, LED D1 should illuminate to indicate that there is power to the board. Once connected to the UUT, the SPEC_V2 should not be powered down, since it may cause the UUT to malfunction.

SPEC_V2-to-UUT Interface Description

The unit under test (UUT) is connected to J1 on the SPEC_V2 board via one of the two supplied ribbon cable assemblies. If the SCNT1-RDB board is being used as the UUT, the ribbon cable assembly with the 16-pin ribbon header at both ends can be used and will be connected to the SCNT1-RDB at connector J3 (the general-purpose interface). If such a connector is not available on the UUT, the ribbon cable assembly with a 16-pin dual header on one end and a PLCC-44 IC clip on the other can be used to clip directly to the SCNT1 chip on the UUT. If the SCNT1 is socketed or otherwise not accessible with an IC clip, some other method of access to the required signals must be provided.

The J1 connector pinouts are shown in Table 34. The J1 signals are assigned such that a straight 16-pin ribbon cable assembly can be connected directly between J1 of the SPEC_V2 and the general-purpose interface, J3, of the T7237/56 Reference Design Board (SCNT1-RDB). In this case, the signal CKOUT should be routed through a BNC cable for isolation and shielding. Signals that are provided on J3 of the SCNT1-RDB but not used by the SPEC_V2 are noted in the last column. If an alternative cabling arrangement is used, note that the signals in the Signal Name column must be provided at the UUT interface point unless otherwise noted (GND_D need be provided only once).

* Siemens is a registered trademark of Siemens Aktiengesellschaft.

Application Briefs (continued)

Available Tools for Evaluation of the T7256 (continued)

IMPORTANT NOTE: In order to use the SPEC_V2 with your product, you must adhere to the following guidelines:

- Make sure none of the signals in the Signal Name column of Table 34 are hardwired to V_{CC} or GND (with the exception of GND_D). If you need to tie any of these signals high or low, do it through a 5.1 kΩ resistor.
- Make sure that circuitry on your board that is driving any of the Signal Name signals can be disabled (3-stated, open collector output driver turned off, or signal trace cut, if necessary) when using the SPEC_V2.

Table 34. SPEC_V2 Interface Connector Pinouts

J1 Pin #	Signal Name	SPEC_V2 Input/ Output	T7237/ 56 Pin #	Notes
1	GND_D	X	16	—
2	—	—	—	Connects to V_{DDD} when interfacing to SCNT1-RDB.
3	GND_D	X	10	—
4	—	—	—	—
5	SCK	O	15	—
6	CKOUT	I	17	—
7	$\overline{INT}$	I	11	—
8	SDO	I	14	—
9	SDI	O	12	—
10	PS1E	I	9	PS1E becomes an output from T7237/56 in test mode.
11	—	—	—	Connects to PS2E (T7237/56 pin #8) when interfacing to SCNT1_RDB.
12	TDMDI	I	7	—
13	SYN8K	O	4	—
14	—	—	—	Connects to $\overline{ILOSS}$ (T7237/56 pin #6) when interfacing to SCNT1-RDB.
15	$\overline{RESET}$	O	43	Recommended but not mandatory.*
16	$\overline{HIGHZ}$	I	44	$\overline{HIGHZ}$ becomes an output from T7237/56 in test mode.

* If $\overline{RESET}$ is not connected, the T7237/56 will not be RESET when exiting mode 2 or 3. If this is the case, the UUT must be powered down to get the SCNT1 out of test mode.

Application Briefs (continued)

Available Tools for Evaluation of the T7256 (continued)

Resetting SCNT1

The SPEC_V2 board has a push-button RESET switch (S1) that may be used to RESET the 8751 microcontroller on the SPEC_V2. Asserting RESET will restart the SPEC_V2 firmware. Upon power-on or RESET, the SPEC_V2 displays the opening screen on the terminal, and it appears as follows:

Lucent Technologies
SPEC_V2 Control Software, V 1.0, 6/2/96
(type "help" (lower case) for a list of commands)

At this point, any of the commands in Table 33 may be entered.

If the current test mode is either single pulse or eye pattern mode, the microcontroller will reset the SCNT1 when exiting that mode. This is necessary because the only way to exit these test modes is by resetting SCNT1 or cycling the power. The reset is accomplished by pulling the SCNT1 $\overline{\text{RESET}}$ line (pin 43) low. Note that this requires that any device on the UUT that drives that $\overline{\text{RESET}}$ pin must have an open-drain or 3-statable type of output. If $\overline{\text{RESET}}$ cannot be pulled low due to device contention on the UUT, the UUT must be powered down to get the SCNT1 out of test mode.

Notes on Single Pulse Mode

Note that, when a single pulse is output on the U-interface, the following will be observed: approximately 25 ms after the rising edge of a single positive pulse, a small positive glitch will occur. This is more pronounced on +1 pulses than on +3 pulses, where it is hardly detectable. The cause of the glitch is well understood and was thoroughly investigated during the chip development to ensure that it causes no harm under normal operating conditions.

The explanation is as follows. The transmit sigma-delta modulator in the SCNT1 is RESET whenever a transition from nonzero data to zero data occurs. It was designed this way for ease of production testing, so that the sigma-delta is always initialized to a known state. This resetting is what causes the glitch. In normal operation, the nonzero to zero case will never occur, except when the transceiver is going from an active state to RESET. In this case, there is a control signal that grounds the input to the line driver to force it to transmit 0 V (i.e., forces it into a low-impedance state—this feature grew out of the ANSI requirements), so the sigma-delta modulator has no effect in this case.

Thus, the glitch never occurs in normal operation and should be ignored when observing the pulse output. This has been confirmed independently at Bellcore using their test bed that digitizes the chip output under normal operation, and then reconstructs the pulse shape using DSP filtering techniques.

Absolute Maximum Ratings

Stresses in excess of the absolute maximum ratings can cause permanent or latent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operation sections of the data sheet. Exposure to absolute maximum ratings for extended periods can adversely affect device reliability.

External leads can be soldered safely at temperatures up to 300 °C.

Parameter	Symbol	Min	Max	Unit
dc Supply Voltage Range	V_{DD}	–0.5	6.5	V
Power Dissipation (package limit)	P_D	—	800	mW
Storage Temperature	T_{stg}	–55	150	°C
Voltage (any pin) with Respect to GND	—	–0.5	6.5	V

Handling Precautions

Although protection circuitry has been designed into this device, proper precautions should be taken to avoid exposure to electrostatic discharge (ESD) during handling and mounting. Lucent employs a human-body model (HBM) and charged-device model (CDM) for ESD-susceptibility testing and protection design evaluation. ESD voltage thresholds are dependent on the circuit parameters used to defined the model. No industry-wide standard has been adopted for the CDM. However, a standard HBM (resistance = 1500 Ω, capacitance = 100 pF) is widely used and, therefore, can be used for comparison. The HBM ESD threshold presented here was obtained by using these circuit parameters:

ESD Threshold Voltage	
Device	**Voltage**
T7256-ML2	>1000
T7256-1ML	>1000

Recommended Operating Conditions

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Ambient Temperature	T_A	V_{DD} = 5 V ± 5%	–40	—	85	°C
Any V_{DD}	V_{DD}	—	4.75	5.0	5.25	V
GND to GND	V_{GG}	—	–10	—	10	mV

Electrical Characteristics

All characteristics are for a 15.36 MHz crystal, 135 Ω line load, random 2B+D data, T_A = –40 °C to +85 °C, V_{DD} = 5 V ± 5%, GND = 0 V, and output capacitance = 50 pF.

Power Consumption

Table 35. Power Consumption

Parameter	Test Conditions	Min	Typ	Max	Unit
Power Consumption	Operating, random data	—	270	350	mW
Power Consumption	Powerdown mode	—	35	50	mW

Pin Electrical Characteristics

Table 36. Digital dc Characteristics (Over Operating Ranges)

Parameter	Symbol	Test Conditions	Min	Max	Unit
Input Leakage Current:					
Low	I_{ILPU}	V_{IL} = 0 (pins 2, 6, 7, 11, 44)	–52	–10	µA
High	I_{IHPU}	V_{IH} = V_{DD} (pins 2, 6, 7, 11, 44)	—	–10	µA
Low	I_{ILPD}	V_{IL} = 0 (pins 8, 9, 12, 15, 43)	–10	—	µA
High	I_{IHPD}	V_{IH} = V_{DD} (pins 8, 9, 12, 15, 43)	–10	–52	µA
Input Voltage:					
Low	V_{IL}	All pins except 2, 6, 43	—	0.8	V
High	V_{IH}	All pins except 2, 6, 43	2.0	—	V
Low-to-high Threshold	V_{ILS}	Pin 43	V_{DD} – 0.5	—	V
High-to-low Threshold	V_{IHS}	Pin 43	—	0.5	V
Low	V_{ILC}	Pins 2, 6	—	0.2 V_{DD}	V
High	V_{IHC}	Pins 2, 6	0.7 V_{DD}	—	V
Output Leakage Current:					
Low	I_{OZL}	V_{OL} = 0, Pin 44 = 0 (pins 3, 14)	—	10	µA
High	I_{OZH}	V_{OH} = V_{DD}, Pin 44 = 0 (pins 3, 14)	–10	—	µA
Low	I_{OZLPU}	V_{OL} = 0, Pin 44 = 0 (pin 11)	–52	–10	µA
High	I_{OZHPU}	V_{OH} = V_{DD}, Pin 44 = 0 (pin 11)	—	10	µA
Low	I_{OZLPD}	V_{OL} = 0, Pin 44 = 0 (pins 4, 8, 9, 17)	–10	—	µA
High	I_{OZHPD}	V_{OH} = V_{DD}, Pin 44 = 0 (pins 4, 8, 9, 17)	10	52	µA
Output Voltage:					
Low, TTL	V_{OL}	I_{OL} = 4.5 mA (pin 3)	—	0.4	V
		I_{OL} = 19.5 mA (pins 4, 9)	—	0.4	V
		I_{OL} = 8.2 mA (pins 8, 17)	—	0.4	V
		I_{OL} = 6.5 mA (pin 14)	—	0.4	V
		I_{OL} = 3.3 mA (pin 11)	—	0.4	V
High, TTL	V_{OH}	I_{OH} = 32.2 mA (pins 4, 9)	2.4	—	V
		I_{OH} = 13.5 mA (pins 8, 17)	2.4	—	V
		I_{OH} = 10.4 mA (pins 3, 14)	2.4	—	V
		I_{OH} = 5.1 mA (pin 11)	2.4	—	V

Electrical Characteristics (continued)

S/T-Interface Receiver Common-Mode Rejection

Table 37. S/T-Interface Receiver Common-Mode Rejection

Parameter	Symbol	Specifications	Unit
Common-mode Rejection (at device pins)	CMR	400	mV

Crystal Characteristics

Table 38. Fundamental Mode Crystal Characteristics

These are the characteristics of a parallel resonant crystal for meeting the ±100 ppm requirements of T1.601 for NT operation. The parasitic capacitance of the PC board to which the T7256 crystal is mounted must be kept within the range of 0.6 pF ± 0.4 pF.

Parameter	Symbol	Test Conditions	Specifications	Unit
Center Frequency	F_O	With 25.0 pF of loading	15.36	MHz
Tolerance Including Calibration, Temperature Stability, and Aging	TOL	—	±70	ppm
Drive Level	DL	Maximum	0.5	mW
Series Resistance	R_S	Maximum	20	Ω
Shunt Capacitance	C_O	—	3.0 ± 20%	pF
Motional Capacitance	C_M	—	12 ± 20%	fF

Table 39. Internal PLL Characteristics

Parameter	Test Conditions	Min	Typ	Max	Unit
Total Pull Range	—	±250	—	—	ppm
Jitter Transfer Function	–3 dB point (NT), 18 kft 26 AWG	—	5*	—	Hz
Jitter Peaking	1.5 Hz typical	—	1.0*	—	dB

* Set by digital PLL; therefore, variations track U-interface line rate.

Timing Characteristics

T_A = –40 °C to +85 °C, V_{DD} = 5 V ± 5%, GND = 0 V, crystal frequency = 15.36 MHz.
For Figure 28, assume register TDR0 = F9, DFR1 = 1E, and DFR0 = F5.

Table 40. TDM Bus Timing

Ref	Parameter	Min	Typ	Max	Unit
1	FS Pulse Frequency	—	8	—	kHz
2	TDMCLK to FS High	—	—	15	ns
3	TDMCLK to FS Low	—	—	15	ns
4	TDMCLK Frequency	—	2.048	—	MHz
5	TDMCLK Width High	162	230	293	ns
6	TDMCLK Width Low	195	260	326	ns
7	Receive (TDMDI) Setup Time	25	—	—	ns
8	Receive (TDMDI) Hold Time	25	—	—	ns
9	Transmit (TDMDO) Time to High Impedance	—	—	45*	ns
10	TDMCLK to Transmit (TDMDO) Valid	—	—	50	ns

* When connecting the T7256 TDM bus to Lucent devices with a CHI (concentration highway interface), the CHI must be able to withstand 45 ns of bus contention. For this length of time, two devices may be driving the bus. After this time, the output current is less than 10% of the output high and output low currents. The TDMD0 pin on the T7256 was designed to withstand 80 ns of bus contention.

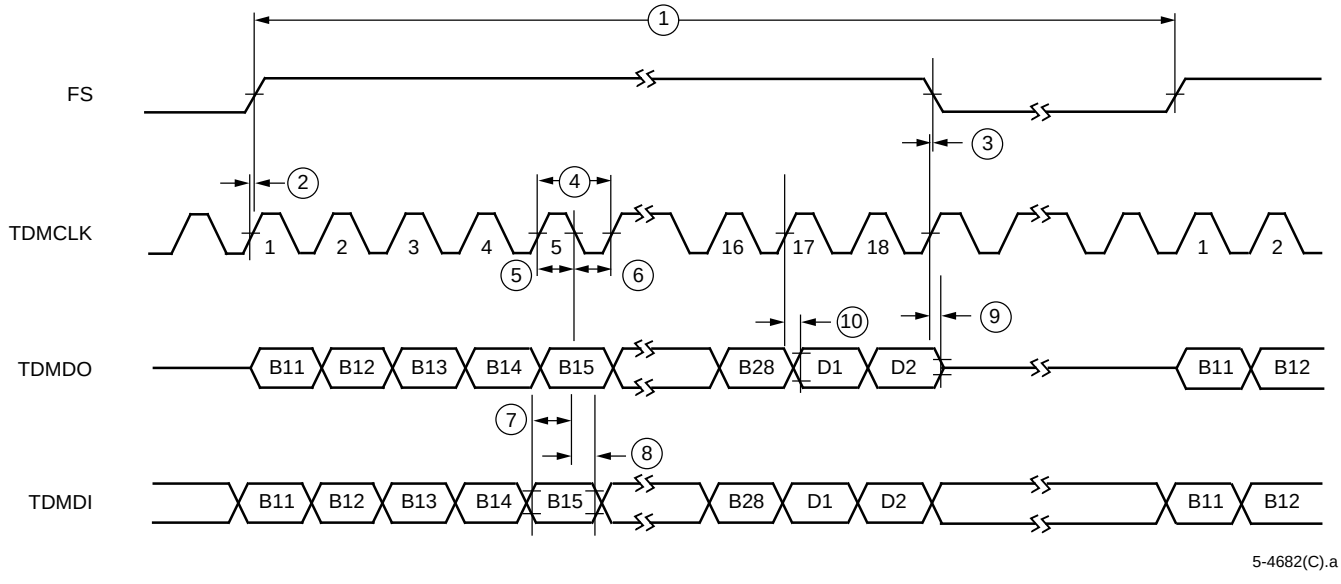


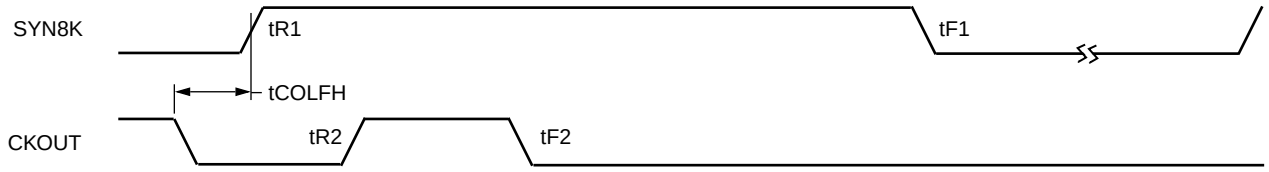
Figure 28. TDM Bus Timing

Timing Characteristics (continued)

Table 41. Clock Timing (See Figure 29.)

Symbol	Parameter	Min	Typ	Max	Unit
SYN8K	Duty Cycle	49.8	—	50.2	%
CKOUT	Duty Cycle:				
	In 15.36 MHz Mode	40	—	60	%
	In 10.24 MHz Mode	23*	—	52*	%
tR1, tF1	Rise or Fall Time	—	30	—	ns
tCOLFH	CKOUT Clock to Frame Sync (SYN8K)	—	—	50	ns
tR2, tF2	CKOUT Clock Rise or Fall	—	15	—	ns

* Includes the effect of phase steps generated by the digital phase-locked loop.

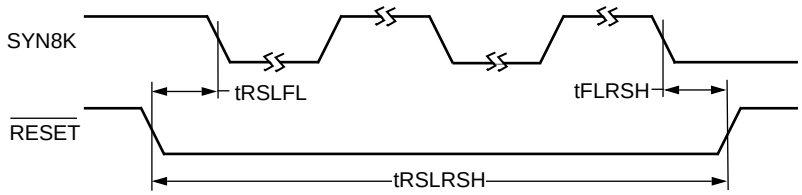


5-3460 (C)

Figure 29. Timing Diagram Referenced to SYN8K

Table 42. $\overline{\text{RESET}}$ Timing

Parameter	Description	Min	Max	Unit
tRSLFL, tFLRSH	$\overline{\text{RESET}}$ Setup and Hold Time	60	—	ns
tRSLRSH	$\overline{\text{RESET}}$ Low Time:			
	From Idle Mode or Normal Operation	375	—	µs
	From Power-on	1.5	—	ms



5-3462 (C)

Figure 30. $\overline{\text{RESET}}$ Timing Diagram

Timing Characteristics (continued)

Switching Test Input/Output Waveform

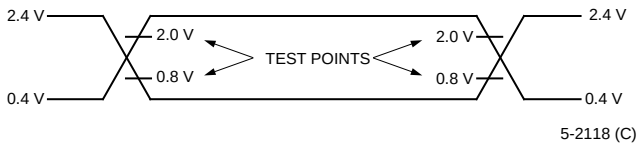


Figure 31. Switching Test Waveform

Figure 31 assumes that pin 12 (SDI) is low when RESET is asserted. The meaning of the setup and hold times tRSLFL and tFLRSH is as follows.

From the time RESET goes low, the following events must occur:

1. A falling edge of SYN8K must occur that meets the setup time with respect to RESET falling edge.
2. At least two additional falling edges of SYN8K (i.e., frames) must occur.
3. A falling edge of SYN8K must occur that meets the hold time with respect to RESET rising edge.

If RESET is asserted asychronously to SYN8K (which will typically be the case), its falling edge may violate the setup time with respect to SYN8K. Therefore, an additional frame time (125 µs) will elapse before a falling edge of SYN8K occurs that will satisfy criterion #1, above. This means, that to guarantee the RESET requirements are met for parameter tRSLRSH, RESET should be held low for a minimum of 500.120 µs (4 frames + 1 setup time + 1 hold time).

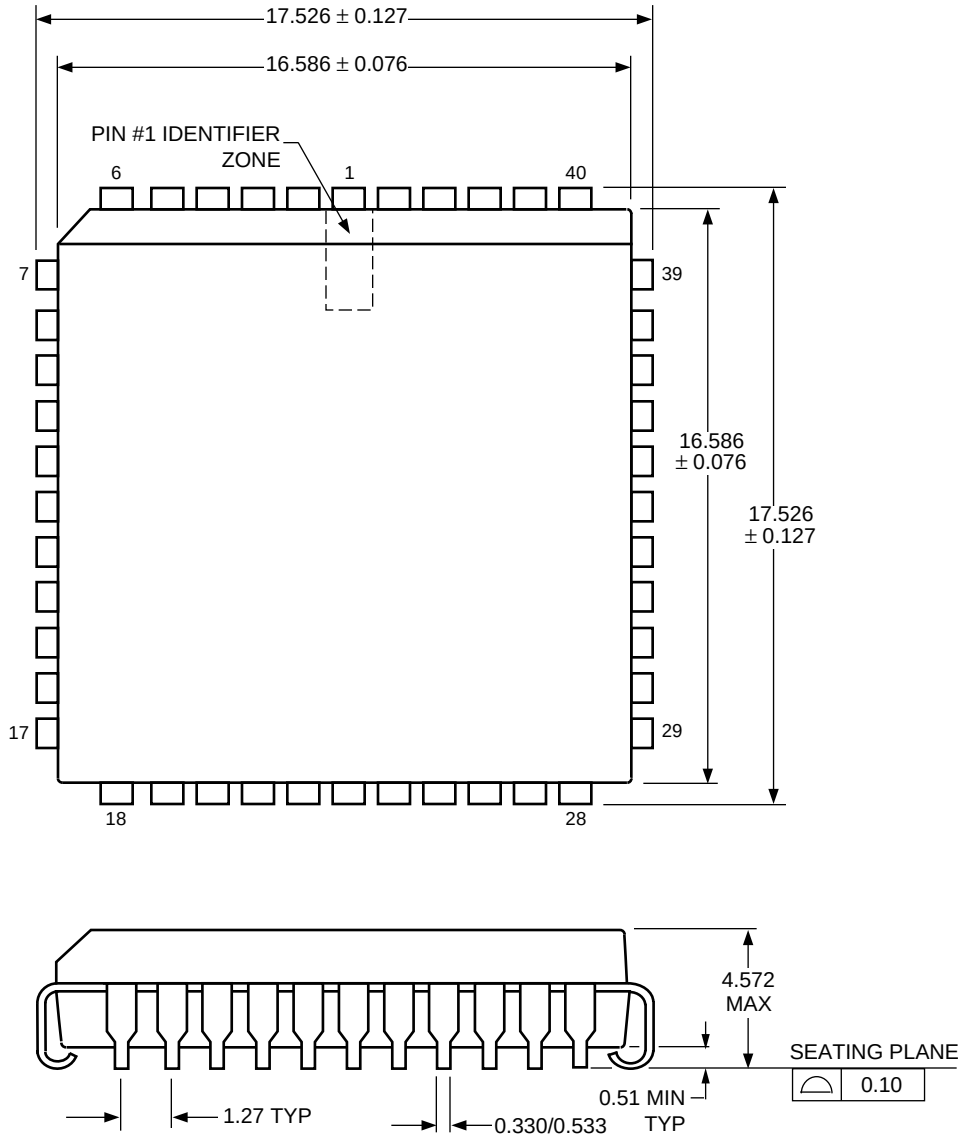
Propagation Delay

The maximum propagation delay from the S/T-interface to the U-interface (upstream direction) is 750 µs. The maximum propagation delay from the U-interface to the S/T-interface (downstream direction) is 550 µs.

Outline Diagram

44-Pin PLCC

Controlling dimensions are in inches.



5-2506r8

Note: The dimensions in this outline diagram are intended for informational purposes only. For detailed schematics to assist your design efforts, please contact your Lucent Technologies Sales Representative.

Ordering Information

Device Code	Shipping Method	Package	Temperature	Reliability	Comcode
T7256- - -ML2-D	Dry Pack—Sticks	44-Pin PLCC	–40 °C to +85 °C	300 ppm	107177065
T7256- - -ML2-DT	Dry Pack—Tape & Reel	44-Pin PLCC	–40 °C to +85 °C	300 ppm	107231672
T7256A - -ML-D	Dry Pack—Sticks	44-Pin PLCC	–40 °C to +85 °C	—	107997413
T7256A - -ML-DT	Dry Pack—Tape & Reel	44-Pin PLCC	–40 °C to +85 °C	—	108051806

Questions and Answers

Introduction

This section is intended to answer questions that may arise when using the T7256 Single-Chip NT1 Transceiver.

The questions and answers are divided into three categories: U-interface, S/T-interface, and miscellaneous.

U-Interface

Q1: Is the line interface for the T7256 the same as for the T7264?

A1: Yes. The U-interface section on these chips is identical, so their line interfaces are also identical.

Q2: Why is a higher transformer magnetizing inductance used (as compared to other vendors)?

A2: It has been determined that a higher inductance provides better linearity. Furthermore, it has been found that a higher inductance at the far end provides better receiver performance at the near end and better probability of start-up at long loop lengths.

Q3: Can the T7256 be used with a transformer that has a magnetizing inductance of 20 mH?

A3: The echo canceler and tail canceler are optimized for a transformer inductance of approximately 80 mH and will not work with lower inductance transformers.

Q4: Are the Lucent Technologies U-interface transformers available as surface-mount components?

A4: Not at this time.

Q5: Are there any future plans to make a smaller height 2-wire transformer?

A5: Due to the rigid design specifications for the transformer, vendors have found it difficult to make the transformer any smaller. We are continuing to work with transformer vendors to see if we can come up with a smaller solution.

Q6: The line interface components' specifications require 16.9 Ω resistors on the line side of the transformer when using the 2754H2. For our application, we would like to change this value. Can the U-interface line-side circuit be redesigned to change the value of the line-side resistors?

A6: Yes. For example, the line-side resistances can be reflected back to the device side of the transformer so that, instead of having 16.9 Ω on each side of the transformer, there are no resistors on the line side of the transformer and 24.4 Ω resistors on the device side (16.9 Ω + 16.9 Ω/N^2, where N is the turns ratio of the transformer). Note that the reflected resistances should be kept separate from the device-side 16.9 Ω resistors, and located between VR1 and T1 in Figure 20. This is necessary because the on-chip hybrid network (pins HP, HN) is optimized for 16.9 Ω of resistance between it and the LOP/LON pins.

Q7: Table 29, T7256 Reference Schematic Parts List, states the 0.1 µF capacitor that is used with the LH1465 (C15) must have an insulation resistance of >2 GΩ. Why?

A7: This capacitor is used to set the gate/source voltage for the main transistor in the device. The charging currents for this capacitor are on the order of microamps. Since the currents are so small, it is important to keep the capacitor leakage to a minimum.

Q8: The dc blocking capacitor (C16 in Figure 20) specified is 1.0 µF. Can it be increased to at least 2 µF?

A8: This value can be increased to 2 µF without an effect on performance. However, for an NT1 to be compliant with T1.601-1992 Section 7.5.2.3, the dc blocking capacitor must be 1.0 µF ± 10%.

Q9: Why is the voltage rating on 1 µF dc blocking capacitor (C16 in Figure 20) so high (250 V)?

A9: In Appendix B of T1.601, the last section states that consideration should be given to the handling of three additional environmental conditions. The third condition listed is maximum accidental ringing voltages of up to –200.5 V peak whose cadence has a 33% duty cycle over a 6 s period.

Questions and Answers (continued)

U-Interface (continued)

A9: (continued)

This statement could be interpreted to mean that a protector such as VR2 in Figure 20 should not trip if subjected to a voltage of that amplitude. This interpretation sets a lower limit on VR2's breakover rating. Since capacitor C16 will be exposed to the same voltage as VR2, its voltage rating must be greater than the maximum breakover rating of VR2. This sets an upper limit on the protector breakover voltage. The result is a need for a capacitor typically rated at about 250 V.

However, an argument can be made that it doesn't matter whether VR2 trips under this condition, since it is a fault condition anyway, and a tripped protector won't do any damage to a central office ringer.

The only other similar requirement, then, is found in Footnote 8, referenced in Section 7.5.3 of ANSI T1.601. The footnote implies that the maximum voltage that an NT will see during metallic testing is 90 V. The breakover voltage VR2 must be large enough not to trip during the application of the test voltage mentioned in the footnote. This means that a protector with a minimum breakover voltage of ≥90 V can be used that would permit a capacitor of lower voltage rating (e.g., 150 V) to be used. This is the approach we currently favor, although Figure 20 illustrates the more conservative approach.

Q10: What is the purpose of the 3300 pF capacitors (C13 and C14) in Figure 20 in the data sheet?

A10: The capacitors are for common-mode noise rejection. The ANSI T1.601 specification contains no requirements on longitudinal noise immunity. Therefore, these capacitors are not required in order to meet the specification. However, there are guidelines in IEC 801-6 which suggest a noise immunity of up to 10 Vrms between 150 kHz and 250 MHz. At these levels, the 10 kHz tone detector in the T7256 may be desensitized such that tone detection is not guaranteed on long loops. The 3300 pF was selected to provide attenuation of this common-mode noise so that tone detector sensitivity is not adversely affected. Since the 3300 pF capacitor was selected based only on guidelines, it is not mandatory, but it is recommended in applications which may be susceptible to high levels of common-mode noise. The final decision depends on the specific application.

As for the size of the capacitors, lab tests indicate the following:

1. The performance of the system suffers no degradation until the values are increased to about 0.1 μF.
2. The return loss at 25 kHz increases with increasing capacitor value.
3. The capacitor value has no effect on longitudinal balance.
4. A large unbalance in the capacitor values did not affect return loss, longitudinal balance, or performance.

Q11: Are there any recommended common-mode filtering parts for the U-interface? I suspect that our product may have emissions problems, and I want to include a provision for common-mode filtering on the U-interface.

A11: The only common-mode filtering parts we have any data on are two common-mode chokes from Pulse Engineering (619-674-8100) that are intended to help protect against external common-mode noise. The part numbers are PE-68654 (12.5 mH) and PE-68635 (4.7 mH), and in lab experiments, no noticeable degradation in transmission performance was observed. These chokes are typically effective in the frequency range 100 kHz—1 MHz.

As far as emissions are concerned, we don't have a lot of data. We have seen some success with the use of RJ-45 connectors that have integral ferrite beads such as those from Corcom*, Inc., (708) 680-7400. These provide some flexibility in that they have the same footprint as some standard RJ-45 connectors.

* Corcom is a registered trademark of Corcom, Inc.

Questions and Answers (continued)

U-Interface (continued)

Q12: I am planning on using a Raychem PTC (p/n TR600-150) on the U-interface of the T7256 as shown in Figure 20. The device is rated at 6 Ω—12 Ω. I am concerned about the loose tolerance on the PTC resistance. Will I be able to pass the return loss requirements in ANSI T1.601 Section 7.1?

A12: The NT1 impedance limits looking into tip/ring are derived from the T1.601 return loss requirements (Figure 17 in T1.601). At the narrowest point in the templates, the permissible range is between 111 Ω to 165 Ω. The tolerance on the PTC will reduce the impedance margin somewhat, but should still be acceptable.

Figure 32 is derived from the return loss template in ANSI T1.601. Return loss is a measure of the match between two impedances on either side of a junction point. The following equation is an expression of return loss in terms of the complex impedances of the two halves of the circuit Z_1, Z_2.

$$RL\ (dB) = 20 \log \left| \frac{Z1 + Z2}{Z1 - Z2} \right|$$

When the impedances are not matched, the junction becomes a reflection point. For a perfectly matched load, the return loss is infinite, whereas for an open or short circuit, the return loss is zero. The return loss expresses the ratio of incident to reflected signal power and should consequently be fairly high.

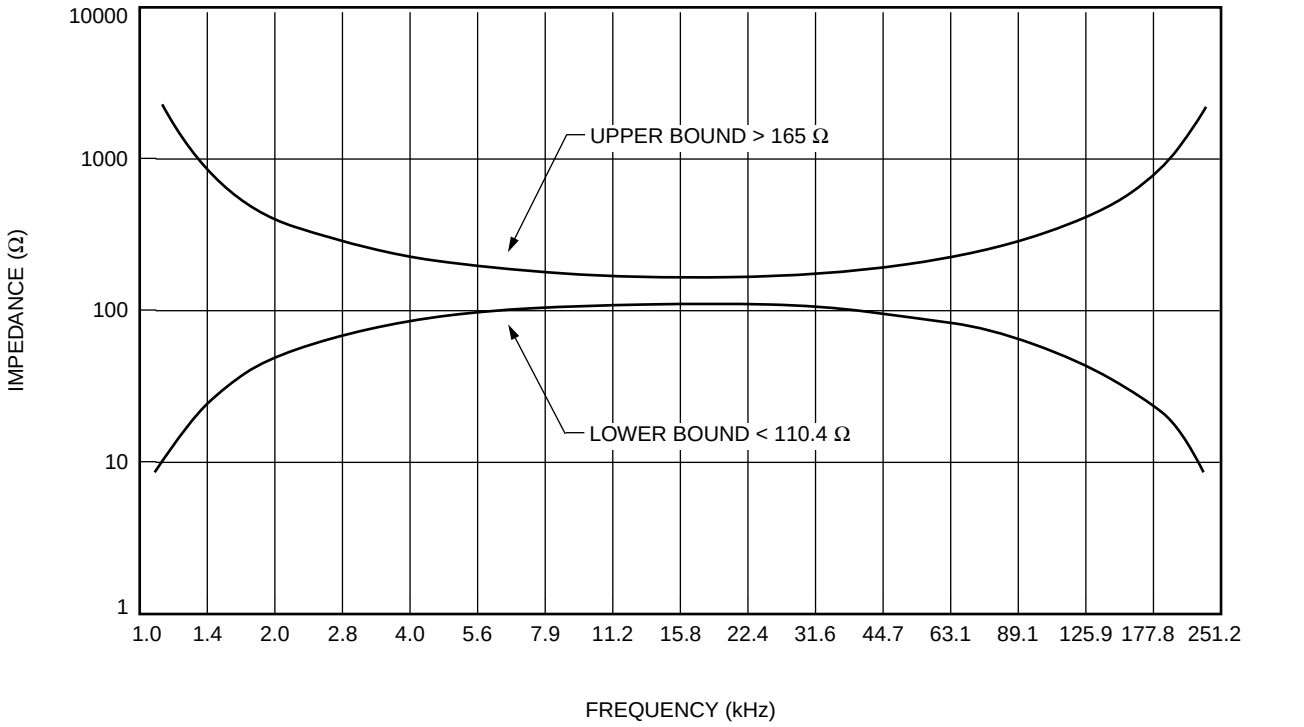


Figure 32. Transceiver Impedance Limits

Questions and Answers (continued)

U-Interface (continued)

A12: (continued)

It is desirable to express the return loss in terms of impedance bounds, since an impedance measurement is relatively simple to make. From the above equation, upper and lower bounds on impedance magnitude can be derived as follows:

Z_O = return loss reference impedance = 135 Ω

Z_U = upper impedance curve

Z_L = lower impedance curve

Upper bound ($Z_U > Z_O$) :

$$RL\ (dB) = 20 \log \left| \frac{Z_O + Z_U}{Z_U - Z_O} \right|$$

Lower bound ($Z_L < Z_O$):

$$RL\ (dB) = 20 \log \left| \frac{Z_O + Z_L}{Z_U - Z_L} \right|$$

Note that the higher the minimum return loss requirement, the tighter the impedance limits will be around Z_O, and vice versa.

So, for the upper bound, solve for Z_U:

$$Z_U = Z_O \left(\frac{10^{\frac{RL}{20}} + 1}{10^{\frac{RL}{20}} - 1} \right) = |Z_O| \left(\frac{1 + 10^{\frac{-RL}{20}}}{1 - 10^{\frac{-RL}{20}}} \right)$$

For the lower bound, solve for Z_L:

$$Z_U = Z_O \left(\frac{10^{\frac{RL}{20}} - 1}{10^{\frac{RL}{20}} + 1} \right) = |Z_O| \left(\frac{1 - 10^{\frac{-RL}{20}}}{1 + 10^{\frac{-RL}{20}}} \right)$$

Plotting the above equations (using 135 for Zo and Figure 16 in T1.601 for the RL values) results in the graph shown in Figure 32, which shows the return loss expressed in terms of impedance upper and lower bounds.

Q13: Why must secondary protection, such as a SGS-Thomson SM6T6V8CA protection diode, be used?

A13: The purpose of the diode is to protect against metallic surges below the breakdown level of the primary protector.

Such metallic surges can be coupled through the transformer and could cause device damage if the currents are high. The protector does not provide absolute protection for the device, but it works in conjunction with the built-in protection on the device leads.

The breakdown voltage level for secondary protection devices must be chosen to be above the normal working voltage of the signal and typically below the breakdown voltage level of the next stage of protection. The SM6T6V8CA has a minimum breakdown voltage level of 6.4 V and a maximum breakdown voltage of 7.1 V.

The chip pins that the SM6T6V8CA protects are pins 36 (HP), 31 (HN), 32 (LOP), and 35 (LON). The 16.9 Ω resistors will help to protect pins 32 and 35, but pins 31 and 36 will be directly exposed to the voltage across the SM6T6V8CA. The on-chip protection on these pins consists of output diodes and a pair of polysilicon resistors. These pins have been thoroughly tested to ensure that a 7.1 V level will not damage them; therefore, no third level of protection is needed between the SM6T6V8CA and the HP and HN pins.

The SM6T6V8CA has a maximum reverse surge voltage level of 10.5 V at 57 A. Sustained currents this large on the device side of the transformer are not a concern in this application.

Thus, there should never be more than 7.1 V across the SM6T6V8CA, except for possibly an ESD or lightning hit. In these cases, the T7256 is able to withstand at least ±1000 V (human-body model) on its pins.

Questions and Answers (continued)

U-Interface (continued)

Q14: Where can information be obtained on lightning and surge protection requirements for 2B1Q products?

A14: Requirements vary among applications and between countries. ANSI T1.601, Appendix B, provides a list of applicable specifications to which you may refer. Also, there are many manufacturers of overvoltage protection devices who are familiar with the specifications and would be willing to assist in surge protection design. The ITU-T K series recommendations are also a good source of information on protection, especially recommendation K.11, “Principles of Protection Against Overvoltages and Overcurrents,” which presents an overview of protection principles. Also refer to the application notes mentioned in the U-interface Description section of this data sheet.

Q15: ITU-T specification K.21 describes a lightning surge test for NT1s (see Figure 1/K.21 and Table 1/K.21, Test #1) in which both Tip and Ring are connected to the source and a 1.5 kV voltage surge is applied between this point and the GND of the NT1. What are the protection considerations for this test? Are the HP and HN pins susceptible to damage?

A15: The critical component in this test is the transformer since its breakdown voltage must be greater than 1.5 kV. Assuming this is the case, the only voltage that will make it through to the secondary side of the transformer will be primarily due to the interwinding capacitance of the transformer coils. This capacitance will look like an impedance to the common-mode surge and will therefore limit current on the device side of the transformer. The device-side voltage will be clamped by the SM6T6V8CA device. The maximum breakdown voltage of the SM6T6V8CA is 7.1 V. The 16.9 Ω resistors will help protect the LOP and LON pins on the T7256 from this voltage. However, this voltage will be seen directly on pins 36 and 31 (HP and HN) on the T7256. The on-chip protection on these pins consists of output diodes and a pair of polysilicon resistors. These pins have been thoroughly tested to ensure that an 7.4 V level will not damage them; therefore, no third level of protection is needed between the SM6T6V8CA and the HP and HN pins.

Q16: Can the range of the T7256 on the U-interface be specified in terms of loss? What is the range over straight 24 awg wire?

A16: ANSI Standard T1.601, Section 5.1, states that transceivers meeting the U-interface standard are intended to operate over cables up to the limits of 18 kft (5.5 km) 1300 Ω resistance design. Resistance design rules specify that a loop (of single- or mixed-gauge cable; e.g., 22 awg, 24 awg, and 26 awg) should have a maximum dc resistance of 1300 Ω, a maximum working length of 18 kft, and a maximum total bridged tap length of 6 kft.

The standard states that, in terms of loss, this is equivalent to a maximum insertion loss of 42 dB @ 40 kHz. Lucent Technologies has found that, for assessing the condition of actual loops in the field in a 2B1Q system, specifying insertion loss as 33.4 dB @ 20 kHz more closely models ANSI circuit operation. This is equivalent to a straight 26 awg cable with 1300 Ω dc resistance (15.6 kft).

The above goals are for actual loops in the outside loop plant. These loops may be subjected to noise and jitter. In addition, as mentioned above, there may be bridge taps at various points on the loop. The T1.601 standard defines 15 loops, plus the null, or 0-length loop, which are intended to represent a generic cross section of the actual loop plant.

A 2B1Q system must perform over all of these loops in the presence of impairments with an error rate of <1e–7. Loop #1 (18 kft, where 16.5 kft is 26 awg cable and 1.5 kft is 24 awg cable) is the longest, so it has the most loss (37.6 dB @ 20 kHz and 47.5 dB @ 40 kHz). Note that this is more loss than discussed in the preceding paragraph. The difference is based on test requirements vs. field deployment. The test requirements are somewhat more stringent than the field goal in order to provide some margin against severe impairments, complex bridged taps, etc.

Questions and Answers (continued)

U-Interface (continued)

A16: (continued)

If a transceiver can operate over Loop #1 error-free, it should have adequate range to meet all the other loops specified in T1.601. Loop #1 has no bridged taps, so passing Loop #1 does not guarantee that a transceiver will successfully start up on every loop. Also, due to the complex nature of 2B1Q transceiver start-up algorithms, there may be shorter loops which could cause start-up problems if the transceiver algorithm is not robust. The T7256 has been tested on all of the ANSI loops per the T1.601 standard and passes them all successfully. Two loops commonly used in the lab to evaluate the performance of the T7256 silicon are as follows:

Loop Configuration	Bridge Taps (BT)	Loss @ 20 kHz (dB)	Loss @ 40 kHz (dB)
18 kft/26 awg	None	38.7	49.5
15 kft/26 awg	Two at near end, each 3 kft/22 awg	37.1	46.5

The T7256 is able to start up and operate error-free on both of these loops. Neither of these loops is specified in the ANSI standard, but both are useful for evaluation purposes. The first loop is used because it is simple to construct and easy to emulate using a lumped parameter cable model, and it is very similar to ANSI Loop #1, but the loss is slightly worse. Thus, if a transceiver can start up on this loop and operate error-free, its range will be adequate to meet the longest ANSI loop. The second loop is used because, due to its difficult bridge tap structure and its length, it stresses the transceiver start-up algorithms more than any of the ANSI-defined loops. Therefore, if a transceiver can start up on this loop, it should be able to meet any of the ANSI-defined loops which have bridge taps. Also, on a straight 26 awg loop, the T7256 can successfully start up at lengths up to 21 kft. This fact, combined with reliable start-up on the 15 kft 2BT loop above, illustrates that the T7256 provides ample start-up sensitivity, loop range, and robustness on all ANSI loops. Another parameter of interest is pulse height loss (PHL). PHL can be defined as the loss in dB of the peak of a 2B1Q pulse relative to a 0-length loop. For an 18 kft 26 awg loop, the PHL is about 36 dB, which is 2 dB worse than on ANSI Loop #1. A signal-to-noise ratio (SNR) measurement can be performed on the received signal after all the signal processing is complete (i.e., at the input to the slicer in the decision feedback equalizer). This is a measure of the ratio of the recovered 2B1Q pulse height vs. the noise remaining on the signal. The SNR must be greater than 22 dB in order to operate with a bit error rate of <1e–7. With no impairments, the T7256 SNR is typically 32 dB on the 18 kft/26 awg loop. When all ANSI-specified impairments are added, the SNR is about 22.7 dB, still leaving adequate margin to guarantee error-free operation over all ANSI loops.

Finally, to estimate range over straight 24 awg cable, the 18 kft loop loss can be used as a limit (since the T7256 can operate successfully with that amount of loss) and the following calculations can be made:

Loss of 18 kft/26 awg loop @ 20 kHz	38.7 dB
Loss per kft of 24 awg cable @ 20 kHz	1.6 dB

$$\frac{38.7\ \text{dB}}{1.6\ \text{dB/kft}} = 24\ \text{kft}$$

Thus, the operating range over 24 awg cable is expected to be about 24 kft.

Q17: What does the energy spectrum of a 2B1Q signal look like?

A17: Figure A1 (curve P1) in the ANSI T1.601 standard illustrates what this spectrum looks like.

Questions and Answers (continued)

U-Interface (continued)

Q18: Please clarify the meaning of ANSI Standard T1.601, Section 7.4.2, Jitter Requirement #3.

A18: The intent of this requirement is to ensure that after a deactivation and subsequent activation attempt (warm start), the phase of the receive and transmit signals at the NT will be within the specified limits relative to what they were prior to deactivation. This is needed so that the LT, upon a warm-start attempt, can make an accurate assumption about the phase of the incoming NT signal with respect to its transmit signal. Note that the T7256 meets this requirement by design because the NT phase offset from transmit to receive is always fixed.

Q19: I need a way to generate a scrambled 2B1Q data stream from the T7256 for test purposes (e.g., ANSI T1.601 Section 5.3.2.2, Total Power and Section 7.2, Longitudinal Output Voltage). How can I do this?

A19: A scrambled 2B1Q data stream (the "SN1" signal described in ANSI T1.601 Table 5) can be generated by pulling $\overline{\text{ILOSS}}$ (pin 6) low on the T7256.

Q20: We are trying to do a return loss measurement on the U-interface of the T7256 per ANSI T1.601 Section 7.1. We are using a circuit similar to the one you recommend in the data sheet. We have observed the following. When the chip is in FULL RESET mode (powered on but no activity on the U- or S/T-interfaces), the return loss is very low, i.e., the termination impedance appears to be very large relative to 135 Ω and falls outside the boundaries of Figure 19 of ANSI T1.601. However, if we inject a 10 kHz tone before making a measurement, the return loss falls within the template. Why is it necessary to inject the 10 kHz tone in order to get this test to pass? Shouldn't a 135 Ω impedance be presented to the network regardless of the state of the T7256 once it is powered on?

A20: The return loss is only relevant when the transmitter section is powered on. When the transmitter is powered, it presents a low-impedance output to the U-interface. The transmitter must be held in this low-impedance state when the return loss **and** longitudinal balance tests are performed. This can be accomplished by pulling $\overline{\text{RESET}}$ low (pin 43). With the $\overline{\text{RESET}}$ pin held low, the transmitter is held in a low-impedance state where each of its differential outputs drives DV. In this state, it is prevented from transmitting any 2BIQ data and won't respond to any incoming wakeup tones. This is different than the ANSI-defined FULL RESET state that the chip enters after power-on or deactivation. In FULL RESET, the transmitter is powered down and in a high-impedance state, with only the tone detector powered on and looking for a far-end wakeup tone. The transmitter powers down when in FULL RESET state to save power and maximize the tone detector sensitivity. The reason that the chip behaves as it does in your tests is that your test begins with the transmitter in its FULL RESET state, causing the return loss to be very low. If a 10 kHz signal is applied, the tone detector senses the applied signal and triggers. This causes the transmitter to enter its low-impedance state, where it will remain until the T7256 start-up state machine times out (typically within 1.5 seconds, depending on the signal from the far end).

Q21: What are the average cold start and warm start times?

A21: Lab measurements have shown the average cold start time to be about 3.3 s—4.2 s over all loop lengths, and the average warm-start time to be around 125 ms—190 ms over all loop lengths.

Q22: What is the U-interface's response time to an incoming wakeup tone from the LT?

A22: Response time is about 1 ms.

Q23: What is the minimum time for a U-interface reframe after a momentary (<480 ms) loss of synchronization?

A23: Five superframes (60 ms).

Q24: Where is the U-interface loopback 2 (i.e., eoc 2B+D loopback) performed in the T7256?

A24: It is performed just inside the chip at the S/T-interface. The S/T receiver is disconnected internally from the chip pins, and the S/T transmit signal is looped back to the receiver inputs so the S/T section synchronizes to its own signal. This ensures that as much of the data path as possible is being tested during the 2B+D loopback.

Q25: Are the embedded operations channel (EOC) initiated B1 and B2 channel loopbacks transparent?

A25: Yes, the B1 and B2 channel loopbacks are transparent, as is the 2B+D loopback.

Questions and Answers (continued)

U-Interface (continued)

Q26: How can proprietary messages be passed across the U-interface?

A26: The embedded operations channel (EOC) provides one way of doing this. ANSI standard T1.601 defines 64 8-bit messages which can be used for nonstandard applications. They range in value from binary 00010000 to 01000000.

There is also a provision for sending bulk data over the EOC. Setting the data/message indicator bit to 0 indicates the current 8-bit EOC word contains data that is to be passed transparently without being acted on. Note that there is no response time requirement placed on the NT in this case (i.e., the NT does not have to echo the message back to the LT). Also note that this is currently only an ANSI provision and is not an ANSI requirement. The T7256 does support this provision.

Q27: What is the value of the ANSI T1.601 cso and nib bits in the 2B1Q frame?

A27: cso and nib are fixed at 0 and 1, respectively, by the device. This is because the device always has warm start capability (CSO = 0), and NT1s are required to have nib = 1 per T1.601-1992.

Q28: Are the PS bits controllable from outside the chip?

A28: Yes, the bits are controlled by two pins (8 and 9) on the chip. When the T7256 TDM highway is enabled, these pins change function and become part of the TDM highway and PS1 and PS2 are controlled by register GR1, bits 1 and 2.

Q29: It looks like the U-interface sai and act bits that the T7256 transmits towards the LT always track one another. If this is the case, I don't understand why they are both needed. Can you explain the purpose of the sai bit and how it relates to the act bit?

A29: The sai bit is equal to 1 when there is activity (INFO 1 or INFO 3) on the S/T-interface. The act bit is 1 whenever layer 1 transparency is established. Most of the time these bits are the same, but there are two situations where they will be different.

1. The sai bit can be used in conjunction with the uoa bit from the LT to support DSL-only activation as described in the ANSI and ETSI standards. The LT can request a U-only activation by setting uoa = 0, which will cause the S/T-interface to remain in a deactivated state. If the TE requests an activation under these conditions by transmitting INFO 1 to the T7256, the sai bit will change from 0 to 1, indicating to the LT that there is activity on the S/T-interface so that the LT can respond accordingly. Typically, this means that LT will set uoa = 1 to exit the DSL-only condition so that layer-1 transparency can be established from TE to LT. Thus, in the case of a DSL-only activation, the T7256's sai bit is 1 and its act bit is 0 from the time a TE requests an activation until the following events occur:

   A. LT sets uoa = 1 towards the NT.

   B. The T7256 detects uoa = 1 and transmits INFO 2 on the S/T-interface.

   C. The TE synchronizes and transmits INFO 3 on the S/T-interface.

   D. Upon reception of the INFO 3 signal, the T7256 sets act = 1.

2. If a link is fully active, then the LT detects a transition of the NT act bit from 1 to 0, it is an indication of loss of layer-1 transparency. This can be caused by either a) S/T loss of sync or b) NT1 received INFO 0. Case a) will result in an act = 0/sai = 1 combination, i.e., S/T sync is lost but there is still activity on the S/T-interface, meaning the TE is having trouble staying synchronized. Case b) will result in an act = 0/sai = 0 combination, i.e., no activity on the S/T-interface (INFO 0), meaning the TE has been disconnected (there is no way the TE can legally send INFO 0 when the link is fully active because the TE is not allowed to initiate deactivation—only the LT is—so the only other possibility is that it has been disconnected or has failed). Note that this procedure allows the CO to determine whether the cause of loss of layer 1 transparency is a TE that is having synchronization problems or a TE that has been disconnected, based on the state of the sai bit when act = 0.

   The ANSI T1.601 and ETSI ETR 080 standards contain finite state matrices that describe DSL-only operation. The T7256 follows the behavior described in the matrices. Refer to those tables for detailed information on each of the states.

Questions and Answers (continued)

S/T-Interface

Q30: What is the S/T transformer's inductance?

A30: For Lucent transformers 2768A or 2776, a minimum inductance of 22 mH is guaranteed.

Q31: We are trying to test the S/T side of our T7256-based NT1 using a Siemens K1403 ISDN tester. The tester is not able to sync up to the NT1. Can you explain this behavior?

A31: Check the connector wiring of the S/T-interface. In the January 1995 T7256 data sheet, the pinouts of the RJ-45 S/T connector (J1) were shown incorrectly. The ones shown are for a TE. The correct (i.e., NT) pinouts are listed in the current T7256 data sheet (swap pins 3 and 6 with pins 4 and 5, respectively). If the pinout is wrong as just described, the Siemens K1403 will not sync up to the S/T-interface.

Q32: Can the S/T-interface leads be short-circuited together without harming the device?

A32: Yes, this will not cause any harm to the device.

Q33: What is the common-mode rejection of the S/T receiver?

A33: The common-mode rejection of the S/T receiver is 400 mV. Refer to the Electrical Characteristics described in the data sheet.

Q34: I notice that the application note entitled Design an S/T Line Interface Circuitry Using the T7250C/T7259 recommends relays on both the transmitter and receiver outputs that disconnect the device when power is removed from the chip. Is this necessary for an NT using the T7256?

A34: The relay on the TE transmitter output is necessary to pass the peak current test (ITU-T I.430 Section 8.5.1.2 and ANSI T1.605-1991, section 9.5.1.2) when the TE is powered down. For the NT, there is no equivalent test, so the relay is not necessary. The relay on the TE receiver input is also necessary to pass the peak current test (ITU-T I.430 Sections 8.5.1.2 and 8.6.1.1, and ANSI T1.605-1991 Sections 9.5.1.2 and 9.6.1.1). For the NT, however, there is enough margin in the line interface capacitance circuitry such that the peak current requirement (ITU-T I.430 Section 8.6.1.2 and ANSI T1.605-1991 Section 9.6.1.2) can be met without using relays. This assumes, of course, that sound layout practices have been applied to keep parasitic capacitance of the line interface circuitry to a minimum (of primary importance is making sure there is no ground plane under the S/T line interface). The reason the TE needs a relay on its receiver is that the TE tests assume a 350 pF cord connected to the line, and this extra capacitance can cause the peak current requirement to be exceeded. So even though the NT peak current requirement is slightly more stringent (0.5 mA as opposed to 0.6 mA), the TE peak current test is the most difficult to meet due to the 350 pF cord capacitance.

Q35: The T7256 reference design in Figure 21 shows 100 Ω termination resistors in parallel with a second pair of optional 100 Ω resistors that can be inserted or removed by installing/removing jumpers from JMP1 and JMP2. What is the purpose of this second pair of resistors?

A35: Typically, a TE or group of TEs connected to an NT1 will have a 100 Ω termination located at the interface point of the TE farthest from the NT1 (refer to ITU-T I.430 Figure 2 and Section 4 or T1.605 Figure 2 and Section 5). However, in some cases it may be desirable to operate an NT1 with a TE that does not provide the 100 Ω termination impedance. In this case, the provisional 100 Ω resistors shown in Figure 21 may be installed to provide the extra termination impedance required.

Questions and Answers (continued)

S/T-Interface (continued)

Q36: I would like to integrate a T7256-based NT1 onto both a T7250C-based 4-wire TE product and a T7903-based 4-wire TE product in order to provide a U-interface on these products. I realize this can be done by simply incorporating my external NT1 design directly onto the TE board, but is there a simpler approach in which I can avoid having two sets of S/T transformers and associated line interface circuitry?

A36: Yes. First note Figures 34, 35, and 36, which show example S/T line interface circuits for the T7256, T7903, and T7250C, respectively. If no external S/T-interface connection is required, the T7256 can be directly connected to the T7903 and T7250C as shown in Figures 37 and 38. If there is a requirement for connecting external TEs, the circuits shown in Figures 39 and 40 can be used. These two circuits show a hybrid scheme in which a direct connect between the T7256 and T7903/T7250C is implemented while providing for an external S/T-interface (thus requiring only one set of S/T transformers rather than the two sets that would be required if the T7256 and T7903/T7250C were transformer-coupled to one another instead directly connected).

The direct connect circuits were derived as shown in Figures 37 and 38 and the following text sections:

Note: In all of these analyses, the final value of resistance chosen may be slightly different than the ideal value computed because standard resistance values were used.

T7903/T7250C Transmit to T7256 Receive

a) Transmitter Load:

T7903: The line interface transformer has a turns ratio of 2.0, and the transmitter drives a total line-side load of 50 Ω. Reflecting this impedance to the device side of the transformer results in 200 Ω (50 Ω x N^2). This resistance, combined with the 40 Ω total resistance of the device-side resistors, results in a total of 240 Ω that the transmitter typically drives.

So, to optimize the transmitter part of the circuit based on the load the transmitter expects to drive, the transmitter should see a total resistance of approximately 240 Ω.

T7250C: The line interface transformer has a turns ratio of 2.5, and the transmitter drives a line-side load of 50 Ω. Reflecting this impedance to the device side of the transformer results in 312.5 Ω (50 Ω x N^2). This resistance, combined with the 113 Ω total resistance of the device-side resistors, results in a total of 425.5 Ω that the transmitter typically drives. So, to optimize the transmitter part of the circuit based on the load the transmitter expects to drive, the transmitter should see a total resistance of approximately 425 Ω.

Questions and Answers (continued)

S/T-Interface (continued)

A36: (continued)

b) Receiver Levels:

The T7256 S/T line interface transformer has a turns ratio of 2.5. The receiver expects to see nominal pulse levels of 750 mV x 2.5 = 1.875 V.

T7903: The transmitter circuit is a current source of 7.5 mA. To generate a voltage of 1.875 V with 7.5 mA requires a resistance of 1.875/0.0075 = 250 Ω.

T7250C: The transmitter circuit is a current source of 6 mA. To generate a voltage of 1.875 V with 6 mA requires a resistance of 1.875/0.006 = 312.5 Ω.

c) Resistor Selection:

In this section, the term receiver implies not only the receive section on the chip, but also the external 10 kΩ resistors connected to the receiver. These resistors remain unchanged from the standard line interface circuit in order to maintain the same total receiver impedance.

T7903: Ideally, the transmitter should be driving into 240 Ω, and the T7256 receiver wants to see the levels that would result if the transmitter drove 7.5 mA through 250 Ω. Since these resistance values are so close, 249 Ω is chosen as the resistor across which the receiver is connected, and no other series resistance is needed in the transmit path, as Figure 37 illustrates.

T7250C: Ideally, the transmitter should be driving into 425 Ω, and the T7256 receiver wants to see the levels that would result if the transmitter drove 6 mA through 312.5 Ω. So, the total transmit path resistance should be divided into three resistors. The first is the resistor across which the receiver is connected and should be approximately 312.5 Ω so that the receiver sees the correct levels. A standard 309 Ω value is adequate for this case. The remainder of the 425 Ω should be divided equally between two other series resistors in the transmit path, and (425 – 309)/2 is 58.0 Ω, so a standard 57.6 Ω value is chosen for the two other series resistors as illustrated in Figure 38.

d) Receiver Bias:

Normally, the transmitter of the T7903/ T7250C is biased at 5 V through 100 kΩ pull-up, and the receiver of the T7256 is biased at 2.16 V through a resistor network that can be simplified as shown in Figure 33 (A). When the direct-connect scheme is implemented, the resulting network between the T7903/ T7250C transmitter and the T7256 receiver is as shown in Figure 33 (B).

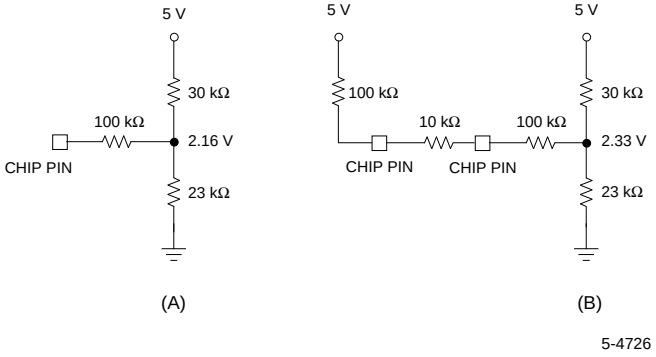


Figure 33. Receiver Bias

Note that the receiver bias in Figure 33 (B) is increased to 2.33 V (from 2.16 V in Figure 33 (A)). This is an increase of about 8% (0.67 dB). This will decrease the overall receiver sensitivity slightly. Normally, the receiver must have a sensitivity to signals down to –7.5 dB of nominal. Therefore, in the case of a direct connect, the sensitivity is not an issue since the receiver will always see a large input signal.

Questions and Answers (continued)

S/T-Interface (continued)

A36: (continued)

T7256 Transmit to T7903/T7250C Receive

a) Transmitter Load:

The T7256 S/T line interface transformer has a turns ratio of 2.5, and the transmitter drives a line-side load of 50 Ω. Reflecting this impedance to the device side of the transformer results in 312.5 Ω (50 Ω x N^2). This resistance, combined with the 242 Ω total resistance of the device-side resistors, results in a total of 554.5 Ω that the transmitter typically drives. So, to optimize the transmitter part of the circuit based on the load the transmitter expects to drive, the transmitter should see a total resistance of approximately 554.5 Ω.

b) Receiver Levels:

T7903: The S/T line interface transformer has a turns ratio of 2.0. The receiver expects to see nominal pulse levels of 750 mV x 2.0 = 1.5 V. The T7256 transmitter circuit is a current source of 6.0 mA. To generate a voltage of 1.5 V with 6.0 mA requires a resistance of 1.5/0.006 = 250 Ω.

T7250C: The S/T line interface transformer has a turns ratio of 2.5. The receiver expects to see nominal pulse levels of 750 mV x 2.5 = 1.875 V. The T7256 transmitter circuit is a current source of 6.0 mA. To generate a voltage of 1.875 V with 6.0 mA requires a resistance of 1.875/0.006 = 312.5 Ω.

c) Resistor Selection:

In this section, the term receiver implies not only the receive section on the chip, but also the external 10 kΩ resistors connected to the receiver. These resistors remain unchanged from the standard line interface circuit in order to maintain the same total receiver impedance.

T7903: Ideally, the T7256 transmitter should be driving into 554.5 Ω, and the T7903 receiver wants to see the levels that would result if the transmitter drove 6 mA through 250 Ω. So, the total transmit path resistance should be divided into three resistors. The first is the resistor across which the receiver is connected and should be approximately 250 Ω so that the receiver sees the correct levels. A standard 249 Ω value is adequate for this case. The remainder of the 554.5 Ω should be divided equally between two other series resistors in the transmit path, and (554.5 Ω – 249 Ω)/2 is 152.7 Ω, so 150 Ω is chosen for the two other series resistors as illustrated in Figure 37.

T7250C: Ideally, the T7256 transmitter should be driving into 554.5 Ω, and the T7250C receiver wants to see the levels which would result if the transmitter drove 6 mA through 312.5 Ω. So, the total transmit path resistance should be divided into three resistors. The first is the resistor across which the receiver is connected and should be approximately 312.5 Ω so that the receiver sees the correct levels. A standard 309 Ω value is adequate for this case. The remainder of the 554.5 Ω should be divided equally between two other series resistors in the transmit path, and (554.5 Ω – 309 Ω)/2 is 122.6 Ω, so 121 Ω is chosen for the two other series resistors as illustrated in Figure 38.

d) Receiver Bias:

The receiver bias is not an issue for the same reasons discussed in the T7903/T7250C Transmit to T7256 Receive section.

Questions and Answers (continued)

S/T-Interface (continued)

A36: (continued)

T7903/T7250C to T7256 Direct Connect with External S/T-Interface Provided

First, we need to address the issue of the transformer turns ratio.

T7903: The T7903 uses a 2.0:1 transformer, and the T7256 uses a 2.5:1 transformer. It is desirable to be able to use a dual transformer, so we want the transmit- and receive-side transformers to have the same turns ratio. Also, it may be desirable to use a product with this arrangement as just a TE (with an external NT1, i.e., no U-Interface connected to the integrated NT1). Therefore, we will select a 2.0:1 turns ratio transformer to ensure T7903 pulses of sufficient amplitude on the line side of the transformer and ensure that an external transmitter won't overdrive the T7903 receiver inputs.

T7250C: The T7250C and T7256 both use a 2.5:1 transformer, which simplifies the analysis for this case.

T7903/T7250C Transmit to T7256 Receive

a) Transmitter Load:

If we use the same S/T transmitter line interface circuit as in the normal (stand-alone TE) case, the transmitter will see the load that it expects to drive and is thus optimized in terms of the load. The 100 Ω terminations must be user selected per the following table:

Configuration	JMP1	JMP2
Integrated NT1 Used as NT1 (No External NT1 Connected)		
No External TE Connected	Installed	Installed
Unterminated External TE Connected	Installed	Installed
Terminated (100 Ω) External TE Connected	Installed	Not Installed

b) Receiver Levels:

The T7256 S/T line interface transformer has a turns ratio of 2.5. The T7256 receiver thus expects to see nominal pulse levels of 750 mV x 2.5 = 1.875 V at the device side of the transformer.

T7903: The T7903 transmitter (or an external TE on a 0-length loop) will drive 750 mV pulses on the S/T line, and that voltage reflected back to the device side of the transformer is 750 mV x 2.0 = 1.5 V. If the T7256 receiver is connected to the device side of the transformer as shown in Figure 39, it will see 1.5 V instead of 1.875 V when a 750 mV pulse is present on the line. Thus, there is an inherent pulse attenuation in this scheme of 1.9 dB at the T7256 receiver.

We need to be sure that the receiver will have adequate sensitivity to detect pulses from an external TE that is some distance away. Referring to ITU I.430, this circuit can only be used in a short passive bus (SPB) mode when using the onboard NT1, because there is a local TE (the T7903), so any external TE that is also used will result in a passive bus configuration. ITU-T I.430 states that the maximum attenuation in SPB configuration is 3.5 dB. Combining this with the inherent 1.9 dB attenuation results in a total possible signal attenuation of 5.4 dB. The receiver must have a sensitivity of at least 7.5 dB per ITU-T I.430 Section 8.6.2.3, so 5.4 dB attenuation will present no problem in this case.

T7250C: The T7250C transmitter (or an external TE on a 0-length loop) will drive 750 mV pulses on the S/T line, and that voltage reflected back to the device side of the transformer is 750 mV x 2.5 = 1.875 V. If theT7256 receiver is connected to the device side of the transformer as shown in Figure 40, it will see the 1.875 V pulse level it expects when a 750 mV pulse is present on the line.

c) Receiver Bias:

In the T7903 to T7256 Direct Connect section we showed that the receiver is biased by about 0.67 dB from nominal due to the direct connect of the T7903 to the T7256. Assuming the receiver sensitivity decreases by this much and combining this with the maximum 5.4 dB attenuation found in the previous section results in a total of 6.07 dB of required sensitivity, which is still within the 7.5 dB requirement on the receiver.

Questions and Answers (continued)

S/T-Interface (continued)

A36: (continued)

T7256 Transmit to T7903/T7250C Receive

a) Transmitter Load:

The T7256 S/T line interface transformer normally has a turns ratio of 2.5, and the transmitter drives a line-side load of 50 Ω. Reflecting this impedance to the device side of the transformer results in 312.5 Ω (50 Ω x N^2). This resistance, combined with the 242 Ω total resistance of the device-side resistors, results in a total of 554.5 Ω that the transmitter typically drives. So, to optimize the transmitter part of the circuit based on the load the transmitter expects to drive, the transmitter should see a total resistance of approximately 554.5 Ω.

T7903: In this case, the T7256 transmitter is driving into a transformer with a turns ratio of 2.0. The pulse amplitude that the transmitter must generate on the device side of the transformer is 1.5 V (resulting in a 750 mV pulse on the line in accordance with the standards). The T7256 transmitter circuit is a current source of 6.0 mA. To generate a voltage of 1.5 V with 6.0 mA requires a resistance of 1.5/0.006 = 250 Ω, which is 62.5 Ω when reflected to the device side of the transformer. This impedance should consist of jumper-selectable 100 Ω and 167 Ω resistors as illustrated in Figure 39. The table below lists the jumper settings for each possible configuration.

The total impedance the T7256 must drive (from the first paragraph of this section) is 554.5 Ω, and the impedance across the transformer leads is 250 Ω (from the second paragraph). The remaining 554.5 Ω – 250 Ω = 304.5 Ω is divided equally between the positive and negative transmitter outputs, requiring 152 Ω in each leg. We can accomplish this with a 143 Ω resistor on the device side of the diode bridge and a 10 Ω resistor on the line side of the bridge. The resistance is split in this way to provide 10 Ω of current limiting through the diode bridge when the bridge is conducting (similar to the T7903 transmitter circuit).

Configuration	JMP3	JMP4
Integrated NT1 Used as NT1 (No External NT1 Connected)		
No External TE Connected	Installed	Installed
Unterminated External TE Connected	Installed	Installed
Terminated (100 Ω) External TE connected	Installed	Not Installed

T7250C: Referring to Figure 40, if we use the same T7256 S/T transmitter line interface circuit as in the normal (stand-alone NT) case, the T7256 transmitter will see the 554.5 Ω load that it normally expects to drive and is thus optimized in terms of the load. The 100 Ω terminations shown are user selected per the preceding table.

b) Receiver Levels:

The T7903 will see the correct pulse levels by design. In the preceding section, the T7256 transmit circuit was designed to produce 750 mV pulses on the line. The T7903 receiver is attached directly to the device side of the transformer, so it will see the 1.5 V pulse levels that it expects to see.

T7903: The T7903 S/T line interface transformer has a turns ratio of 2.0. The T7903 receiver thus expects to see nominal pulse levels of 750 mV x 2.0 = 1.5 V at the device side of the transformer. The T7256 transmitter section was designed to produce 750 mV pulses on the S/T line (as would an external TE on a 0-length loop). That voltage reflected back to the device side of the T7901 transformer is 750 mV x 2.0 = 1.5 V, so the T7901 sees the pulse level it expects when a 750 mV pulse is present on the line.

T7250C: The T7250C S/T line interface transformer has a turns ratio of 2.5. The T7250C receiver thus expects to see nominal pulse levels of 750 mV x 2.5 = 1.875 V at the device side of the transformer. The T7256 transmitter section was designed to produce 750 mV pulses on the S/T line (as would an external TE on a 0-length loop). That voltage reflected back to the device side of the T7250C transformer is 750 mV x 2.5 = 1.875 V, so the T7250C see the pulse level it expects when a 750 mV pulse is present on the line.

c) Receiver Bias:

The receiver bias is sufficiently small that it is not an issue (see preceding sections).

Questions and Answers (continued)

S/T-Interface (continued)

A36: (continued)

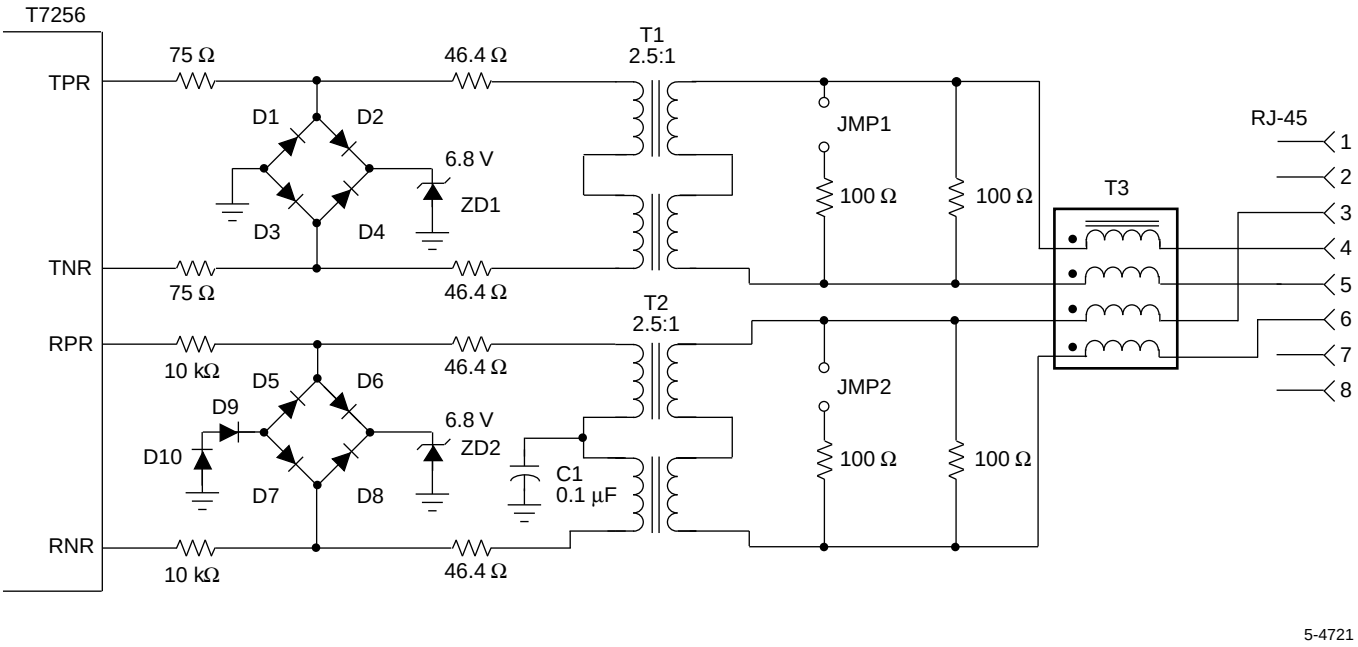
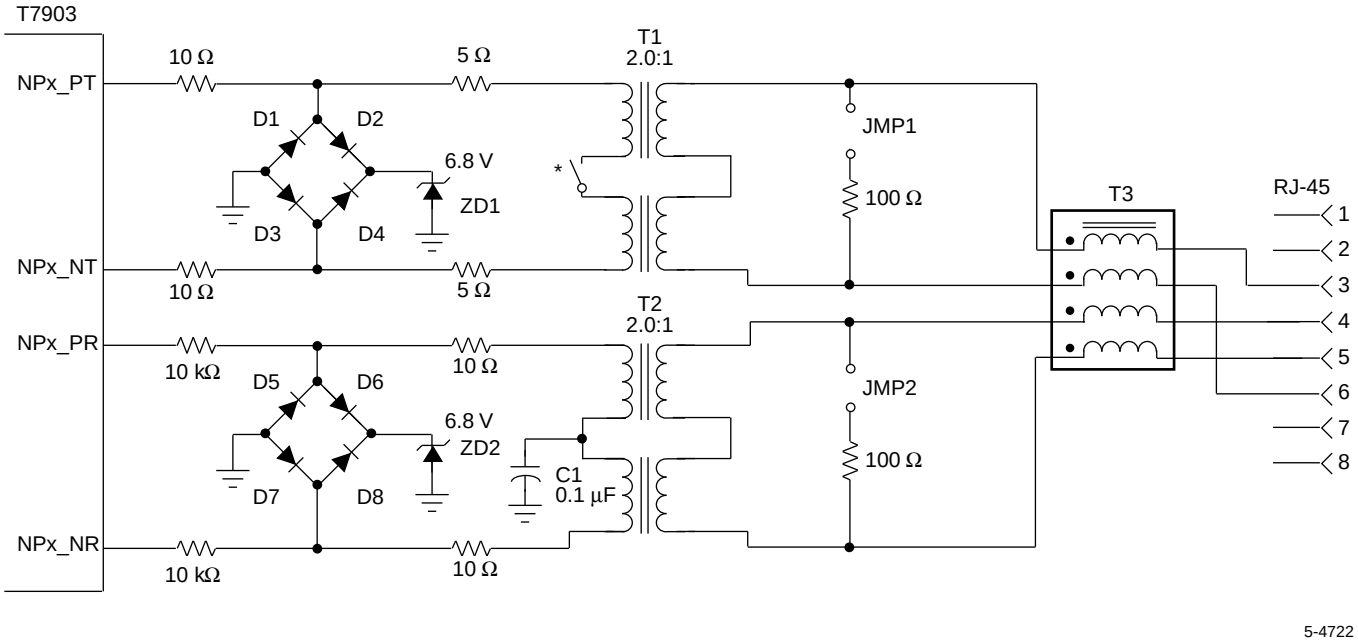


Figure 34. T7256 S/T Line Interface Scheme



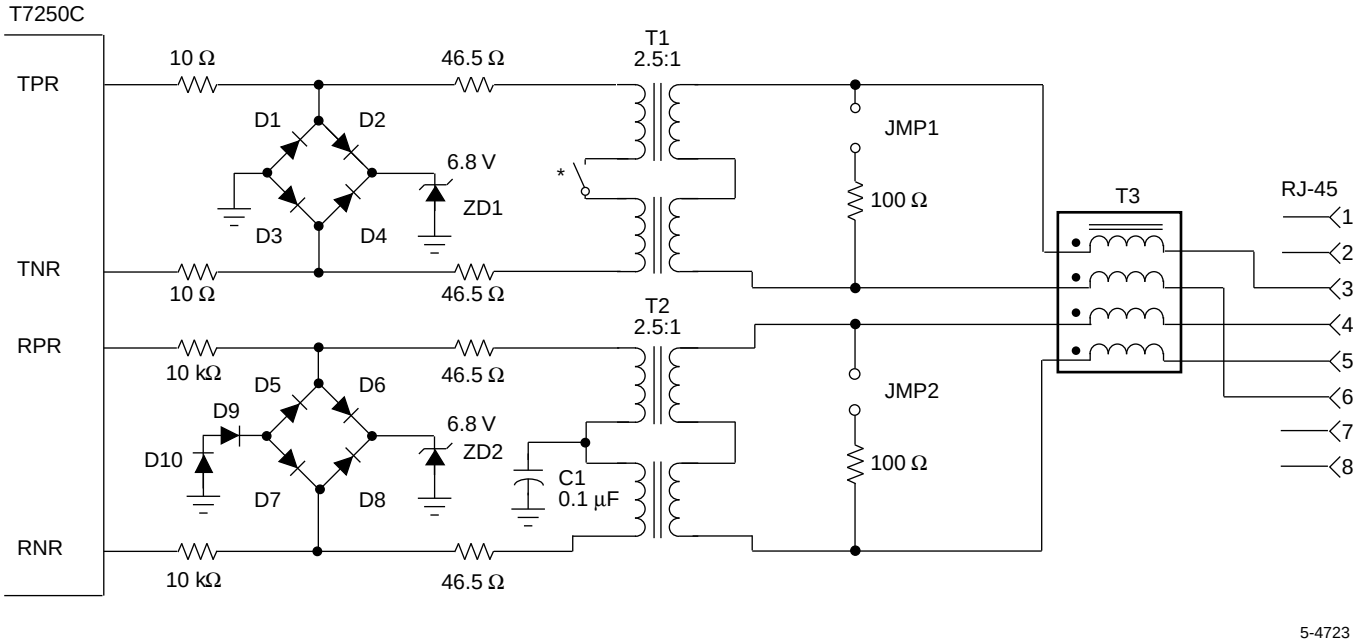
* Refer to the T7903 data sheet, Figure F-10 for an example of a switch circuit that can be used here.

Figure 35. T7903 S/T Line Interface Scheme

Questions and Answers (continued)

S/T-Interface (continued)

A36: (continued)



* Refer to the T7250 data sheet, Figure F-10 for an example of a switch circuit that can be used here.

Figure 36. T7250C S/T Line Interface Scheme

Note: The circuit shown above has subtle differences from that shown in the T7250C data sheet. Either circuit is suitable, since they will both pass the required conformance tests.

Questions and Answers (continued)

S/T-Interface (continued)

A36: (continued)

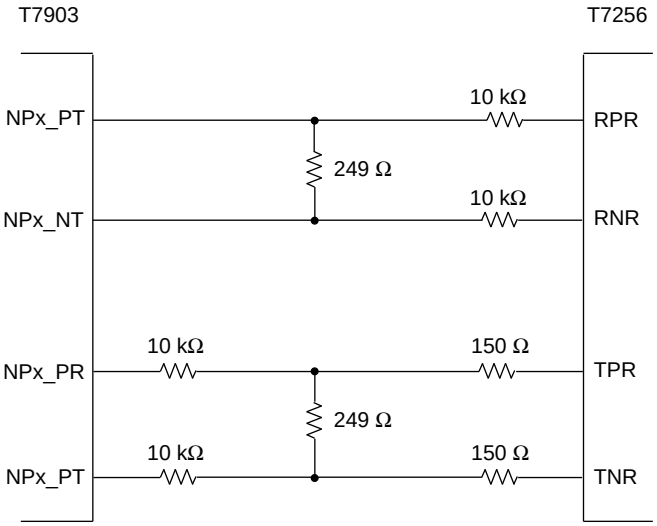


Figure 37. T7903 to T7256 Direct-Connect Scheme

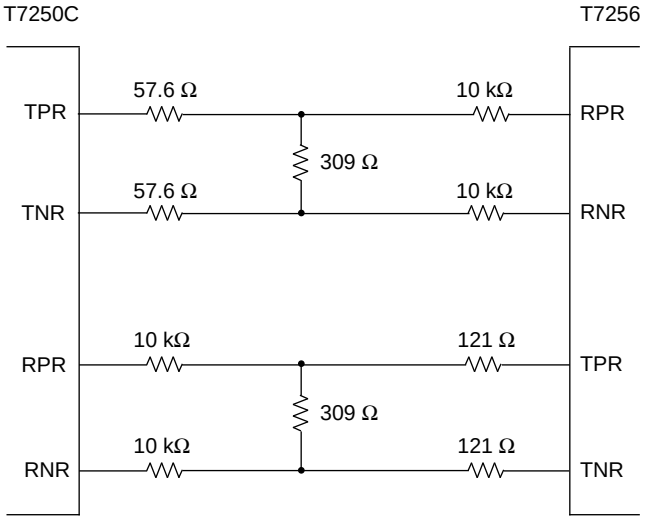
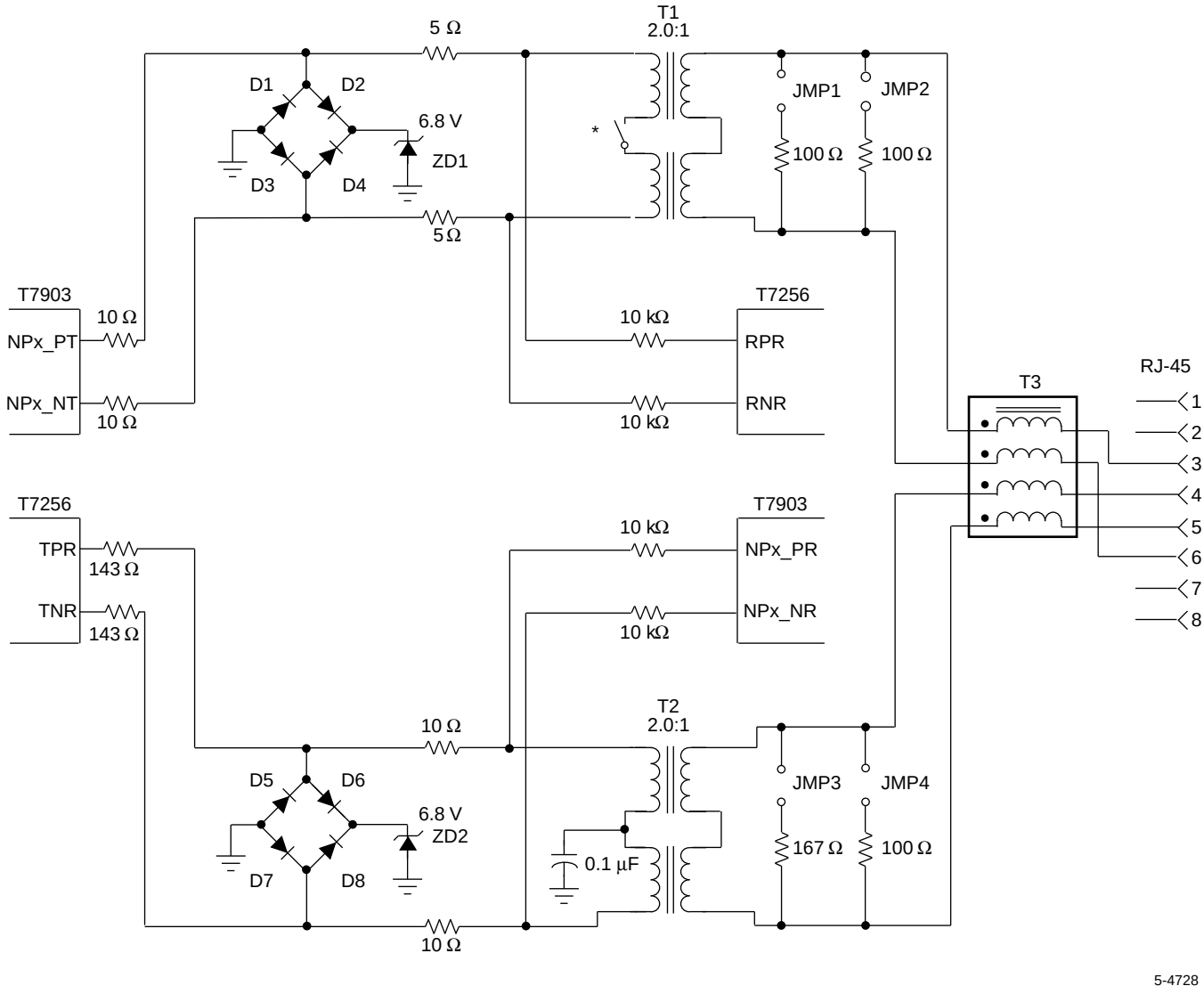


Figure 38. T7250C to T7256 Direct-Connect Scheme

Questions and Answers (continued)

S/T-Interface (continued)

A36: (continued)



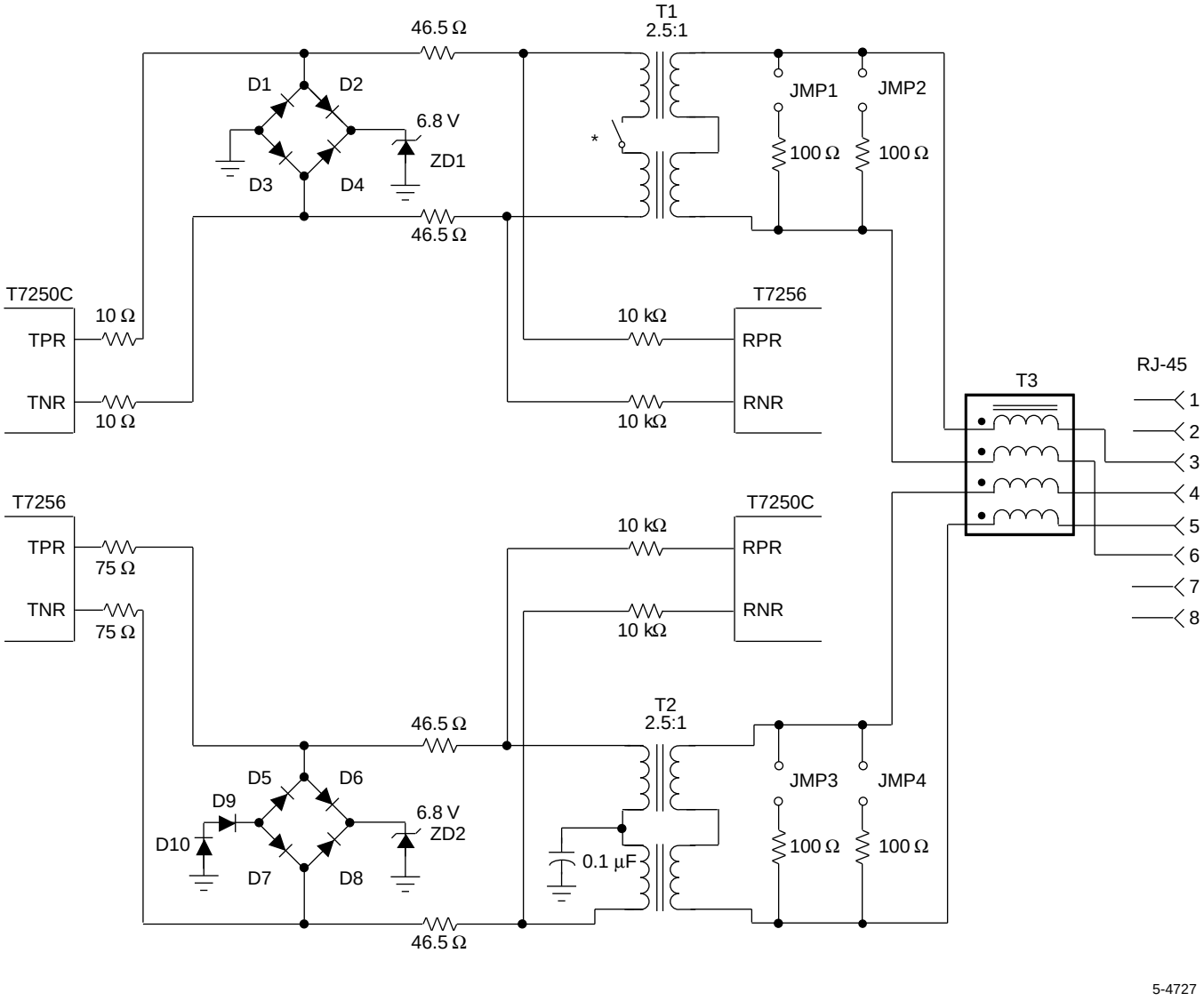
* Refer to the T7903 data sheet, Figure F-10 for an example of a switch circuit that can be used here.

Figure 39. T7903 to T7256 Direct-Connect Scheme with External S/T-Interface

Questions and Answers (continued)

S/T-Interface (continued)

A36: (continued)



* Refer to the T7250 data sheet, Figure F-10 for an example of a switch circuit that can be used here.

Figure 40. T7250C to T7256 Direct-Connect Scheme with External S/T-Interface

Questions and Answers (continued)

S/T-Interface (continued)

Q37: What is the state of the D-echo bit during an EOC 2B+D loopback?

A37: The D-echo bit (SXE, GR2, bit 3) should be set to zero to meet the ITU-T I.430 requirement in Appendix I, Note 4, which states that during a loopback 2 (eoc 2B+D loopback), the NT1 should send INFO 4 frames toward the TE with the D-echo channel bits set binary zero. If AUTOEOC = 1 (register GRO, bit 4), SXE is internally overridden to 0 by the T7256. If AUTOEOC = 0, SXE must be set to 0 by the user.

Q38: Is it possible to make a nontransparent single B-channel loopback toward the S/T-interface via the microprocessor?

A38: Yes. Refer to the data sheet for a description of the ITU-T I.430 Loop C loopback control bits (register DFRO).

Q39: What is the purpose of the SFECV bit in register SIR0?

A39: ANSI T1 T1.605 Table 6, “Codes for Q-Channel and SC1-Subchannel Messages,” defines an SC1-Subchannel message, “Far-End Code Violation” (SC11, SC12, SC13, SC14 = 1110). This is an S-channel message that the NT can send to the TE to indicate that a previous multiframe received by the NT contains one or more illegal S/T line code violations. In an NT1 that supports multiframing, the SFECV bit can be used to generate an interrupt to the T7256 microprocessor indicating that it should transmit the “Far-End Code Violation” message to the TE in S-subchannel one. This subchannel is accessed via register MCR1 bits 0—3.

Q40: In the Analog Interface section of the S/T-interface description in the data sheet, where does the value of 0 ms—3.1 ms maximum differential delay in adaptive timing mode come from?

A40: The minimum value of 0 ms is necessary so that the NT's transmitter and receiver can be directly connected in a loopback and still synchronize. The maximum value of 3.1 ms comes about because the window size needed in the adaptive timing algorithm is 2.1 ms. The window size is the time during each bit period in which no transitions may occur. Since a period is 5.2 ms, the time during which there may be transitions is 5.2 ms – 2.1 ms, or 3.1 ms. This is the same as the maximum differential delay, since the earliest and latest bit transitions represent the nearest and farthest TEs relative to the NT receiver.

Miscellaneous

Q41: Is the ±100 ppm free-run frequency recommendation met in the T7256?

A41: In the free-run mode, the output frequency is primarily dependent on the crystal, not the silicon design. For low-cost crystals, initial tolerance, temperature, and aging effects may account for two-thirds of this budget, and just a couple of pF of variation in load capacitance will use up the rest; therefore, the ±100 ppm goal can be met if the crystal parameters are well controlled. See the Crystal Characteristics section in this data sheet.

Q42: What happens if Co and Cm of the crystal differs from the specification shown in the Crystal Characteristics table?

A42: None of the parameters should be varied. We have not characterized any such crystals, and have no easy method of doing so. A crystal whose parameters deviate from the requirements may work in most applications but fail in isolated cases involving certain loop configurations or other system variations. Therefore, customers choosing to vary any of these parameters do so at their own risk.

Q43: It has been noted in some other designs that the crystal has a capacitor from each pin to ground. Changing these capacitances allows the frequency to be adjusted to compensate for board parasitics. Can this be done with the T7256 crystal? Also, can we use a crystal from our own manufacturer?

A43: For the T7256, these capacitors are located on the chip, so their values are fixed. The advantage to this is that no external components are required. The disadvantage is that board parasitics must be very small.

Questions and Answers (continued)

Miscellaneous (continued)

A43: (continued)

The crystal characteristics section of the data sheet notes that the board parasitics must be within the range of 0.6 pF ± 0.4 pF.

Q44: What clocks are available on the T7256?

A44: The following clocks are available and are always present once enabled, regardless of the state of activation on the U- or S/T-interfaces:

1. SYN8K, pin 4 (8 kHz clock) is enabled by holding SDI (pin 12) low during an external $\overline{\text{RESET}}$.
2. TDMCLK, pin 9 (2.048 MHz clock) is enabled by writing TDMEN = 0 (register GR2, bit 5).
3. CKOUT, pin 17 (10.24 MHz or 15.36 MHz clock) is enabled by writing register GRO bit 2 or 1, respectively, to 0. Normally 3-stated.

Note that using clocks 2 or 3 above requires a microprocessor for setting the appropriate configuration.

Q45: I plan to program the T7256 to output 15.36 MHz from its CKOUT pin. Is this clock a buffered version of the 15.36 MHz oscillator clock? I am concerned that if it is not buffered, the capacitive loading on this pin could affect the system clock frequency.

A45: The 15.36 MHz output is a buffered version of the XTAL clock and therefore hanging capacitance on it will not affect the T7256's system clock frequency.

Q46: How does the filtering at the OPTOIN input work?

A46: The signals applied to OPTOIN are digitally filtered for 20 ms. Any transitions under 20 ms will be ignored.

Q47: What is the isolation voltage of the 6N139 optoisolator used in the dc termination circuit of the T7256?

A47: 2500 VAC, 1 minute.

Q48: Can the T7256 operate with an external 15.36 MHz clock source instead of using a crystal?

A48: Yes, by leaving X1 disconnected and driving X2 with an external CMOS-level oscillator.

Q49: What is the effect of ramping down the power-supply voltage on the device? When will it provide a valid reset? This condition can occur when a line-powered NT1's line cord is repeatedly plugged in and removed and plugged in again before the power supply has had enough time to fully ramp-up.

A49: The device's reset is more dependent on the $\overline{\text{RESET}}$ pin than the power supply to the device. As long as the proper input conditions on the $\overline{\text{RESET}}$ pin (see Table 42) are met, the device will have a valid reset. Note that this input is a Schmitt-trigger input.

Q50: Is there a recommended method for powering the T7256? For example, is it desirable to separate the power supplies, etc.?

A50: The T7256 is not extremely sensitive to power-supply schemes. Following standard practices of decoupling power supplies close to the chip and, if power and ground planes are not used, keeping power traces away from high-frequency signals, etc., should yield acceptable results. Separating the T7256 analog power supplies from the digital power supplies near the chip may yield a small improvement, and the same holds true for using power and ground planes vs. discrete traces.

Note that if analog and digital power supplies are separated, the crystal power supply (V_{DDO}) should be tied to the digital supplies (V_{DDD}).

See the SCNTI Family Reference Design Board Hardware User Manual (MN96-011ISDN), Appendix A for an example of a board layout that performs well.

Q51: What are the filter characteristics of the PLL at the NT?

A51: The –3 dB frequency is approximately 5 Hz, peaking is about 1.2 dB.

Q52: Can the T7256 operate in the LT mode?

A52: No, the T7256 is optimized for the NT side of the loop and cannot operate in the LT mode.

Questions and Answers (continued)

Miscellaneous (continued)

Q53: Can you provide detailed information on the active and idle power consumption of the T7256?

A53: The IDLE power of the T7256 is typically 35 mW. The IDLE power will be increased if CKOUT or the TDM highway are active. The discussion below presents accurate numbers for adding in the effects of CKOUT and the TDM highway.

When considering active power measurement figures, it is important to note that the conditions under which power measurements are made are not always completely stated by 2B1Q IC vendors. For example, loop length is not typically mentioned in the context of power dissipation, yet power dissipation on a short loop is noticeably greater than on a long loop. There are two reasons for the increased power dissipation at shorter loop lengths:

1. The overall loop impedance is smaller, requiring a higher current to drive the loop.
2. The far-end transceiver is closer, requiring the near-end transceiver to sink more far-end current in order to maintain a virtual ground at its transmitter outputs.

The following lab measurements provide an example of how power dissipation varies with loop length for a specific T7256 with its 15.36 MHz CKOUT output disabled (see the following table for information on CKOUT). Note that power dissipation on a 0-length loop (the worst-case loop) is about 35 mW higher than on a loop of >3 kft length—a significant difference. Thus, loop length needs to be considered when determining worst-case power numbers.

Table 43. Power Dissipation Variation

Loop Configuration	Power (mW)
18 kft/26 awg	270
6 kft/26 awg	270
3 kft/26 awg	274
2 kft/26 awg	277
1 kft/26 awg	285
0.5 kft/26 awg	293
0 kft	305
135 Ω load, $\overline{\text{ILOSS}}$ or LPBK active, no far-end transceiver*	278

* This is the configuration used by some IC manufacturers.

Also, in the case of the T7256, the use of the output clock CKOUT (pin 17) needs to be considered since its influence on power dissipation is significant. Some applications may make use of this clock, while others may leave it 3-stated. The power dissipation of CKOUT is shown in Table 44.

Table 44. Power Dissipation of CKOUT

CKOUT Frequency (MHz)	Power Due to CKOUT 40 pF Load (mW)	Power Due to CKOUT No Load (mW)
15.36	21.3	11.0
10.24	17.7	9.1

Another factor influencing power consumption is the S/T-interface data pattern. For example, when transmitting an INFO 4 pattern with all 1s data in the B and D channels, the power consumption is 25 mW lower than it is when transmitting INFO 2, because INFO 2 is worst case in terms of the amount of +0 and –0 transitions, and INFO 4 is best case if the data is all 1s. A typical number would lie about midway between these two. The T7256 TDM highway, when active, can add another 3 mW of power.

Questions and Answers (continued)

Miscellaneous (continued)

A53: (continued)

Therefore, it is apparent that the conditions under which power is measured must be clearly specified. The methods Lucent has used to evaluate typical and worst-case power consumption are based on our commitment to provide our customers with accurate and reliable data. Measurements are performed as part of the factory test procedure using automated test equipment. Bench top tests are performed in actual T7256-based systems to correlate the automated test data with an actual implementation. A conservative margin is then added to the test results for publication in our data sheets.

The following table provides power-consumption data for several scenarios so that knowledgeable customers can fairly compare transceiver solutions. A baseline scenario is presented in the Case 1 column, and then adders are listed in the Cases 2—6 columns to account for the worst-case condition listed in each column so that an accurate worst-case figure can be determined based on the conditions that are present in a particular application. Note that the tests were run at 5 V, so changes in the supply voltage will change the power accordingly.

Table 45. Power Consumption

Variables	Baseline	Adders				
	Case 1	Case 2	Case 3	Case 4	Case 5	Case 6
Loop Configuration	>3 kft, 26 awg	0 kft*	—	—	—	—
S/T State	INFO 4 with all 1s data	—	INFO 2†	—	—	—
CKOUT, MHz (40 pF load)‡	3-stated	—	—	15.36	—	—
Temperature (°C)	25	—	—	—	85	—
TDM Highway	Inactive	—	—	—	—	Active
Typical Power Consumption (mW)	254	35	26	22	5	3

* Some 2B1Q silicon vendors specify power using a configuration in which the IC is active and transmitting into a 135 Ω termination, with no far-end transmitter attached. This configuration would cause an increase of 9 mW over the Case 1 column, instead of the 35 mW shown here. This highlights the importance of specifying measurement conditions accurately when making comparisons between chip vendors' power numbers.

† This is a worst-case number representing the state of the S/T-interface where the most +0/–0 transitions occur. In a real application, this will be a transient state, as INFO 4 will occur as soon as synchronization is achieved. The average power consumed during a typical INFO 4, assuming a 50% mix of 1s and 0s in the B and D channels, would be approximately half this number, or 13 mW.

‡ See the preceding table for a comparison of power dissipation with negligible capacitive loading on CKOUT. The 40 pF figure chosen here is intended to represent a worst-case condition.

Q54: What would cause the STLED indicator to flash sporadically at an 11 Hz rate?

A54: If the T7256 S/T-interface is operating over a long loop that is outside the range specified in the I.430/T1.605 standard, the T7256 may go into a state where it is constantly going in and out of synchronization. This causes it to cycle between ANSI states H7 and H8, producing STLED state changes between 1 Hz flashing and always on. When the S/T-interface loses synchronization, it takes about 96 ms before synchronization can be reacquired. This 96 ms cycle, coupled with the STLED switching from always on to 1 Hz flashing, can appear as 11 Hz or sporadic flashing, depending on how frequently S/T synchronization is being lost.

Questions and Answers (continued)

Miscellaneous (continued)

A54: (continued)

Either of these states could cause potential confusion to maintenance personnel in the event that a T7256-based NT1 is connected to an S/T loop that is longer than permitted by the standards. For example, an 11 Hz rate is difficult to visually distinguish from the 8 Hz rate, but the 11 Hz case indicates a problem on the S/T-interface and the 8 Hz case indicates a problem on the U-interface. To troubleshoot the STLED indication, unplug the S/T connector and repower the T7256 and initiate a start-up on the U-interface. If there is no problem on the U-interface, the STLED will reach a 1 Hz flashing state and remain there, indicating that the fast flashing was a result of S/T-interface problems.

Q55: The STLED on my T7256-based NT1 behaves in an unexpected way. When a start-up attempt is received, it flashes at an 8 Hz rate. Then it flashes briefly at 1 Hz, indicating synchronization on the U-interface. This is expected. However, after this, it starts flashing at 8 Hz, and yet it appears as though the system is operating fine (data is being passed end to end, etc.). Shouldn't the STLED signal be always low (i.e., ON) at this point?

A55: Yes it should. Referring to the STLED Control Flow diagram in Figure 18 of this data sheet, it appears as though you may be receiving aib = 0 from the upstream U-interface element. This will cause the behavior you are seeing. If you have access to the microprocessor registers, you can check this by monitoring register CFR1, bit 6 to see if it ever goes to 0.

Q56: We have equipment that operates fine against a 5ESS® switch, but never gets to layer 3 when operating against a Northern Telecom DMS-100 switch. The equipment uses the SCNT1 device talking to a Motorola MC68360 device over the TDM highway and serial μP port. We do not use the S/T-interface connection on the SCNT1—instead we originate and terminate the calls on the SCNT1 TDM highway. Do you have any idea what the problem may be?

A56: Some DMS-100 switches require that the upstream U-overhead bit sai (S/T-interface activity indicator) is set to 1 before they allow full transparency at layer 3. The state of the transmitted sai bit in the SCNT1 is controlled by register GR1, bits 7 & 8. The default state of these bits causes transmission of an sai that reflects the S/T-interface status. Since there is no TE connected in this particular product, sai = 0 is transmitted upstream to the switch by default. To override this value and force sai to 1 (which is necessary for transparency in this case), bit 7, 6 should be set to 0, 1, respectively. Note that the switch software in this case is not in accordance with ANSI T1.601-1992.

Q57: We are testing out T7256-based equipment against a Lucent SLC Series 5, and performance seems OK except that we get a burst of errors, and even drop calls, approximately every 15 minutes. Can you explain why?

A57: Check to make sure that your equipment is setting the ps1/ps2 power status bits correctly. The SLC equipment monitors the ps1/2 bits and, if they are both zero (meaning all power is lost), it assumes that there is some sort of terminal error, since this is not an appropriate steady-state value for ps1/2. When this condition is detected, the SLC deactivates and reactivates the line approximately every 15 minutes. This causes the symptoms you describe.

Q58: When I try to activate our T7256-based NT1, it appears as though the U-interface is synchronizing (i.e., STLED flashes at 1 Hz), but the S/T-interface won't activate, and there is not even any signal activity on the S/T-interface (i.e., no INFO 1 or INFO 2). What might the problem be?

A58: The behavior you have observed can be caused if the uoa bit received on the U-interface from the network is set to 0. This causes the T7256 to activate the U-interface only, keeping the S/T-interface quiet, per the ANSI and ETSI standards. We have heard of some network equipment that incorrectly sets this bit low. If you have access to the microprocessor registers, you can check this by monitoring register CFR1 bit 3 to see if it is low. If it is, the problem is in the network equipment, not your NT1.

Questions and Answers (continued)

Miscellaneous (continued)

Q59: What is the state of the T7256 TDM bus output when the unused bits of the D-channel octet are transmitted?

A59: The T7256 3-states the TDM bus output when B- and D-channel information is not transmitted to the TDM bus. This includes the 6-bit interval in the D-channel octet.

Q60: What is the purpose of the ACTSEL bit in register GR2 bit 6?

A60: This bit is to provide compatibility with the ANSI T1.601 and ETSI ETR 080 standards. The 1992 version of T1.601 (the most recent as of this writing) specifies that, upon a loopback 2 eoc request, the NT1's 2B+D data should be looped back immediately and the upstream (NT-to-LT) act bit should be set to 0. ANSI specified that the upstream act bit should be set to 0 to indicate to the LT that end-to-end data transparency (TE-to-LT) is interrupted during a loopback 2. The fact that 2B+D data is looped back immediately means that upstream data transparency at the NT is established independent of the status of the act bit from the LT. Normally, upstream data transparency at the NT is dependent on act = 1 being received from the LT. The reason that loopback 2 transparency criteria differ is that there is no guarantee that the NT1 will receive act = 1 from the LT. Consider the case where an LT wants to activate the U-interface and perform a loopback 2 test on an NT1 with no TE connected. In this case, the LT will never receive act = 1 since, prior to the loopback 2 request, act = 0 because there is no TE attached, and after the loopback 2 request, act = 0 because layer 1 transparency is interrupted. Since the LT will never receive act = 1 from the NT1, it will never send act = 1 back to the NT1. Since the NT1 receipt of act = 1 normally enables upstream transparency, ANSI chose to make an exception to the data transparency requirements in this case and enable upstream transparency immediately upon receipt of the loopback 2 eoc command at the NT1.

The major difference between the ANSI and ETSI standards with regard to how the NT1 handles a loopback 2 request lies in what happens to the upstream act bit. ANSI's position is that act should be set to 0 because a loopback 2 is an interruption to layer 1 transparency. ETSI's position is that the state of the act bit should only be dependent on whether or not the NT1 is receiving INFO 3 from the TE (this is consistent with ANSI T1.601 paragraph 6.4.6.4 and ETSI ETR 080 paragraph A.10.1.5.1). During a loopback 2, the T7256 will always receive INFO 3 at the S/T-interface (even if there is no TE attached) because it loops back its S/T transmit signal and synchronizes itself to that signal. Therefore, the possibility that LT will never receive act = 1 from the NT does not exist under these rules. As a result, no special exceptions need to be applied to the case of loopback 2 in ETSI. For example, again consider the case where an LT wants to activate the U-interface and perform a loopback 2 test on an NT1 with no TE connected. The NT1 will synchronize to its own S/T signal and detect INFO 3. This will cause act = 1 to be transmitted upstream. The LT will detect act = 1 and set its downstream act = 1. When the NT detects the downstream act = 1, it will enable upstream data transparency. The handling of the act bit and transparency in this case is the same as for a normal activation.

In the ETSI standard, transparency at the NT during loopback 2 is dependent upon the reception of the act bit from the LT, i.e., if act = 1, loopback transparency is established, and if act = 0, loopback data is forced to all 1s. The LT won't send act = 1 until it receives act = 1 from the NT. The NT will not send act = 1 to the LT until it receives an INFO 3 indication (i.e., until its S/T-interface is synchronized as described in the register GR2 ACTSEL bit definition). Thus, data transparency requires that the NT1 set its upstream act bit to 1.

There is a contribution that has been voted onto the ANSI T1E1.4 living list that changes the act bit behavior during loopback 2 to match that specified for ETSI (contribution #T1E1.4/92-089). Thus, the next issue of the T1.601 standard will bring the ANSI and ETSI standards into harmony as pertains to handling of the act bit during a loopback 2.

Glossary

ACTMODE/$\overline{\text{INT}}$: Act bit mode, serial interface microprocessor interrupt.

ACTR: Receive activation (register CFR1, bit 0).

ACTSC: Activation/deactivation state change on U-interface (register UIR0, bit 1).

ACTSCM: Activation/deactivation state change on U-interface interrupt mask (register UIR1, bit 1).

ACTSEL: Act mode select (register GR2, bit 6).

ACTT: Transmit activation (register GR1, bit 4).

AFRST: Adaptive filter reset (register CFR0, bit 1).

AIB: Alarm indication bit (register CFR1, bit 6).

ANSI: American National Standards Institute.

ASI: Alternate space inversion.

AUTOACT: Automatic activation control (register GR0, bit 6).

AUTOCTL: Auto control enable (register GR0, bit 3).

AUTOEOC: Automatic eoc processor enable (register GR0, bit 4).

A[3:1]R: Receive eoc address (register ECR2, bits 0—2).

A[3:1]T: Transmit eoc address (register ECR0, bits 0—2).

BERR: Block error on U-interface (register UIR0, bit 2).

BERRM: Block error on U-interface interrupt mask (register UIR1, bit 2).

CCRC: Corrupt cyclic redundancy check (register ECR0, bit 7).

CDM: Charged-device model.

CFR0: Control flow state machine control—maintenance/reserved bits register.

CFR1: Control flow state machine status register.

CFR2: Control flow state machine status—reserved bits register.

CKOUT: Clock output.

CODEC: Coder/decoder, typically used for analog-to-digital conversions or digital-to-analog conversions.

CRATE[1:0]: CKOUT rate control (register GR0, bits 2—1).

CRC: Cyclic redundancy check.

DFR0: Data flow control—U and S/T B-channels register.

DFR1: Data flow control—D-channels and TDM bus register.

DMR: Receive eoc data or message indicator (register ECR2, bit 3).

DMT: Transmit eoc data or message indicator (register ECR0, bit 3).

DPGS: Digital pair gain system.

ECR0: eoc state machine control—address register.

ECR2: eoc state machine status—address register.

ECR3: eoc state machine status—information register.

EMINT: Exit maintenance mode interrupt (register MIR0, bit 2).

EMINTM: Exit maintenance mode interrupt mask (register MIR1, bit 2).

EOC: Embedded operations channel.

EOCSC: eoc state change on U-interface (register UIR0, bit 0).

EOCSCM: eoc state change on U-interface mask (register UIR1, bit 0).

Glossary (continued)

ERC1: eoc state machine control—information register.

ESD: Electrostatic discharge.

ETSI: European Telecommunications Standards Institute.

FEBE: Far-end block error (register CFR1, bit 5).

FSC[2:0]: Frame strobe (FS) control, (register TDR0, bits 2—0).

FSP: Frame strobe (FS) polarity (register TDR0, bit 3).

FT: Fixed/adaptive timing control (register GR2, bit 0).

FTE/TDMDI: Fixed/adaptive timing mode select.

GIR0: Global interrupt register.

GND_A: Analog ground.

GND_O: Crystal oscillator ground.

GR0: Global device control—device configuration register.

GR1: Global device control—U-interface register.

GR2: Global device control—S/T-interface register.

HBM: Human-body model.

HDLC: High-level data link control.

$\overline{\text{HIGHZ}}$: High impedance control.

HN: Hybrid negative input for U-interface.

HP: Hybrid positive input for U-interface.

I4C: INFO 4 change (register SIR0, bit 3).

I4CM: INFO 4 change mask (register SIR1, bit 3).

I4I: INFO 4 indicator (register CFR1, bit 7).

ILINT: Insertion loss interrupt (register MIR0, bit 1).

ILINTM: Insertion loss interrupt mask (register MIR1, bit 1).

ILOSS: Insertion loss test control (register CFR0, bit 0).

$\overline{\text{ILOSS}}$: Insertion loss test control.

ISDN: Integrated services digital network.

ITU-T: International Telecommunication Union-Telecommunication Sector.

I[8:1]R: Receive eoc information (register ECR3, bits 0—7).

I[8:1]T: Transmit eoc information (register ERC1, bits 0—7).

LON: Line driver negative output for U-interface.

LOP: Line driver positive output for U-interface.

LPBK: U-interface analog loopback (register GR1, bit 0).

MCR0: Q-channel bits register.

MCR1: S subchannel 1 register.

MCR2: S subchannel 2 register.

MCR3: S subchannel 3 register.

MCR4: S subchannel 4 register.

MCR5: S subchannel 5 register.

MINT: Maintenance interrupt (register GIR0, bit 2).

MIR0: Maintenance interrupt register.

MIR1: Maintenance interrupt mask register.

MLT: Metallic loop termination.

MULTIF: Multiframing control (register GR0, bit 5).

NEBE: Near-end block error (register CFR1, bit 4).

NTM: NT test mode (register GR1, bit 3).

OOF: Out of frame (register CFR1, bit 2).

OPTOIN: Optoisolator input.

OUSC: Other U-interface state change (register UIR0, bit 3).

Glossary (continued)

OUSCM: Other U-interface state change mask (register UIR1, bit 3).

PS1: Power status #1 (register GR1, bit 2).

PS1E/TDMDO: Power status #1, TDM clock.

PS2: Power status #2 (register GR1, bit 1).

PS2E/TDMCLK: Power status #2, TDM data out.

QMINT: Quiet mode interrupt (register MIR0, bit 0).

QMINTM: Quiet mode interrupt mask (register MIR1, bit 0).

QSC: Q-bits state change (register SIR0, bit 1).

QSCM: Q-bits state change mask (register SIR1, bit 1).

Q[4:1]: Q-channel bits (register MCR0, bits 0—3).

R25R: Receive reserved bits (register CFR2, bit 2).

R25T: Transmit reserved bit (register CFR0, bit 4).

R64T: Transmit reserved bit (register CFR0, bit 5).

$\overline{\text{RESET}}$: Reset.

RNR: Receive negative rail for S/T-interface.

RPR: Receive positive rail for S/T-interface.

RSFINT: Receive superframe interrupt (register UIR0, bit 4).

RSFINTM: Receive superframe interrupt mask (register UIR1, bit 4).

R[16:15]R: Receive reserved bits (register CFR2, bits 1—0).

R[16:15]T: Transmit reserved bits (register CFR0, bits 3—2).

R[64:54:44:34]R: Receive reserved bits (register CFR2, bits 6—3).

SAI[1:0]: S/T-interface activity indicator control (register GR1, bits 6—7).

SC1[4:1]: S subchannel 1 (register MCR1, bits 0—3).

SC2[4:1]: S subchannel 2 (register MCR2, bits 0—3).

SC3[4:1]: S subchannel 3 (register MCR3, bits 0—3).

SC4[4:1]: S subchannel 4 (register MCR4, bits 0—3).

SC5[4:1]: S subchannel 5 (register MCR5, bits 0—3).

SCK: Serial interface clock.

SDI: Serial interface data input.

SDINN: Sigma-delta A/D negative input for U-interface.

SDINP: Sigma-delta A/D positive input for U-interface.

SDO: Serial interface data output.

SFECV: S-channel far-end code violation (register SIR0, bit 2).

SFECVM: S-subchannel far-end code violation mask (register SIR1, bit 2).

SINT: S/T-transceiver interrupt (register GIR0, bit 1).

SIR0: S/T-interface interrupt register.

SIR1: S/T-interface interrupt mask register.

SOM: Start of multiframe (register SIR0, bit 0).

SOMM: Start of multiframe mask (register SIR1, bit 0).

SPWRUD: S/T-interface powerdown control (register GR2, bit 1).

SRESET: S/T-interface reset (register GR2, bit 2).

STLED: Status LED driver.

STOA: S/T-only activation (register GR2, bit 7).

Superframe: Eight U-frames grouped together.

Glossary (continued)

SXB1[1:0]: S/T-interface transmit path source for B1 channel (register DFR0, bits 5—4).

SXB2[1:0]: S/T-interface transmit path source for B2 channel (register DFR0, bits 7—6).

SXD: S/T-interface transmit path source for D channel (register DFR1, bit 1).

SXE: S/T-interface D-channel echo bit control (register GR2, bit 3).

SYN8K/LBIND/FS: Synchronous 8 kHz clock or loopback indicator, frame strobe.

TDM: Time-division multiplexed.

TDMB1S: TDM bus transmit control for B1 channel from S/T-interface (register DFR1, bit 2).

TDMB1U: TDM bus transmit control for B1 channel from U-interface (register DFR1, bit 5).

TDMB2S: TDM bus transmit control for B2 channel from S/T-interface (register DFR1, bit 3).

TDMB2U: TDM bus transmit control for B2 channel from U-interface (register DFR1, bit 6).

TDMDS: TDM bus transmit control for D channel from S/T-interface (register DFR1, bit 4).

TDMDU: TDM bus transmit control for D channel from U-interface (register DFR1, bit 7).

TDMEN: TDM bus select (register GR2, bit 5).

TDR0: TDM bus timing control register.

TNR: Transmit negative rail for S/T-interface.

TPR: Transmit positive rail for S/T-interface.

TSFINT: Transmit superframe interrupt (register UIR0, bit 5).

TSFINTM: Transmit superframe interrupt mask (register UIR1, bit 5).

U frame: An 18-bit synchronous word.

U2BDLN: Nontransparent 2B+D loopback control (register GR2, bit 4).

U2BDLT: Transparent 2B+D loopback control (register ECR0, bit 6).

UB1LP: U-interface loopback of B1 channel control (register ECR0, bit 4).

UB2LP: U-interface loopback of B2 channel control (register ECR0, bit 5).

UINT: U-transceiver interrupt (register GIR0, bit 0).

UIR0: U-interface interrupt register.

UIR1: U-interface interrupt mask register.

UOA: U-interface only activation, (register CFR1, bit 3).

UXB1[1:0]: U-interface transmit path source for B1 channel (register DFR0, bits 1—0).

UXB2[1:0]: U-interface transmit path source for B2 channel (register DFR0, bits 3—2).

UXD: U-interface transmit path source for D channel (register DFR1, bit 0).

V_{DDA}: Analog power.

V_{DDO}: Crystal oscillator power.

VRCM: Common-mode voltage reference for U-interface circuits.

VRN: Negative voltage reference for U-interface circuits.

VRP: Positive voltage reference for U-interface circuits.

X1: Crystal #1.

X2: Crystal #2.

XACT: U-transceiver active (register CFR1, bit 1).

XPCY: Transparency (register GR1, bit 5).

Standards Documentation

Telecommunication technical standards and reference documentation may be obtained from the following organizations:

ANSI (U.S.A.):

American National Standards Institute (ANSI)

11 West 42nd Street
New York, New York 10036

Tel: 212-642-4900
FAX: 212-302-1286

Lucent Technologies Publications:

Lucent Technologies Customer Information Center (CIC)

Tel: 800-432-6600
FAX: 800-566-9568 (in U.S.A.)
FAX: 317-322-6484 (outside U.S.A.)

Bellcore (U.S.A.):

Bellcore Customer Service

8 Corporate Plaza
Piscataway, New Jersey 08854

Tel: 800-521-CORE (in U.S.A.)
Tel: 908-699-5800
FAX: 212-302-1286

ITU-T:

International Telecommunication Union-Telecommunication Sector

Place des Nations
CH 1211
Geneve 20, Switzerland

Tel: 41-22-730-5285
FAX: 41-22-730-5991

ETSI:

European Telecommunications Standards Institute

BP 152
F-06561 Valbonne Cedex, France

Tel: 33-92-94-42-00
FAX: 33-93-65-47-16

TTC (Japan):

TTC Standard Publishing Group of the Telecommunications Technology Committee

2nd Floor, Hamamatsucho-Suzuki Building,
1 2-11, Hamamatsu-cho, Minato-ku, Tokyo

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Notes

Notes

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