

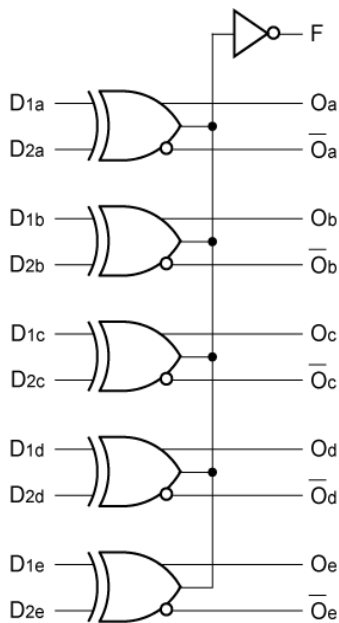
FEATURES

- Max. propagation delay of 1000ps
- IEE min. of -58mA
- Extended supply voltage option:
VEE = -4.2V to -5.5V
- Voltage and temperature compensation for improved noise immunity
- Internal 75kΩ input pull-down resistors
- 50% faster than Fairchild 300K at lower power
- Function and pinout compatible with Fairchild F100K
- Available in 28-pin PLCC package

DESCRIPTION

The SY100S307 is an ultra-fast quint exclusive-OR/NOR gate designed for use in high-performance ECL systems. A function output that is the wire-OR result of the exclusive-OR outputs is also available. The inputs on the device have 75kΩ pull-down resistors.

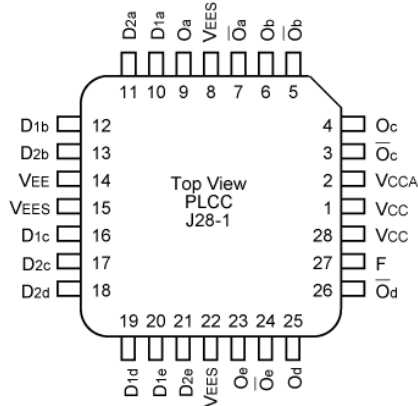
BLOCK DIAGRAM



PIN NAMES

Pin	Function
Dna – Dne	Data Inputs (n-1...5)
E	Enable Input
Oa – Oe	Data Outputs
Oa – Oe	Complementary Data Outputs
VEES	VEE Substrate
VCCA	Vcco for ECL Outputs

PACKAGE/ORDERING INFORMATION



28-Pin PLCC (J28-1)

Ordering Information

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY100S307JC	J28-1	Commercial	SY100S307JC	Sn-Pb
SY100S307JCTR ⁽¹⁾	J28-1	Commercial	SY100S307JC	Sn-Pb
SY100S307JZ ⁽²⁾	J28-1	Commercial	SY100S307JZ with Pb-Free bar-line indicator	Matte-Sn
SY100S307JZTR ^(1,2)	J28-1	Commercial	SY100S307JZ with Pb-Free bar-line indicator	Matte-Sn
SY100S307JY ⁽²⁾	J28-1	Industrial	SY100S307JY with Pb-Free bar-line indicator	Matte-Sn
SY100S307JYTR ^(1,2)	J28-1	Industrial	SY100S307JY with Pb-Free bar-line indicator	Matte-Sn

Notes:

1. Tape and Reel.
2. Pb-Free package is recommended for new designs.

LOGIC EQUATION

$$F = (D1a \oplus D2a) + (D1b \oplus D2b) + (D1c \oplus D2c) + (D1d \oplus D2d) + (D1e \oplus D2e).$$

DC ELECTRICAL CHARACTERISTICS

$V_{EE} = -4.2V$ to $-5.5V$ unless otherwise specified, $V_{CC} = V_{CCA} = GND$

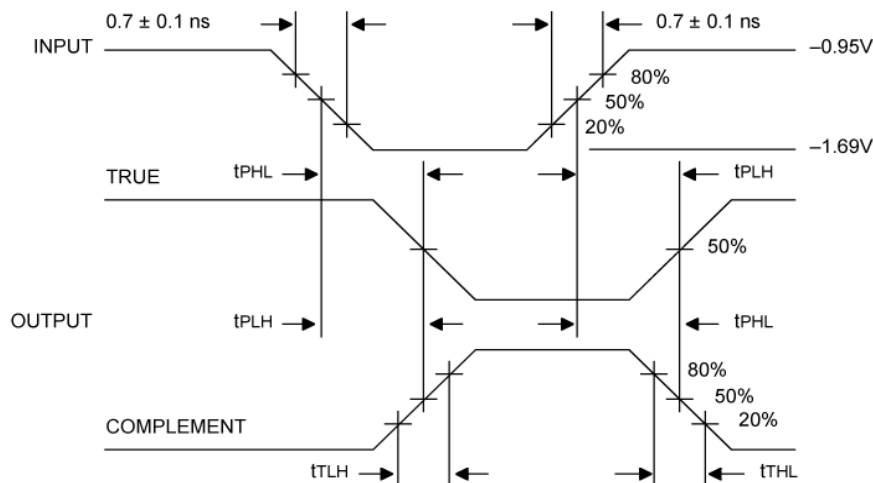
Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
I_{IH}	Input HIGH Current D2a — D2e D2a — D2e	—	—	200 250	μA	$V_{IN} = V_{IH} (Max.)$
I_{EE}	Power Supply Current	-58	-40	-27	mA	Inputs Open

AC ELECTRICAL CHARACTERISTICS

$V_{EE} = -4.2V$ to $-5.5V$ unless otherwise specified, $V_{CC} = V_{CCA} = GND$

Symbol	Parameter	$T_A = -40^\circ C$		$T_A = 0^\circ C$		$T_A = +25^\circ C$		$T_A = +85^\circ C$		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
t_{PLH} t_{PH2}	Propagation Delay D2a — D2e to O, \bar{O}	300	1000	300	1000	300	1000	300	1000	ps	
t_{PLH} t_{PHL}	Propagation Delay D1a — D1e to O, \bar{O}	300	900	300	900	300	900	300	930	ps	
t_{PLH} t_{PHL}	Propagation Delay Data to F	300	1425	300	1425	300	1425	300	1425	ps	
t_{TLH} t_{THL}	Transition Time 3 20% to 80%, 80% to 20%	00	900	00	900	300	900	300	900	ps	

TIMING DIAGRAM

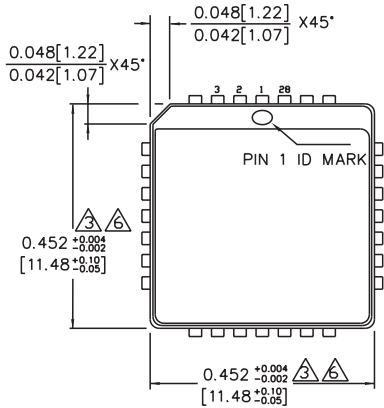


Propagation Delay and Transition Times

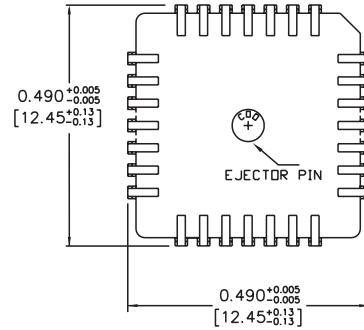
NOTE:

$V_{EE} = -4.2V$ to $-5.5V$ unless otherwise specified, $V_{CC} = V_{CCA} = GND$

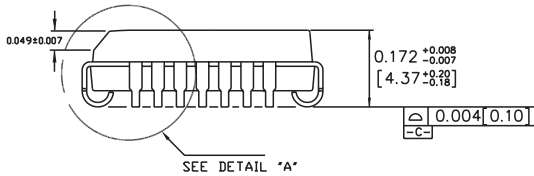
28-PIN PLCC (J28-1)



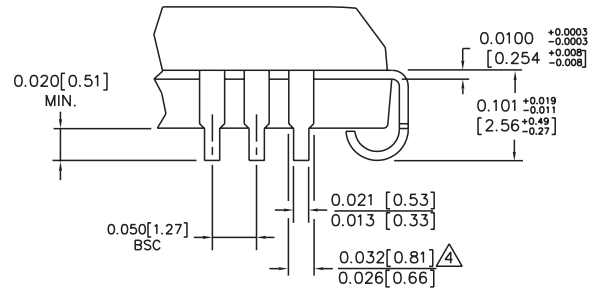
TOP VIEW



BOTTOM VIEW



SIDE VIEW



DETAIL "A"

NOTES:

1. DIMENSIONS ARE IN INCHES [MM].
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, EITHER OF WHICH SHALL NOT EXCEED 0.008 [0.203].
4. LEAD DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION.
5. MAXIMUM AND MINIMUM SPECIFICATIONS ARE INDICATED AS FOLLOWS: MAX/MIN
6. PACKAGE TOP DIMENSION MAY BE SLIGHTLY SMALLER THAN BOTTOM DIMENSION.

Rev. A

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