P-Channel 80-V (D-S) 175 °C MOSFET

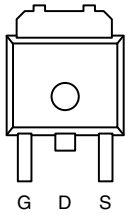
PRODUCT SUMMARY			
V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)[a]	Q_g (Typ)
- 80	0.026 at V_{GS} = - 10 V	- 50	102 nC

FEATURES

- TrenchFET® Power MOSFET

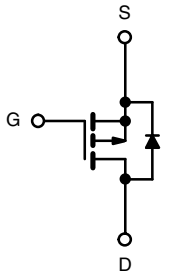
RoHS COMPLIANT

TO-252



Top View

Drain Connected to Tab



P-Channel MOSFET

Ordering Information: SUD50P08-26-E3 (Lead (Pb)-free)

ABSOLUTE MAXIMUM RATINGS T_A = 25 °C, unless otherwise noted				
Parameter		**Symbol**	**Limit**	**Unit**
Drain-Source Voltage		V_{DS}	- 80	V
Gate-Source Voltage		V_{GS}	± 20	
Continuous Drain Current (T_J = 175 °C)	T_C = 25 °C	I_D	- 50[a]	A
	T_C = 70 °C		- 43.6[a]	
	T_A = 25 °C		- 12.9[b, c]	
	T_A = 70 °C		- 10.8[b, c]	
Pulsed Drain Current		I_{DM}	- 60	
Continuous Source-Drain Diode Current	T_C = 25 °C	I_S	- 50[a]	
	T_A = 25 °C		- 6.9[b, c]	
Avalanche Current	L = 0.1 mH	I_{AS}	- 45	
Single-Pulse Avalanche Energy		E_{AS}	101	mJ
Maximum Power Dissipation	T_C = 25 °C	P_D	136	W
	T_C = 70 °C		95	
	T_A = 25 °C		8.3[b, c]	
	T_A = 70 °C		5.8[b, c]	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	- 55 to 175	°C

THERMAL RESISTANCE RATINGS					
Parameter		**Symbol**	**Typical**	**Maximum**	**Unit**
Maximum Junction-to-Ambient[b, d]	t ≤ 10 sec	R_{thJA}	15	18	°C/W
Maximum Junction-to-Case (Drain)	Steady State	R_{thJC}	0.85	1.1	

Notes:
a. Package limited.
b. Surface Mounted on 1" x 1" FR4 board.
c. t = 10 sec.
d. Maximum under Steady State conditions is 40 °C/W.

SPECIFICATIONS T_J = 25 °C, unless otherwise noted						
Parameter	**Symbol**	**Test Conditions**	**Min**	**Typ**	**Max**	**Unit**
Static						
Drain-Source Breakdown Voltage	V_{DS}	V_{GS} = 0 V, I_D = - 250 µA	- 80			V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	I_D = - 250 µA		- 80		mV/°C
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$			7.5		
Gate-Source Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = - 250 µA	- 2	- 3	- 4	V
Gate-Source Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ± 20 V			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = - 80 V, V_{GS} = 0 V			- 1	µA
		V_{DS} = - 80 V, V_{GS} = 0 V, T_J = 55 °C			- 10	
On-State Drain Current[a]	$I_{D(on)}$	$V_{DS} \geq$ 5 V, V_{GS} = - 10 V				A
Drain-Source On-State Resistance[a]	$r_{DS(on)}$	V_{GS} = - 10 V, I_D = - 12.9 A		0.022	0.026	Ω
Forward Transconductance[a]	g_{fs}	V_{DS} = - 15 V, I_D = - 12.9 A		39		S
Dynamic[b]						
Input Capacitance	C_{iss}	V_{DS} = - 40 V, V_{GS} = 0 V, f = 1 MHz		5160		pF
Output Capacitance	C_{oss}			320		
Reverse Transfer Capacitance	C_{rss}			220		
Total Gate Charge	Q_g	V_{DS} = - 40 V, V_{GS} = - 10 V, I_D = - 12.9 A		102	155	nC
Gate-Source Charge	Q_{gs}			22		
Gate-Drain Charge	Q_{gd}			29		
Gate Resistance	R_g	f = 1 MHz		4		Ω
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = - 40 V, R_L = 3.7 Ω $I_D \cong$ - 10.8 A, V_{GEN} = - 10 V, R_g = 1 Ω		15	25	ns
Rise Time	t_r			50	75	
Turn-Off Delay Time	$t_{d(off)}$			90	135	
Fall Time	t_f			65	100	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	T_C = 25 °C			- 50	A
Pulse Diode Forward Current[a]	I_{SM}				- 60	
Body Diode Voltage	V_{SD}	I_S = - 10.8 A		- 0.8	- 1.2	V
Body Diode Reverse Recovery Time	t_{rr}	I_F = - 10.8 A, di/dt = 100 A/µs, T_J = 25 °C		60	90	ns
Body Diode Reverse Recovery Charge	Q_{rr}			150	235	nC
Reverse Recovery Fall Time	t_a			45		ns
Reverse Recovery Rise Time	t_b			15		

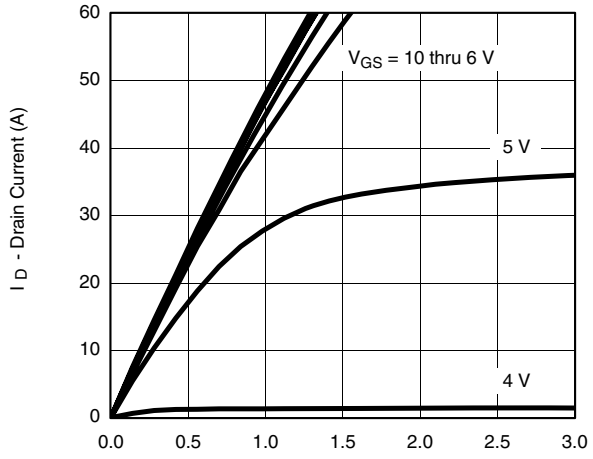
Notes:

a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %.

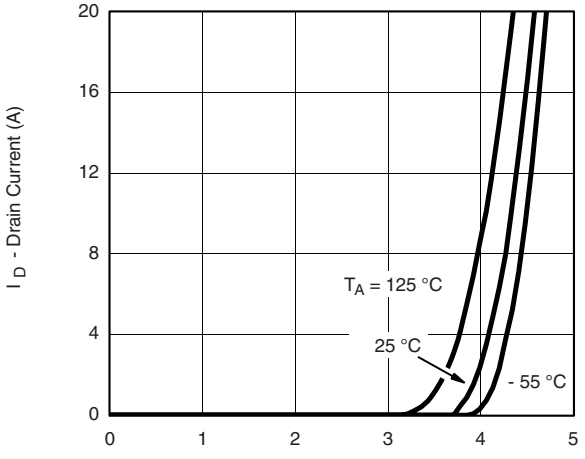
b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

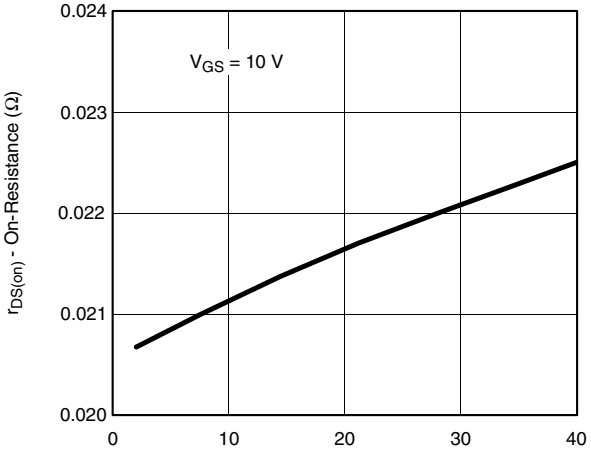
TYPICAL CHARACTERISTICS 25 °C unless noted



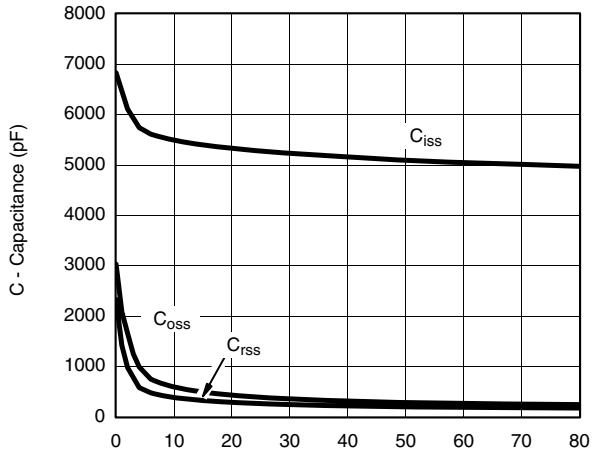
Output Characteristics



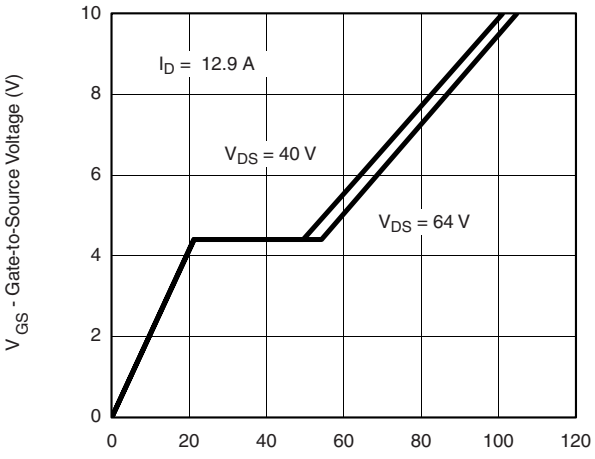
Transfer Characteristics



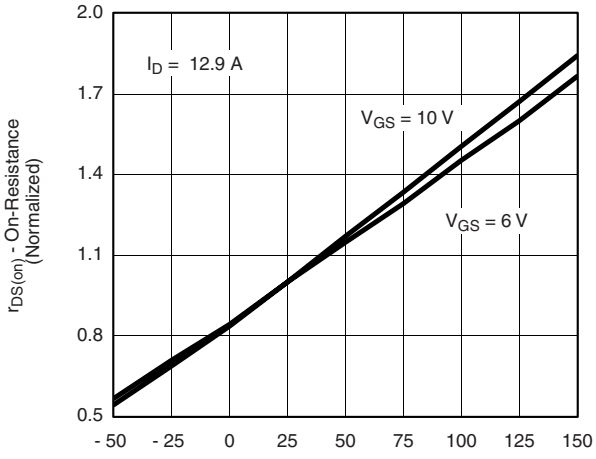
On-Resistance vs. Drain Current



Capacitance

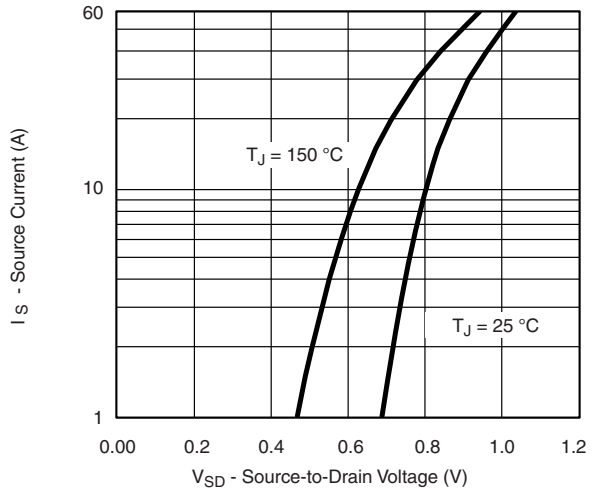


Q_g - Gate Charge

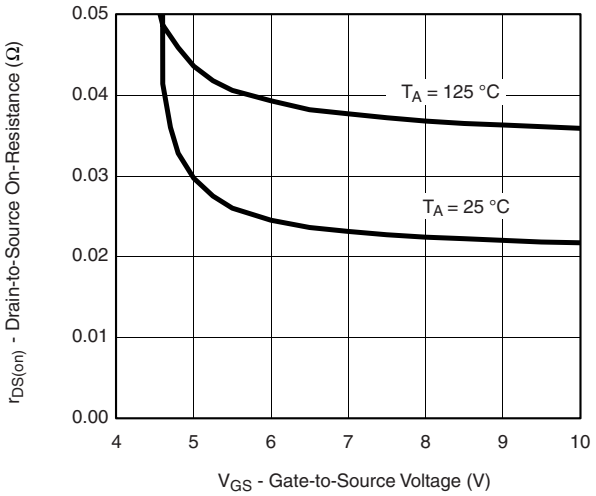


On-Resistance vs. Junction Temperature

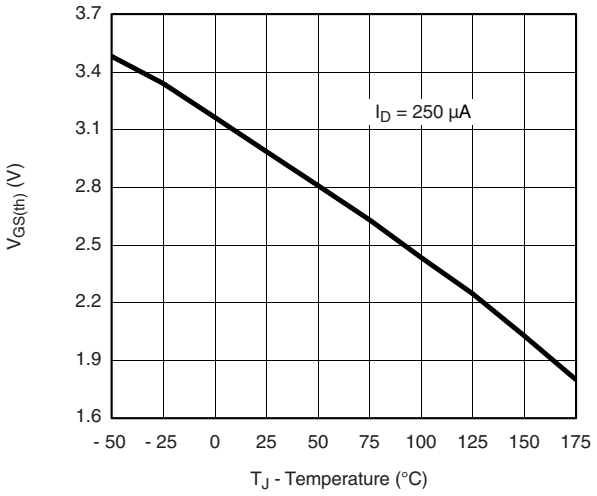
TYPICAL CHARACTERISTICS 25 °C unless noted



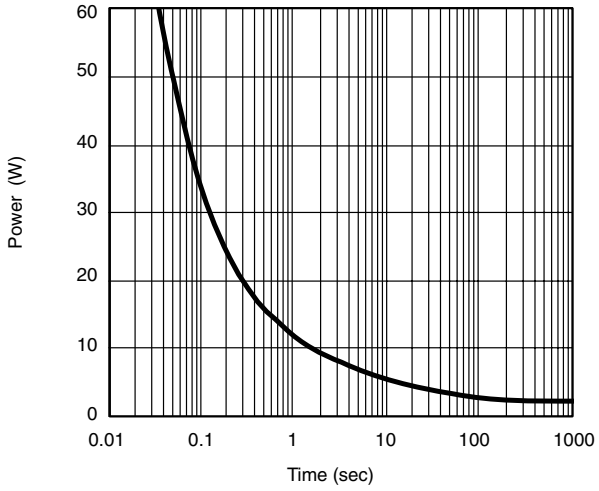
Source-Drain Diode Forward Voltage



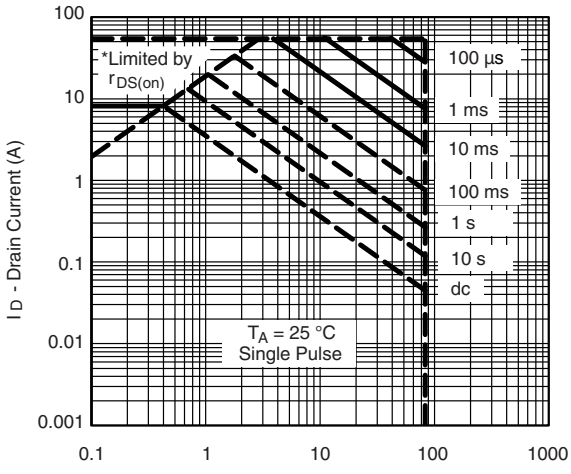
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



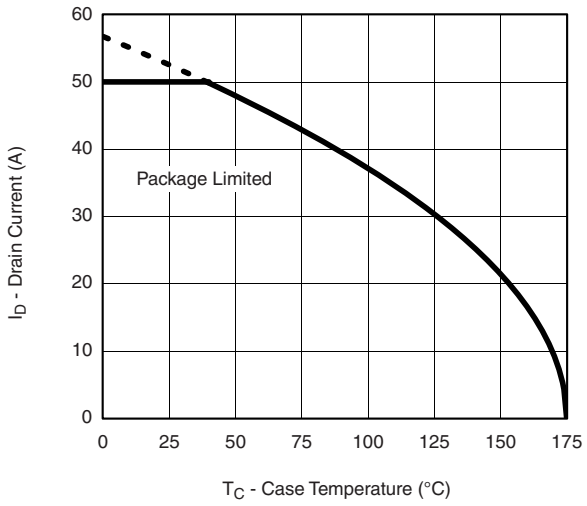
Single Pulse Power, Junction-to-Ambient



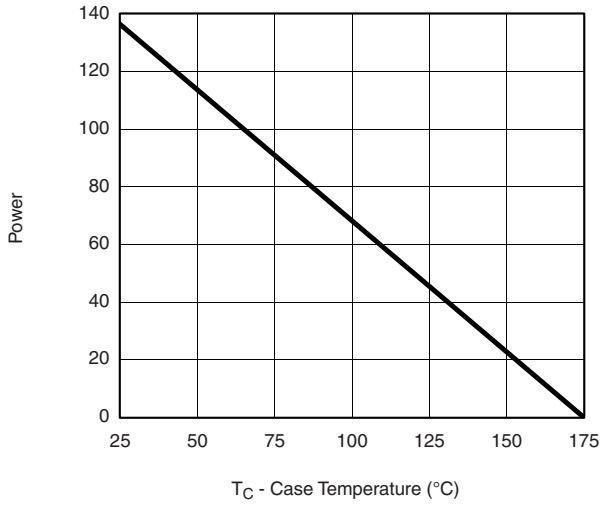
*V_{GS} > minimum V_{GS} at which $r_{DS(on)}$ is specified

Safe Operating Area, Junction-to-Ambient

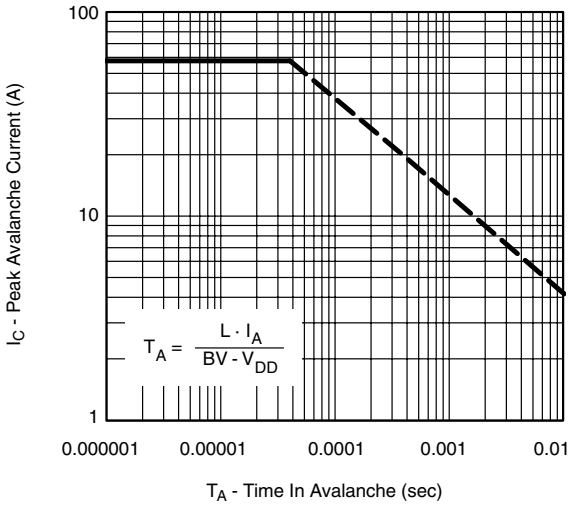
TYPICAL CHARACTERISTICS 25 °C unless noted



Current Derating*



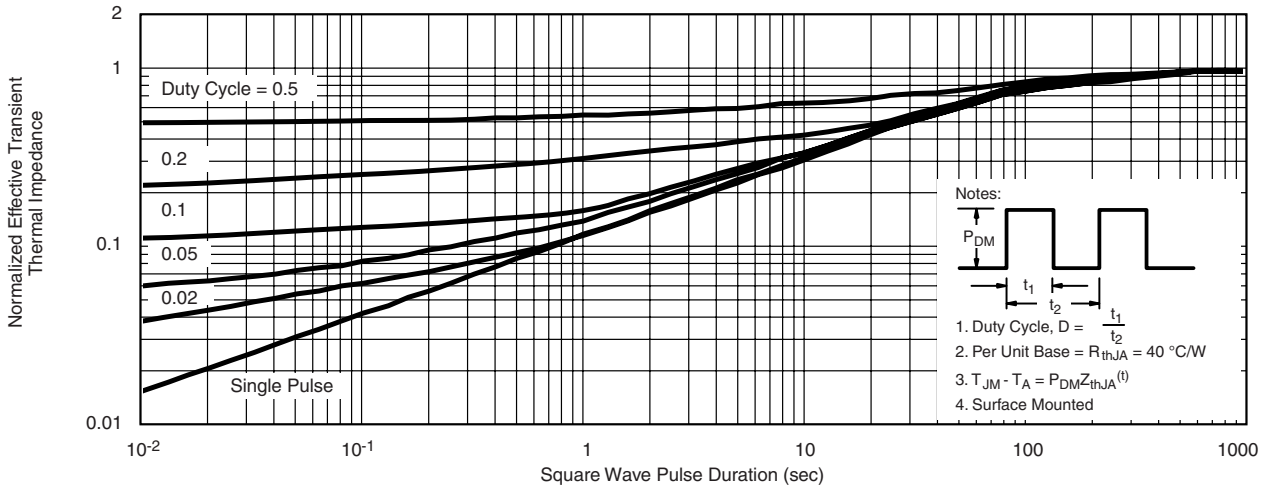
Power Derating



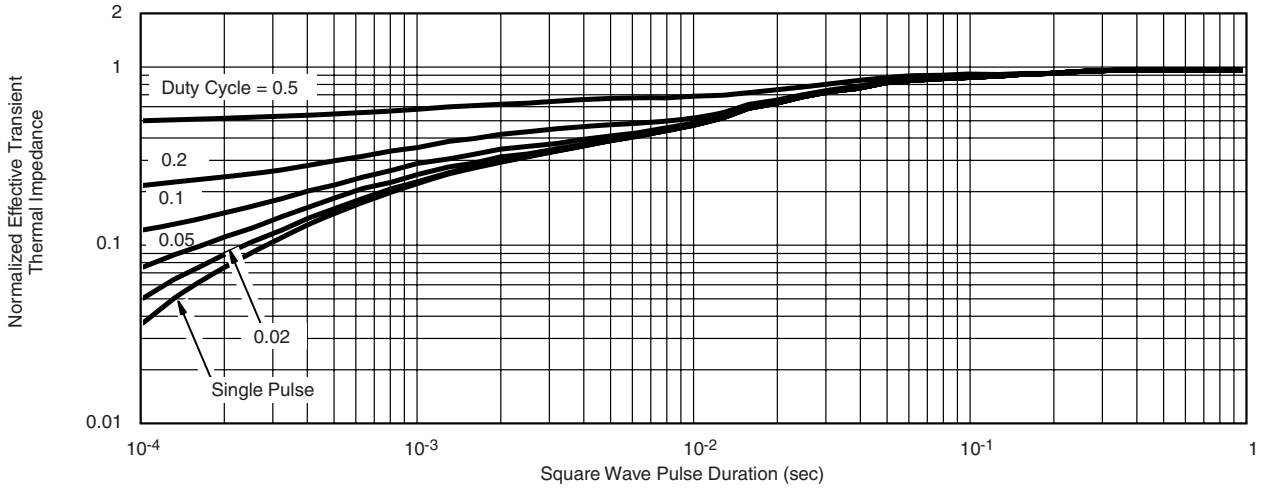
Single Pulse Avalanche Capability

*The power dissipation P_D is based on $T_{J(max)}$ = 175 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

TYPICAL CHARACTERISTICS 25 °C unless noted



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

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