



STV8164

+5 V, +5 V and Adjustable Triple-Voltage Regulator with Disable and Reset Functions

FEATURES

- Input Voltage range between 7V and 18V, limited to $V_{OUT} + 6.5V$
- Maximum Available Output Currents greater than 0.8 A
- Fixed Precision Output 1 voltage of $5 V \pm 2%$ (at 10 mA)
- Fixed Precision Output 2 voltage of $5 V \pm 2%$ (at 10 mA)
- Programmable Output 3 voltage: 2.5 to 16 V $\pm 2%$
- Output 1 with Reset facility
- Outputs 2 and 3 can be disabled by digital input
- Short Circuit Protection on each output
- Thermal Protection
- Low Dropout Voltages

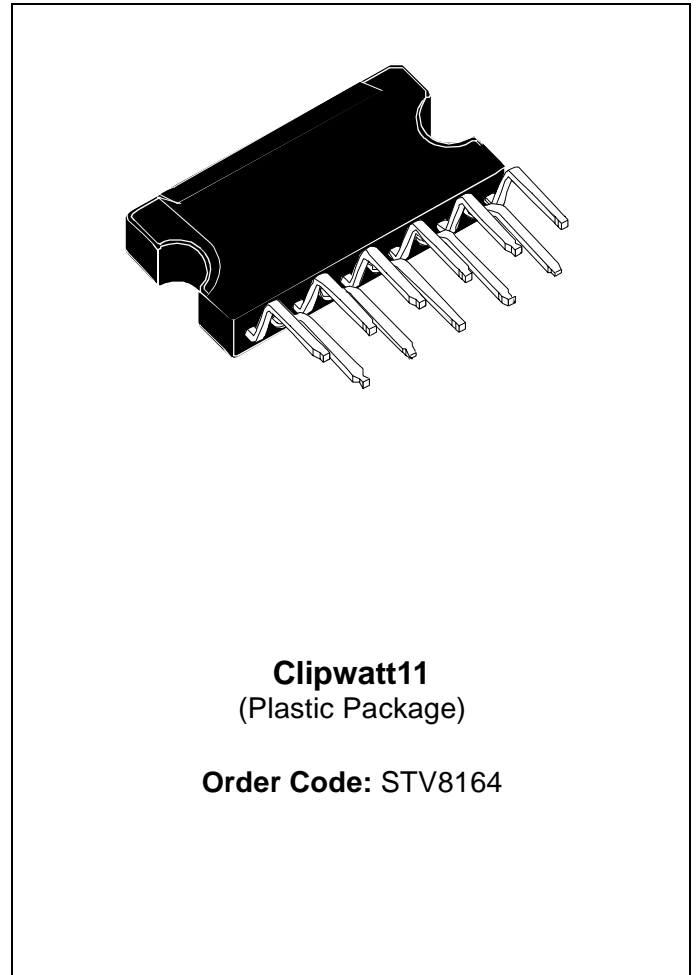
DESCRIPTION

The STV8164 is a monolithic triple positive voltage regulator designed to provide two fixed precision output voltages of 5 V and an adjustable voltage for currents up to 0.6 A.

The adjustable value of the third output can be fixed from 2.5 V to 16 V.

An internal reset circuit generates a reset pulse when the voltage of Output 1 drops below the regulated voltage value.

Outputs 2 and 3 can be disabled by a digital input.



Short-circuit and thermal protections are included in all versions.

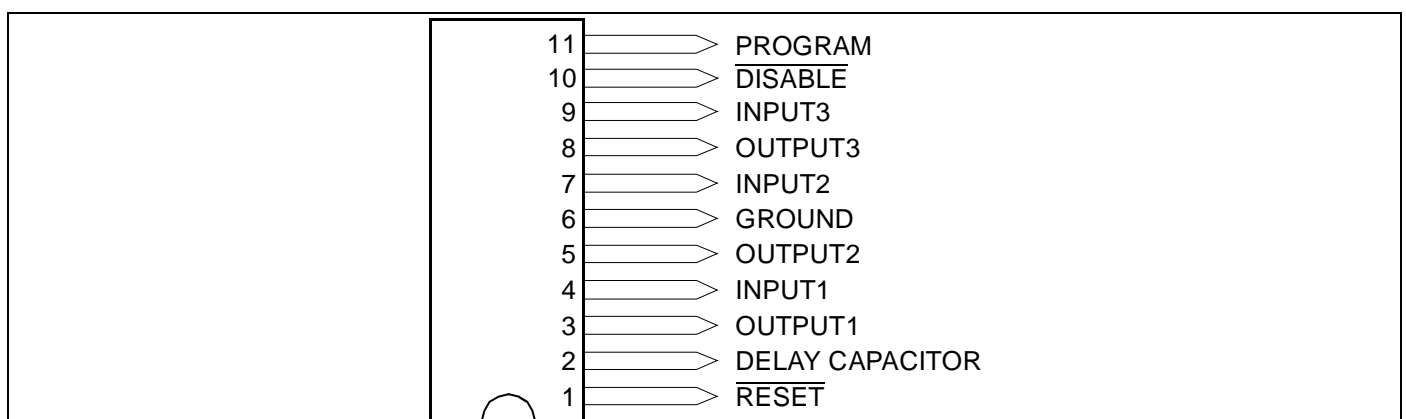
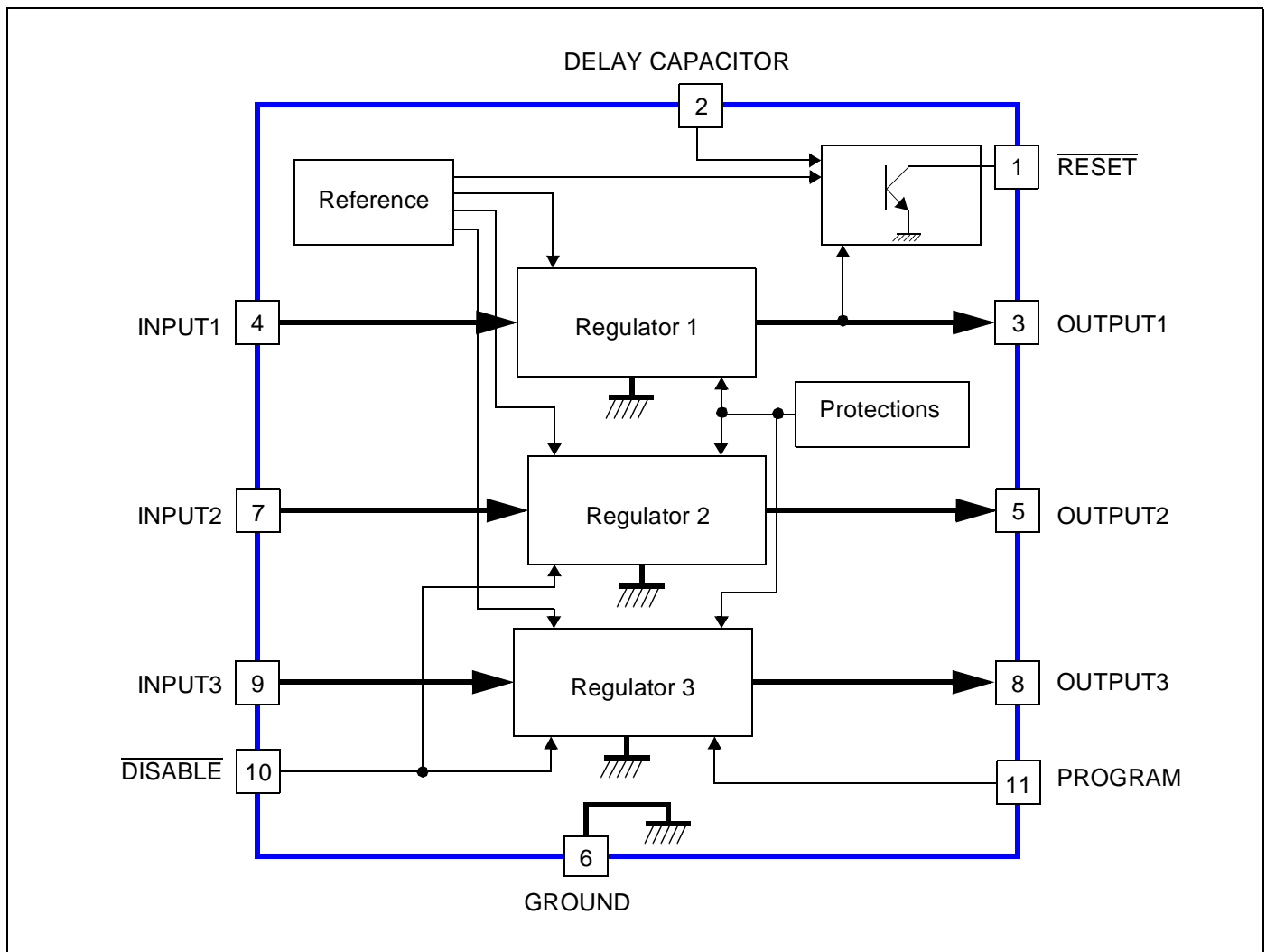


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1 GENERAL INFORMATION

Figure 1: STV8164 Block Diagram



2 ELECTRICAL CHARACTERISTICS

2.1 Absolute Maximum Ratings

| Symbol | Parameter | Value | Unit |
|--------------|--|--------------------|------|
| V_{IN} | DC Input Voltage at pins INPUT1, INPUT2 and INPUT3 | 20 | V |
| V_{DIS} | Disable Input Voltage at pin $\overline{DISABLE}$ | 20 | V |
| V_{RST} | Output Voltage at pin \overline{RESET} | 20 | V |
| I_{OUTPUT} | Output Currents | Internally Limited | |
| P_t | Power Dissipation | Internally Limited | |
| T_{STG} | Storage Temperature | -65 to +150 | °C |
| T_J | Junction Temperature | 0 to +150 | °C |

2.2 Thermal Data

| Symbol | Parameter | Value | Unit |
|------------|--|-------------|------|
| R_{thJC} | Thermal Resistance (Junction-to-Case) | 3 | °C/W |
| R_{thJA} | Thermal Resistance (Junction-to-Ambient) | $\geq 10^1$ | °C/W |
| T_J | Maximum Recommended Junction Temperature | 140 | °C |
| T_{OPER} | Operating Free Air Temperature Range | 0 to +70 | °C |

1. Depending on heat sink conditions.

2.3 Electrical Characteristics

$T_{AMB} = 25^\circ \text{C}$, $V_{IN1} = 7 \text{V}$, $V_{IN2} = 7 \text{V}$ and $V_{IN3} = 10 \text{V}$, unless otherwise specified.

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|------------|-----------------|--|------|------|------|------|
| V_{OUT1} | Output Voltage | $I_{OUT1} = 10 \text{mA}$ | 4.90 | 5.00 | 5.10 | V |
| V_{OUT2} | Output Voltage | $I_{OUT2} = 10 \text{mA}$ | 4.90 | 5.00 | 5.10 | V |
| V_{OUT3} | Output Voltage | $I_{OUT3} = 10 \text{mA}$ | 2.5 | | 16 | V |
| V_{OUT1} | Output Voltage | $7 \text{V} < V_{IN2} < 12 \text{V}$ $5 \text{mA} < I_{OUT2} < 600 \text{mA}$ | 4.80 | | 5.20 | V |
| V_{OUT2} | Output Voltage | $7 \text{V} < V_{IN2} < 12 \text{V}$ $5 \text{mA} < I_{OUT2} < 600 \text{mA}$ | 4.80 | | 5.20 | V |
| V_{IO1} | Dropout Voltage | $I_{OUT1} = 0.6 \text{A}$ | | 1 | 1.4 | V |
| V_{IO2} | Dropout Voltage | $I_{OUT2} = 0.6 \text{A}$ | | 1 | 1.4 | V |
| V_{IO3} | Dropout Voltage | $I_{OUT3} = 0.6 \text{A}$ | | 1 | 1.4 | V |

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|--|---|---|-------|--------|--------|-----------------------|
| V_{OUT1LI} | Line Regulation | $7\text{ V} < V_{IN2} < 12\text{ V}$, $I_{OUT2} = 200\text{ mA}$ | | | 50 | mV |
| V_{OUT2LI} | Line Regulation | $7\text{ V} < V_{IN2} < 12\text{ V}$, $I_{OUT2} = 200\text{ mA}$ | | | 50 | mV |
| V_{OUT3LI} | Line Regulation | $10\text{ V} < V_{IN3} < 15\text{ V}$, $I_{OUT3} = 200\text{ mA}$, $V_{OUT3} = 8\text{ V}$ | | | 80 | mV |
| V_{OUT1LO} | Load Regulation | $5\text{ mA} < I_{O1} < 600\text{ mA}$ | | | 100 | mV |
| V_{OUT2LO} | Load Regulation | $5\text{ mA} < I_{OUT2} < 600\text{ mA}$ | | | 100 | mV |
| V_{OUT3LO} | Load Regulation | $5\text{ mA} < I_{OUT3} < 600\text{ mA}$, $V_{OUT3} = 8\text{ V}$ | | | 160 | mV |
| I_Q | Quiescent Current | $I_{OUT1} = 10\text{ mA}$ Outputs 2 and 3 disabled | | 2.2 | 3.0 | mA |
| V_{O1RST} | Reset Threshold Voltage | $K = V_{OUT1}$ | K-0.4 | K-0.25 | K-0.10 | V |
| V_{RTH} | Reset Threshold Hysteresis | See circuit description. | 30 | 75 | 120 | mV |
| t_{RD} | Reset Pulse Delay | $C_E = 100\text{ nF}$ See circuit description. | | 25 | | ms |
| V_{RL} | Saturation Voltage in Reset Condition | $I_{\overline{\text{RESET}}} = 5\text{ mA}$ | | | 0.4 | V |
| I_{RH} | Leakage Current in Normal Condition, at $\overline{\text{RESET}}$ pin | $V_{\overline{\text{RESET}}} = 10\text{ V}$ | | | 10 | μA |
| K_{OUT1} K_{OUT2} K_{OUT3} | Output Voltage Thermal Drift | $T_J = 0\text{ to }125^\circ\text{C}$ $K_{OUT} = \frac{\Delta V_{OUT} \cdot 10^6}{\Delta T \cdot V_{OUT}}$ | | 100 | | ppm/ $^\circ\text{C}$ |
| I_{OUT1SC} | Short Circuit Output Current | $V_{IN1} = 7\text{ V}$ | 0.8 | 1.3 | 1.8 | A |
| I_{OUT2SC} | Short Circuit Output Current | $V_{IN2} = 7\text{ V}$ | 0.8 | 1.3 | 1.8 | A |
| I_{OUT3SC} | Short Circuit Output Current | $V_{IN3} = V_{OUT3} + 2\text{V}$ | 0.8 | 1.3 | 1.8 | A |
| V_{PROG} | Input Voltage at PROGRAM pin | | | 2 | | V |
| I_{PROG} | Input Current at PROGRAM pin | | | | 5 | μA |
| V_{DISH} | Voltage High Level at $\overline{\text{DISABLE}}$ pin (Outputs 2 and 3 active) | | 2 | | | V |
| V_{DISL} | Voltage Low Level at $\overline{\text{DISABLE}}$ pin (Outputs 2 and 3 disabled) | | | | 0.8 | V |
| I_{DIS} | Bias Current at $\overline{\text{DISABLE}}$ pin | $0\text{ V} < V_{\overline{\text{DISABLE}}} < 7\text{ V}$ | -100 | | 2 | μA |
| T_{JSD} | Junction Temperature for Thermal Shutdown | | | 150 | | $^\circ\text{C}$ |
| T_{SDH} | Thermal Shutdown Temperature Hysteresis | | | 15 | | $^\circ\text{C}$ |

3 CIRCUIT DESCRIPTION

The STV8164 is a triple-voltage regulator with Reset and Disable functions.

The three regulation parts are supplied from a single voltage reference circuit trimmed by zener zapping during EWS testing. Since the supply voltage of this voltage reference is connected to pin INPUT1 (V_{IN1}), the second and third regulators will not work if pin INPUT1 is not supplied.

The output stages are designed using a Darlington configuration with a typical dropout voltage of 1.0 V.

The adjustable voltage of pin OUTPUT3 is defined by output bridge resistors (R1 and R2). The values of these resistors are calculated to obtain, with the targeted value for pin OUTPUT3, the VPROG voltage (2.0 V) on the median point connected to pin PROGRAM.

IMPORTANT: *In all applications, all three inputs must be polarized. If Outputs 2 or 3 are not used, the corresponding inputs must be connected to Input 1.*

The Disable circuit will switch off pins OUTPUT2 and OUTPUT3 if a voltage less than 0.8 V is applied to pin $\overline{\text{DISABLE}}$.

The Reset circuit checks the voltage at pin OUTPUT1. If this voltage drops below $V_{OUT1}-0.25$ V (4.75 V Typ.), the "a" comparator (Figure 2) rapidly discharges the external capacitor (C_e) and the reset output immediately switches to low. When the voltage at pin OUTPUT1 exceeds $V_{OUT1}-0.175$ V (4.825 V Typ.), the V_{C_e} voltage increases linearly to the reference voltage ($V_{REF} = 2.5$ V) corresponding to a Reset Pulse Delay (t_{RD}) as shown in Figure 3.

$$t_{RD} = \frac{C_e \times 2.5V}{10\mu A}$$

Afterwards, the reset output returns to high. To avoid glitches in the reset output, the second comparator "b" has a large hysteresis (1.9 V).

3.1 Currents versus Maximum Power Limitation

The currents provided by the three outputs can reach 1.6 A. However, the power dissipation in the STV8164 must be established so as not to activate the automatic thermal shutdown ($T_J = 150^\circ\text{C}$). It is recommended not to have all three currents at their maximum value simultaneously.

For example, if $T_{AMB(MAX.)} = 70^\circ\text{C}$, the maximum power dissipation in the STV8164 will be (with $R_{thJA} = 12^\circ\text{C/W}$):

$$\frac{140^\circ\text{C} - 70^\circ\text{C}}{12^\circ\text{C/W}} = 5.8\text{W}$$

This means that the following conditions apply to input voltages and currents:

$$(V_{IN1} - 5\text{ V}) \times I_{IO1} + (V_{IN2} - 5\text{ V}) \times I_{IO2} + (V_{IN3} - V_{OUT3}) \times I_{IO3} < 5.8\text{ W}$$

Figure 2: Reset Diagram

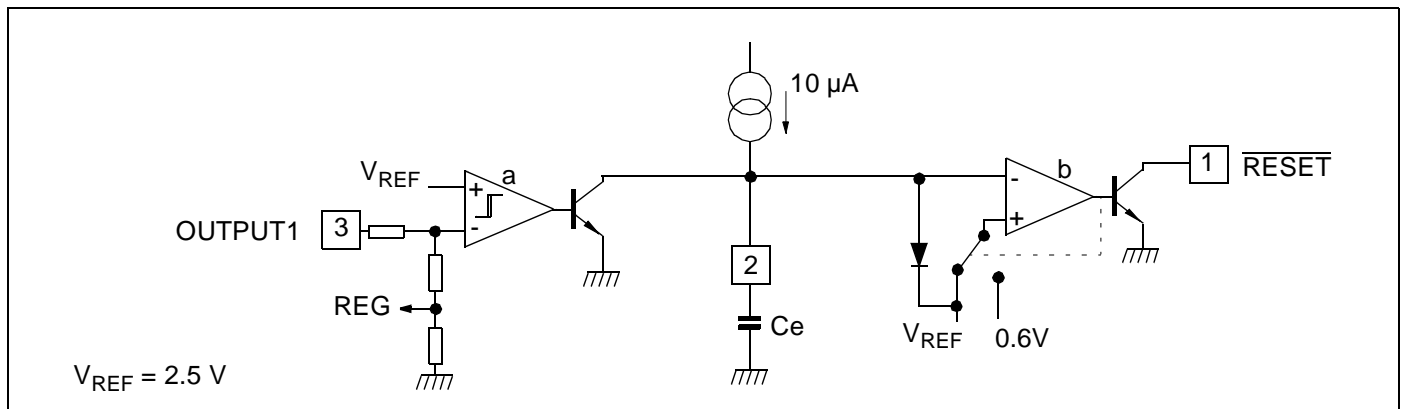
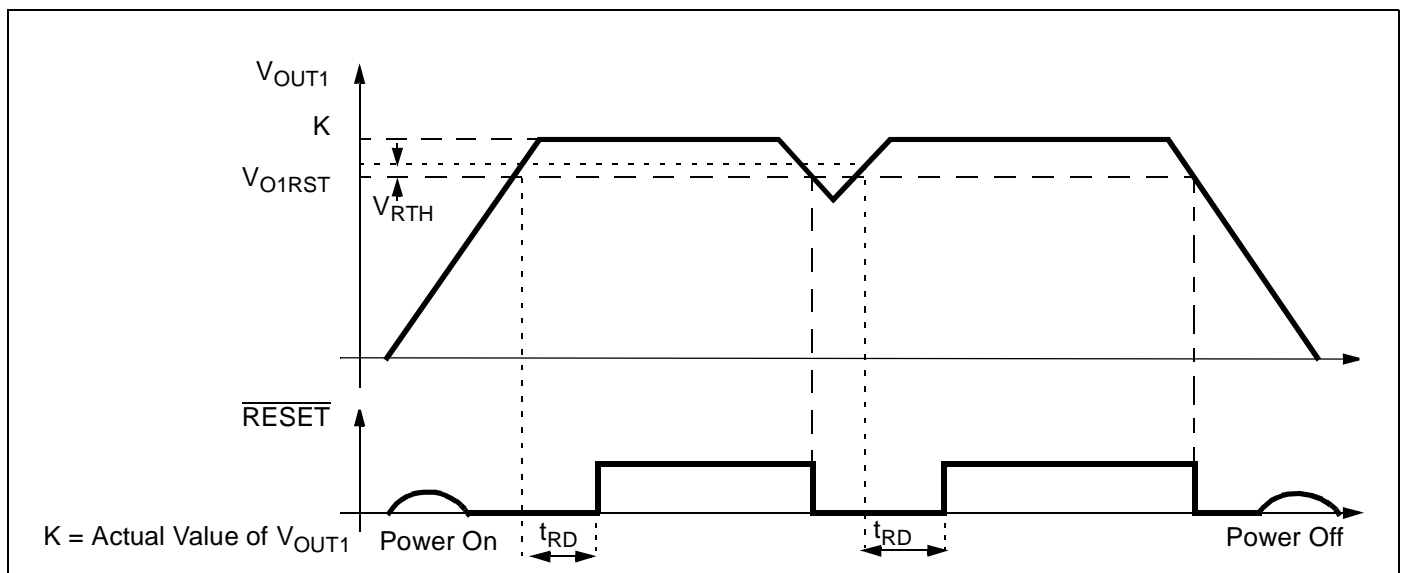
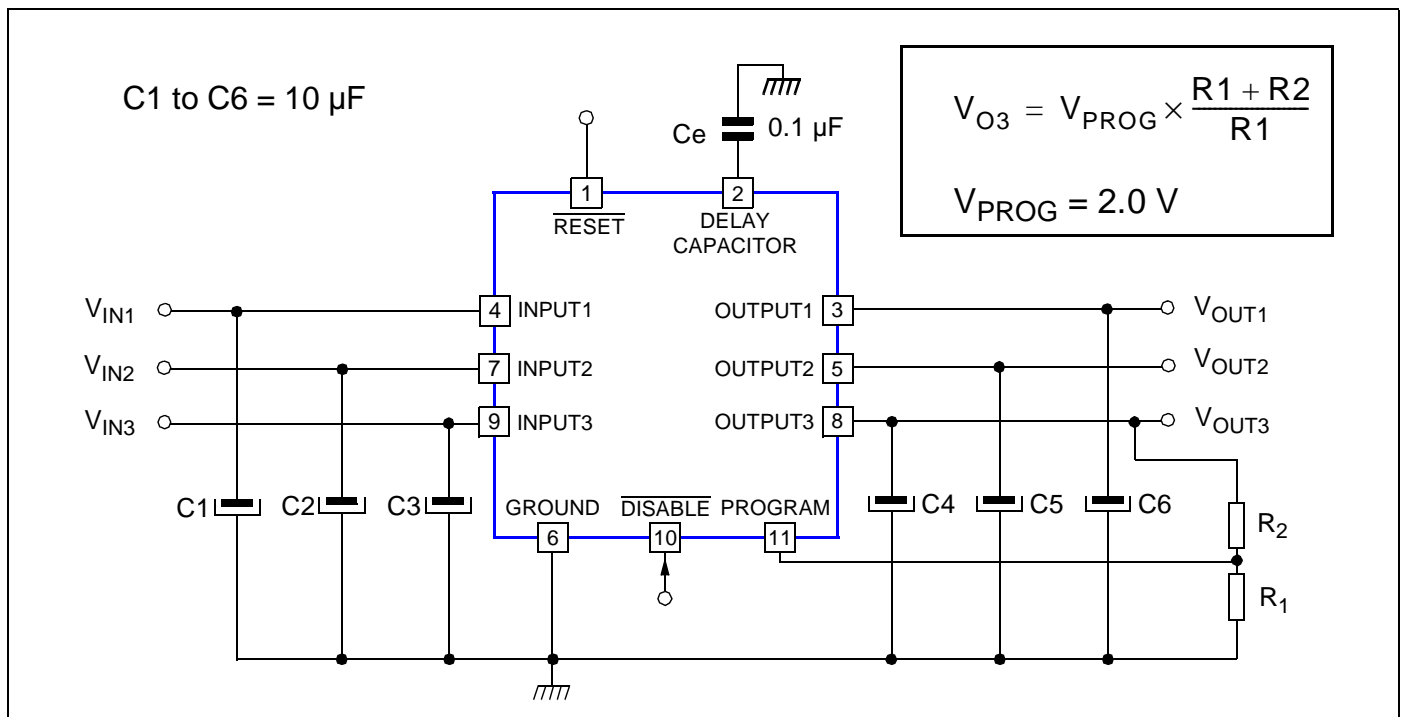


Figure 3: Internal Reset Voltage



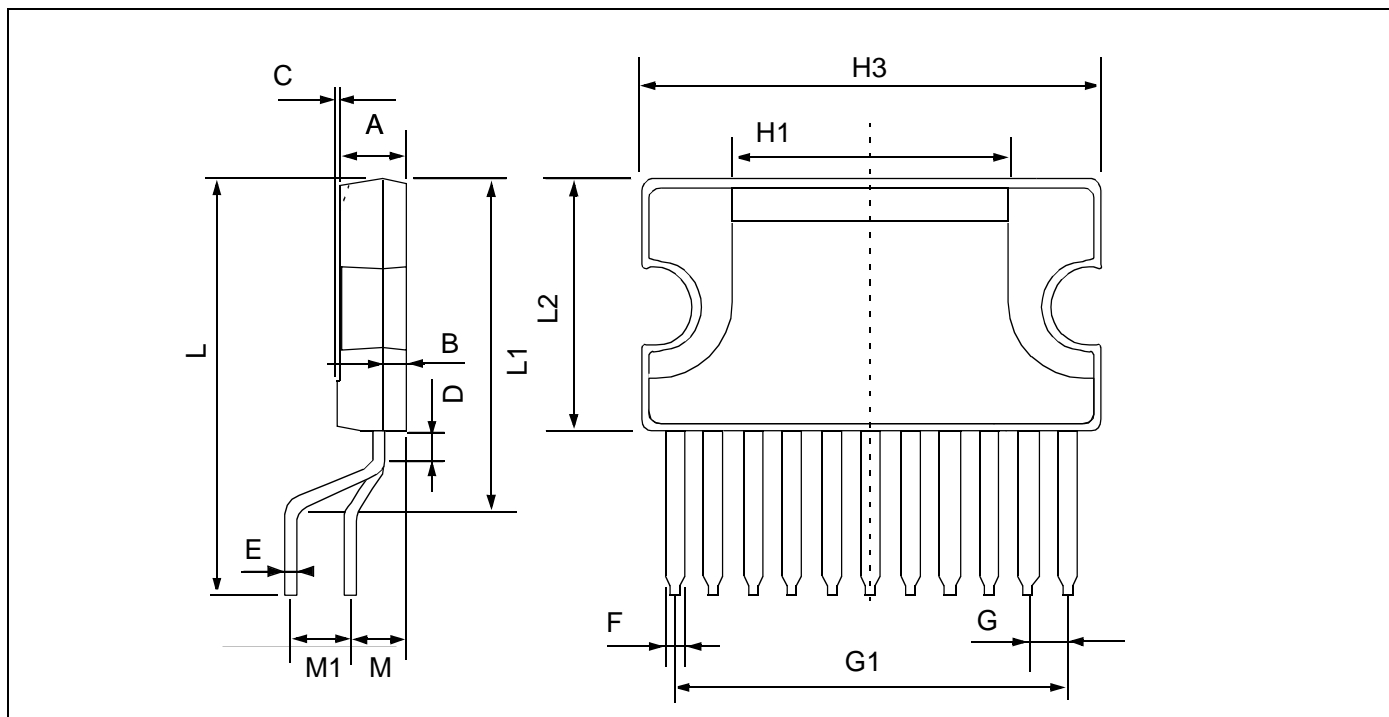
4 APPLICATION DIAGRAM

Figure 4: STV8164 Typical Application



5 PACKAGE MECHANICAL DATA

Figure 5: 11-Pin Plastic Clipwatt Package



| Dim. | mm | | | Inches | | |
|------|-----------------------|-------|-------|--------|-------|-------|
| | Min. | Typ. | Max. | Min. | Typ. | Max. |
| A | | | 3.20 | | | 0.126 |
| B | | | 1.05 | | | 0.041 |
| C | | 0.15 | | | 0.006 | |
| D | | 1.50 | | | 0.059 | |
| E | 0.49 | 0.55 | | 0.019 | 0.002 | |
| F | 0.80 | | 0.91 | 0.031 | | 0.036 |
| G | 1.57 | 1.70 | 1.83 | 0.062 | 0.067 | 0.072 |
| H1 | | 12.00 | | | 0.480 | |
| H2 | | 18.60 | | | 0.732 | |
| H3 | 19.85 | | | 0.781 | | |
| L | | 17.90 | | | 0.700 | |
| L1 | | 14.45 | | | 0.569 | |
| L2 | 10.70 | 11.00 | 11.20 | 0.421 | 0.433 | 0.441 |
| L3 | | 5.50 | | | 0.217 | |
| M | | 2.54 | | | 0.100 | |
| M1 | | 2.54 | | | 0.100 | |
| | Number of Pins | | | | | |
| N | 11 | | | | | |

6 REVISION HISTORY

| Revision | Main Changes | Date |
|----------|--|-----------------|
| 1.0 | First Edition | 20 June 2001 |
| 1.1 | New edition. Pin name changed from DISABLE to $\overline{\text{DISABLE}}$. Reset Threshold values updated. Update of Quiescent Current value in Chapter 2.3: Electrical Characteristics on page 4 . | 8 January 2002 |
| 1.2 | Update of reset voltage characteristics. Update of I_Q and V_{O1RST} values in Chapter 2.3: Electrical Characteristics on page 4 . | 31 January 2002 |
| 1.3 | Modification of Short Circuit Output Current values in Section 2.3: Electrical Characteristics . | 21 May 2002 |
| 1.4 | Output voltages and current further specified on Title page | 12 June 2002 |

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