

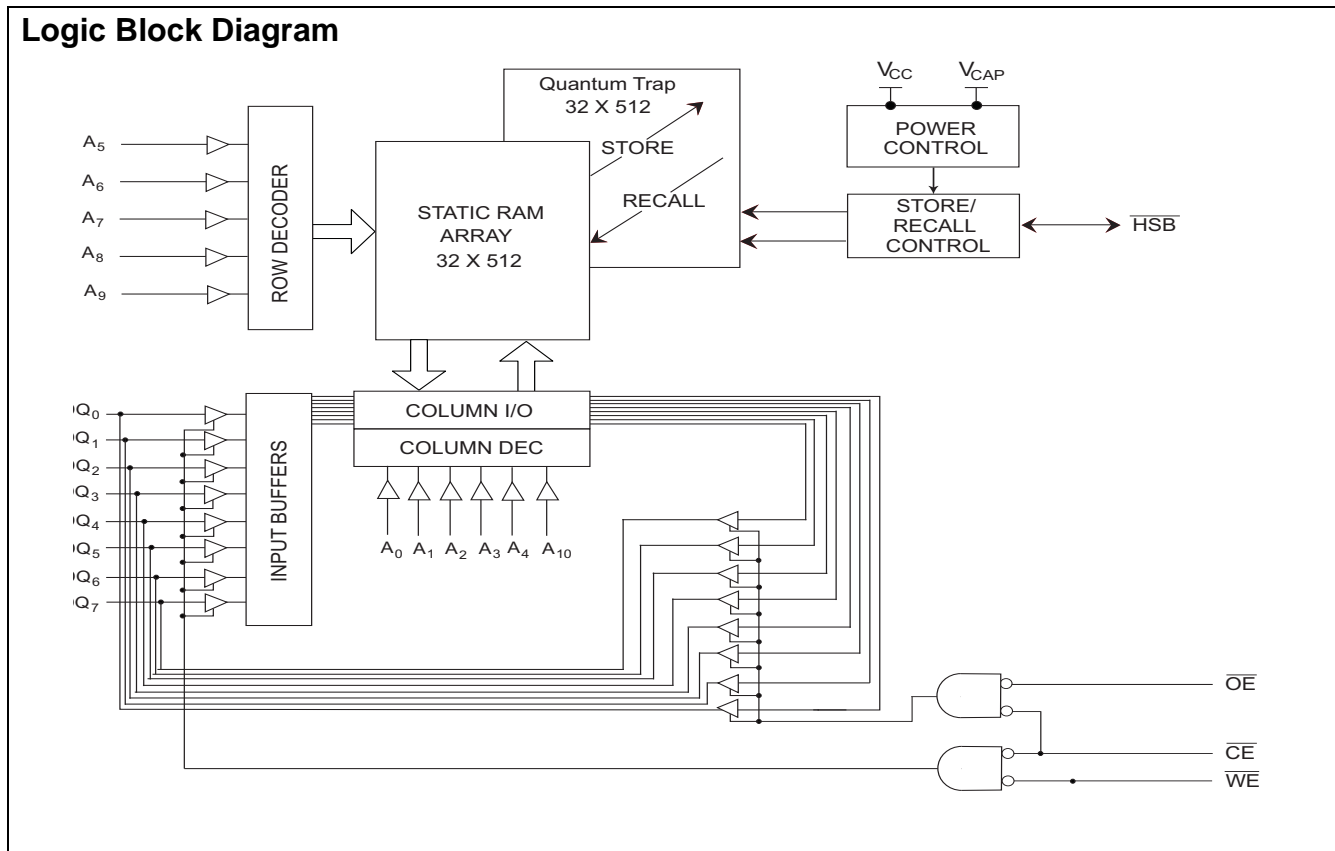
**16 Kbit (2K x 8) AutoStore nvSRAM**

**Features**

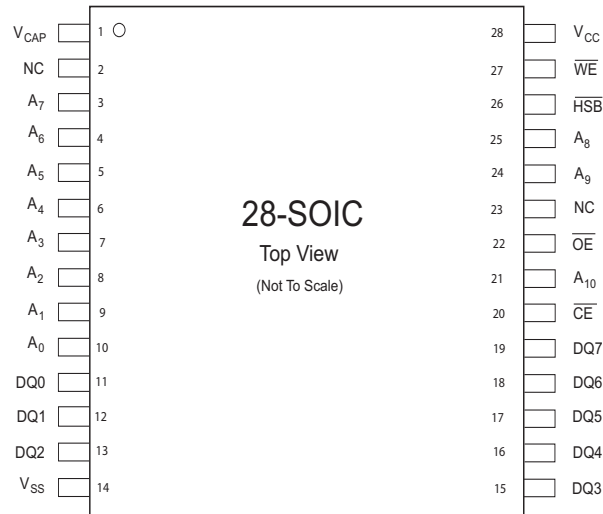
- 25 ns and 45 ns access times
- Hands off automatic STORE on power down with external 68  $\mu$ F capacitor
- STORE to QuantumTrap™ nonvolatile elements is initiated by software, hardware, or AutoStore™ on power down
- RECALL to SRAM initiated by software or power up
- Unlimited Read, Write, and Recall cycles
- 1,000,000 STORE cycles to QuantumTrap
- 100 year data retention to QuantumTrap
- Single 5V±10% operation
- Commercial and industrial temperatures
- 28-pin 300 mil and (330 mil) SOIC package
- RoHS compliance

**Functional Description**

The Cypress STK22C48 is a fast static RAM with a nonvolatile element in each memory cell. The embedded nonvolatile elements incorporate QuantumTrap technology producing the world's most reliable nonvolatile memory. The SRAM provides unlimited read and write cycles, while independent nonvolatile data resides in the highly reliable QuantumTrap cell. Data transfers from the SRAM to the nonvolatile elements (the STORE operation) takes place automatically at power down. On power up, data is restored to the SRAM (the RECALL operation) from the nonvolatile memory. A hardware STORE is initiated with the HSB pin.



## Pin Configurations

**Figure 1. Pin Diagram - 28-Pin SOIC**

**Table 1. Pin Definitions**

Pin Name	Alt	IO Type	Description
A <sub>0</sub> -A <sub>10</sub>		Input	<b>Address Inputs.</b> Used to select one of the 2,048 bytes of the nvSRAM.
DQ <sub>0</sub> -DQ <sub>7</sub>		Input or Output	<b>Bidirectional Data IO Lines.</b> Used as input or output lines depending on operation.
$\overline{WE}$	$\overline{W}$	Input	<b>Write Enable Input, Active LOW.</b> When the chip is enabled and $\overline{WE}$ is LOW, data on the IO pins is written to the specific address location.
$\overline{CE}$	$\overline{E}$	Input	<b>Chip Enable Input, Active LOW.</b> When LOW, selects the chip. When HIGH, deselects the chip.
$\overline{OE}$	$\overline{G}$	Input	<b>Output Enable, Active LOW.</b> The active LOW $\overline{OE}$ input enables the data output buffers during read cycles. Deasserting $\overline{OE}$ HIGH causes the IO pins to tri-state.
V <sub>SS</sub>		Ground	<b>Ground for the Device.</b> The device is connected to ground of the system.
V <sub>CC</sub>		Power Supply	<b>Power Supply Inputs to the Device.</b>
$\overline{HSB}$		Input or Output	<b>Hardware Store Busy (HSB).</b> When LOW, this output indicates a Hardware Store is in progress. When pulled low external to the chip, it initiates a nonvolatile STORE operation. A weak internal pull up resistor keeps this pin high if not connected (connection optional).
V <sub>CAP</sub>		Power Supply	<b>AutoStore Capacitor.</b> Supplies power to nvSRAM during power loss to store data from SRAM to nonvolatile elements.
NC		No Connect	<b>No Connect.</b> This pin is not connected to the die.

## Device Operation

The STK22C48 nvSRAM is made up of two functional components paired in the same physical cell. These are an SRAM memory cell and a nonvolatile QuantumTrap cell. The SRAM memory cell operates as a standard fast static RAM. Data in the SRAM is transferred to the nonvolatile cell (the STORE operation) or from the nonvolatile cell to SRAM (the RECALL operation). This unique architecture enables the storage and recall of all cells in parallel. During the STORE and RECALL operations, SRAM Read and Write operations are inhibited. The STK22C48 supports unlimited reads and writes similar to a typical SRAM. In addition, it provides unlimited RECALL operations from the nonvolatile cells and up to one million STORE operations.

## SRAM Read

The STK22C48 performs a Read cycle whenever  $\overline{CE}$  and  $\overline{OE}$  are LOW while WE and HSB are HIGH. The address specified on pins A<sub>0-10</sub> determines the 2,048 data bytes accessed. When the Read is initiated by an address transition, the outputs are valid after a delay of t<sub>AA</sub> (Read cycle 1). If the Read is initiated by  $\overline{CE}$  or  $\overline{OE}$ , the outputs are valid at t<sub>ACE</sub> or at t<sub>DOE</sub>, whichever is later (Read cycle 2). The data outputs repeatedly respond to address changes within the t<sub>AA</sub> access time without the need for transitions on any control input pins, and remains valid until another address change or until  $\overline{CE}$  or  $\overline{OE}$  is brought HIGH, or  $\overline{WE}$  or HSB is brought LOW.

## SRAM Write

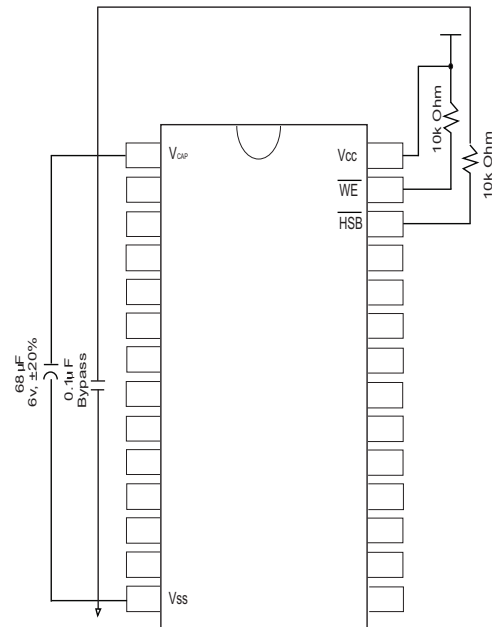
A Write cycle is performed whenever  $\overline{CE}$  and  $\overline{WE}$  are LOW and HSB is HIGH. The address inputs must be stable prior to entering the Write cycle and must remain stable until either  $\overline{CE}$  or WE goes HIGH at the end of the cycle. The data on the common IO pins DQ<sub>0-7</sub> are written into the memory if it has valid t<sub>SD</sub>, before the end of a WE controlled Write or before the end of an  $\overline{CE}$  controlled Write. Keep  $\overline{OE}$  HIGH during the entire Write cycle to avoid data bus contention on common IO lines. If  $\overline{OE}$  is left LOW, internal circuitry turns off the output buffers t<sub>HZWE</sub> after  $\overline{WE}$  goes LOW.

## AutoStore Operation

During normal operation, the device draws current from V<sub>CC</sub> to charge a capacitor connected to the V<sub>CAP</sub> pin. This stored charge is used by the chip to perform a single STORE operation. If the voltage on the V<sub>CC</sub> pin drops below V<sub>SWITCH</sub>, the part automatically disconnects the V<sub>CAP</sub> pin from V<sub>CC</sub>. A STORE operation is initiated with power provided by the V<sub>CAP</sub> capacitor.

Figure 2 shows the proper connection of the storage capacitor (V<sub>CAP</sub>) for automatic store operation. A charge storage capacitor between 68 μF and 220 μF (±20%) rated at 6V should be

Figure 2. AutoStore Mode

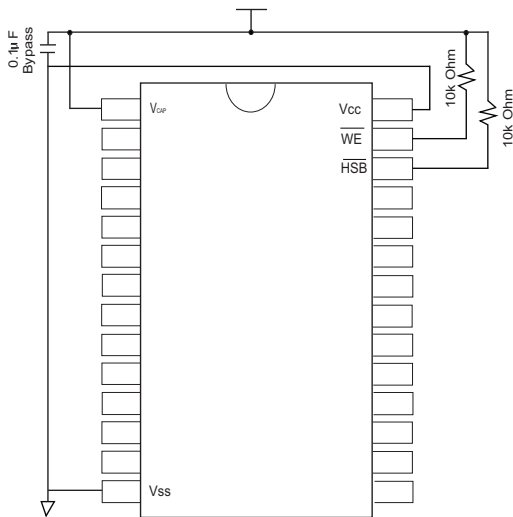


In system power mode, both V<sub>CC</sub> and V<sub>CAP</sub> are connected to the +5V power supply without the 68 μF capacitor. In this mode, the AutoStore function of the STK22C48 operates on the stored system charge as power goes down. The user must, however, guarantee that V<sub>CC</sub> does not drop below 3.6V during the 10 ms STORE cycle.

To prevent unneeded STORE operations, automatic STORES and those initiated by externally driving HSB LOW are ignored, unless at least one WRITE operation takes place since the most recent STORE or RECALL cycle. An optional pull up resistor is shown connected to HSB. This is used to signal the system that the AutoStore cycle is in progress.

## AutoStore Inhibit mode

If an automatic STORE on power loss is not required, then V<sub>CC</sub> is tied to ground and +5V is applied to V<sub>CAP</sub> (Figure 3). This is the AutoStore Inhibit mode, where the AutoStore function is disabled. If the STK22C48 is operated in this configuration, references to V<sub>CC</sub> are changed to V<sub>CAP</sub> throughout this data sheet. In this mode, STORE operations are triggered with the HSB pin. It is not permissible to change between these three options "on the fly".

**Figure 3. AutoStore Inhibit Mode**


## Hardware STORE (HSB) Operation

The STK22C48 provides the  $\overline{\text{HSB}}$  pin for controlling and acknowledging the STORE operations. The  $\overline{\text{HSB}}$  pin is used to request a hardware STORE cycle. When the  $\overline{\text{HSB}}$  pin is driven LOW, the STK22C48 conditionally initiates a STORE operation after  $t_{\text{DELAY}}$ . An actual STORE cycle only begins if a Write to the SRAM takes place since the last STORE or RECALL cycle. The  $\overline{\text{HSB}}$  pin also acts as an open drain driver that is internally driven LOW to indicate a busy condition, while the STORE (initiated by any means) is in progress. Pull up this pin with an external 10K ohm resistor to  $V_{\text{CAP}}$  if  $\overline{\text{HSB}}$  is used as a driver.

SRAM Read and Write operations, that are in progress when  $\overline{\text{HSB}}$  is driven LOW by any means, are given time to complete before the STORE operation is initiated. After  $\overline{\text{HSB}}$  goes LOW, the STK22C48 continues SRAM operations for  $t_{\text{DELAY}}$ . During  $t_{\text{DELAY}}$ , multiple SRAM Read operations take place. If a Write is in progress when  $\overline{\text{HSB}}$  is pulled LOW, it allows a time,  $t_{\text{DELAY}}$  to complete. However, any SRAM Write cycles requested after  $\overline{\text{HSB}}$  goes LOW are inhibited until  $\overline{\text{HSB}}$  returns HIGH.

During any STORE operation, regardless of how it is initiated, the STK22C48 continues to drive the  $\overline{\text{HSB}}$  pin LOW, releasing it only when the STORE is complete. After completing the STORE operation, the STK22C48 remains disabled until the  $\overline{\text{HSB}}$  pin returns HIGH.

If  $\overline{\text{HSB}}$  is not used, it is left unconnected.

## Hardware RECALL (Power Up)

During power up or after any low power condition ( $V_{\text{CC}} < V_{\text{RESET}}$ ), an internal RECALL request is latched. When  $V_{\text{CC}}$  once again exceeds the sense voltage of  $V_{\text{SWITCH}}$ , a RECALL cycle is automatically initiated and takes  $t_{\text{HRECALL}}$  to complete.

## Data Protection

The STK22C48 protects data from corruption during low voltage conditions by inhibiting all externally initiated STORE and Write operations. The low voltage condition is detected when  $V_{\text{CC}}$  is less than  $V_{\text{SWITCH}}$ . If the STK22C48 is in a Write mode (both  $\overline{\text{CE}}$  and  $\overline{\text{WE}}$  are low) at power up after a RECALL or after a STORE, the Write is inhibited until a negative transition on  $\overline{\text{CE}}$  or  $\overline{\text{WE}}$  is detected. This protects against inadvertent writes during power up or brown out conditions.

## Noise Considerations

The STK22C48 is a high speed memory. It must have a high frequency bypass capacitor of approximately 0.1  $\mu\text{F}$  connected between  $V_{\text{CC}}$  and  $V_{\text{SS}}$ , using leads and traces that are as short as possible. As with all high speed CMOS ICs, careful routing of power, ground, and signals reduce circuit noise.

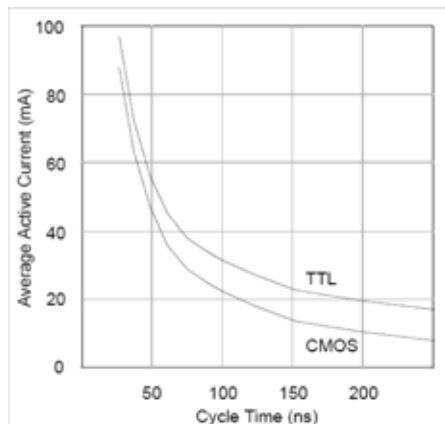
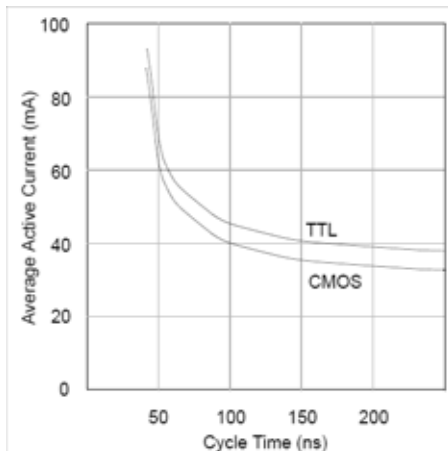
## Hardware Protect

The STK22C48 offers hardware protection against inadvertent STORE operation and SRAM Writes during low voltage conditions. When  $V_{\text{CAP}} < V_{\text{SWITCH}}$ , all externally initiated STORE operations and SRAM Writes are inhibited. AutoStore can be completely disabled by tying  $V_{\text{CC}}$  to ground and applying +5V to  $V_{\text{CAP}}$ . This is the AutoStore Inhibit mode; in this mode, STORES are only initiated by explicit request using either the software sequence or the  $\overline{\text{HSB}}$  pin.

## Low Average Active Power

CMOS technology provides the STK22C48 the benefit of drawing significantly less current when it is cycled at times longer than 50 ns. Figure 4 shows the relationship between  $I_{\text{CC}}$  and Read or Write cycle time. Worst case current consumption is shown for both CMOS and TTL input levels (commercial temperature range,  $V_{\text{CC}} = 5.5\text{V}$ , 100% duty cycle on chip enable). Only standby current is drawn when the chip is disabled. The overall average current drawn by the STK22C48 depends on the following items:

- The duty cycle of chip enable
- The overall cycle rate for accesses
- The ratio of Reads to Writes
- CMOS versus TTL input levels
- The operating temperature
- The  $V_{\text{CC}}$  level
- IO loading

**Figure 4. Current Versus Cycle Time (Read)**

**Figure 5. Current Versus Cycle Time (Write)**


## Preventing Store

The STORE function is disabled by holding  $\overline{\text{HSB}}$  high with a driver capable of sourcing 30 mA at a  $V_{\text{OH}}$  of at least 2.2V, because it must overpower the internal pull down device. This

**Table 2. Hardware Mode Selection**

$\overline{\text{CE}}$	$\overline{\text{WE}}$	$\overline{\text{HSB}}$	A10–A0	Mode	IO	Power
H	X	H	X	Not Selected	Output High Z	Standby
L	H	H	X	Read SRAM	Output Data	Active <sup>[1]</sup>
L	L	H	X	Write SRAM	Input Data	Active
X	X	L	X	Nonvolatile STORE	Output High Z	$I_{\text{CC2}}$ <sup>[2]</sup>

### Notes

1. I/O state assumes  $\overline{\text{OE}} \leq V_{\text{IL}}$ . Activation of nonvolatile cycles does not depend on state of  $\overline{\text{OE}}$ .
2. HSB STORE operation occurs only if an SRAM Write is done since the last nonvolatile cycle. After the STORE (if any) completes, the part goes into standby mode, inhibiting all operations until HSB rises.

device drives  $\overline{\text{HSB}}$  LOW for 20 ns at the onset of a STORE. When the STK22C48 is connected for AutoStore operation (system  $V_{\text{CC}}$  connected to  $V_{\text{CC}}$  and a 68  $\mu\text{F}$  capacitor on  $V_{\text{CAP}}$ ) and  $V_{\text{CC}}$  crosses  $V_{\text{SWITCH}}$  on the way down, the STK22C48 attempts to pull HSB LOW. If  $\overline{\text{HSB}}$  does not actually get below  $V_{\text{IL}}$ , the part stops trying to pull HSB LOW and abort the STORE attempt.

## Best Practices

nvSRAM products have been used effectively for over 15 years. While ease of use is one of the product's main system values, experience gained working with hundreds of applications has resulted in the following suggestions as best practices:

- The nonvolatile cells in an nvSRAM are programmed on the test floor during final test and quality assurance. Incoming inspection routines at customer or contract manufacturer's sites sometimes reprogram these values. Final NV patterns are typically repeating patterns of AA, 55, 00, FF, A5, or 5A. The end product's firmware should not assume that an NV array is in a set programmed state. Routines that check memory content values to determine first time system configuration, cold or warm boot status, and so on must always program a unique NV pattern (for example, complex 4-byte pattern of 46 E6 49 53 hex or more random bytes) as part of the final system manufacturing test to ensure these system routines work consistently.
- Power up boot firmware routines should rewrite the nvSRAM into the desired state. While the nvSRAM is shipped in a preset state, best practice is to again rewrite the nvSRAM into the desired state as a safeguard against events that might flip the bit inadvertently (program bugs, incoming inspection routines, and so on).
- The  $V_{\text{CAP}}$  value specified in this data sheet includes a minimum and a maximum value size. The best practice is to meet this requirement and not exceed the maximum  $V_{\text{CAP}}$  value because the higher inrush currents may reduce the reliability of the internal pass transistor. Customers who want to use a larger  $V_{\text{CAP}}$  value to make sure there is extra store charge should discuss their  $V_{\text{CAP}}$  size selection with Cypress.

## Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. These user guidelines are not tested.

Storage Temperature ..... -65°C to +150°C  
 Temperature under bias..... -55°C to +125°C  
 Supply Voltage on V<sub>CC</sub> Relative to GND ..... -0.5V to 7.0V  
 Voltage on Input Relative to V<sub>SS</sub>..... -0.6V to V<sub>CC</sub> + 0.5V

Voltage on DQ<sub>0-7</sub> or  $\overline{\text{HSB}}$  ..... -0.5V to V<sub>CC</sub> + 0.5V  
 Power Dissipation ..... 1.0W  
 DC Output Current (1 output at a time, 1s duration).... 15 mA

## Operating Range

Range	Ambient Temperature	V <sub>CC</sub>
Commercial	0°C to +70°C	4.5V to 5.5V
Industrial	-40°C to +85°C	4.5V to 5.5V

## DC Electrical Characteristics

Over the operating range (V<sub>CC</sub> = 4.5V to 5.5V) [3]

Parameter	Description	Test Conditions	Min	Max	Unit
I <sub>CC1</sub>	Average V <sub>CC</sub> Current	t <sub>RC</sub> = 25 ns t <sub>RC</sub> = 45 ns Dependent on output loading and cycle rate. Values obtained without output loads. I <sub>OUT</sub> = 0 mA.	Commercial	85	mA
			Industrial	90	mA
I <sub>CC2</sub>	Average V <sub>CC</sub> Current during STORE	All Inputs Do Not Care, V <sub>CC</sub> = Max Average current for duration t <sub>STORE</sub>		3	mA
I <sub>CC3</sub>	Average V <sub>CC</sub> Current at t <sub>RC</sub> = 200 ns, 5V, 25°C Typical	WE ≥ (V <sub>CC</sub> - 0.2V). All other inputs cycling. Dependent on output loading and cycle rate. Values obtained without output loads.		10	mA
I <sub>CC4</sub>	Average V <sub>CAP</sub> Current during AutoStore Cycle	All Inputs Do Not Care, V <sub>CC</sub> = Max Average current for duration t <sub>STORE</sub>		2	mA
I <sub>SB1</sub> [4]	Average V <sub>CC</sub> Current (Standby, Cycling TTL Input Levels)	t <sub>RC</sub> = 25 ns, CE ≥ V <sub>IH</sub> t <sub>RC</sub> = 45 ns, CE ≥ V <sub>IH</sub>	Commercial	25	mA
			Industrial	18	mA
I <sub>SB2</sub> [4]	V <sub>CC</sub> Standby Current	CE ≥ (V <sub>CC</sub> - 0.2V). All others V <sub>IN</sub> ≤ 0.2V or ≥ (V <sub>CC</sub> - 0.2V). Standby current level after nonvolatile cycle is complete. Inputs are static. f = 0 MHz.		1.5	mA
I <sub>ILK</sub>	Input Leakage Current	V <sub>CC</sub> = Max, V <sub>SS</sub> ≤ V <sub>IN</sub> ≤ V <sub>CC</sub>	-1	+1	μA
I <sub>OLK</sub>	Off State Output Leakage Current	V <sub>CC</sub> = Max, V <sub>SS</sub> ≤ V <sub>IN</sub> ≤ V <sub>CC</sub> , CE or OE ≥ V <sub>IH</sub> or WE ≤ V <sub>IL</sub>	-5	+5	μA
V <sub>IH</sub>	Input HIGH Voltage		2.2	V <sub>CC</sub> + 0.5	V
V <sub>IL</sub>	Input LOW Voltage		V <sub>SS</sub> - 0.5	0.8	V
V <sub>OH</sub>	Output HIGH Voltage	I <sub>OUT</sub> = -4 mA except HSB	2.4		V
V <sub>OL</sub>	Output LOW Voltage	I <sub>OUT</sub> = 8 mA except HSB		0.4	V
V <sub>BL</sub>	Logic '0' Voltage on HSB Output	I <sub>OUT</sub> = 3 mA		0.4	V
V <sub>CAP</sub>	Storage Capacitor	Between V <sub>CAP</sub> pin and V <sub>SS</sub> , 6V rated. 68 uF -10%, +20% nom.	61	220	μF

## Data Retention and Endurance

Parameter	Description	Min	Unit
DATA <sub>R</sub>	Data Retention	100	Years
NV <sub>C</sub>	Nonvolatile STORE Operations	1,000	K

### Notes

- V<sub>CC</sub> reference levels throughout this data sheet refer to V<sub>CC</sub> if that is where the power supply connection is made, or V<sub>CAP</sub> if V<sub>CC</sub> is connected to ground.
- CE ≥ V<sub>IH</sub> does not produce standby current levels until any nonvolatile cycle in progress has timed out.

### Capacitance

In the following table, the capacitance parameters are listed.<sup>[5]</sup>

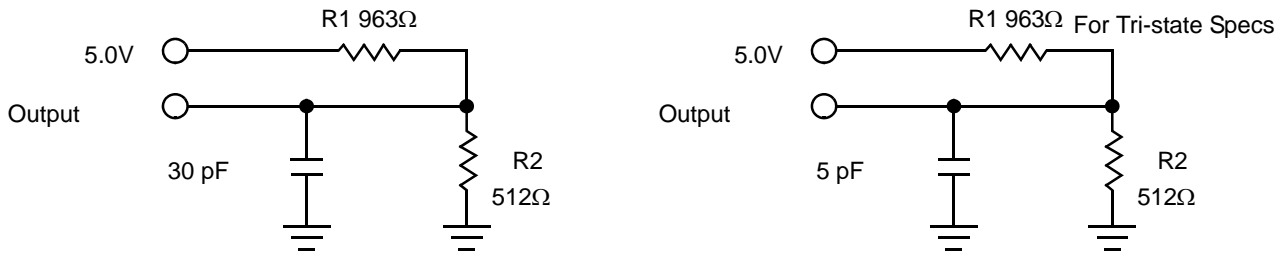
Parameter	Description	Test Conditions	Max	Unit
C <sub>IN</sub>	Input Capacitance	T <sub>A</sub> = 25°C, f = 1 MHz, V <sub>CC</sub> = 0 to 3.0V	8	pF
C <sub>OUT</sub>	Output Capacitance		7	pF

### Thermal Resistance

In the following table, the thermal resistance parameters are listed.<sup>[5]</sup>

Parameter	Description	Test Conditions	28-SOIC (300 mil)	28-SOIC (330 mil)	Unit
Θ <sub>JA</sub>	Thermal Resistance (Junction to Ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA / JESD51.	TBD	TBD	°C/W
Θ <sub>JC</sub>	Thermal Resistance (Junction to Case)		TBD	TBD	°C/W

Figure 6. AC Test Loads



### AC Test Conditions

Input Pulse Levels ..... 0V to 3V  
 Input Rise and Fall Times (10% to 90%) ..... ≤5 ns  
 Input and Output Timing Reference Levels ..... 1.5V

**Note**

5. These parameters are guaranteed by design and are not tested.

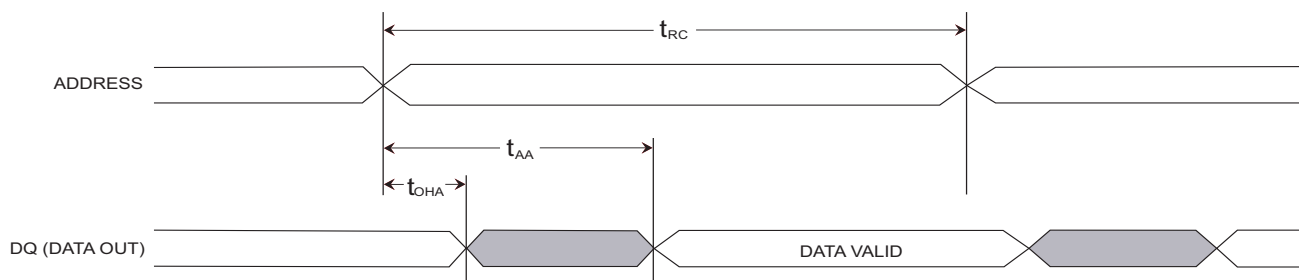
## AC Switching Characteristics

### SRAM Read Cycle

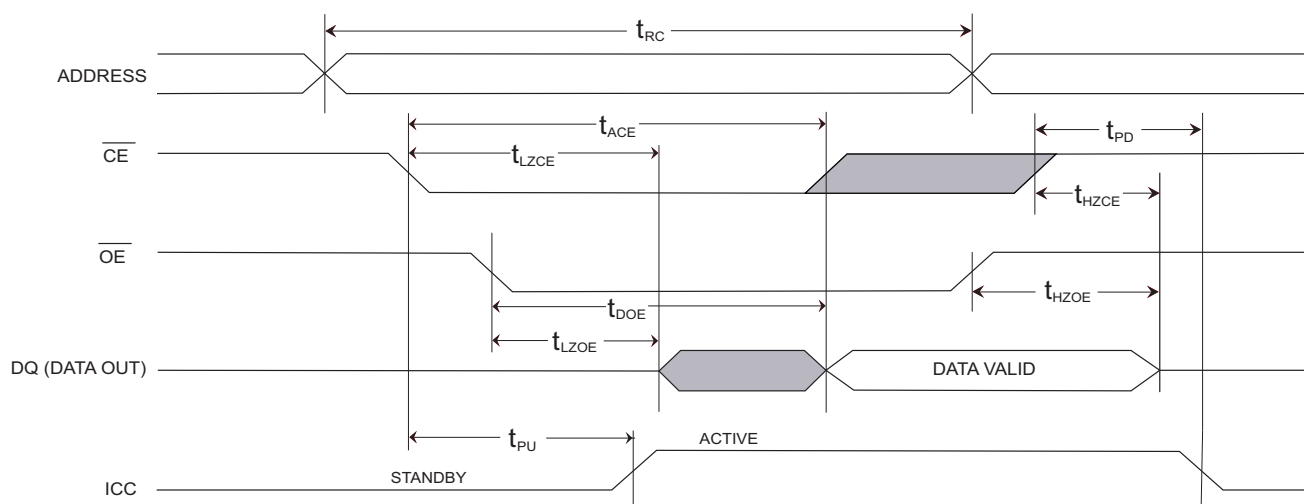
Parameter		Description	25 ns		45 ns		Unit
Cypress Parameter	Alt		Min	Max	Min	Max	
$t_{ACE}$	$t_{ELQV}$	Chip Enable Access Time		25		45	ns
$t_{RC}^{[6]}$	$t_{AVAV}, t_{ELEH}$	Read Cycle Time	25		45		ns
$t_{AA}^{[7]}$	$t_{AVQV}$	Address Access Time		25		45	ns
$t_{DOE}$	$t_{GLQV}$	Output Enable to Data Valid		10		20	ns
$t_{OHA}^{[7]}$	$t_{AXQX}$	Output Hold After Address Change	5		5		ns
$t_{LZCE}^{[8]}$	$t_{ELQX}$	Chip Enable to Output Active	5		5		ns
$t_{HZCE}^{[8]}$	$t_{EHQZ}$	Chip Disable to Output Inactive		10		15	ns
$t_{LZOE}^{[8]}$	$t_{GLQX}$	Output Enable to Output Active	0		0		ns
$t_{HZOE}^{[8]}$	$t_{GHQZ}$	Output Disable to Output Inactive		10		15	ns
$t_{PU}^{[5]}$	$t_{ELICCH}$	Chip Enable to Power Active	0		0		ns
$t_{PD}^{[5]}$	$t_{EHICCL}$	Chip Disable to Power Standby		25		45	ns

### Switching Waveforms

**Figure 7. SRAM Read Cycle 1: Address Controlled** <sup>[6, 7]</sup>



**Figure 8. SRAM Read Cycle 2:  $\overline{CE}$  and  $\overline{OE}$  Controlled** <sup>[6]</sup>



#### Notes

6.  $\overline{WE}$  and  $\overline{HSB}$  must be High during SRAM Read cycles.
7. Device is continuously selected with  $\overline{CE}$  and  $\overline{OE}$  both Low.
8. Measured  $\pm 200$  mV from steady state output voltage.



SRAM Write Cycle

Parameter		Description	25 ns		45 ns		Unit
Cypress Parameter	Alt		Min	Max	Min	Max	
$t_{WC}$	$t_{AVAV}$	Write Cycle Time	25		45		ns
$t_{PWE}$	$t_{WLWH}, t_{WLEH}$	Write Pulse Width	20		30		ns
$t_{SCE}$	$t_{ELWH}, t_{ELEH}$	Chip Enable To End of Write	20		30		ns
$t_{SD}$	$t_{DVWH}, t_{DVEH}$	Data Setup to End of Write	10		15		ns
$t_{HD}$	$t_{WHDX}, t_{EHDX}$	Data Hold After End of Write	0		0		ns
$t_{AW}$	$t_{AVWH}, t_{AVEH}$	Address Setup to End of Write	20		30		ns
$t_{SA}$	$t_{AVWL}, t_{AVEL}$	Address Setup to Start of Write	0		0		ns
$t_{HA}$	$t_{WHAX}, t_{EHAX}$	Address Hold After End of Write	0		0		ns
$t_{HZWE}^{[8,9]}$	$t_{WLQZ}$	Write Enable to Output Disable		10		14	ns
$t_{LZWE}^{[8]}$	$t_{WHQX}$	Output Active After End of Write	5		5		ns

Switching Waveforms

Figure 9. SRAM Write Cycle 1:  $\overline{WE}$  Controlled [10, 11]

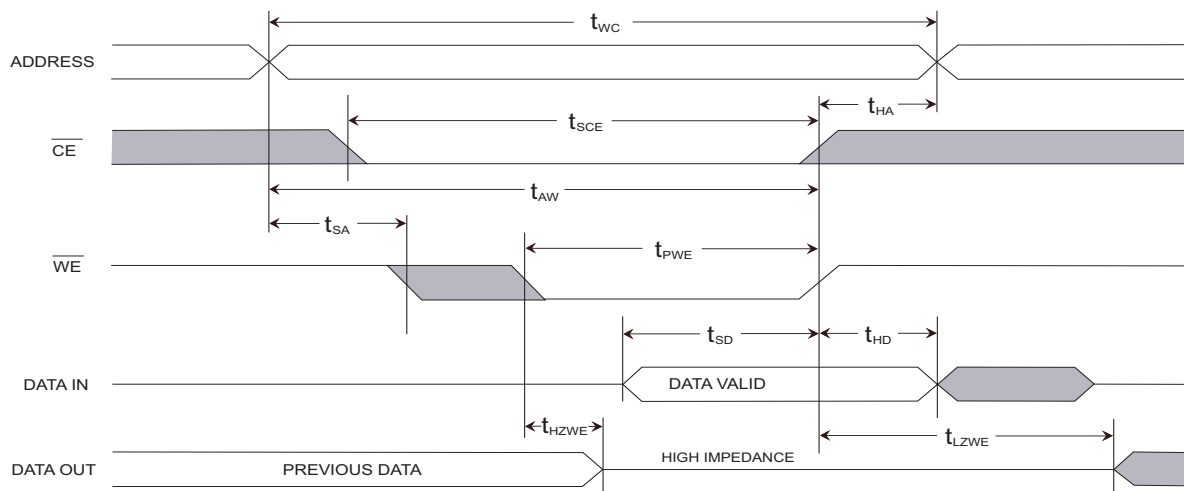
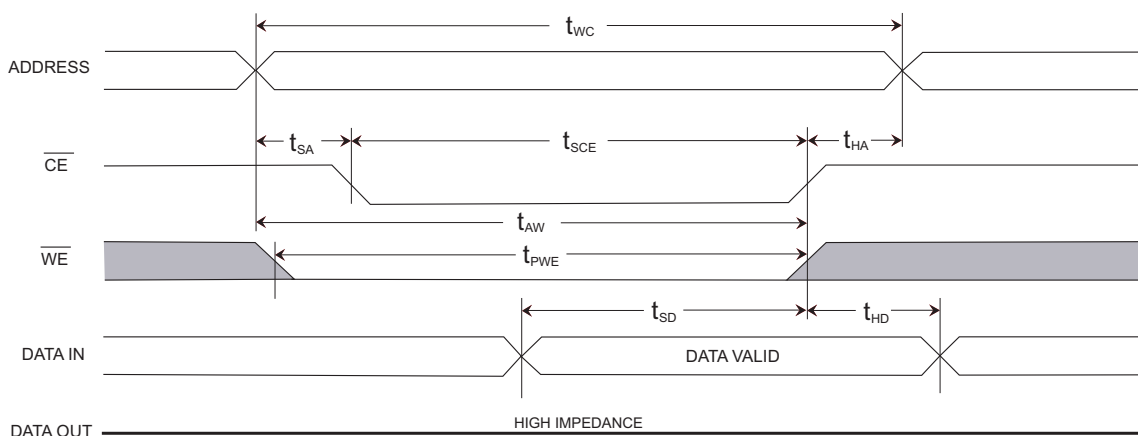


Figure 10. SRAM Write Cycle 2:  $\overline{CE}$  Controlled [10, 11]

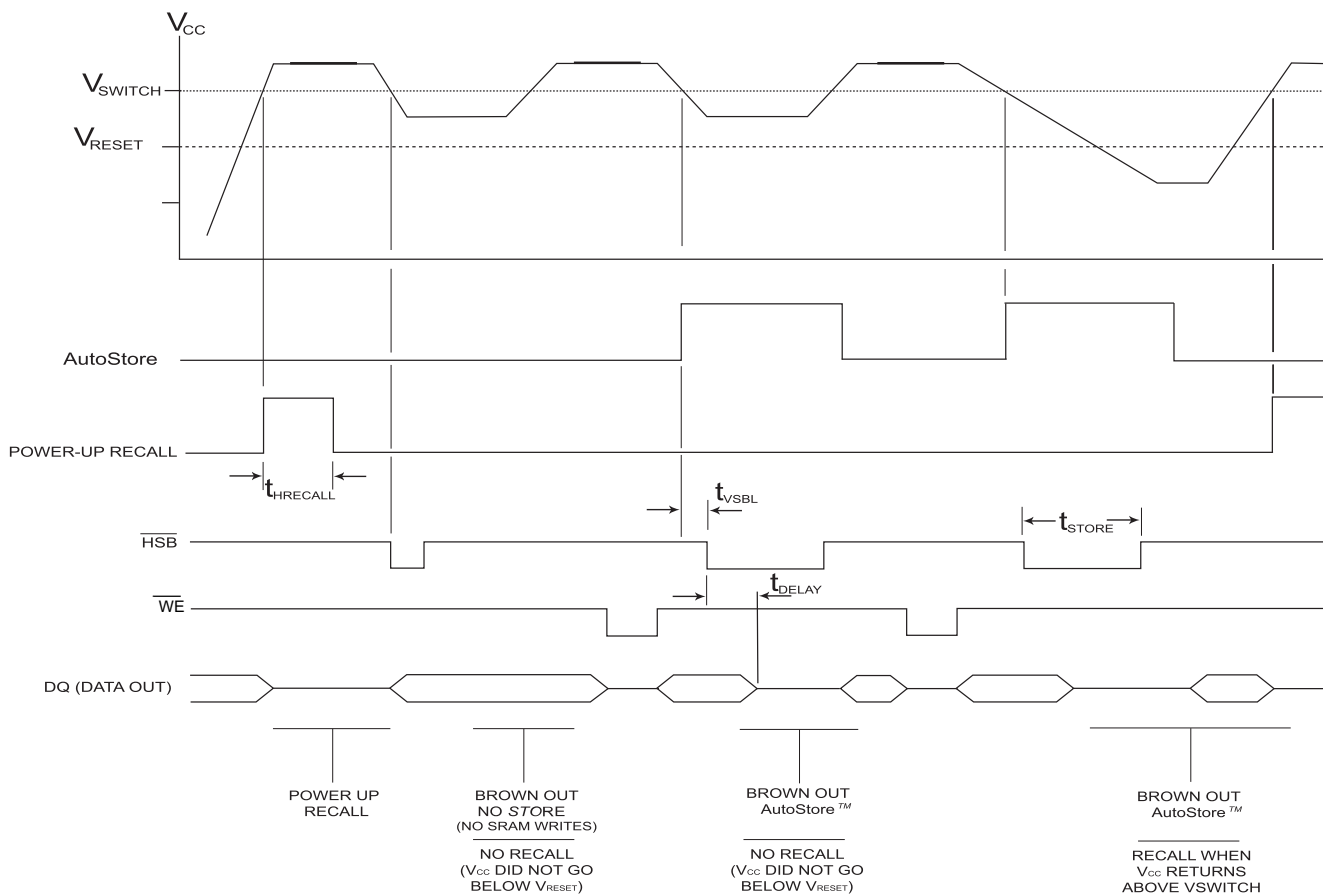


Notes

- 9. If  $\overline{WE}$  is Low when  $\overline{CE}$  goes Low, the outputs remain in the high impedance state.
- 10. HSB must be high during SRAM Write cycles.
- 11.  $\overline{CE}$  or  $\overline{WE}$  must be greater than  $V_{IH}$  during address transitions.

**AutoStore or Power Up RECALL**

Parameter	Alt	Description	STK22C48		Unit
			Min	Max	
$t_{HRECALL}^{[12]}$	$t_{RESTORE}$	Power up RECALL Duration		550	$\mu s$
$t_{STORE}^{[14, 15]}$	$t_{HLHZ}$	STORE Cycle Duration		10	ms
$t_{DELAY}^{[13]}$	$t_{HLQZ}, t_{BLQZ}$	Time Allowed to Complete SRAM Cycle	1		$\mu s$
$V_{SWITCH}$		Low Voltage Trigger Level	4.0	4.5	V
$V_{RESET}$		Low Voltage Reset Level		3.6	V
$t_{VSBL}^{[10]}$		Low Voltage Trigger ( $V_{SWITCH}$ ) to HSB Low		300	ns

**Switching Waveform**
**Figure 11. AutoStore/Power Up RECALL**

**Notes**

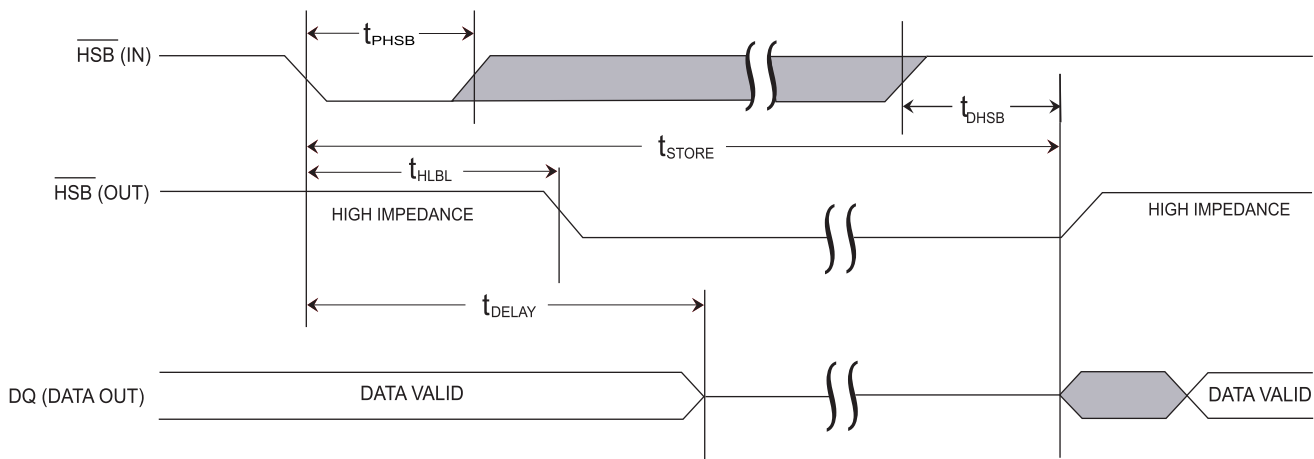
12.  $t_{HRECALL}$  starts from the time  $V_{CC}$  rises above  $V_{SWITCH}$ .
13.  $\overline{CE}$  and  $\overline{OE}$  low for output behavior.
14.  $\overline{CE}$  and  $\overline{OE}$  low and  $\overline{WE}$  high for output behavior.
15. HSB is asserted low for 1us when  $V_{CAP}$  drops through  $V_{SWITCH}$ . If an SRAM Write has not taken place since the last nonvolatile cycle,  $\overline{HSB}$  is released and no store takes place.

### Hardware STORE Cycle

Parameter	Alt	Description	STK22C48		Unit
			Min	Max	
$t_{DHSB}^{[13, 16]}$	$t_{RECOVER}, t_{HHQX}$	Hardware STORE High to Inhibit Off		700	ns
$t_{PHSB}$	$t_{HLHX}$	Hardware STORE Pulse Width	15		ns
$t_{HLBL}$		Hardware STORE Low to STORE Busy		300	ns

### Switching Waveform

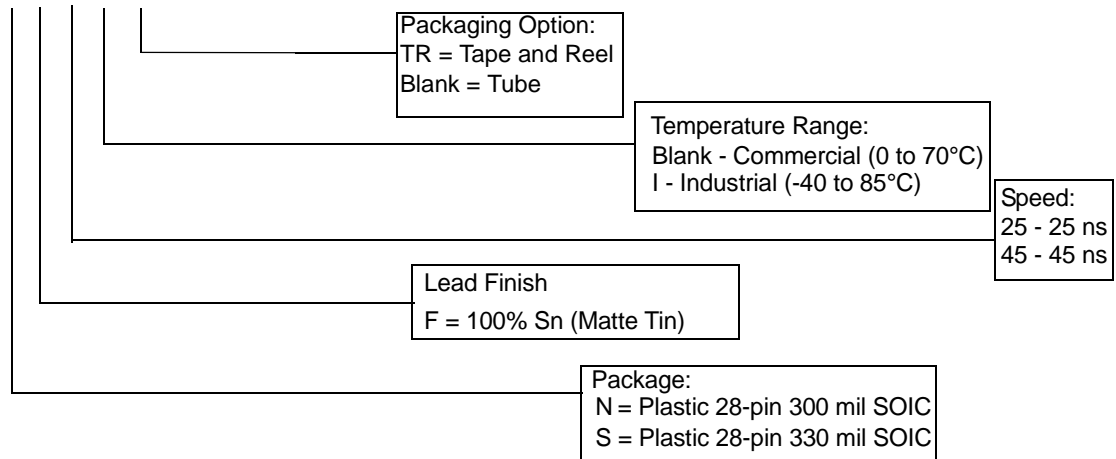
Figure 12. Hardware STORE Cycle



**Note**

16.  $t_{DHSB}$  is only applicable after  $t_{STORE}$  is complete.

**STK22C48 - N F 45 I TR**



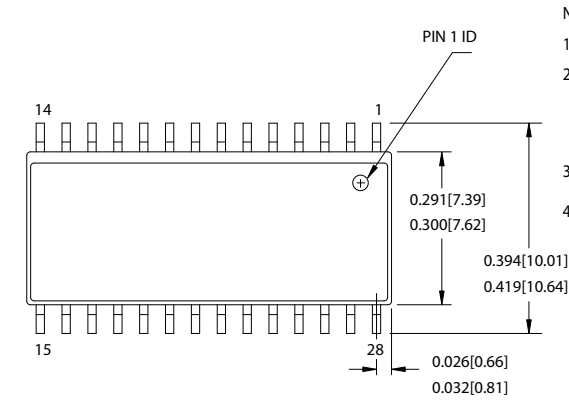
**Ordering Information**

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range	
25	STK22C48-NF25TR	51-85026	28-pin SOIC (300 mil)	Commercial	
	STK22C48-NF25	51-85026	28-pin SOIC (300 mil)		
	STK22C48-SF25TR	51-85058	28-pin SOIC (330 mil)		
	STK22C48-SF25	51-85058	28-pin SOIC (330 mil)		
	25	STK22C48-NF25ITR	51-85026	28-pin SOIC (300 mil)	Industrial
		STK22C48-NF25I	51-85026	28-pin SOIC (300 mil)	
		STK22C48-SF25ITR	51-85058	28-pin SOIC (330 mil)	
		STK22C48-SF25I	51-85058	28-pin SOIC (330 mil)	
45	STK22C48-NF45TR	51-85026	28-pin SOIC (300 mil)	Commercial	
	STK22C48-NF45	51-85026	28-pin SOIC (300 mil)		
	STK22C48-SF45TR	51-85058	28-pin SOIC (330 mil)		
	STK22C48-SF45	51-85058	28-pin SOIC (330 mil)		
	45	STK22C48-NF45ITR	51-85026	28-pin SOIC (300 mil)	Industrial
		STK22C48-NF45I	51-85026	28-pin SOIC (300 mil)	
		STK22C48-SF45ITR	51-85058	28-pin SOIC (330 mil)	
		STK22C48-SF45I	51-85058	28-pin SOIC (330 mil)	

All parts are Pb-free. The above table contains Final information. Please contact your local Cypress sales representative for availability of these parts

Package Diagrams

Figure 13. 28-Pin (300 mil) SOIC (51-85026)



- NOTE:
1. JEDEC STD REF MO-119
  2. BODY LENGTH DIMENSION DOES NOT INCLUDE MOLD PROTRUSION/END FLASH, BUT DOES INCLUDE MOLD MISMATCH AND ARE MEASURED AT THE MOLD PARTING LINE. MOLD PROTRUSION/END FLASH SHALL NOT EXCEED 0.010 in (0.254 mm) PER SIDE
  3. DIMENSIONS IN INCHES MIN. MAX.
  4. PACKAGE WEIGHT 0.85gms

PART #	
S28.3	STANDARD PKG.
SZ28.3	LEAD FREE PKG.

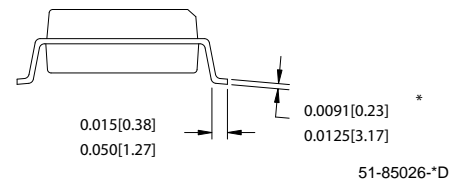
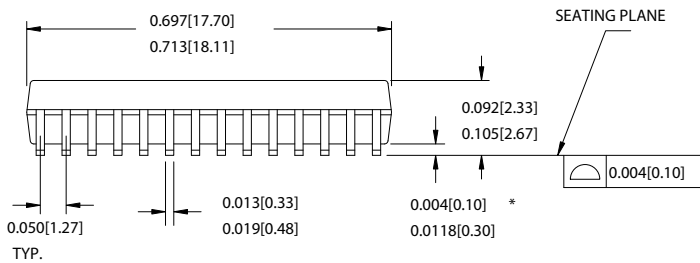
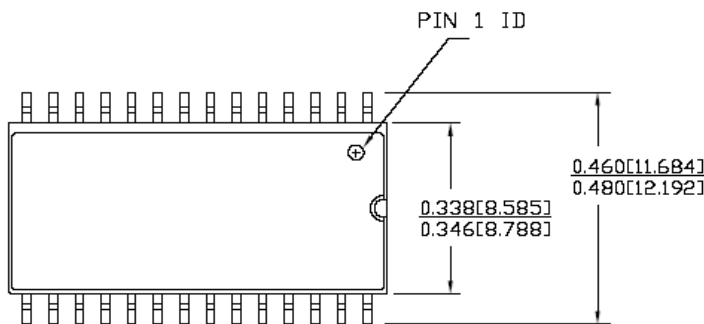
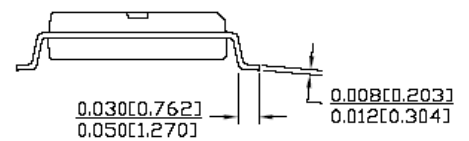
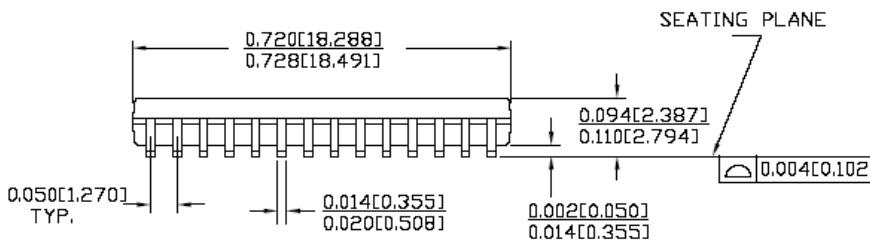


Figure 14. 28-Pin (330 mil) SOIC (51-85058)



DIMENSIONS IN INCHES[MM] MIN. MAX.  
PACKAGE WEIGHT 0.79gms

PART #	
S28.33	STANDARD PKG.
SZ28.33	LEAD FREE PKG.



51-85058-\*A

## Document History Page

Document Title: STK22C48 16 Kbit (2K x 8) AutoStore nvSRAM Document Number: 001-51000				
Rev.	ECN No.	Orig. of Change	Submission Date	Description of Change
**	2625139	GVCH/PYRS	01/30/09	New data sheet

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